

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
8 April 2010 (08.04.2010)

(10) International Publication Number
WO 2010/038599 A1

(51) International Patent Classification:

H01L 21/822 (2006.01) *H01L 23/52* (2006.01)
G06K 19/077 (2006.01) *H01L 27/04* (2006.01)
H01L 21/3205 (2006.01) *H01L 27/06* (2006.01)
H01L 21/8234 (2006.01) *H01L 27/08* (2006.01)

(21) International Application Number:

PCT/JP2009/065970

(22) International Filing Date:

7 September 2009 (07.09.2009)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

2008-256056 1 October 2008 (01.10.2008) JP

(71) Applicant (for all designated States except US): SEMICONDUCTOR ENERGY LABORATORY CO., LTD. [JP/JP]; 398, Hase, Atsugi-shi, Kanagawa, 2430036 (JP).

(72) Inventor; and

(75) Inventor/Applicant (for US only): YAKUBO, Yuto [JP/JP]; c/o SEMICONDUCTOR ENERGY LABORATORY CO., LTD., 398, Hase, Atsugi-shi, Kanagawa, 2430036 (JP).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

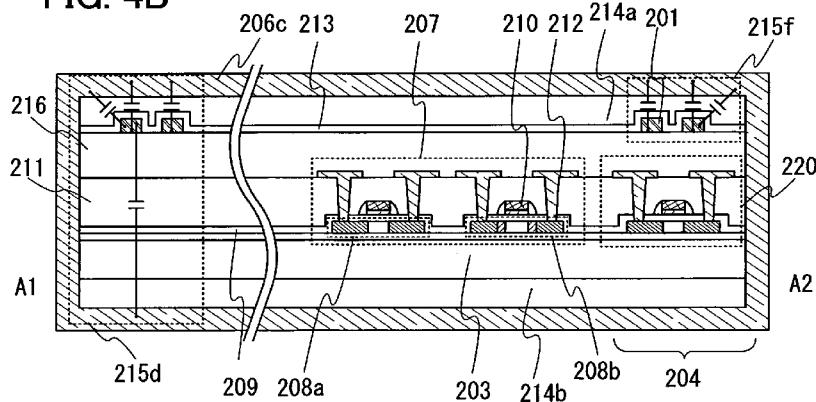
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: SEMICONDUCTOR DEVICE

FIG. 4B



(57) Abstract: To provide a semiconductor device whose reliability is improved by increase in resistance to external stress and electrostatic discharge with reduction in thickness and size achieved. An IC chip provided with an integrated circuit and a resonant capacitor portion, an antenna provided over the IC chip, and a conductive blocking body provided so as to at least partially overlap the antenna with an insulating film interposed therebetween are included. A capacitor is formed with a layered structure of the antenna, the insulating film over the antenna, and the conductive blocking body over the insulating film.

WO 2010/038599 A1

DESCRIPTION

SEMICONDUCTOR DEVICE

TECHNICAL FIELD

5 [0001]

The present invention relates to a semiconductor device such as a wireless chip capable of communicating data through wireless communication.

BACKGROUND ART

[0002]

10 In recent years, with the spread of the Internet, IT (Information Technology) has spread all over the world and revolutionized society. In particular, recently, an environment where the network can be accessed anytime and anywhere has been developed as is called a ubiquitous information society. In such an environment, individual identification technology has attracted attention, where ID (identification number) is assigned to each object so that the history thereof is revealed and utilized in production, management, and the like. Specifically, RFIDs (radio frequency identification) such as wireless chips (also called ID tags, IC tags, IC chips, RF (radio frequency) tags, wireless tags, and electronic tags) are beginning to be introduced in companies, markets, and the like on a trial basis. Such semiconductor devices such as 15 wireless chips are mounted on cards or the like and the semiconductor devices have recently been suggested to be applied in a variety of fields (for example, Patent 20 Document 1).

[0003]

25 With the expansion of the market of semiconductor devices, there have been a variety of requirements of a shape, characteristics, and the like. For example, as a requirement regarding shapes, further reduction in size and thickness, and the like are given. In addition, as a requirement regarding characteristics, increase in strength, resistance to electrostatic discharge, and the like which is related to reliability are given.

[Reference]

30 [0004]

[Patent Document 1] Japanese Published Patent Application No. 2001-260580

DISCLOSURE OF INVENTION

[0005]

However, in general, it is significantly difficult to achieve both reduction in size and thickness and improvement of reliability of the semiconductor devices.

[0006]

5 As a method for downsizing an IC chip, for example, there is a method in which an antenna and an IC chip are disposed so as to be overlapped with each other. However, in the case where an antenna and an IC chip are disposed so as to be overlapped with each other in a wireless chip, in general, an integrated circuit might malfunction due to parasitic capacitance between the antenna and the IC chip.

10 [0007]

In the semiconductor devices, electrostatic discharge from the outside becomes a more serious problem as the semiconductor devices are reduced in thickness and size. Therefore, for example, productivity might be reduced by the time the semiconductor devices are used as products after the manufacturing process and inspection are 15 completed.

[0008]

In view of the above problems, an object of the present invention is to provide a semiconductor device whose reliability is improved by increase in resistance to external stress and electrostatic discharge with reduction in thickness and size achieved.

20 [0009]

An embodiment of the present invention provides a wireless chip having the following structure to achieve the above object.

[0010]

According to an embodiment of the present invention, an IC chip including an 25 integrated circuit and a resonant capacitor portion, an antenna provided over the IC chip, and a conductive blocking body provided so as to at least partially overlap the antenna with an insulating film interposed therebetween are included. A capacitor is formed with a layered structure of the antenna, the insulating film over the antenna, and the conductive blocking body over the insulating film.

30 [0011]

According to an embodiment of the present invention, a conductive blocking body, an insulating film provided over the conductive blocking body, an IC chip

provided with an integrated circuit and a resonant capacitor portion and provided over the insulating film, and an antenna provided over the IC chip are included. The conductive blocking body and the antenna are provided so as to be at least partially overlapped with each other with the insulating film and the IC chip interposed therebetween. A capacitor is formed with a layered structure of the conductive blocking body, the insulating film, and the antenna.

[0012]

According to an embodiment of the present invention, an IC chip provided with an integrated circuit and a resonant capacitor portion, an antenna provided over the IC chip, an insulating film provided so as to surround the IC chip and the antenna, and a conductive blocking body provided so as to surround the insulating film. A capacitor is formed with a layered structure of the antenna, the insulating film, and the conductive blocking body.

[0013]

According to an embodiment of the present invention, a resonant capacitor portion includes a wiring, and a capacitor is formed with a layered structure of the resonant capacitor portion, an insulating film, and a conductive blocking body.

[0014]

According to an embodiment of the present invention, a first conductive blocking body, a first insulating film provided over the first conductive blocking body, an IC chip provided with an integrated circuit and a resonant capacitor portion and provided over the first insulating film, an antenna provided over the IC chip, a second insulating film provided over the antenna, and a second conductive blocking body provided over the second insulating film are included. The first conductive blocking body and the antenna are provided so as to be partially overlapped with each other with the first insulating film and the IC chip interposed therebetween. The second conductive blocking body and the antenna are provided so as to be partially overlapped with each other with the second insulating film interposed therebetween. A capacitor is formed with a layered structure of the first conductive blocking body, the first insulating film, and the antenna and another capacitor is formed with a layered structure of the second conductive blocking body, the second insulating film, and the antenna.

[0015]

According to an embodiment of the present invention, a resonant capacitor portion includes a wiring, a capacitor is formed with a layered structure of the resonant capacitor portion, a first insulating film, and a first conductive blocking body and another capacitor is formed with a layered structure of a second resonant capacitor portion, a second insulating film, and a second conductive blocking body.

5 [0016]

The insulating film according to an embodiment of the present invention includes an impact diffusion layer.

10 [0017]

The first insulating film and the second insulating film according to an embodiment of the present invention each include an impact diffusion layer.

15 [0018]

The impact diffusion layer according to an embodiment of the present invention is a structure body in which a fibrous body is impregnated with an organic resin.

20 [0019]

By using an embodiment of the present invention, a capacitor is formed between a conductive blocking body and an antenna and the number of capacitors of a resonant capacitor portion formed in a chip can be reduced as compared to the case where a conductive blocking body is not provided. Accordingly, the size of a wireless chip and the size of an IC chip can be reduced and the limited area in the IC chip and the wireless chip can be utilized efficiently. Further, since the sizes of the IC chip and the wireless chip can be reduced, current consumption can be reduced and thus a communication distance can be prevented from being shortened.

25 [0020]

Further, by using the conductive blocking body, resistance to static electricity and physical strength of the wireless chip, which becomes a significant problem when the wireless chip is downsized, can be increased.

30 BRIEF DESCRIPTION OF DRAWINGS

[0021]

In the accompanying drawings:

FIGS. 1A and 1B illustrate a structure of a wireless chip of an embodiment of the present invention (Embodiment 1);

FIGS. 2A and 2B illustrate a structure of a wireless chip of an embodiment of the present invention (Embodiment 2);

5 FIGS. 3A and 3B illustrate a structure of a wireless chip of an embodiment of the present invention (Embodiment 3);

FIGS. 4A and 4B illustrate a structure of a wireless chip of an embodiment of the present invention (Embodiment 4);

10 FIGS. 5A and 5B illustrate a structure of a wireless chip of an embodiment of the present invention (Embodiment 5);

FIGS. 6A to 6D illustrate manufacturing steps of a wireless chip of an embodiment of the present invention (Embodiment 6);

FIGS. 7A to 7C illustrate manufacturing steps of a wireless chip of an embodiment of the present invention (Embodiment 7);

15 FIGS. 8A to 8G illustrate application examples of a wireless chip of an embodiment of the present invention (Embodiment 8);

FIG. 9 shows results of measurement of resonant frequencies with respect to resonant capacitance in IC chips (Example 1); and

20 FIG. 10 shows results of measurement of resonant frequencies with respect to resonant capacitance in IC chips (Example 1).

BEST MODE FOR CARRYING OUT THE INVENTION

[0022]

The embodiments and example of the present invention will be specifically 25 described with reference to the drawings. However, the present invention disclosed herein is not limited to the following description because it will be easily understood by those skilled in the art that various changes and modifications can be made to the modes and their details without departing from the spirit and scope of the present invention disclosed herein. Therefore, the present invention disclosed herein should not be 30 construed as being limited to the description in the following embodiments and example. Note that a common reference numeral refers to the same part throughout the drawings in the structure of the present invention described below. Although a capacitor is

provided also in a portion other than the portion which is shown, a capacitor other than a typical capacitor is not shown.

[0023]

5 In the following embodiments, part of structural examples using the present invention will be described with reference to drawings.

[0024]

[Embodiment 1]

A structure of a wireless chip 200 of FIG. 1A will be described. FIG. 1B is a cross section taken along line A1-A2 in the wireless chip 200 of FIG. 1A.

10 [0025]

As illustrated in FIGS. 1A and 1B, a wireless chip 200 described in this embodiment includes an antenna 201 and an IC chip 202 that are stacked over the same substrate 203. The antenna 201 and the IC chip 202 are disposed so as to be at least partially overlapped with each other with an insulating film interposed therebetween.

15 The IC chip 202 includes a resonant capacitor portion 204 in the chip, which is provided with a capacitor 220, and a logic portion 205 including a power supply generating means, a control means, a memory means, and the like. Note that both terminals of the antenna 201 are electrically connected to an integrated circuit 207 of the logic portion 205. Further, a conductive blocking body 206a is disposed so as to overlap an antenna 201 with insulating films such as a protective film 213 and an impact diffusion layer 214a interposed therebetween, so that the conductive blocking body 206a is provided on the uppermost surface of the wireless chip 200.

20 [0026]

25 This embodiment will describe a structure in which a capacitor 215a includes the antenna 201 and the conductive blocking body 206a, and the conductive blocking body 206a is provided above the substrate 203.

[0027]

30 The integrated circuit 207 includes at least semiconductor films 208a and 208b each having an impurity region, a gate electrode 210 provided over the semiconductor films 208a and 208b with a gate insulating film 209 interposed therebetween, a first interlayer insulating film 211 provided so as to cover the gate electrode 210, and source and drain electrodes 212 provided over the first interlayer insulating film 211 and

electrically connected to the impurity regions of the semiconductor films 208a and 208b.

[0028]

Further, the antenna 201 connected to the integrated circuit 207 is disposed with a second interlayer insulating film 216 interposed therebetween. The conductive blocking body 206a is disposed over the antenna 201 with the protective film 213 and the impact diffusion layer 214a interposed therebetween. Note that the conductive blocking body 206a is not connected to the antenna 201 physically.

[0029]

According to the above structure, the conductive blocking body 206a and the antenna 201 function as electrodes with the protective film 213 and the impact diffusion layer 214a interposed therebetween, so that the capacitor 215a is formed.

[0030]

Next, a manufacturing method of the above structure will be briefly described below.

[0031]

First, the substrate 203 is prepared. As the substrate 203, a glass substrate such as barium borosilicate glass and aluminoborosilicate glass, a quartz substrate, a ceramic substrate, and the like can be used. Alternatively, a metal substrate including stainless steel or a semiconductor substrate having a surface provided with an insulating film may be employed. Although a substrate formed of a flexible synthetic resin such as plastic generally has a lower resistance temperature than the aforementioned substrates, it may be used as long as being resistant to a processing temperature during manufacturing steps. Note that the surface of the substrate 203 may be planarized by polishing such as a CMP method.

[0032]

Then, the integrated circuit 207 included in the logic portion 205 is formed over the substrate 203. The integrated circuit 207 has at least the semiconductor films 208a and 208b, the gate electrode 210 provided over the semiconductor films 208a and 208b with the gate insulating film 209 interposed therebetween, the first interlayer insulating film 211 provided so as to cover the gate electrode 210, and the source and drain electrodes 212 provided over the first interlayer insulating film 211. Note that

the capacitor 220 may be formed through the same steps as and in a similar manner to the element included in the integrated circuit 207; therefore, description thereof is omitted here.

[0033]

5 The semiconductor films 208a and 208b may have any state selected from an amorphous semiconductor, a semiconductor where an amorphous state and a crystalline state are mixed, a microcrystalline semiconductor where a crystal grain with sizes from 0.5 to 20 nm can be observed, and a crystalline semiconductor. In this embodiment, an amorphous semiconductor film is formed and crystallized by heat treatment to obtain 10 the semiconductor films 208a and 208b. The heat treatment can be performed by using a furnace, laser irradiation, irradiation of light emitted from a lamp instead of a laser beam (lamp annealing), or a combination of them.

[0034]

15 Next, the gate insulating film 209 is formed so as to cover the semiconductor films 208a and 208b. The gate insulating film 209 can be formed to have a single-layer structure or a layered structure using, for example, any of silicon oxide, silicon nitride, silicon nitride oxide, and the like. The deposition may be performed by a plasma CVD method, a sputtering method, or the like.

[0035]

20 Then, the gate electrode 210 is formed over each of the semiconductor films 208a and 208b with the gate insulating film 209 interposed therebetween. The gate electrode 210 may be formed to have a single-layer structure or a layered structure of a plurality of metal films. The gate electrode 210 may be formed by a CVD method or a sputtering method using an element selected from tantalum (Ta), tungsten (W), titanium 25 (Ti), molybdenum (Mo), aluminum (Al), copper (Cu), chromium (Cr), and neodymium (Nd), or an alloy or compound material mainly containing any of these elements. In this embodiment, a first conductive layer and a second conductive layer are stacked in this order using tantalum nitride and tungsten (W), respectively.

[0036]

30 Then, impurities imparting n-type or p-type conductivity are selectively added to the semiconductor films 208a and 208b using the gate electrode 210 or a resist that has been patterned as a mask. Each of the semiconductor films 208a and 208b has a

channel forming region and impurity regions (including a source region, a drain region, and an LDD region), and an n-channel thin film transistor (hereinafter also referred to as an n-channel TFT) or a p-channel thin film transistor (hereinafter also referred to as a p-channel TFT) can be obtained depending on the conductivity of the added impurity elements.

5

[0037]

In FIG. 1B, an n-channel TFT has side walls at sides of the gate electrode 210. The semiconductor film 208b of the n-channel TFT is selectively added with impurities imparting n-type conductivity to form a source region, a drain region, and an LDD region. Meanwhile, the semiconductor film 208a of a p-channel TFT is selectively added with impurities imparting p-type conductivity, so that a source region and a drain region are formed. In this embodiment, the side walls are formed at sides of the gate electrode 210 and the LDD region is selectively formed in the n-channel TFT; however, an embodiment of the present invention is not limited to this structure. An LDD region may also be formed in the p-channel TFT, and aside wall is not necessarily formed in the p-channel TFT. Alternatively, a CMOS structure where an n-channel TFT and a p-channel TFT are used in a complementary manner may be employed.

10
15
15

[0038]

Next, the first interlayer insulating film 211 is formed so as to cover the gate electrode 210. The first interlayer insulating film 211 may be formed to have a single-layer structure or a layered structure of an insulating film containing oxygen or nitrogen, such as silicon oxide (SiO_x), silicon nitride (SiN_x), silicon oxynitride (SiO_xN_y) ($x > y$), and silicon nitride oxide (SiN_xO_y) ($x > y$). Alternatively, a resin material such as an epoxy resin, an acrylic resin, a phenol resin, a novolac resin, a melamine resin, a urethane resin, or a silicone resin may be used. Alternatively, the first interlayer insulating film 211 may be formed using an organic material such as benzocyclobutene, parylene, fluorinated arylene ether, or polyimide, a compound material obtained by polymerization such as siloxane-based polymer, a composition material containing water-soluble homopolymer and water-soluble copolymer, or the like.

20
25
30

[0039]

After that, the source and drain electrodes 212 are formed over the first interlayer insulating film 211. The source and drain electrodes 212 are electrically

connected to the impurity regions of the semiconductor films 208a and 208b. In FIG. 1B, a wiring is formed using the same material as the source and drain electrodes 212. The source and drain electrodes 212 and the wiring may be formed to have a single-layer structure or a layered structure using an element selected from aluminum 5 (Al), tungsten (W), titanium (Ti), tantalum (Ta), molybdenum (Mo), nickel (Ni), platinum (Pt), copper (Cu), gold (Au), silver (Ag), manganese (Mn), neodymium (Nd), carbon (C), and silicon (Si), or an alloy or compound material mainly containing any of these elements by a CVD method, a sputtering method, or the like. The alloy material mainly containing aluminum is, for example, a material that contains aluminum as a 10 main component and contains nickel, or an alloy material that contains aluminum as a main component and contains nickel and one or both of carbon and silicon. The source and drain electrodes 212 and the wiring may be formed to have, for example, a layered structure of a barrier film, an aluminum silicon (Al-Si) film and a barrier film, or a layered structure of a barrier film, an aluminum silicon (Al-Si) film, a titanium 15 nitride film, and a barrier film. Note that the barrier film is a thin film containing titanium, nitride of titanium, molybdenum, or nitride of molybdenum. Aluminum and aluminum silicon have a low resistance value and are inexpensive; therefore, they are suitable for the source and drain electrodes 212 and the wiring. When the barrier films are formed for the top layer and the bottom layer, hillock formation in aluminum and 20 aluminum silicon can be prevented. If the barrier film is formed of titanium that is a highly reducing element, even when a thin natural oxide film is formed on the semiconductor films 208a and 208b, the natural oxide film can be reduced and contact with the semiconductor films 208a and 208b can be improved.

[0040]

25 Then, the second interlayer insulating film 216 is formed so as to cover the source and drain electrodes 212 and the wiring. The second interlayer insulating film 216 may be formed using any of the above materials for the first interlayer insulating film 211.

[0041]

30 Then, the antenna 201 is formed over the second interlayer insulating film 216, a protective film 213 is formed over the antenna 201, an impact diffusion layer 214a is formed over the protective film 213, and a conductive blocking body 206a is formed

over the impact diffusion layer 214a, whereby the wireless chip 200 is completed. The antenna 201 is formed to have a single-layer structure or a layered structure using a conductive material by a CVD method, a sputtering method, a screen printing method, a droplet discharge method, or the like. The conductive material is an element selected 5 from aluminum (Al), titanium (Ti), silver (Ag), copper (Cu), gold (Au), and nickel (Ni), or an alloy or compound material mainly containing any of these elements. The protective film 213 can be formed using any of the above materials for the first interlayer insulating film 211. Note that, the coil antenna 201 wound twice is used as one electrode of the capacitor 215a in FIGS. 1A and 1B; however, an embodiment of the 10 present invention is not limited to this and an antenna wound once or a plurality of times may be used as one electrode of the capacitor 215a. As the impact diffusion layer 214a, for example, a structure body in which a fibrous body is impregnated with an organic resin, or the like can be used. In this case, the impact diffusion layer 214a may be bonded to the protective film 213. The conductive blocking body 206a can be 15 formed by a dry process such as a sputtering method, a plasma CVD method, or an evaporation method, or a wet process such as a coating method, a printing method, or a droplet discharge method (inkjet method).

[0042]

Note that this embodiment describes the case where one of two electrodes of 20 the capacitor 215a is the antenna 201 and the other is the conductive blocking body 206a, and the protective film 213 and the impact diffusion layer 214a are provided between the antenna 201 and the conductive blocking body 206a, but an embodiment of the present invention is not limited to this. A structure may alternatively be employed 25 in which only the protective film 213 or the impact diffusion layer 214a is provided between the electrodes. Still alternatively, an insulating film other than the protective film and the impact diffusion layer described here may be disposed. That is, any other structure than the structure described in this embodiment can be employed as long as a capacitor can be formed.

[0043]

30 With the above structure, a capacitor 215a is formed between the conductive blocking body 206a and the antenna 201, and the number of capacitors in the capacitor 220 of the resonant capacitor portion 204 formed in the chip can be reduced as

compared to the case where the conductive blocking body 206a is not disposed. Accordingly, the size of the wireless chip 200 and the size of the IC chip 202 can be reduced and the limited area in the IC chip and the wireless chip can be utilized efficiently. Further, since the sizes of the IC chip and the wireless chip can be reduced, 5 current consumption can be reduced and thus a communication distance can be prevented from being shortened. Further, by using the conductive blocking body 206a, resistance to static electricity and physical strength of the wireless chip, which becomes a significant problem when the wireless chip is downsized, can be increased.

[0044]

10 [Embodiment 2]

In this embodiment, a wireless chip 200 having a structure different from that of the above embodiment is described with reference to drawings. In specific, the structure will be described in which the antenna 201 is provided as one of two electrodes of the capacitor 215b and the conductive blocking body 206b as the other 15 electrode is disposed below the substrate 203.

[0045]

A structure of the wireless chip 200 of FIG. 2A will be described. FIG. 2B is a cross section taken along line A1-A2 in the wireless chip 200 of FIG. 2A.

[0046]

20 FIGS. 2A and 2B illustrate a structure in which the antenna 201 is provided as one of the two electrodes of the capacitor 215b and the conductive blocking body 206b as the other electrode is disposed below the substrate 203. The wireless chip 200 described in this embodiment includes an antenna 201 and an IC chip 202 that are stacked over the same substrate 203, and the antenna 201 and the IC chip 202 are 25 disposed so as to be at least partially overlapped with each other with an insulating film interposed therebetween. The IC chip 202 includes the resonant capacitor portion 204 in the chip, which is provided with the capacitor 220, and a logic portion 205 including a power supply generating means, a control means, a memory means, and the like. Note that the two terminals of the antenna 201 are electrically connected to the 30 integrated circuit 207 of the logic portion 205. Further, the antenna 201 and the conductive blocking body 206b are disposed with the substrate 203, the first interlayer insulating film 211, the second interlayer insulating film 216, the protective film 213,

the impact diffusion layer 214b, and the like interposed therebetween. Note that the conductive blocking body 206b is provided for the lowermost layer of the wireless chip 200.

[0047]

5 Further, the antenna 201 connected to the integrated circuit 207 is disposed with the second interlayer insulating film 216 interposed therebetween as in the above embodiment. In this embodiment, the impact diffusion layer 214b is formed under the substrate 203, and the conductive blocking body 206b is formed under the impact diffusion layer 214b. The conductive blocking body 206b is not connected to the
10 antenna 201 physically.

[0048]

15 In this embodiment, the conductive blocking body 206b and the antenna 201 function as electrodes with the substrate 203, the first interlayer insulating film 211, the second interlayer insulating film 216, and the impact diffusion layer 214b interposed therebetween, so that the capacitor 215b is formed.

[0049]

20 Note that this embodiment describes the case where one of two electrodes of the capacitor 215b is the antenna 201 and the other is the conductive blocking body 206b, and the substrate 203, the first interlayer insulating film 211, the second interlayer insulating film 216, the protective film 213, the impact diffusion layer 214b, and the like are provided between the antenna 201 and the conductive blocking body 206b, but an embodiment of the present invention is not limited to this. Any other structure than the structure described in this embodiment can be employed as long as a capacitor can be formed.

25 [0050]

With the above structure, a capacitor 215b is formed between the conductive blocking body 206b and the antenna 201 and the number of capacitors in the capacitor 220 of the resonant capacitor portion 204 required to be formed in the chip can be reduced as compared to the case where the conductive blocking body 206b is not disposed. Accordingly, the size of the wireless chip 200 and the size of the IC chip 202 can be reduced and the limited area in the IC chip and the wireless chip can be utilized efficiently. Further, since the sizes of the IC chip and the wireless chip can be

reduced, current consumption can be reduced and thus a communication distance can be prevented from being shortened. Further, by using the conductive blocking body 206b, resistance to static electricity and physical strength of the wireless chip, which becomes a significant problem when the wireless chip is downsized, can be increased. Further, 5 since the conductive blocking body 206b is not provided over the antenna, favorable communication accuracy can be secured without hindering reception of carrier waves or amplitude modulation waves transmitted from a R/W as compared to the structure described in Embodiment 1.

[0051]

10 [Embodiment 3]

In this embodiment, the wireless chip 200 having a structure different from those of Embodiments 1 and 2 is described with reference to drawings. In specific, the wireless chip 200 includes the capacitor 215a and a capacitor 215c. The capacitor 215a has a structure similar to that in Embodiment 1 and is formed to have a layered 15 structure of the antenna 201, the protective film 213, the impact diffusion layer 214a, and the conductive blocking body 206a. Further, the structure will be described in which the antenna 201 is provided as one of two electrodes of the capacitor 215c, and both the conductive blocking body 206a provided over the substrate 203 and the conductive blocking body 206b provided under the substrate 203 are disposed as the 20 other electrodes.

[0052]

A structure of the wireless chip 200 of FIG. 3A will be described. FIG. 3B is a cross section taken along line A1-A2 in the wireless chip 200 of FIG. 3A.

[0053]

25 FIGS. 3A and 3B illustrate a structure including the capacitor 215a and the capacitor 215c. Since the capacitor 215a has a structure similar to that in Embodiment 1, description thereof is omitted here. The structure will be described in which the antenna 201 is provided as one of two electrodes of the capacitor 215c, and both the conductive blocking body 206a provided over the substrate 203 and the conductive 30 blocking body 206b provided under the substrate 203 are disposed as the other electrodes. The wireless chip 200 described in this embodiment includes the antenna 201 and the IC chip 202 that are stacked over the same substrate 203. The antenna 201

and the IC chip 202 are disposed so as to be at least partially overlapped with each other with an insulating film interposed therebetween. The IC chip 202 includes the resonant capacitor portion 204 in the chip, which is provided with the capacitor 220, and the logic portion 205 including a power supply generating means, a control means, 5 a memory means, and the like. Note that both terminals of the antenna 201 are electrically connected to the integrated circuit 207 of the logic portion 205. Further, the antenna 201 and conductive blocking body 206a are disposed with insulating films such as the protective film 213 and the impact diffusion layer 214a and are provided on the uppermost surface of the wireless chip 200. Further, the antenna 201 and the 10 conductive blocking body 206b are provided with the substrate 203, the first interlayer insulating film 211, the second interlayer insulating film 216, the protective film 213, the impact diffusion layer 214b, and the like interposed therebetween. Note that the conductive blocking body 206b is provided for the lowermost layer of the wireless chip 200.

15 [0054]

Further, the antenna 201 connected to the integrated circuit 207 is disposed with the second interlayer insulating film 216 interposed therebetween. The conductive blocking body 206a and the conductive blocking body 206b are not connected to the antenna 201 physically.

20 [0055]

In this embodiment, the conductive blocking body 206a disposed on a top surface of the substrate and the antenna 201 function as electrodes with the protective film 213 and the impact diffusion layer 214a interposed therebetween, so that a resonant capacitor is formed. Further, the conductive blocking body 206b disposed on a bottom 25 surface of the substrate and the antenna 201 function as electrodes with the substrate, the first interlayer insulating film 211, the second interlayer insulating film 216, and the impact diffusion layer 214b interposed therebetween, so that a resonant capacitor is formed. That is, the capacitor 215c includes the resonant capacitor formed between the conductive blocking body 206a and the antenna 201 and the resonant capacitor 30 formed between the conductive blocking body 206b and the antenna 201.

[0056]

Therefore, since many resonant capacitors are formed in this embodiment as

compared to the above embodiment, the number of capacitors in the capacitor 220 of the resonant capacitor portion 204 in the chip can be reduced as compared to that in the above embodiment. Further, since the IC chip 202 is sandwiched between the conductive blocking body 206a and the conductive blocking body 206b, physical strength of the wireless chip can be further increased as compared to the above embodiment.

5 [0057]

Note that the structure described in this embodiment is not necessarily employed. An insulating layer other than the protective film and the impact diffusion layer may be disposed and the protective film and the impact diffusion layer are not necessarily disposed as long as a capacitor can be formed.

10 [0058]

[Embodiment 4]

In this embodiment, a wireless chip 200 having a structure different from those 15 of the above embodiments will be described with reference to drawings. In specific, the structure will be described in which the antenna 201 is provided as one of two electrodes of each of capacitors 215d and 215f, and a conductive blocking body 206c provided as the other electrode is disposed so as to surround the other components included in the wireless chip 200.

20 [0059]

A structure of a wireless chip 200 in FIG. 4A will be described. FIG. 4B is a cross section taken along line A1-A2 in the wireless chip 200 of FIG. 4A.

[0060]

FIGS. 4A and 4B illustrate a structure in which the antenna 201 is provided as 25 one of two electrodes of each of the capacitors 215d and 215f, and the conductive blocking body 206c provided as the other electrode is disposed so as to surround the other components included in the wireless chip 200. The wireless chip 200 described in this embodiment includes the antenna 201 and the IC chip 202 that are stacked over the same substrate 203. The antenna 201 and the IC chip 202 are disposed so as to be 30 at least partially overlapped with each other with an insulating film interposed therebetween. The IC chip 202 includes the resonant capacitor portion 204 in a chip, which is provided with the capacitor 220, and the logic portion 205 including a power

supply generating means, a control means, a memory means, and the like. Note that both terminals of the antenna 201 are electrically connected to the integrated circuit 207 of the logic portion 205. Further, the antenna 201 and the conductive blocking body 206c are disposed with insulating films such as the protective film 213 and the impact diffusion layers 214a and 214b interposed therebetween. Note that the conductive blocking body 206c is provided around the outermost perimeter of the wireless chip 200.

[0061]

Further, the antenna 201 connected to the integrated circuit 207 is disposed with the second interlayer insulating film 216 interposed therebetween. The conductive blocking body 206c is not connected to the antenna 201 physically.

[0062]

In the above structure, the resonant capacitor is formed using the conductive blocking body 206c surrounding the antenna 201; thus, it is very difficult to accurately illustrate the capacitor 215d formed in this embodiment. In FIGS. 4A and 4B, the capacitor 215d is illustrated in a portion where the resonant capacitor is formed, for example.

[0063]

Note that the structure described in this embodiment is not necessarily employed as long as the conductive blocking body 206c can be provided around the IC chip and the capacitors 215d and 215f can be formed using the antenna 201 and the conductive blocking body 206c.

[0064]

With the above structure, many resonant capacitors can be formed as compared to the above embodiments. Further, physical strength can be increased by combining this embodiment and any of the above embodiments.

[0065]

[Embodiment 5]

In this embodiment, the wireless chip 200 having a structure different from those of the above embodiments will be described with reference to drawings. In specific, the structure will be described in which a capacitor 215e in which a wiring 217 of the resonant capacitor portion 204 in the chip, which is formed widely, and the

conductive blocking body 206a are electrodes is provided in addition to the capacitor 215a in which the antenna 201 and the conductive blocking body 206a are electrodes.

[0066]

A structure of the wireless chip 200 in FIG. 5A will be described. FIG. 5B is a 5 cross section taken along line A1-A2 in the wireless chip 200 of FIG. 5A.

[0067]

FIGS. 5A and 5B illustrate the structure in which one of two capacitors of the capacitor 215e has the antenna 201 and the conductive blocking body 206a as electrodes and the other has a wiring 217 of the resonant capacitor portion 204 in the chip, which 10 is formed widely, and the conductive blocking body 206a as electrodes. Note that since the wiring 217 can be formed in the same layer and through the same steps as the source and drain electrodes 212, a special step is not required.

[0068]

The wireless chip 200 described in this embodiment includes the antenna 201 15 and the IC chip 202 that are stacked over the same substrate 203. The antenna 201 and the IC chip 202 are disposed so as to be at least partially overlapped with each other with an insulating film interposed therebetween. The IC chip 202 includes the resonant capacitor portion 204 in the chip and the logic portion 205 including a power supply generating means, a control means, a memory means, and the like. Note that 20 both terminals of the antenna 201 are electrically connected to the integrated circuit 207 of the logic portion 205. Further, the wiring 217 and the conductive blocking body 206a are disposed with insulating films such as the protective film 213, the impact diffusion layer 214a, and the second interlayer insulating film 216 interposed therebetween, and the conductive blocking body 206a is provided on the uppermost 25 surface of the wireless chip 200.

[0069]

Further, the antenna 201 connected to the integrated circuit 207 is disposed with the second interlayer insulating film 216 interposed therebetween, and the conductive blocking body 206a is disposed over the antenna 201 with the protective 30 film 213 and the impact diffusion layer 214a interposed therebetween. The conductive blocking body 206a is not connected to the antenna 201 physically.

[0070]

The capacitor 215e formed in this embodiment includes the capacitor including the antenna 201 and the conductive blocking body 206a as electrodes as in Embodiment 1, and the capacitor including the wiring 217 of the resonant capacitor portion 204 in the chip, in which the wiring 217 is formed widely, and the conductive blocking body 206a as electrodes.

[0071]

Note that although the structure is described in which the conductive blocking body 206a is provided on an outermost surface as in Embodiment 1, this embodiment can also be implemented in free combination with any of Embodiments 2 to 4. Further, the structure described in this embodiment is not necessarily employed as long as the capacitor 215e can be formed.

[0072]

With the above structure, the number of capacitors in the chip can be reduced as compared to the case where the conductive blocking body 206a is not provided, which results in reduction in the size of the wireless chip 200 and the size of the IC chip 202, effective utilization of the limited area in the IC chip, reduction in current consumption, and prevention of shortening of a communication distance. Further, by using the conductive blocking body 206a, resistance to static electricity and physical strength of the wireless chip, which becomes a significant problem when the wireless chip is downsized, can be increased.

[0073]

Further, more capacitors can be formed as compared to Embodiments 1 to 4 which do not employ this structure by combining this structure with any of Embodiments 1 to 4.

[0074]

[Embodiment 6]

This embodiment will describe a method for manufacturing a semiconductor device with high reliability and high yield with reference to FIGS. 6A to 6D. Note that although the structure including a substrate is described in Embodiments 1 to 5, this embodiment will describe a method for manufacturing a semiconductor device from which a substrate is separated. Note that any of Embodiments 1 to 5 can be freely combined with this embodiment. Further, this embodiment will describe a CMOS

(complementary metal oxide semiconductor) as an example of semiconductor devices.

[0075]

Transistors 902 and 903, a capacitor 904, and an insulating layer 905 are provided over a substrate 900 with a separation layer 901 interposed therebetween, so that a semiconductor integrated circuit 910 is formed (see FIG. 6A). Note that in this embodiment, since a capacitor using a resonant capacitor formed in an IC chip is formed, the capacitor 904 can be smaller than a conventional capacitor.

[0076]

The transistors 902 and 903 are thin film transistors and each include source and drain regions, a low concentration impurity region, a channel formation region, a gate insulating layer, a gate electrode, wirings serving as source and drain electrodes. The source and drain regions are in contact with and electrically connected with the wirings serving as source and drain electrodes.

[0077]

The transistor 902 is an n-channel transistor and the source or drain region and the low concentration impurity region include impurity elements imparting n-type conductivity (such as phosphorus (P) or arsenic (As)). The transistor 903 is a p-channel transistor and the source or drain region and the low concentration impurity region include impurities imparting p-type conductivity (such as boron (B), aluminum (Al), or gallium (Ga)).

[0078]

The capacitor 904 is formed through the same steps as the transistors 902 and 903 and one electrode is formed of a semiconductor layer and the other electrode is formed of the gate electrode. In this case, to secure a capacitance value efficiently, an impurity element may be added to the semiconductor layer included in the capacitor 904 before a gate electrode layer is formed. Through this step, an impurity element is added also to the semiconductor layer disposed in a region of a lower layer of the gate electrode layer, and thus the capacitor 904 can function efficiently as a capacitor.

[0079]

Next, an antenna 911 is formed over the insulating layer 905 by using a conductive film, and a protective film 912 is formed over the antenna 911. The antenna 911 is electrically connected to the semiconductor integrated circuit. In FIG.

6A, the antenna 911 is electrically connected to one electrode of the capacitor 904.

[0080]

Next, an impact diffusion layer 920 is formed over the protective film 912. As the impact diffusion layer 920, for example, a structure body in which a fibrous body 921 is impregnated with an organic resin 922 may be used.

[0081]

After the protective film 912 and the impact diffusion layer 920 are bonded together, the semiconductor integrated circuit 910, the antenna 911, and the protective film 912 are separated from the substrate 900 along the separation layer 901 as an interface. Accordingly, the semiconductor integrated circuit 910, the antenna 911, and the protective film 912 are provided on the impact diffusion layer 920 side (see FIG. 6B).

[0082]

Although not illustrated particularly, bonding of the protective film 912 and the impact diffusion layer 920 may be performed using an adhesive, pressure bonding, or thermocompression bonding.

[0083]

After that, an impact diffusion layer 930 is bonded to an exposed separation surface of the semiconductor integrated circuit 910 with the separation layer 901 interposed therebetween, so that the semiconductor integrated circuit 910, the antenna 911, and the protective film 912 are sandwiched between the impact diffusion layer 920 and the impact diffusion layer 930 (see FIG. 6C).

[0084]

As the impact diffusion layer 930, for example, a structure body in which a fibrous body 931 is impregnated with an organic resin 932 may be used, similarly to the case of the impact diffusion layer 920.

[0085]

Although there is no particular illustration, the impact diffusion layer 920 and the impact diffusion layer 930 sandwich a plurality of structure bodies each including the semiconductor integrated circuit 910, the antenna 911, and the protective film 912 so that they are arranged in a planar direction. By division, individual semiconductor integrated circuit chips each having a structure in which the semiconductor integrated

circuit 910, the antenna 911, and the protective film 912 are sandwiched between the impact diffusion layer 920 and the impact diffusion layer 930 are manufactured. There is no particular limitation on a dividing means as long as physical division is possible, and as a favorable example, division is performed by laser beam irradiation along a 5 dividing line in this embodiment.

[0086]

By division by laser beam irradiation, the impact diffusion layer 920 and the impact diffusion layer 930 melt and weld together at dividing surfaces 941 and 942 of the semiconductor integrated circuit chip. Thus, the individual semiconductor 10 integrated circuit chips each have a structure in which the semiconductor integrated circuit 910, the antenna 911, and the protective film 912 are entirely sealed with the impact diffusion layer 920 and the impact diffusion layer 930 (see FIG. 6D).

[0087]

Although not illustrated particularly, an insulator may be further provided on 15 outer sides or inner sides than the impact diffusion layer 920 and the impact diffusion layer 930 to cover the entire surfaces of the semiconductor integrated circuit 910, the antenna 911, and the protective film 912 more favorably.

[0088]

Finally, a conductive blocking body 1101 is provided as illustrated in FIG. 7A, 20 so that the semiconductor device of this embodiment is completed. Note that although FIG. 7A illustrates an example in which the conductive blocking body 1101 is formed so as to entirely cover the outside similarly to the structure described in Embodiment 4, the structure described as an example in any of the other embodiments may be employed. Note that in FIG. 7A, the conductive blocking body 1101 is formed so as to cover a top 25 surface, a bottom surface, and side surfaces of the semiconductor integrated circuit chip. The conductive blocking body 1101 may be formed so as to cover the entire surfaces by forming the conductive blocking body on the top surface and part of the side surfaces and then turning over the semiconductor integrated circuit and forming the conductive blocking body on the bottom surface and part of the side surfaces.

30 [0089]

The conductive blocking body 1101 may be formed to a thickness small enough that reception of carrier waves or amplitude modulation waves transmitted from

a R/W is not hindered as much as possible.

[0090]

Alternatively, as illustrated in FIG. 7B, a conductive blocking body 1102 may be provided on inner sides than impact diffusion layers so as to cover an entire surface of the semiconductor integrated circuit. To thus form the conductive blocking body 1102 so as to cover the entire surface of the semiconductor integrated circuit, it is required that individual semiconductor integrated circuit chips are formed by division before the semiconductor integrated circuit is sandwiched between the impact diffusion layers and bonding is performed; however, this mode is not necessarily employed. For example, the following method may be employed: a conductive blocking body is formed in advance on a top surface and a bottom surface of the semiconductor integrated circuit before the semiconductor integrated circuit chip is sandwiched between impact diffusion layers and bonding is performed, the semiconductor integrated circuit chip is sandwiched between impact diffusion layers and bonding is performed, and then division is performed by laser beam irradiation, so that the conductive blocking bodies melt at dividing surfaces and weld so as to cover side surfaces of the semiconductor integrated circuit from above and below.

[0091]

FIG. 7C is an example in which a conductive blocking body 1103 is provided on an inner side than an impact diffusion layer so that it is formed on one surface of a semiconductor integrated circuit. In this example, the conductive blocking body 1103 is formed on the antenna side as in Embodiment 1; however, the conductive blocking body 1103 may be formed on the separation surface side as in Embodiment 2.

[0092]

By forming the conductive blocking body on one surface of the semiconductor integrated circuit, the conductive blocking body does not hinder reception of carrier waves or amplitude modulation waves transmitted from a R/W and thus favorable communication accuracy can be secured.

[0093]

By such a formation method, impact diffusion layers are provided with a semiconductor integrated circuit interposed therebetween; therefore, adverse effects such as a damage and a characteristic defect of the semiconductor integrated circuit due

to external stress or stress can be prevented also in the manufacturing process. Thus, a semiconductor device can be manufactured with high reliability and high yield.

[0094]

5 Note that the semiconductor device manufactured according to this embodiment can be flexible by using a flexible impact diffusion layer.

[0095]

10 Semiconductor layers included in the transistors 902 and 903 and the capacitor 904 can be formed using any of the following materials: an amorphous semiconductor manufactured by a vapor-phase growth method or a sputtering method using a semiconductor material gas typified by silane or germane; a polycrystalline semiconductor formed by crystallizing the amorphous semiconductor with the use of light energy or thermal energy; a microcrystalline (also referred to as semiamorphous) semiconductor; or the like. The semiconductor layer can be formed by a sputtering method, an LPCVD method, a plasma CVD method, or the like.

15 [0096]

20 The microcrystalline semiconductor film belongs to a metastable state which is intermediate between an amorphous state and a single crystal state when Gibbs free energy is considered. That is, the microcrystalline semiconductor film is a semiconductor having a third state which is stable in terms of free energy and has a short range order and lattice distortion. Columnar-like or needle-like crystals grow in a normal direction with respect to a substrate surface. The Raman spectrum of 25 microcrystalline silicon, which is a typical example of a microcrystalline semiconductor, is shifted to a lower wavenumber than 520 cm^{-1} which represents a peak of the Raman spectrum of single crystal silicon. That is to say, a peak of the Raman spectrum of microcrystalline silicon lies between 520 cm^{-1} and 480 cm^{-1} which represent that of 30 single crystal silicon and that of amorphous silicon, respectively. The microcrystalline semiconductor film contains hydrogen or halogen of at least 1 at.% to terminate dangling bonds. Further, a rare gas element such as helium, argon, krypton, or neon may be contained to further promote lattice distortion, so that stability is enhanced and a favorable microcrystalline semiconductor film can be obtained.

[0097]

The microcrystalline semiconductor film can be formed by a high-frequency

plasma CVD method with a frequency of several tens of MHz to several hundred MHz or a microwave plasma CVD apparatus with a frequency of 1 GHz or more. The microcrystalline semiconductor film can be typically formed using silicon hydride such as SiH₄, Si₂H₆, SiH₂Cl₂, SiHCl₃, SiCl₄, or SiF₄ which is diluted with hydrogen.

5 Alternatively, with a dilution with one or plural kinds of rare gas elements selected from helium, argon, krypton, and neon in addition to silicon hydride and hydrogen, the microcrystalline semiconductor film can be formed. In that case, the flow ratios of hydrogen to silicon hydride is set to be from 5 : 1 to 200 : 1, preferably, from 50 : 1 to 150 : 1, more preferably, the flow ratio of hydrogen to silicon hydride is set to be 100 :
10 1.

[0098]

Hydrogenated amorphous silicon may be typically used as an amorphous semiconductor, while polysilicon (polycrystalline silicon) and the like may be typically used as a crystalline semiconductor. As examples of polysilicon, so-called 15 high-temperature polysilicon which contains polysilicon as a main component and is formed at a process temperature of 800°C or higher, so-called low-temperature polysilicon that contains polysilicon as a main component and is formed at a process temperature of 600°C or lower, polysilicon obtained by crystallizing amorphous silicon by using an element promoting crystallization or the like, and the like are given. It is 20 needless to say that as mentioned above, a microcrystalline semiconductor or a semiconductor containing a crystal phase in part of a semiconductor layer may be used.

[0099]

As a material of the semiconductor, as well as an elementary substance of silicon (Si), germanium (Ge), or the like, a compound semiconductor such as GaAs, InP, 25 SiC, ZnSe, GaN, or SiGe can be used. Alternatively, an oxide semiconductor such as zinc oxide (ZnO), tin oxide (SnO₂), magnesium zinc oxide, gallium oxide, or indium oxide, an oxide semiconductor formed of any of the above oxide semiconductors, or the like may be used. For example, an oxide semiconductor formed of ZnO, indium oxide, and gallium oxide may be used. Note that in the case of using ZnO for the 30 semiconductor layer, a gate insulating layer is preferably formed using Y₂O₃, Al₂O₃, TiO₂, or a stack of any of the above. For the gate electrode layer, the source electrode

layer, and the drain electrode layer, indium tin oxide (ITO), Au, Ti, or the like is preferably used. Alternatively, ZnO to which In, Ga, or the like is added may be used.

[0100]

In the case of using a crystalline semiconductor layer for the semiconductor layer, the crystalline semiconductor layer may be formed by any of various methods (such as a laser crystallization method, a thermal crystallization method, and a thermal crystallization method using an element promoting crystallization, such as nickel). Further, a microcrystalline semiconductor may be crystallized by laser irradiation to enhance crystallinity. In the case where the element promoting crystallization is not introduced, before irradiating the amorphous silicon film with a laser beam, hydrogen is released until the concentrations of hydrogen contained in the amorphous silicon film become 1×10^{20} atoms/cm³ or less by heating the amorphous silicon film at a temperature of 500°C for one hour in a nitrogen atmosphere. This is because the amorphous silicon film containing a large amount of hydrogen is destroyed when being irradiated with a laser beam.

[0101]

A method for introducing a metal element into the amorphous semiconductor layer is not particularly limited as long as it is capable of introducing the metal element to a surface of or inside the amorphous semiconductor layer. For example, a sputtering method, a CVD method, a plasma treatment method (including a plasma CVD method), an adsorption method, or a method for applying a solution of metal salt can be used. Among them, a method of using a solution is simple and advantageous in that the concentration of the metal element can be easily controlled. At this time, it is desirable to form an oxide film by UV irradiation in an oxygen atmosphere, a thermal oxidation method, treatment with either ozone water containing hydroxyl radicals or hydrogen peroxide, or the like to improve wettability of the surface of the amorphous semiconductor layer so that an aqueous solution is diffused on the entire surface of the amorphous semiconductor layer.

[0102]

In a crystallization step in which an amorphous semiconductor layer is crystallized to form a crystalline semiconductor layer, an element promoting

crystallization (also referred to as a catalytic element or a metal element) may be added to the amorphous semiconductor layer and crystallization may be performed by heat treatment (at 550°C to 750°C for 3 minutes to 24 hours). The element promoting crystallization can be one or more of elements such as iron (Fe), nickel (Ni), cobalt (Co),
5 ruthenium (Ru), rhodium (Rh), palladium (Pd), osmium (Os), iridium (Ir), platinum (Pt), copper (Cu), and gold (Au).

[0103]

In order to remove or reduce the element promoting crystallization from the crystalline semiconductor layer, a semiconductor layer containing an impurity element 10 is formed in contact with the crystalline semiconductor layer and is made to function as a gettering sink. As the impurity element, an impurity element imparting n-type conductivity, an impurity element imparting p-type conductivity, a rare gas element, or the like can be used; for example, one or more of phosphorus (P), nitrogen (N), arsenic (As), antimony (Sb), bismuth (Bi), boron (B), helium (He), neon (Ne), argon (Ar),
15 krypton (Kr), and xenon (Xe) can be used. A semiconductor layer containing a rare gas element is formed on the crystalline semiconductor layer containing the element promoting crystallization, and heat treatment (at 550°C to 750°C for 3 minutes to 24 hours) is performed. The element promoting crystallization, which is contained in the crystalline semiconductor layer, moves into the semiconductor layer containing a rare gas element and thus, the element promoting crystallization, which is contained in the crystalline semiconductor layer, is removed or reduced. After that, the semiconductor layer containing a rare gas element, which has served as a gettering sink, is removed.
20

[0104]

An amorphous semiconductor layer may be crystallized by the combination of
25 heat treatment and laser beam irradiation, or one of heat treatment and laser beam irradiation may be performed a plurality of times.

[0105]

A crystalline semiconductor layer may be directly formed on a substrate by a plasma method. Alternatively, a crystalline semiconductor layer may be selectively
30 formed over a substrate by a plasma method.

[0106]

The gate insulating layer may be formed using silicon oxide or may be formed to have a layered structure including silicon oxide and silicon nitride. The gate insulating layer may be formed by depositing an insulating film by a plasma CVD method or a low pressure CVD method or may be formed by solid-phase oxidation or solid-phase nitridation by plasma treatment. This is because a gate insulating layer which is formed using a single crystal semiconductor layer which is oxidized or nitrided by plasma treatment is dense, has high withstand voltage, and is excellent in reliability. For example, a surface of the semiconductor layer is oxidized or nitrided using nitrous oxide (N₂O) diluted with Ar by 1 to 3 times (flow ratio) by application of microwave (2.45 GHz) powers of 3 kW to 5 kW at pressures of 10 Pa to 30 Pa. By this treatment, an insulating film with thicknesses of 1 nm to 10 nm (preferably, 2 nm to 6 nm) is formed. Further, nitrous oxide (N₂O) and silane (SiH₄) are introduced and microwave (2.45 GHz) powers of 3 kW to 5 kW are applied to the insulating film at pressures of 10 Pa to 30 Pa to form a silicon oxynitride film by a vapor-phase growth method, which is to be a gate insulating layer. With a combination of a solid-phase reaction and a reaction by a vapor-phase growth method, the gate insulating layer with low interface state density and an excellent withstand voltage can be formed.

[0107]

As the gate insulating layer, a high dielectric constant material such as zirconium dioxide, hafnium oxide, titanium dioxide, or tantalum pentoxide may be used. By using a high dielectric constant material for the gate insulating layer, a gate leakage current can be reduced.

[0108]

The gate electrode layer can be formed employing a CVD method, a sputtering method, a droplet discharge method, or the like. The gate electrode layer may be formed of an element selected from Ag, Au, Cu, Ni, Pt, Pd, Ir, Rh, W, Al, Ta, Mo, Cd, Zn, Fe, Ti, Si, Ge, Zr, and Ba; or an alloy or compound material containing any of the elements as its main component. Alternatively, a semiconductor film typified by a polycrystalline silicon film doped with an impurity element such as phosphorus, or an AgPdCu alloy may be used. Further, either a single-layer structure or a multi-layer structure may be employed; for example, a two-layer structure of a tungsten nitride film and a molybdenum film may be employed or a three-layer structure in which a tungsten

film with a thickness of 50 nm, a film of an aluminum-silicon (Al-Si) alloy with a thickness of 500 nm, and a titanium nitride film with a thickness of 30 nm are stacked in this order may be employed. In the case of the three-layer structure, a tungsten nitride film may be used instead of the tungsten film as the first conductive film, an 5 aluminum-titanium (Al-Ti) alloy film may be used instead of the aluminum-silicon (Al-Si) alloy film as the second conductive film, and a titanium film may be used instead of the titanium nitride film as the third conductive film.

[0109]

As the gate electrode layer, a light-transmitting material which transmits visible 10 light may be used. As a light-transmitting conductive material, indium tin oxide (ITO), indium tin oxide containing silicon oxide (ITSO), organoindium, organotin, zinc oxide, or the like can be used. Alternatively, indium zinc oxide (IZO) containing zinc oxide (ZnO), zinc oxide (ZnO), ZnO doped with gallium (Ga), tin oxide (SnO₂), indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide 15 containing titanium oxide, indium tin oxide containing titanium oxide, or the like may be used.

[0110]

In the case where etching processing is needed to form the gate electrode layer, a mask may be formed and dry etching or wet etching may be performed. The 20 electrode layers can be etched to have a tapered shape by using an ICP (inductively coupled plasma) etching method and appropriately controlling the etching condition (the amount of power applied to a coiled electrode, the amount of power applied to an electrode on a substrate side, the temperature of the electrode on the substrate side, or the like). Note that as an etching gas, a chlorine-based gas typified by Cl₂, BCl₃, SiCl₄, 25 CCl₄, and the like; a fluorine-based gas typified by CF₄, SF₆, NF₃, and the like; or O₂ can be used as appropriate.

[0111]

Although a single-gate structure is described as a transistor structure in this embodiment, a multi-gate structure such as a double-gate structure may alternatively be 30 employed. In this case, gate electrode layers may be provided above and below the semiconductor layer or a plurality of gate electrode layers may be provided only on one side of (above or below) the semiconductor layer.

[0112]

Alternatively, silicides may be provided over the source and drain regions of the transistor. The silicides are formed by forming conductive films over the source and drain regions of the semiconductor layer and reacting silicon in the exposed source and drain regions of the semiconductor layer with the conductive films by heat treatment, a GRTA method, an LRTA method, or the like. Alternatively, the silicides may be formed by laser irradiation or light irradiation using a lamp. As a material used for forming the silicide, any of the followings can be used: titanium (Ti), nickel (Ni), tungsten (W), molybdenum (Mo), cobalt (Co), zirconium (Zr), hafnium (Hf), tantalum (Ta), vanadium (V), neodymium (Nd), chromium (Cr), platinum (Pt), palladium (Pd), and the like.

[0113]

The wiring layers each function as a source electrode layer or a drain electrode layer can be formed by depositing a conductive film by a PVD method, a CVD method, an evaporation method, or the like, and then etching the conductive film such that it has desired shapes. Alternatively, the wiring layer can be formed selectively at a predetermined place by a printing method, an electroplating method, or the like. Alternatively, a reflow method or a damascene method may be used. As a material of the wiring layers, metal such as Ag, Au, Cu, Ni, Pt, Pd, Ir, Rh, W, Al, Ta, Mo, Cd, Zn, Fe, Ti, Zr, or Ba, a semiconductor such as Si or Ge, or an alloy or a nitride thereof may be used. Alternatively, a light-transmitting material may be used.

[0114]

As the light-transmitting conductive material, indium tin oxide (ITO), indium tin oxide containing silicon oxide (ITSO), indium zinc oxide (IZO) containing zinc oxide (ZnO), zinc oxide (ZnO), ZnO doped with gallium (Ga), tin oxide (SnO₂), indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, or the like can be used.

[0115]

30 A material for forming the conductive blocking body is preferably a conductor or a semiconductor; for example, a metal film, a metal oxide film, a semiconductor film, a metal nitride film, and the like are given. Specifically, the conductive blocking body

may be formed using an element selected from titanium, molybdenum, tungsten, aluminum, copper, silver, gold, nickel, platinum, palladium, iridium, rhodium, tantalum, cadmium, zinc, iron, silicon, germanium, zirconium, and barium; or an alloy material, a compound material, a nitride material, or an oxide material each containing any of the
5 above elements as a main component.

[0116]

As the nitride material, tantalum nitride, titanium nitride, or the like can be used.

[0117]

10 As the oxide material, indium tin oxide (ITO), indium tin oxide containing silicon oxide (ITSO), organoindium, organotin, zinc oxide, or the like can be used. Alternatively, indium zinc oxide (IZO) containing zinc oxide (ZnO), zinc oxide (ZnO), ZnO containing gallium (Ga), tin oxide (SnO₂), indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide,
15 indium tin oxide (ITO) containing titanium oxide, or the like may be used.

[0118]

20 Alternatively, a semiconductor film having conductivity, which is obtained by adding an impurity element or the like to a semiconductor, or the like can be used. For example, a polycrystalline silicon film doped with an impurity element such as phosphorus can be used.

[0119]

25 Still alternatively, a conductive macromolecule (also referred to as a conductive polymer) may be used for the conductive blocking body. As the conductive macromolecule, a so-called π -electron conjugated conductive macromolecule can be used. For example, polyaniline and/or a derivative thereof, polypyrrole and/or a derivative thereof, polythiophene and/or a derivative thereof, and a copolymer of two or more kinds of those materials can be given.

[0120]

30 Specific examples of a conjugated conductive macromolecule are as follows: polypyrrole, poly(3-methylpyrrole), poly(3-butylpyrrole), poly(3-octylpyrrole), poly(3-decylpyrrole), poly(3,4-dimethylpyrrole), poly(3,4-dibutylpyrrole), poly(3-hydroxypyrrrole), poly(3-methyl-4-hydroxypyrrrole), poly(3-methoxypyrrrole),

poly(3-ethoxypyrrole), poly(3-octoxypyrrole), poly(3-carboxylpyrrole),
poly(3-methyl-4-carboxylpyrrole), polyN-methylpyrrole, polythiophene,
poly(3-methylthiophene), poly(3-butylthiophene), poly(3-octylthiophene),
poly(3-decylthiophene), poly(3-dodecylthiophene), poly(3-methoxythiophene),
5 poly(3-ethoxythiophene), poly(3-octoxythiophene), poly(3-carboxylthiophene),
poly(3-methyl-4-carboxylthiophene), poly(3,4-ethylenedioxythiophene), polyaniline,
poly(2-methylaniline), poly(2-octylaniline), poly(2-isobutylaniline),
poly(3-isobutylaniline), poly(2-anilinesulfonic acid), and poly(3-anilinesulfonic acid).

[0121]

10 The conductive blocking body containing a conductive macromolecule may contain an organic resin or a dopant (a halogen, a Lewis acid, an inorganic acid, an organic acid, a transition metal halide, an organic cyano compound, a nonionic surfactant, or the like).

[0122]

15 The conductive blocking body can be formed by a dry process such as a sputtering method, a plasma CVD method, or an evaporation method, or a wet process such as a coating method, a printing method, or a droplet discharge method (inkjet method).

[0123]

20 (Embodiment 7)

According to an embodiment of the present invention, a semiconductor device that serves as a wireless tag (hereinafter also referred to as a wireless chip, a wireless processor, or a wireless memory) can be formed. The application range of the semiconductor device according to an embodiment of the present invention is so wide 25 that it may be applied to any object in order that the history thereof or the like is revealed without contact and utilized in production, management, and the like. For example, the semiconductor device may be incorporated in bills, coins, securities, certificates, bearer bonds, containers for packages, books, recording media, personal belongings, vehicles, groceries, garments, healthcare items, daily commodities, 30 medicals, electronic appliances, or the like. These examples are described with reference to FIGS. 8A to 8G.

[0124]

The bills and coins are money that circulates in the market, and includes one that can be used in the same way as money in a specific area (cash voucher), a commemorative coin, and the like. The securities include checks, certificates, promissory notes, and the like and can each be provided with a chip 1001 including a processor circuit (see FIG. 8A). The certificates refer to driver's licenses, certificates of residence, and the like and can each be provided with a chip 1002 including a processor circuit (see FIG. 8B). The personal belongings include bags, pairs of glasses, and the like and can each be provided with a chip 1003 including a processor circuit (see FIG. 8C). The bearer bonds refer to stamps, rice coupons, various merchandise coupons, and the like. The containers for packages refer to wrapping paper for food containers, plastic bottles, and the like and can each be provided with a chip 1004 including a processor circuit (see FIG. 8D). The books refer to hardbacks, paperbacks, and the like and can each be provided with a chip 1005 including a processor circuit (see FIG. 8E). The recording media refer to DVD software, video tapes, and the like and can each be provided with a chip 1006 including a processor circuit (see FIG. 8F). The vehicles refer to wheeled vehicles such as bicycles, ships, and the like and can each be provided with a chip 1007 including a processor circuit (see FIG. 8G). The groceries indicate foods, beverages, and the like. The garments indicate clothes, shoes, and the like. The healthcare items indicate a medical apparatus, a health appliance, and the like. The daily commodities indicate furniture, lighting apparatus, and the like. The medicals indicate a drug, an agricultural chemical, and the like. The electronic appliances indicate a liquid crystal display device, an EL display device, television sets (a television receiver and a thin television receiver), a cellular phone, and the like.

[0125]

The semiconductor device can be provided by being attached to the surface of an article or being embedded in an article. For example, in the case of a book, the semiconductor device may be embedded in the paper; and in the case of a package made of an organic resin, the semiconductor device may be embedded in the organic resin.

[0126]

As described above, the efficiency of an inspection system, a system used in a rental shop, or the like can be improved by providing the containers for packages, the recording media, the personal belongings, the groceries, the garments, the daily

commodities, the electronic appliances, or the like with the semiconductor devices. In addition, by providing the vehicles with the semiconductor devices, forgery or theft can be prevented. In addition, when the semiconductor devices are implanted into creatures such as animals, each creature can be identified easily. For example, by 5 implanting/attaching the semiconductor device with a sensor in/to a creature such as livestock, its health condition such as a current body temperature as well as its birth year, sex, breed, or the like can be easily managed.

[0127]

Note that this embodiment can be implemented in combination with any of 10 Embodiments 1 to 7 and Example 1, as appropriate.

[Example 1]

[0128]

Example 1 will describe results obtained by measuring and comparing resonant capacitance in IC chips of a wireless chip having a structure in which a conductive 15 blocking body is provided on top and bottom surfaces of the IC chip, which is described in Embodiment 3, and a wireless chip provided with no conductive blocking body.

[0129]

FIG. 9 shows results of measurement of resonant frequencies with respect to 20 resonant capacitance in the IC chips of the wireless chip provided with a conductive blocking body, according to an embodiment of the present invention, and the conventional wireless chip provided with no conductive blocking body. Each of the wireless chips has an antenna with a size (a length from one edge to the other edge of the outermost perimeter of the antenna) of 6 mm. Resonant frequencies (MHz) are plotted on the vertical axis with in-chip resonant capacitance (pF) represented on the 25 horizontal axis.

[0130]

Note that as for the antennas used for measurement in this case, the line width is 135 μ m, the distance between lines is 5 μ m, and the number of coils is 15. Further, the antenna used for measurement in this case is formed using Al to a thickness of 5 μ m. 30 Measurement on the wireless chip provided with a conductive blocking body, according to an embodiment of the present invention, and the conventional wireless chip provided

with no conductive blocking body is performed under the condition that in-chip resonant capacitance in the IC chips are 24, 32, and 42 pF.

[0131]

For example, in the case where a desired resonant frequency is 13.5 MHz, 5 in-chip resonant capacitance required in the wireless chip provided with a conductive blocking body, according to an embodiment of the present invention, is about 29 pF. On the other hand, in-chip resonant capacitance required in the wireless chip provided with no conductive blocking body is about 35 pF.

[0132]

10 That is to say, by providing a conductive blocking body, in-chip resonant capacitance can be reduced by about 6 pF.

[0133]

15 Next, FIG. 10 shows results of measurement of resonant frequencies with respect to resonant capacitance in the IC chips of the wireless chips each having an antenna with a size (a length from one edge to the other edge of the outermost perimeter of the antenna) of 8 mm. Note that resonant frequencies are plotted on the vertical axis with in-chip resonant capacitance represented on the horizontal axis.

[0134]

20 Note that as for the antennas used for measurement in this case, the line width is 105 μ m, the distance between lines is 5 μ m, and the number of coils is 17. The antenna is formed using Al to a thickness of 5 μ m. Measurement on the wireless chip provided with a conductive blocking body, according to an embodiment of the present invention, and the conventional wireless chip provided with no conductive blocking body is performed under the condition that in-chip resonant capacitance in the IC chips 25 are 20, 28, and 38 pF.

[0135]

For example, in the case where a desired resonant frequency is 13.5 MHz, 30 in-chip resonant capacitance required in the wireless chip provided with a conductive blocking body is about 24 pF. On the other hand, in-chip resonant capacitance required in the wireless chip provided with no conductive blocking body is about 35 pF.

[0136]

That is to say, by providing a conductive blocking body, in-chip resonant capacitance can be reduced by about 11 pF.

[0137]

According to the measurement results shown in FIGS. 9 and 10, it is
5 understood that provision of a conductive blocking body can reduce resonant capacitance in the IC chip, which leads to downsizing of the IC chip.

CLAIMS

1. A semiconductor device comprising:

a first conductive blocking body;

a first insulating film provided over the first conductive blocking body;

5 an IC chip provided with an integrated circuit and a resonant capacitor portion including a wiring, the IC chip being provided over the first insulating film;

an antenna provided over the IC chip;

a second insulating film provided over the antenna; and

a second conductive blocking body provided over the second insulating film,

10 wherein the first conductive blocking body and the antenna are provided so as to be at least partially overlapped with each other with the first insulating film interposed therebetween,

wherein the second conductive blocking body and the antenna are provided so as to be at least partially overlapped with each other with the second insulating film 15 interposed therebetween, and

wherein the wiring, the second insulating film, and the second conductive blocking body constitute a capacitor.

2. The semiconductor device according to claim 1,

20 wherein the first insulating film and the second insulating film each include an impact diffusion layer.

3. The semiconductor device according to claim 2,

wherein the impact diffusion layer is a structure body in which a fibrous body 25 is impregnated with an organic resin.

4. A semiconductor device comprising:

a first conductive blocking body;

a first insulating film provided over the first conductive blocking body;

30 an IC chip provided with an integrated circuit, the IC chip being provided over the first insulating film;

an antenna provided over the IC chip;

a second insulating film provided over the antenna; and
a second conductive blocking body provided over the second insulating film,
wherein the first conductive blocking body and the antenna are provided so as
to be at least partially overlapped with each other with the first insulating film
5 interposed therebetween,

wherein the second conductive blocking body and the antenna are provided so
as to be at least partially overlapped with each other with the second insulating film
interposed therebetween,

10 wherein the first conductive blocking body, the first insulating film, and the
antenna constitute a first capacitor, and

wherein the second conductive blocking body, the second insulating film, and
the antenna constitute a second capacitor.

5. The semiconductor device according to claim 4,

15 wherein the first insulating film and the second insulating film each include an
impact diffusion layer.

6. The semiconductor device according to claim 5,

20 wherein the impact diffusion layer is a structure body in which a fibrous body
is impregnated with an organic resin.

7. A semiconductor device comprising:

an IC chip provided with an integrated circuit;

an antenna provided over the IC chip; and

25 a conductive blocking body provided so as to at least partially overlap the
antenna with an insulating film interposed therebetween,

wherein the antenna, the insulating film over the antenna, and the conductive
blocking body over the insulating film constitute a first capacitor.

30 8. The semiconductor device according to claim 7,

wherein the IC chip is further provided with a resonant capacitor portion.

9. The semiconductor device according to claim 8,
wherein the resonant capacitor portion includes a wiring, and
wherein the resonant capacitor portion, the insulating film, and the conductive
blocking body constitute a second capacitor.

5

10. The semiconductor device according to claim 7,
wherein the insulating film includes an impact diffusion layer.

10

11. A semiconductor device comprising:
a conductive blocking body;
an insulating film provided over the conductive blocking body;
an IC chip provided with an integrated circuit, the IC chip being provided over
the insulating film; and
an antenna provided over the IC chip,

15

wherein the conductive blocking body and the antenna are provided so as to be
at least partially overlapped with each other with the insulating film interposed
therebetween, and

wherein the conductive blocking body, the insulating film, and the antenna
constitute a first capacitor.

20

12. The semiconductor device according to claim 11,
wherein the IC chip is further provided with a resonant capacitor portion.

25

13. The semiconductor device according to claim 12,
wherein the resonant capacitor portion includes a wiring, and
wherein the resonant capacitor portion, the insulating film, and the conductive
blocking body constitute a second capacitor.

30

14. The semiconductor device according to claim 11,
wherein the insulating film includes an impact diffusion layer.

15. A semiconductor device comprising:

an IC chip provided with an integrated circuit;
an antenna provided over the IC chip;
an insulating film provided so as to surround the IC chip and the antenna; and
a conductive blocking body provided so as to surround the insulating film,
5 wherein the antenna, the insulating film, and the conductive blocking body
constitute a first capacitor.

16. The semiconductor device according to claim 15,
wherein the IC chip is further provided with a resonant capacitor portion.

10
17. The semiconductor device according to claim 16,
wherein the resonant capacitor portion includes a wiring, and
wherein the resonant capacitor portion, the insulating film, and the conductive
blocking body constitute a second capacitor.

15
18. The semiconductor device according to claim 15,
wherein the insulating film includes an impact diffusion layer.

FIG. 1A

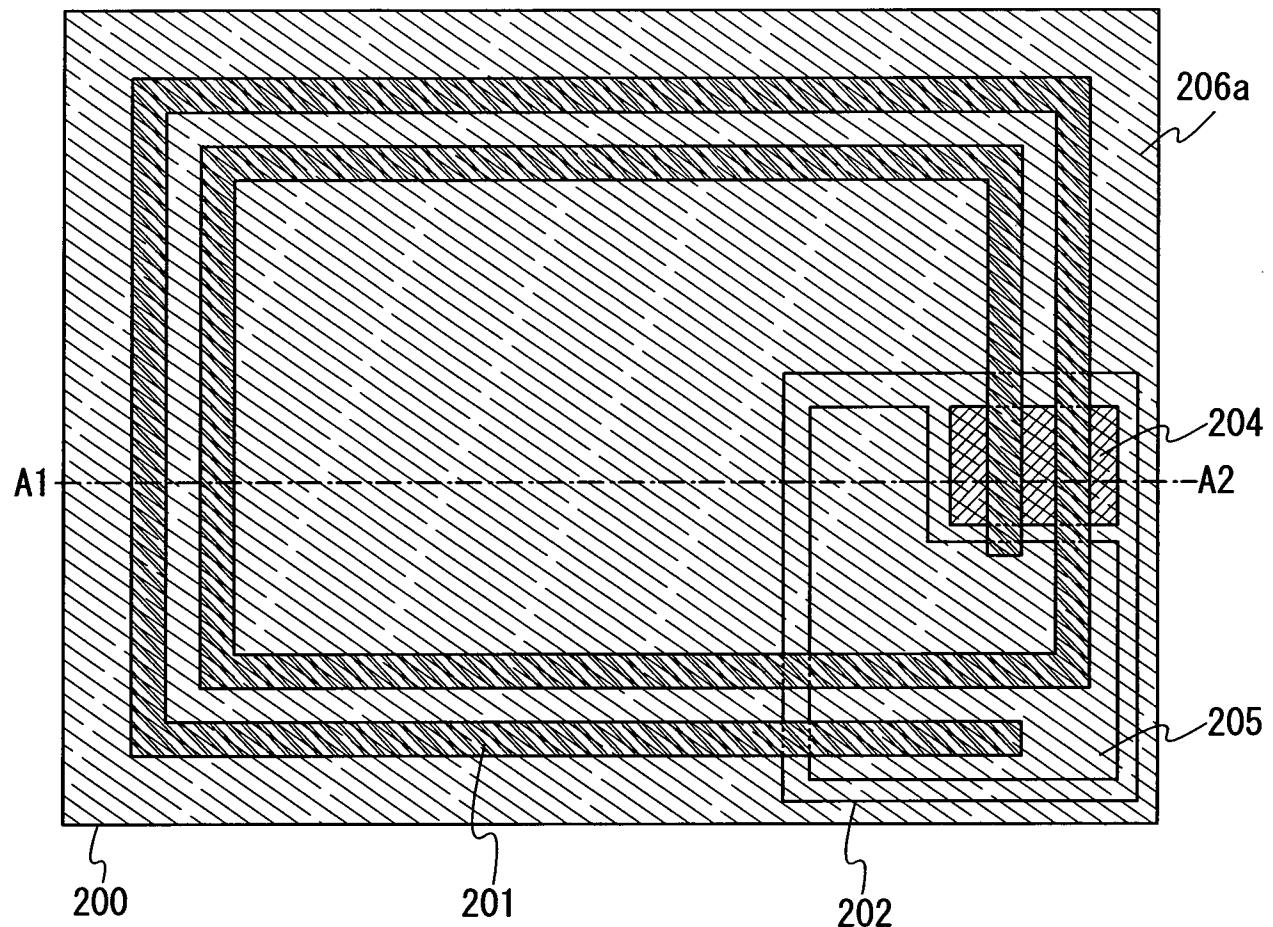


FIG. 1B

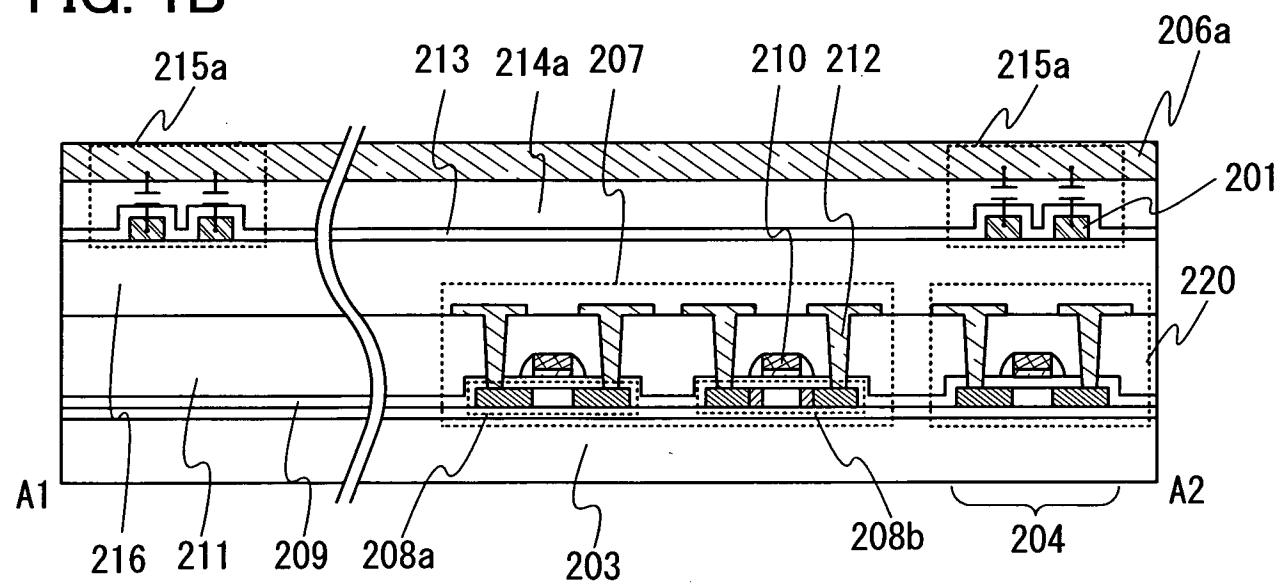


FIG. 2A

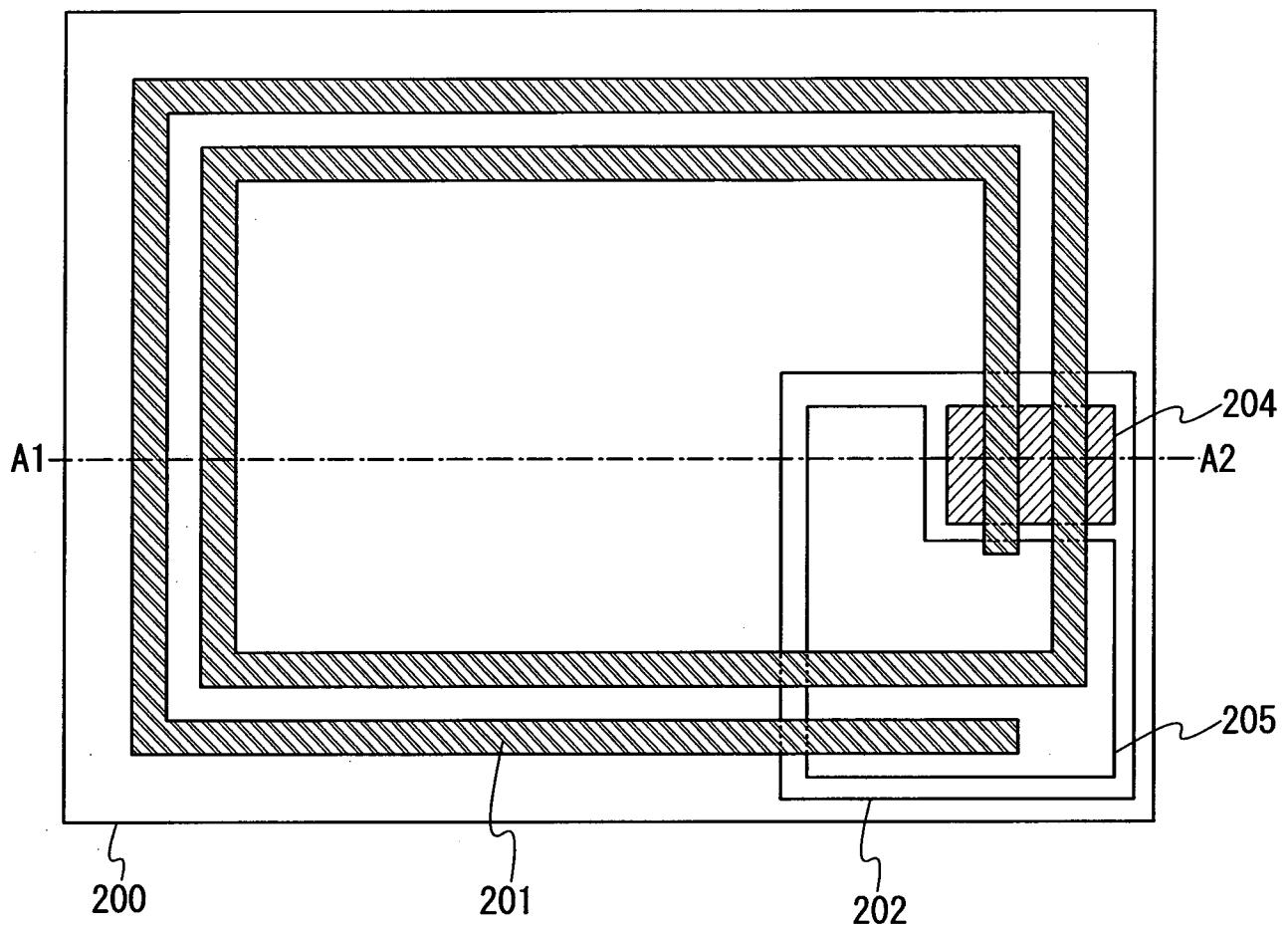


FIG. 2B

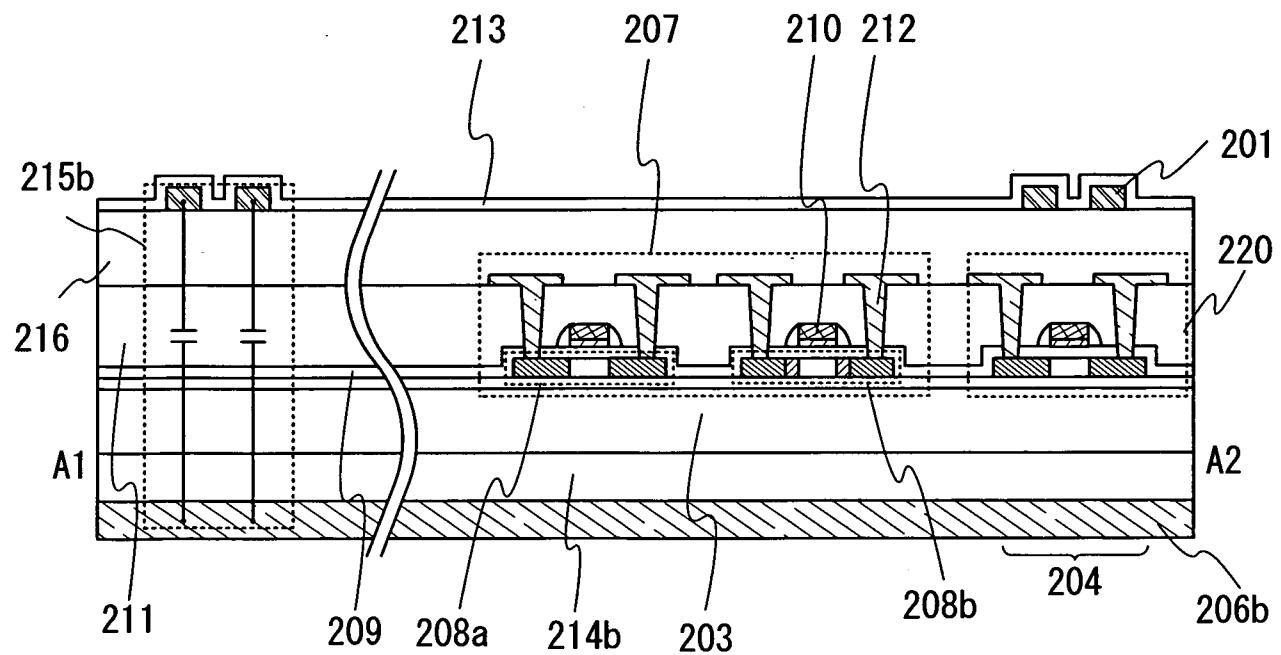


FIG. 3A

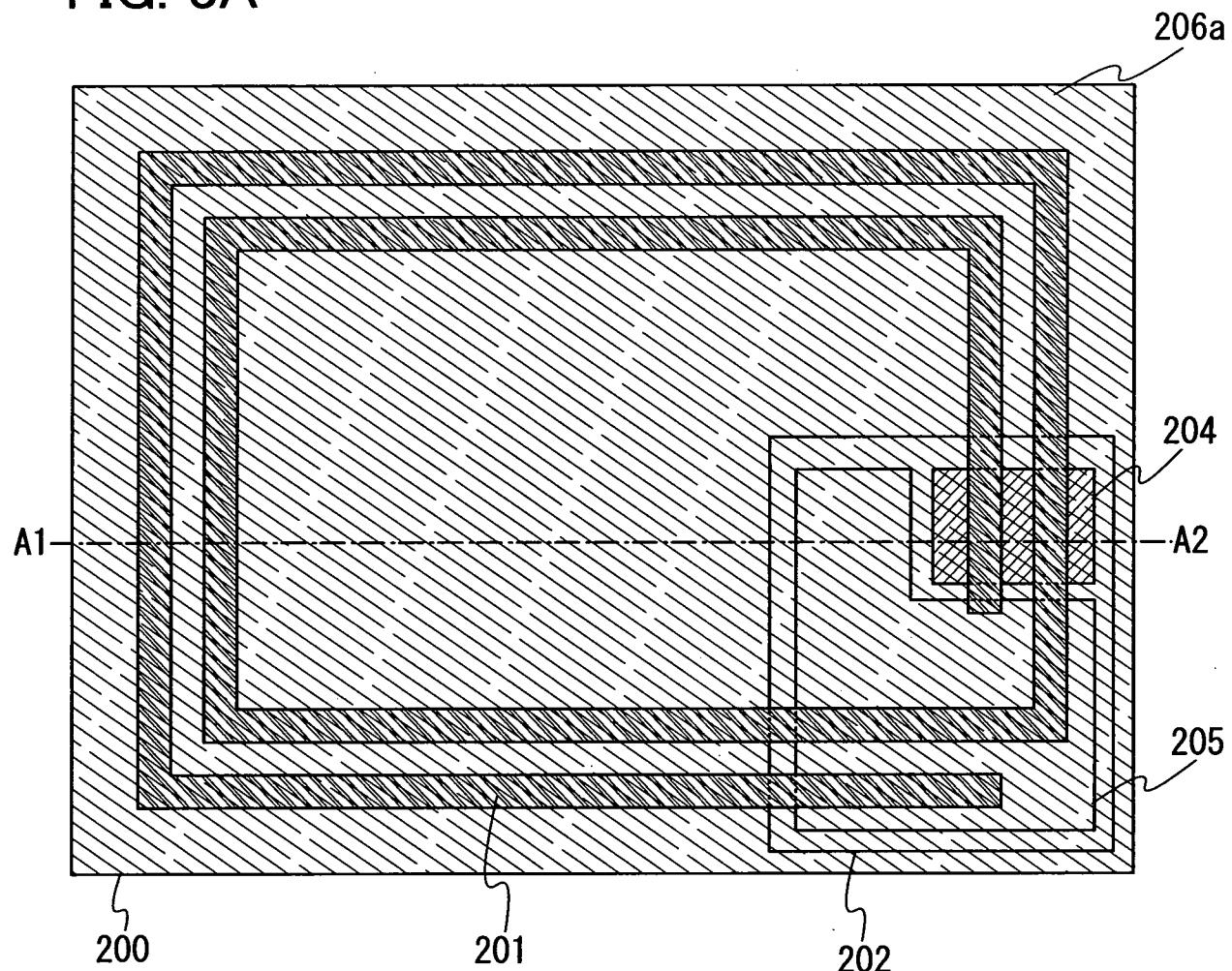


FIG. 3B

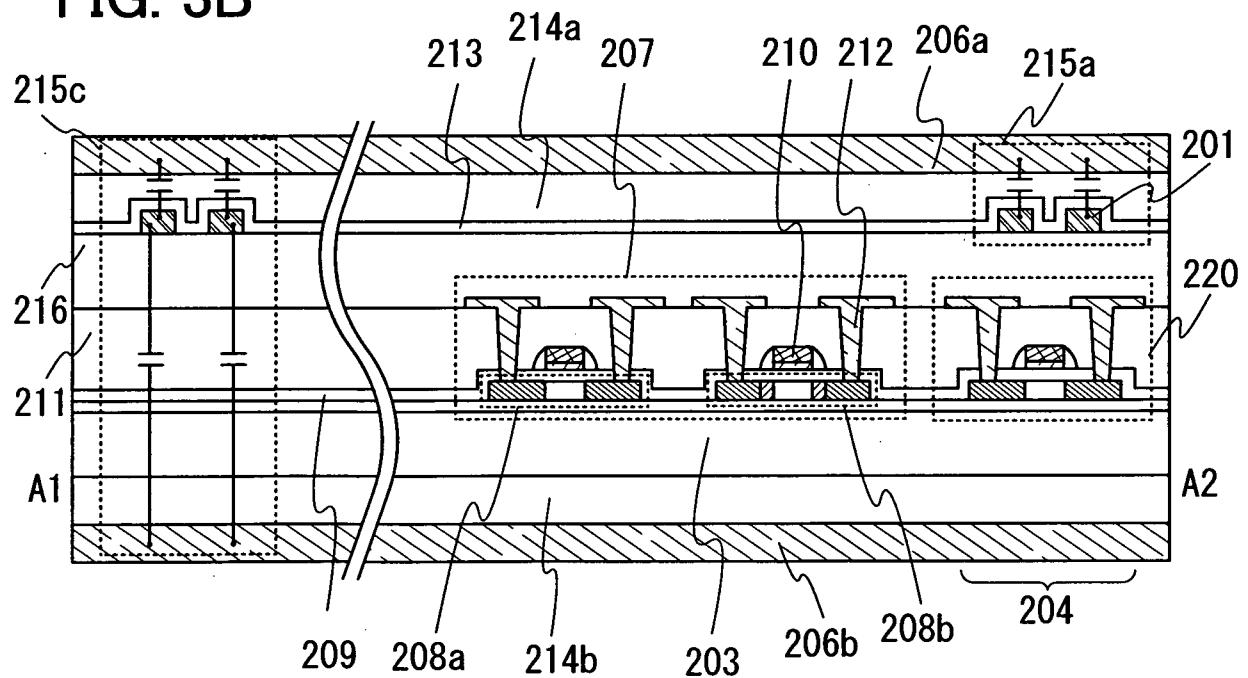


FIG. 4A

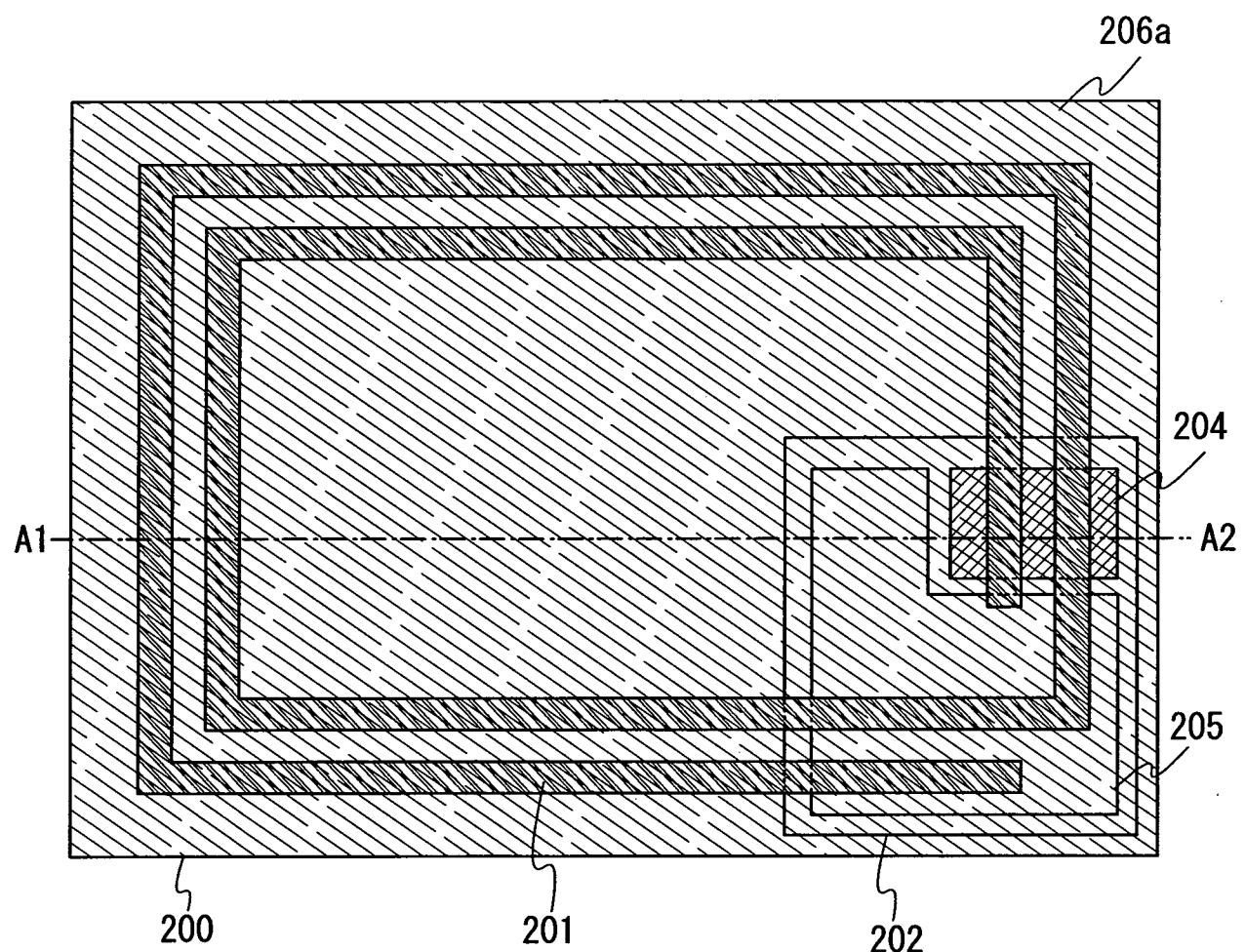


FIG. 4B

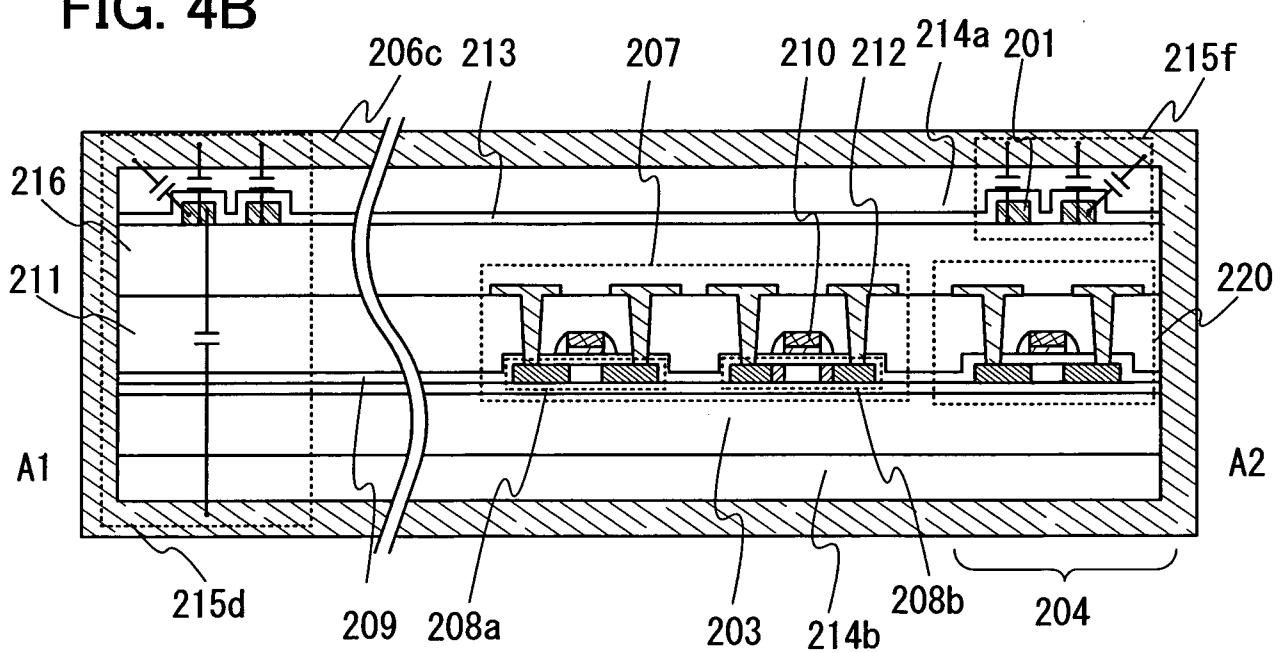


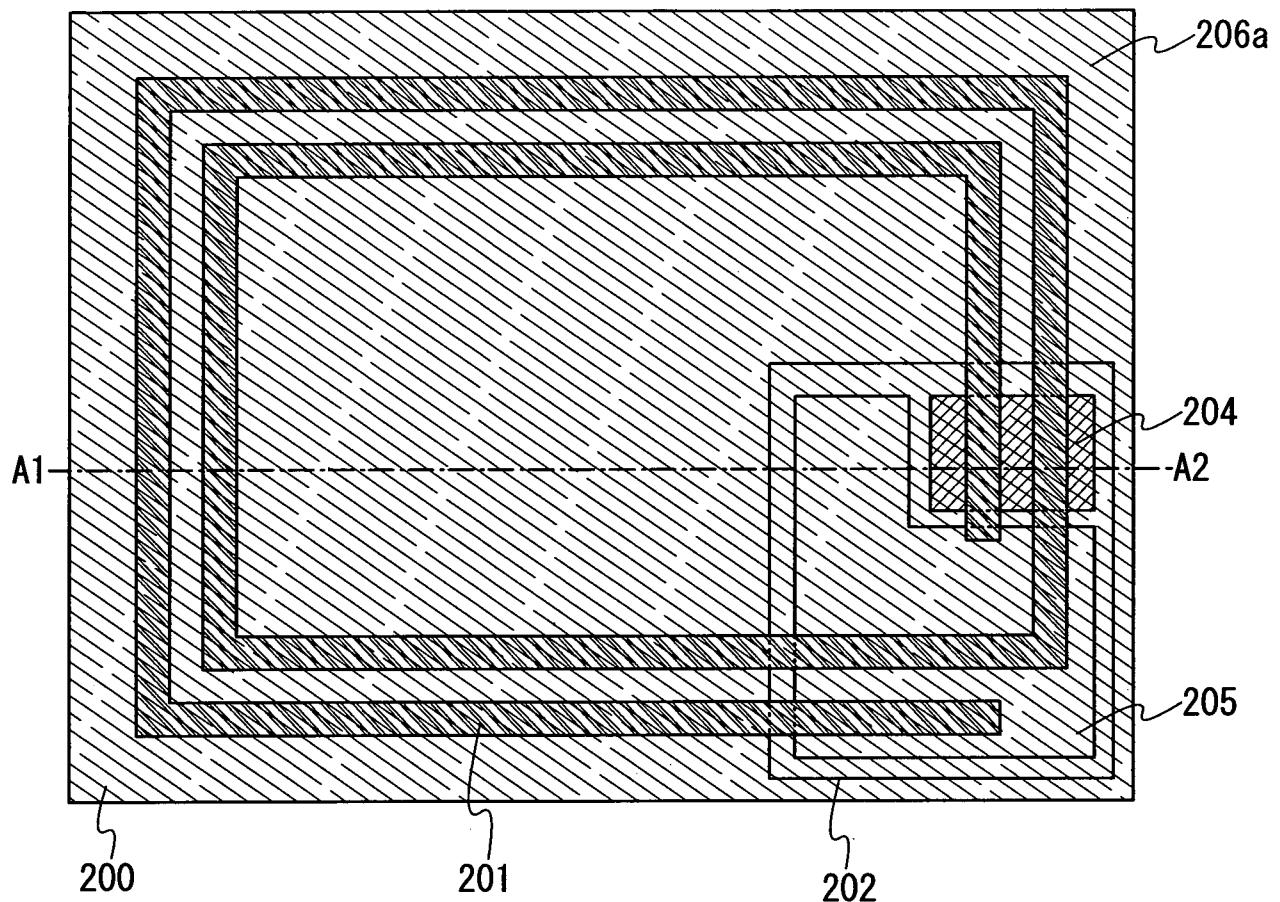
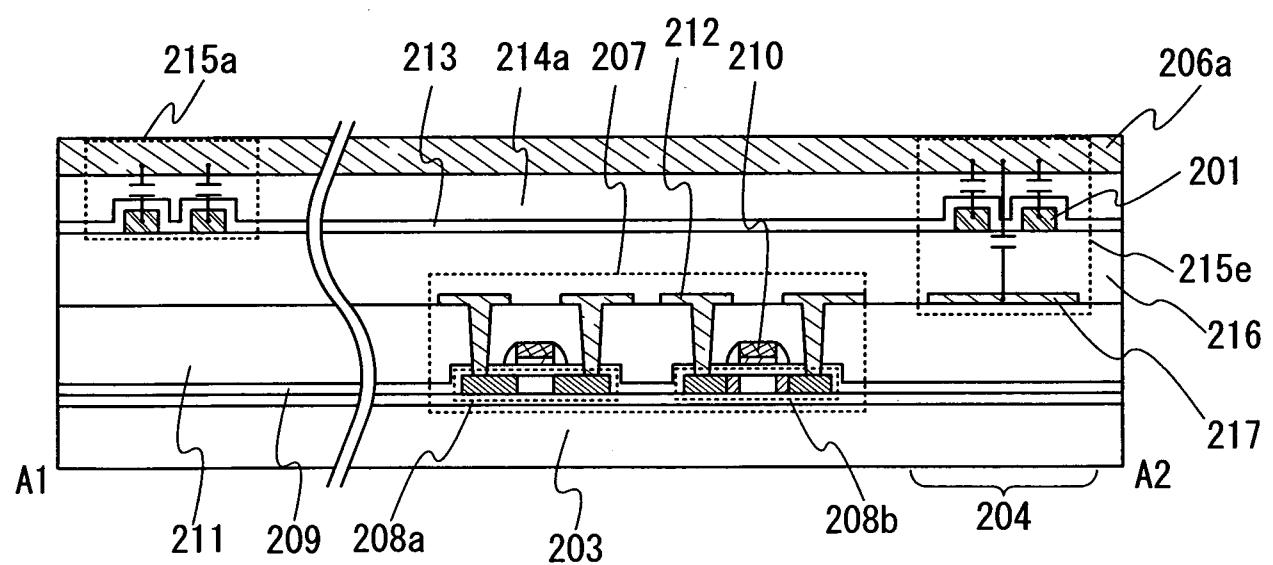
FIG. 5A**FIG. 5B**

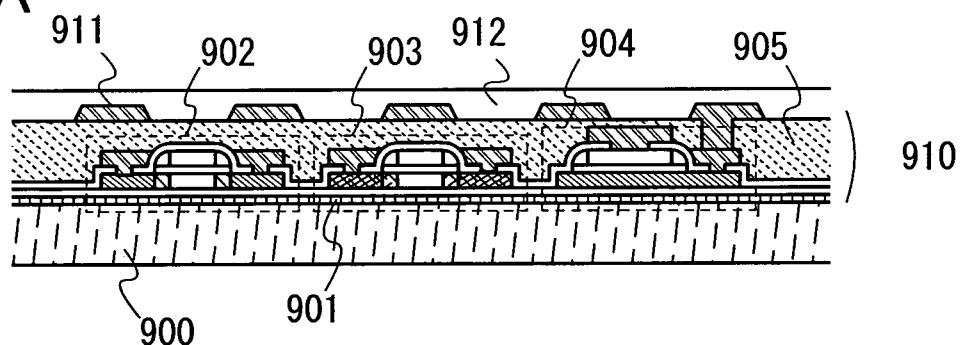
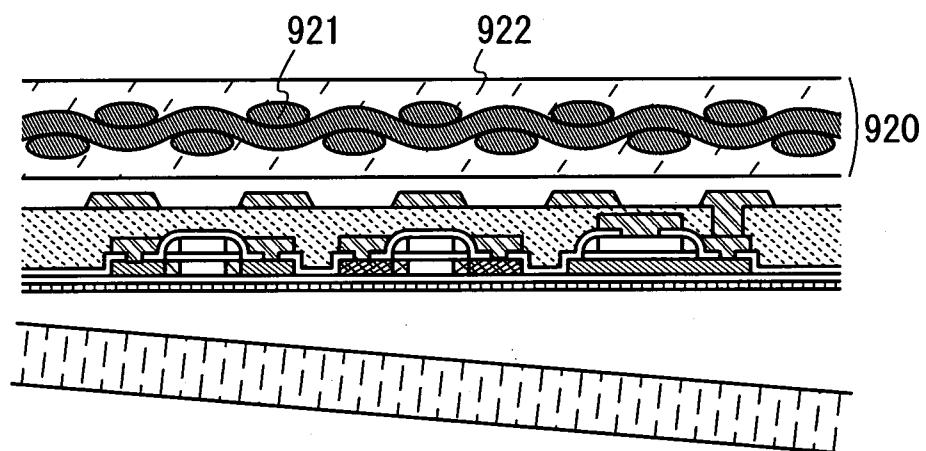
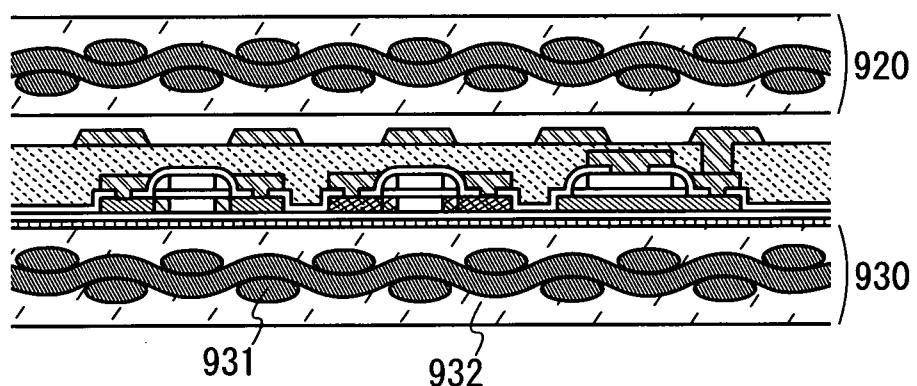
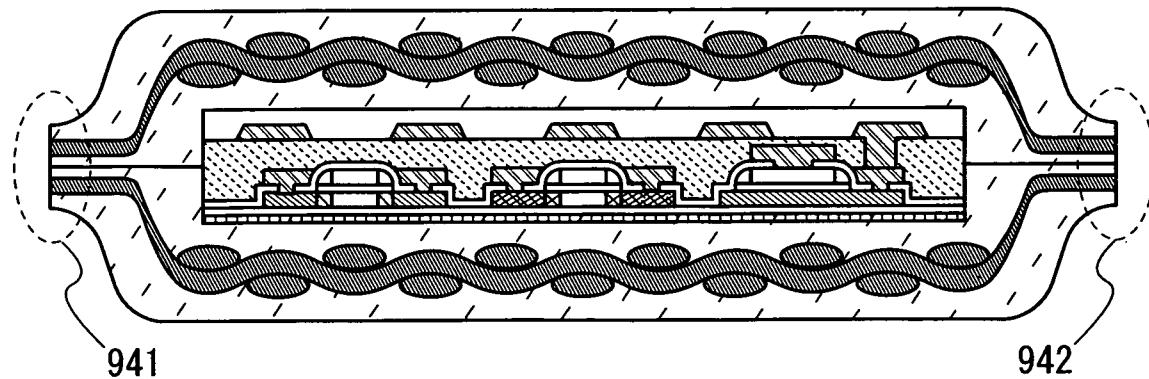
FIG. 6A**FIG. 6B****FIG. 6C****FIG. 6D**

FIG. 7A

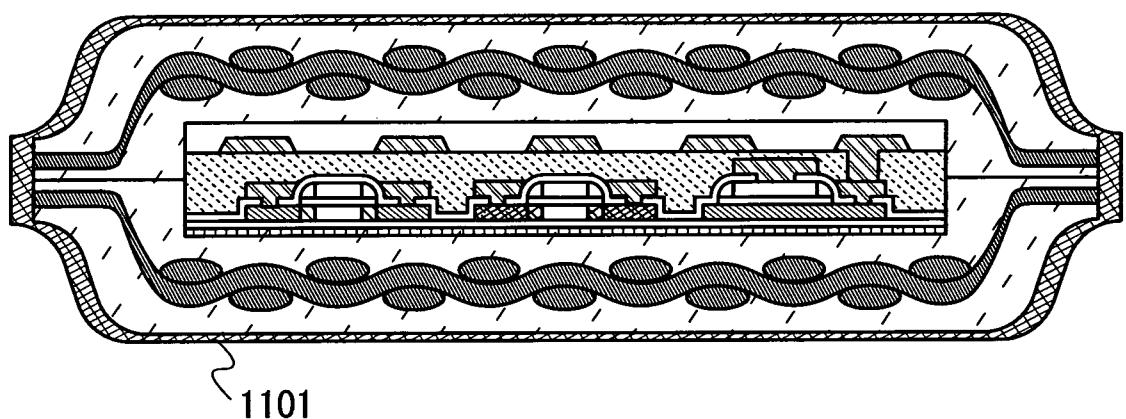


FIG. 7B

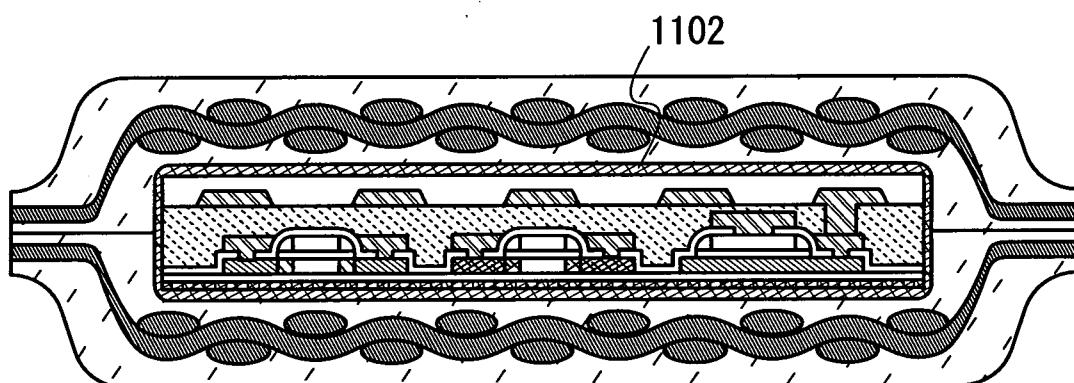


FIG. 7C

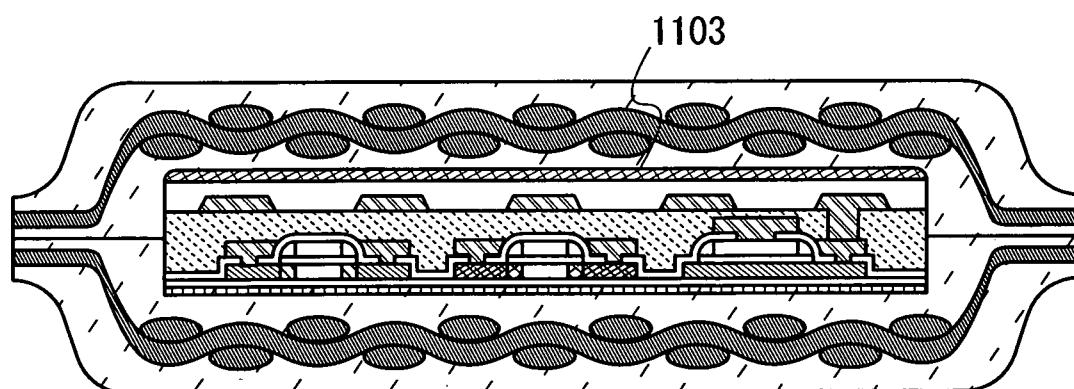


FIG. 8A

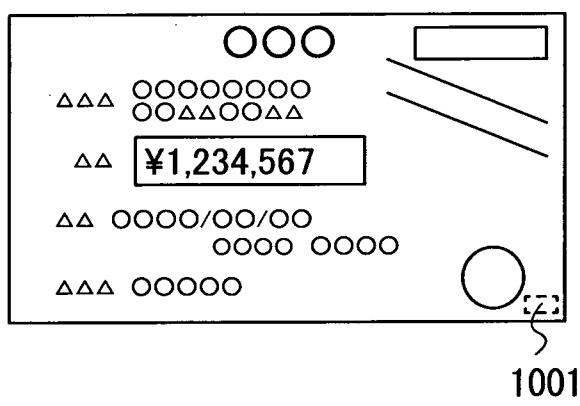


FIG. 8B

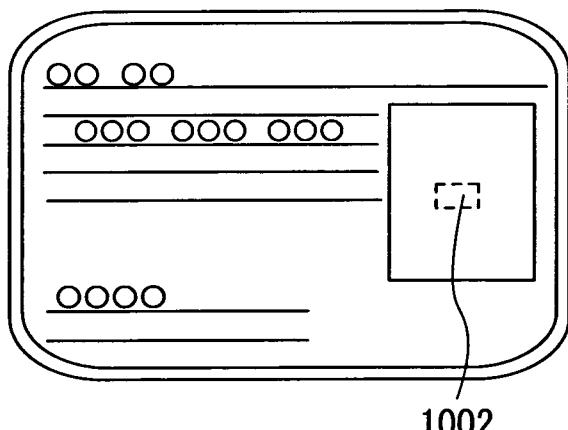


FIG. 8C

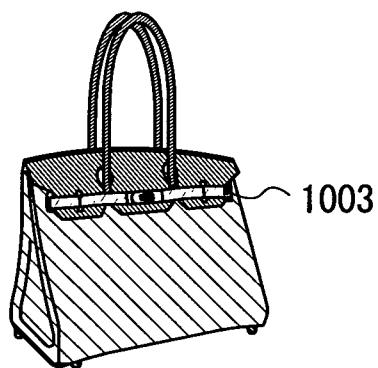


FIG. 8D

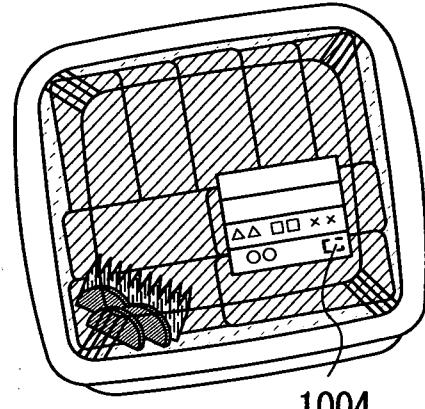


FIG. 8E

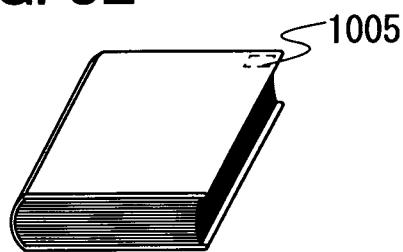


FIG. 8F

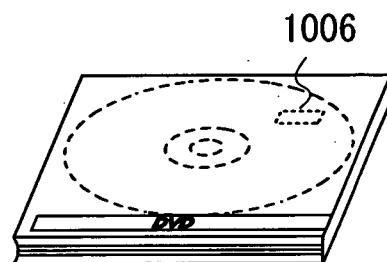


FIG. 8G

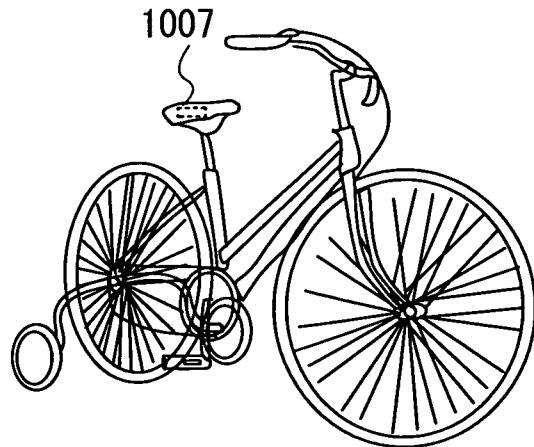


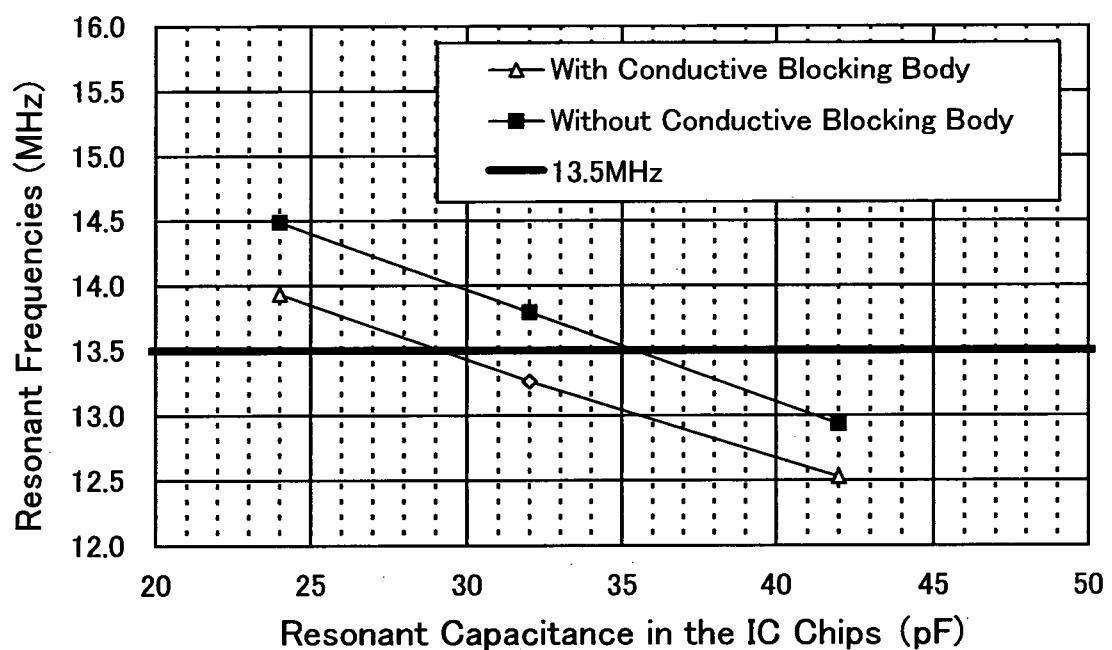
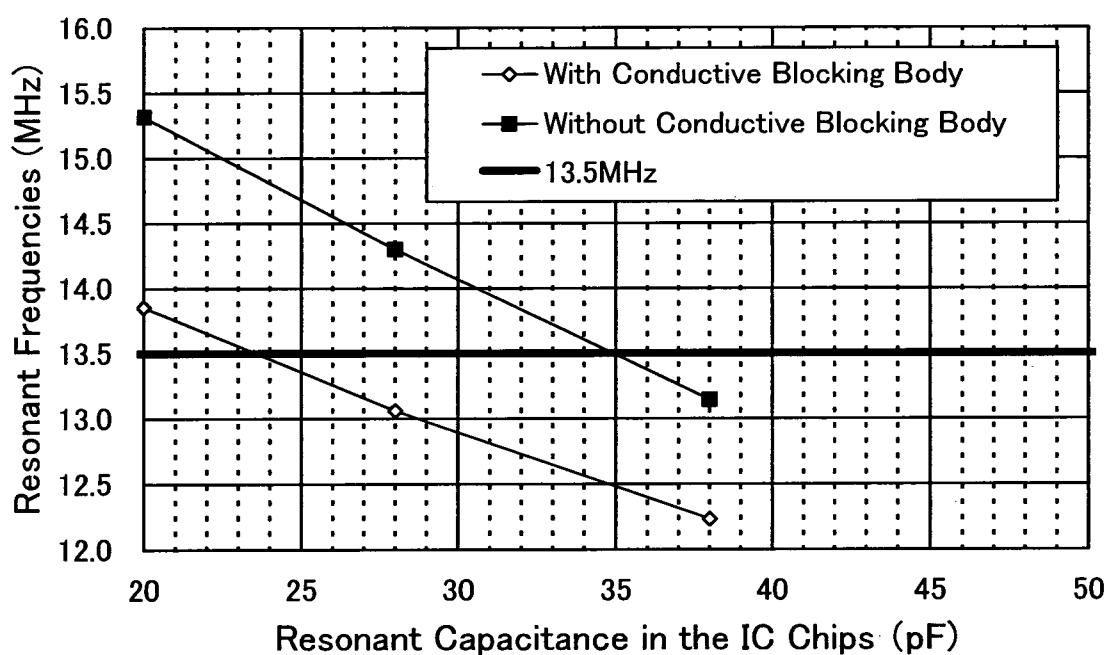
FIG. 9

FIG. 10

EXPLANATION OF REFERENCE

200: wireless chip, 201: antenna, 202: IC chip, 203: substrate, 204: resonant capacitor portion, 205: logic portion, 206a: conductive blocking body, 206b: conductive blocking body, 206c: conductive blocking body, 5 207: integrated circuit, 208: crystalline semiconductor film, 208a: semiconductor film, 208b: semiconductor film, 209: gate insulating film, 210: gate electrode, 211: interlayer insulating film, 212: source or drain electrode, 213: protective film, 214a: impact diffusion layer, 214b: impact 10 diffusion layer, 215a: capacitor, 215b: capacitor, 215c: capacitor, 215d: capacitor, 215e: capacitor, 216: interlayer insulating film, 217: wiring, 900: substrate, 901: separation layer, 902: transistor, 903: transistor, 904: capacitor, 905: insulating layer, 910: semiconductor integrated circuit, 911: antenna, 912: protective film, 920: impact diffusion layer, 930: impact 15 diffusion layer, 921: fibrous body, 931: fibrous body, 922: organic resin, 932: organic resin, 941: dividing surface, 1001–1007: chip, and 1101–1103: conductive blocking body.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2009/065970

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L21/822, G06K19/077, H01L21/3205, H01L21/8234, H01L23/52, H01L27/04, H01L27/06, H01L27/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996

Published unexamined utility model applications of Japan 1971-2009

Registered utility model specifications of Japan 1996-2009

Published registered utility model applications of Japan 1994-2009

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2006-108654 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2006.04.20, Paragraphs 0020-0048, Figs.1, 2 & US 2007/0257292 A1	1-18
Y	JP 2008-210380 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2008.09.11, Paragraphs 0096-0100, Fig.9 & US 2008/0186181 A1	1-18
Y	JP 2004-153717 A (TOPPAN FORMS CO., LTD.) 2004.05.27, Paragraph 0066 (Family: none)	1-18

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search 09.10.2009	Date of mailing of the international search report 20.10.2009
Name and mailing address of the ISA/JP Japan Patent Office 3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	Authorized officer KAZUNARI TANADA Telephone No. +81-3-3581-1101 Ext. 3462

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2009/065970

CLASSIFICATION OF SUBJECT MATTER

H01L21/822 (2006. 01) i, G06K19/077 (2006. 01) i, H01L21/3205 (2006. 01) i,
H01L21/8234 (2006. 01) i, H01L23/52 (2006. 01) i, H01L27/04 (2006. 01) i,
H01L27/06 (2006. 01) i, H01L27/08 (2006. 01) i