

April 2, 1968

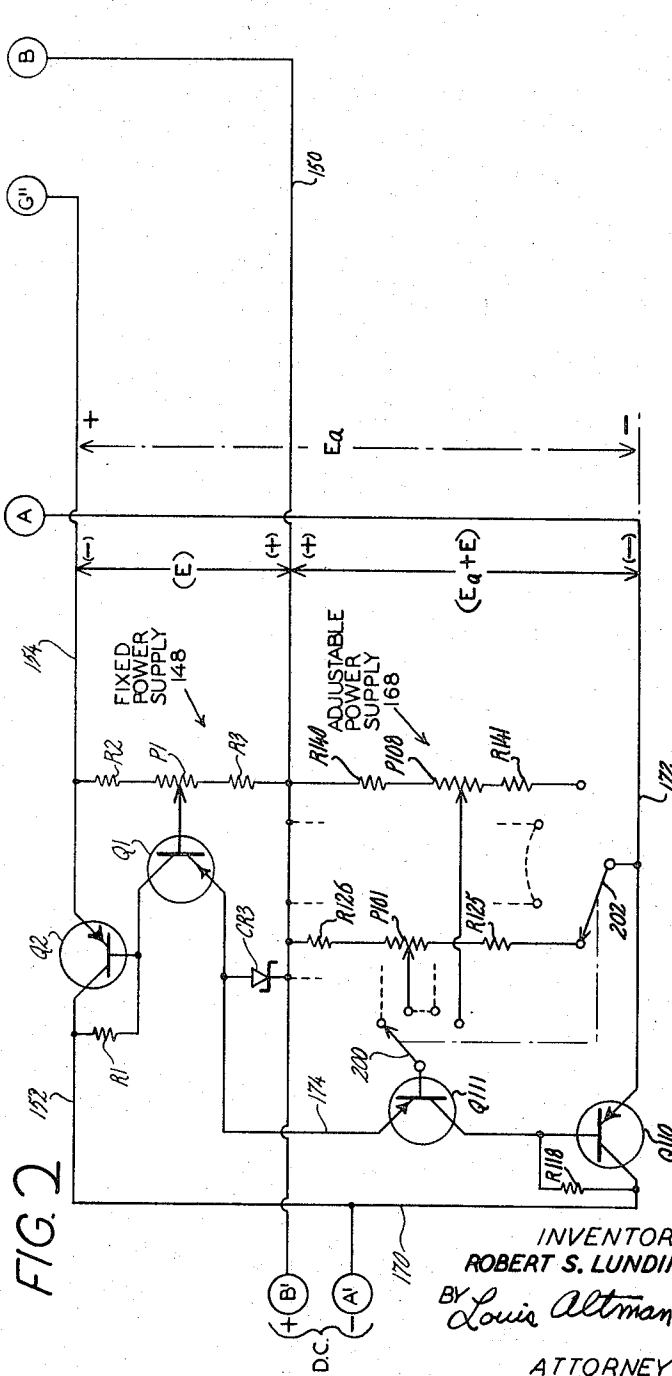
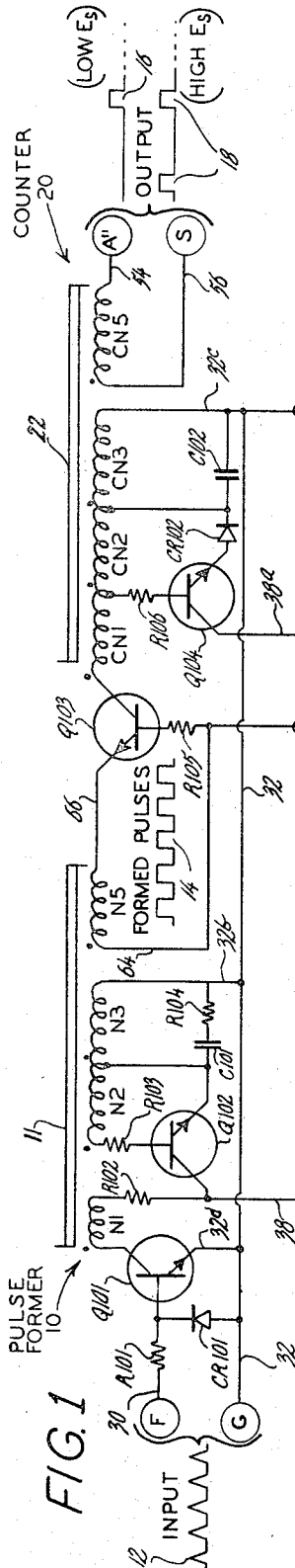
R. S. LUNDIN

3,376,410

VOLTAGE-CONTROLLED ADJUSTABLE COUNTER

Filed April 29, 1964

6 Sheets-Sheet 1



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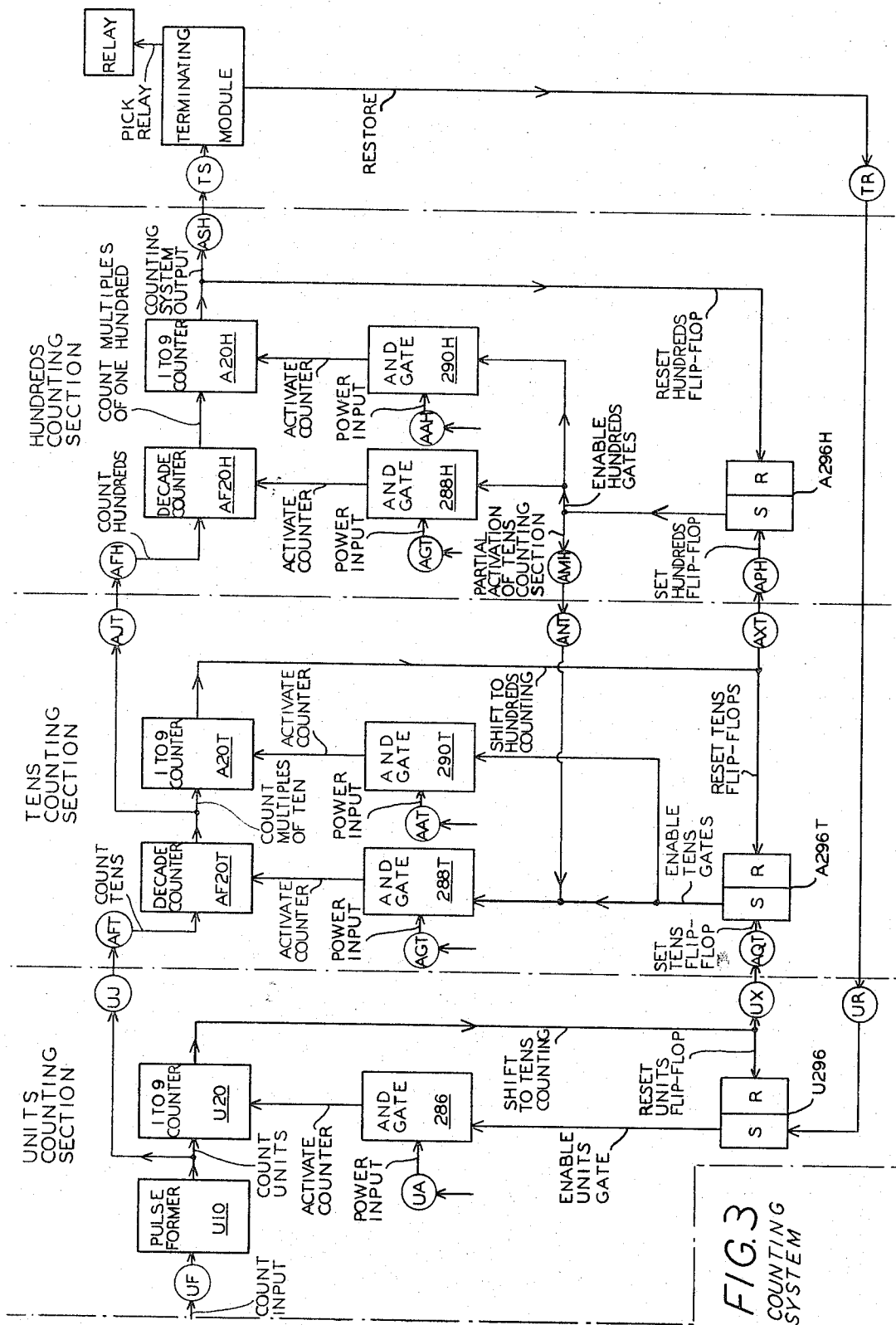
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VOLTAGE-CONTROLLED ADJUSTABLE COUNTER

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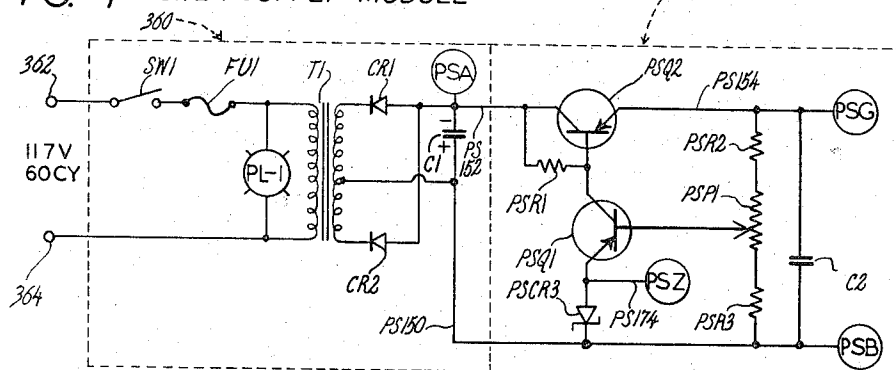


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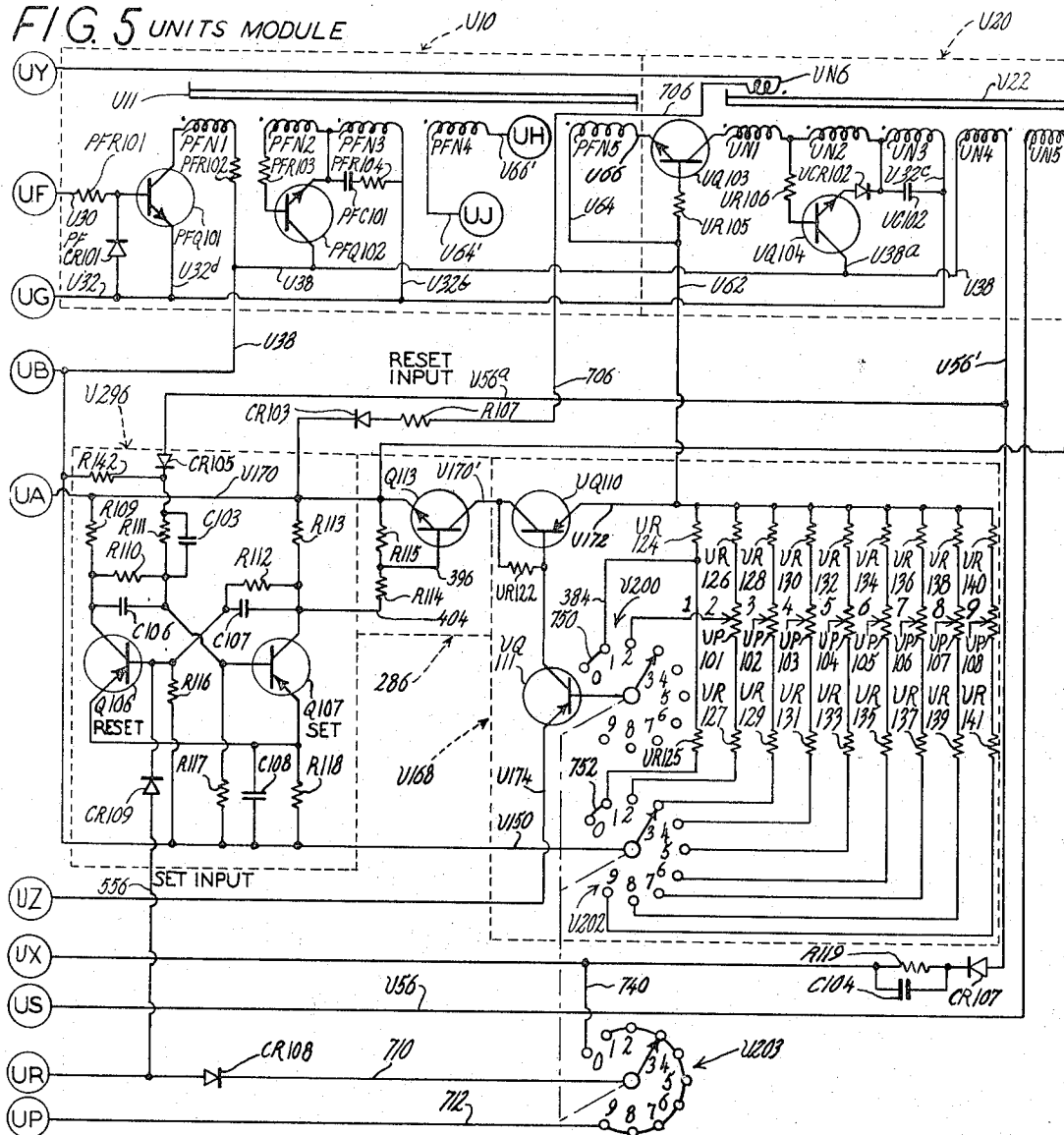
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VOLTAGE-CONTROLLED ADJUSTABLE COUNTER

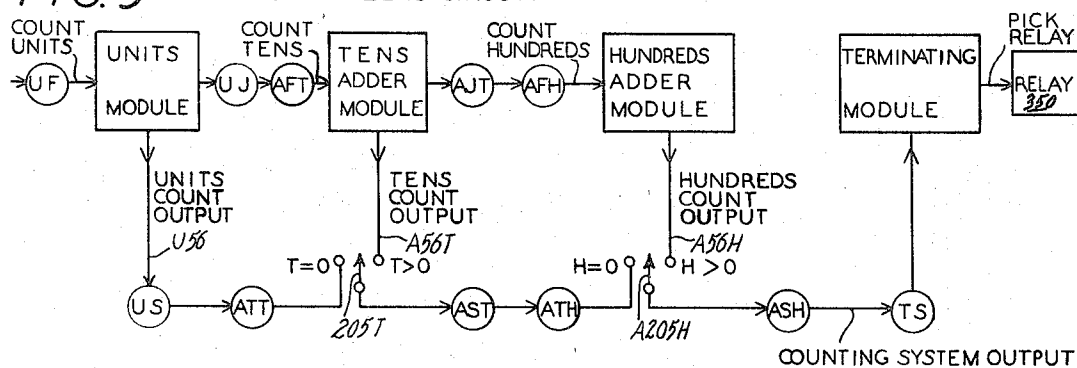
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HUNDREDS
ADDER
MODULE



April 2, 1968

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3,376,410

VOLTAGE-CONTROLLED ADJUSTABLE COUNTER

Filed April 29, 1964

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FIG. 10 LOWER ORDER ZERO CIRCUIT

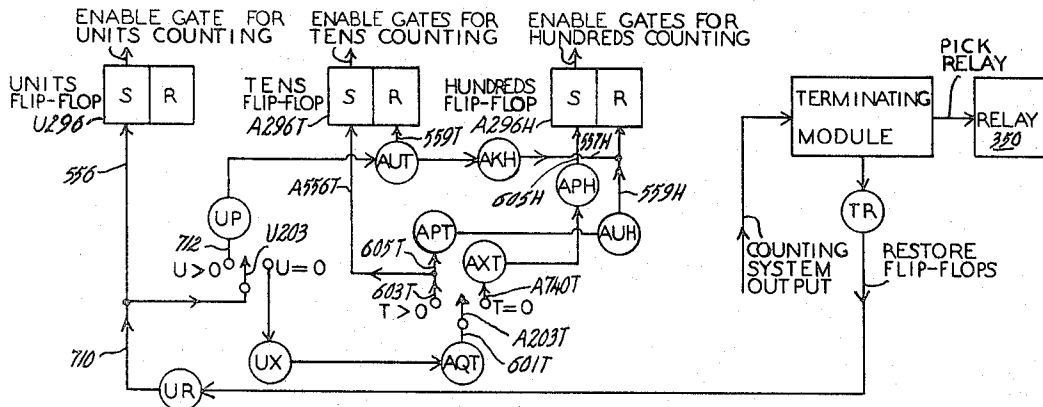
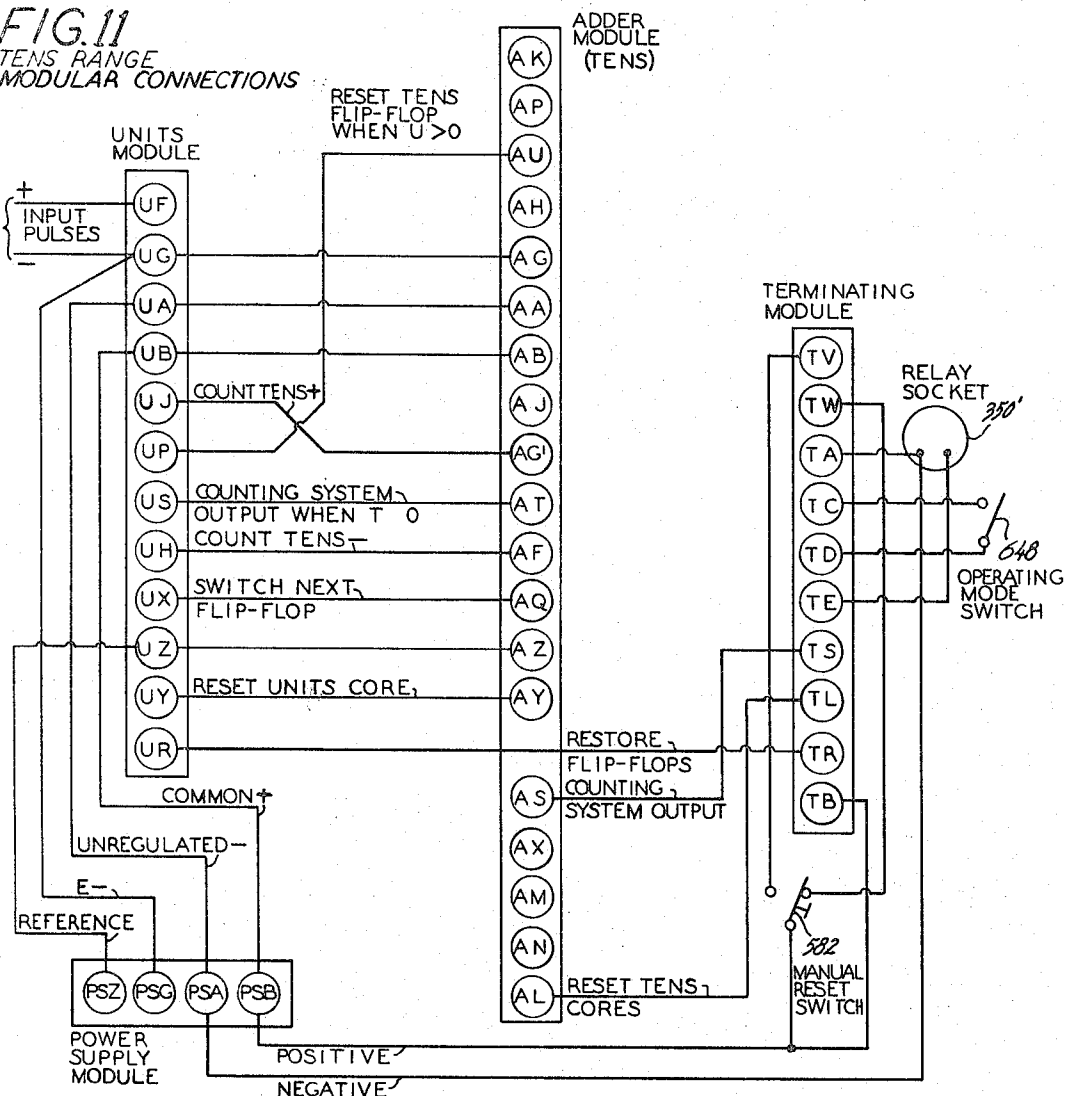


FIG. 11 TENS RANGE MODULAR CONNECTIONS



VOLTAGE-CONTROLLED ADJUSTABLE COUNTER

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17 Claims. (Cl. 235-92)

ABSTRACT OF THE DISCLOSURE

A counting system wherein the count is selectively adjustable. The modulus of a saturable core magnetic count stage is adjusted by a selectively adjustable voltage source in series with the input winding. Particular circuitry permits selection of zero for any digit in the count total.

This invention relates to a device for counting and storing various numbers of electrical pulses. It particularly concerns the adjustability of storage counters in which a core is magnetized incrementally.

In various control applications there is a need for a small, light, counting and storing device which is adjustable to count any desired number within a selected range, and which may be inexpensively mass-produced.

U.S. Patent No. 2,897,380 of Neitzert, which belongs to the assignee of the present invention, describes an incremental magnetic counter of the type to which the present invention relates. The magnetic core of such a counter requires a given total energy or volt-second-product input to switch it from one state of magnetic saturation to the opposite state. If this volt-second product is added in n equal increments, the core remains in successive intermediate magnetic states between the inputs, no matter how widely separated in time the inputs may be, and then saturates fully with the n th input. Afterwards the core is automatically reset to its original saturation state to be ready for the next counting cycle, and at the time of reset an output pulse is produced to indicate the receipt of the n input pulses. This device is therefore a scale-of- n counter or pulse-frequency-divider with long-term storage capabilities.

For accuracy of the count, all n input pulses must have nearly identical volt-second integrals. To provide such reliable input pulses, use is made of the fact that the volt-second content of the output pulses derived from this same type of counter is substantially constant for a given device. Therefore in a high count system individual counters of this type can be connected in cascade so that each output pulse from a preceding stage provides an input pulse of stable energy content to the following stage. In this way each stage acts as a reliable pulse-former for the following stage. The first counting stage may be preceded by a simple pulse-forming stage which is the same type of device except that it is designed to have a very low dividing ratio (such as 1:1 or 2:1) and therefore is not itself critically dependent on receiving a well formed input pulse.

The constancy of the output pulse energy content of these devices is normally substantially immune to variations of supply voltage over a wide range, enabling such devices to be reliably operated from fluctuating power sources without too much attention to voltage-regulation and the costly components which such regulation requires. A change in the power supply voltage to a preceding stage may cause a change in the voltage amplitude of the output pulse which it supplies to the following stage. But, for reasons explained below, this change in pulse voltage amplitude is compensated by an opposing change in pulse time duration, i.e., voltage and time vary

in opposite directions by the right amount to keep the volt-second product unchanged.

Such stability of the pulse energy content is an advantage from the standpoint of count stability, but it stands in the way somewhat when one wishes to design an adjustable counter in which it is desirable for the count to be varied. Therefore a general object of this invention is to provide an incremental magnetic counter in which the count is adjustable. More particularly, it is an object of this invention to provide a device of this type which is well adapted for inexpensive mass production.

Some earlier approaches to the problem of adjustability have involved varying the effect of a given input pulse energy content on the counter stage core. According to this invention the count is varied in a different way, with resulting advantages. In the prior art devices the energy for injecting a pulse into a counter stage was derived solely from the voltage induced in the output winding of the preceding stage during its reset. But in the device of this invention an auxiliary source of voltage is employed to augment or decrease the amplitude of each of the pulses received by the counting stage. Consequently a smaller number of augmented pulses, or a larger number of decreased pulses, is required to saturate the core of the counting stage, even though the preceding stage has not altered its output. By varying the voltage of the auxiliary source, various different counts can be selected.

But with this approach the volt-second product of the input pulses to a counting stage is determined in part by the voltage of a source other than the constant-energy-content output of the preceding stage. As a result, the problems of voltage-regulation must again be met, with attendant expense for components. Moreover, these problems now arise in a particularly troublesome way, because it turns out that it is important not only to hold the auxiliary voltage constant, but also to maintain a given ratio between that voltage and the main supply voltage.

It is therefore another object of this invention to provide the voltage-regulation necessary to meet these requirements, and to do so at the lowest cost and in a manner suitable for mass production. More particularly, one aspect of the invention provides a novel voltage-regulating circuit in which two sources at different voltage levels are controlled by the same regulating component, resulting in the twin advantages that the two voltage levels maintain a constant relationship and the number of required components is reduced.

Another object of the invention is to provide a selectively variable voltage source in which precise count selection is achieved at low cost and in a manner suitable for mass production. More particularly, a circuit is provided in which inexpensive, wide-tolerance components may be employed, together with variable elements easily adjusted at the factory to compensate for the inaccuracies introduced by the wide-tolerance components.

Still another object is to provide a counter device which, after factory adjustment of the variable components, remains permanently set so that thereafter the user can vary the count by simple operation of a switch having predetermined count-selecting positions.

A further object is to provide an adjustable counter which is switched from one counting modulus to another by discrete increments, with each step being achieved by turning to a discrete switch position which selects a discrete circuit path so as to avoid intermediate positions in which the count may be ambiguous.

A still further object is to provide circuitry by means of which a number of adjustable counter stages can be interconnected to count any desired number within a given range, including even those numbers which are not

the product of any of the available counting moduli of the individual counter stages.

Still another object is to provide a modular counter in which the range of adjustability can be extended by simply connecting additional units to the system, and in which certain of the units are constructed in the form of identical modules for interchangeability and for economy of production.

The foregoing has been a brief summary of some of the principal features of the invention. A detailed description will now be presented, making reference to the following drawings which accompany this specification:

FIG. 1 is a schematic circuit diagram of a basic two-stage counter with power supply and other connections designed for adjustability of the count in accordance with this invention;

FIG. 2 is a schematic circuit diagram of a regulated two-level power supply in accordance with this invention, with one level variable, for use with the counter of FIG. 1;

FIG. 3 is a block diagram generally illustrating a multi-stage hundreds range high count system in accordance with this invention, which is able to select even those counts that are not the product of any of the available moduli of its individual counting stages;

FIG. 4 is a circuit diagram of the power supply module for a system according to FIG. 3 which is constructed in modular form;

FIG. 5 is a circuit diagram of the units counting module of the aforesaid system;

FIG. 6 is a circuit diagram of a tens or hundreds counting adder module for this system;

FIG. 7 is a circuit diagram of a terminating module for use with this system;

FIG. 8 is a diagram of the interconnections among the modules of FIGS. 4 to 7 employed to form a hundreds range counting system;

FIG. 9 is a block diagram showing the manner in which the counter of this invention meets the problem of zeroes in the higher orders;

FIG. 10 is a block diagram showing the manner in which this counter meets the problem of zeroes in the lower orders; and

FIG. 11 is a diagram of the interconnections among the modules of FIGS. 4 to 7 employed to form a tens range counting system.

BASIC COUNTER CIRCUIT

FIG. 1 shows a counter device comprising two separate stages 10 and 20. The first stage 10 includes a first square loop magnetic core 11 and its associated circuitry. This stage is a pulse-former which receives a number of poorly shaped inputs such as the spikes 12, and puts out, for example, an equal number of relatively square pulses 14 of uniform volt-second content. The pulses 14 are then passed through an interstage transistor Q103 to the second stage 20 which comprises a second square loop magnetic core 22 and its associated circuitry. This is the counting stage. Upon receiving a number n of the pulses 14 this stage produces a single output pulse and also resets to be ready to count the next n pulses. In accordance with this invention the count n is adjustable in a manner which will be described after the circuit of the counter has been explained in more detail. To illustrate this, the output of the counter is shown as either one pulse 16 for every $n=6$ of the inputs 14, or pulses 18 in the ratio of one for every $n=3$ of the inputs 14. These values of n are merely exemplary, and in fact have been chosen low for the sake of simplicity of illustration. In actual units the maximum count per stage may be anywhere from unity up to several decades.

The pulse-former and counting stages will now be described in that order. The discussion of the pulse-former stage 10 of FIG. 1 is intended to apply also to the pulse-former U10 of FIG. 5. To facilitate comparison, both

pulse-formers are given reference characters which are similar except for certain distinguishing prefixes.

As more fully explained in the aforesaid Neitzert patent, the input spikes 12 are applied across a pair of input terminals F and G to which are connected leads 30 and 32 respectively. The positive side of the signal is transmitted through limiting resistor R101 to the base of an NPN input transistor Q101. The negative side of the signal goes over leads 32 and 32d to the emitter of Q101. Each spike causes the input transistor to be turned on so that core-saturating current is drawn from a power supply lead 38 through a limiting resistor R102, a core-saturating winding N1 which links the core 11, the input transistor Q101, and back over leads 32d and 32 to a power supply lead 32a. Since the stage 10 is a pulse-former, it is so designed that this surge of current is sufficient to drive the core 11 from one condition of magnetic saturation beyond the opposite condition of magnetic saturation.

As each spike 12 terminates, the saturating current in the winding N1 also terminates and, in accordance with its hysteresis characteristics, the core 11 drops from over-saturation to its residual level. This flux change induces a voltage in a triggering winding N2 linking the core 11. The emitter-base circuit of a resetting transistor Q102 is connected across this winding N2 in such a manner that the induced voltage turns on Q102. As a result resetting current is drawn from the power supply lead 38 through the resetting transistor Q102, a resetting winding N3, and back over leads 32b and 32 to power supply lead 32a. This current is in the direction to reset the core 11 to its original condition of magnetic saturation. The change in flux occurring during this resetting of the core 11 continues the voltage previously induced in the triggering winding N2. The continuance of this voltage causes the resetting transistor Q102 to stay on until the reset operation is completed. When that is achieved, the permeability of the core 11 drops, lowering the voltage induced in the triggering winding N2 and thus allowing the resetting transistor Q102 to shut off. This terminates the cycle with the core 11 reset and thus ready for the next spike 12. Each succeeding spike 12 causes the described cycle to be repeated.

During the time that resetting of the core 11 occurs, the accompanying change in flux causes a voltage to be induced in an output winding N5 which also links the core 11. As a result this winding acts as a source of EMF for providing the pulse 14. One such pulse is produced (in this particular example) for each of the spikes 12.

The counting stage 20 will be described next. This description is intended to apply also to the counting stages U20 of FIG. 5 and AF20 and A20 of FIG. 6. To facilitate comparison corresponding elements have similar reference characters, except for certain distinguishing prefixes.

The pulse 14 developed across the winding N5 is applied across the emitter of transistor Q103 and its base resistor R105 in a manner to render Q103 conductive. The pulse 14 thus passes through Q103 to an input winding CN1, CN2, CN3 linking the core 22. Since the stage 20 is a counter, it is designed so that each pulse 14 serves to drive the core 22 only part of the way from saturation in one direction toward saturation in the opposite direction. Between inputs, core 22 retains the incremental magnetization level which it attained as a result of the most recent input. Finally the n th one of the inputs 14 drives the core 22 beyond saturation. Then reset takes place in the same manner as described for the stage 10. That is, after the n th input 14 terminates, the core 22 drops from over-saturation to the residual magnetization level, this change in flux inducing a voltage in a triggering winding CN2. This induced voltage turns on a resetting transistor Q104 which then draws reset current from the power supply lead 38 through lead 38a, transistor Q104, diode CR102, a resetting winding CN3, and back over a lead 32c to the power supply lead 32a. The change in flux ac-

completing the resetting of the core 2 sustains the induced voltage in the triggering winding CN2 necessary to keep reset transistor Q104 turned on until reset is completed.

The output of counter stage 20 is also generated in a manner similar to that of pulse-former stage 10. The change in flux accompanying reset of core 22 induces a voltage pulse 16 or 18 in an output coil CN5 linking the core 22. This output is applied by leads 54 and 56 across a pair of output terminals A' and S, terminals being driven positive relative to terminal A'. The output may be employed to perform any desired control or data-processing function, but in high count devices having several counting stages in cascade, the output would typically be coupled through another transistor to drive another counter stage. The following transistor and counter stage would be connected to the stage 20 in the same manner as the interstage transistor Q103 and the stage 20 are connected to the stage 10.

The illustrated resistors, capacitors, and diodes are included in the circuits 10 and 20 for such purposes as cushioning transient voltages, establishing desired biasing levels, limiting currents, etc., in accordance with established practices.

The output pulses 14, 16, or 18 derived from each stage 10 or 20 are of constant volt-second content despite considerable variation in supply voltage. The reason for this is as follows. According to the basic equation of magnetic induction the instantaneous value of the voltage induced in the output winding of any stage (e.g., winding N5 of stage 10) is $e = -N d\phi/dt$, where N is the number of turns in the output winding and $d\phi/dt$ is the instantaneous time rate of core flux change during reset. When this equation is rewritten as $edt = -Nd\phi$ and integrated over the time interval during which the reset pulse occurs, it is seen that the total volt-second integral is equal to the product $N\phi_t$ where ϕ_t is the total hysteresis loop excursion which the core undergoes during reset. At a given temperature the number of turns N and the total hysteresis loop excursion ϕ_t are both fixed for a given core such as 11 and a given output winding such as N5. Therefore the volt-second content must be a constant regardless of voltage variations. For example, if the supply voltage were to increase the core would reset faster, thus decreasing the total reset time. But faster reset also means an increase in the rate of flux change $d\phi/dt$, which results in a higher instantaneous induced voltage. These opposing changes in voltage and time cancel each other out so that the resulting volt-second product is unchanged. Therefore a given preceding stage output coil always provides the same energy-content input pulse to the following stage.

It is this constancy that enables the device to count reliably and also enables each counter stage to be employed as a pulse former for its following stage so that cascading for high counts is easily accomplished. Each counting stage (e.g., stage 20) requires a fixed energy input to achieve the total flux excursion of its hysteresis loop. With the energy content of input pulses (e.g., pulses 14) reliably fixed, this total excursion can be confidently chosen to require n times that fixed energy content so that n pulses are reliably counted.

ADJUSTING THE COUNT

In some prior art devices a different quantity n has been chosen by employing magnetic bias (e.g., by means of a permanent magnet) to reduce the magnetization excursion which remains for the core to travel on its hysteresis loop. Therefore the core will then require a number of pulses less than n to finish the remainder of the total excursion. But when this is done the reset excursion is also reduced. This in turn alters the energy content of the pulses sent to the next stage and thus alters the count of that next stage. In certain applications it may be desirable to vary the counting modulus of one stage without affecting the modulus of any other stage in the counting chain.

In other words we may wish to keep the advantages of constant-energy output pulses, yet be able to vary the count.

In other prior art devices some of the energy output of a core stage has simply been discarded, either by shunting part of it away from the following stage, or by tapping the output coil so that less than the full output voltage is employed. This approach incurs certain disadvantages. For one, the power expended is always at the same maximum level even when some of it is discarded in order to change the count. Further, it is difficult and expensive to put many closely spaced taps (one for each available count setting) on a coil which is wound with fine wire on a miniature magnetic core. Using bigger components is undesirable because it increases the bulk, weight, and power requirements of the counter. Finally, some of these prior art devices have been too critical in their adjustment to be suitable for volume production.

An advantageous feature of this invention is that the power consumption is normally set at the minimum level, and only when it is necessary to change the count is additional power expended. The additional power comes from a variable auxiliary source of voltage E_a . As in prior art devices, the primary power source is a voltage E placed across the leads 32a and 38. This primary source is represented schematically in FIG. 1 as a battery of fixed voltage E tentatively connected to these leads. In the circuit of this invention voltage E is still the sole source of power (1) to saturating winding N1 for setting the core 11 when input transistor Q101 is turned on, (2) to the reset winding N3 for resetting the core 11 when the reset transistor Q102 is turned on, and (3) to the reset winding CN3 for resetting the core 22 when reset transistor Q104 is turned on. Advantageously, the auxiliary power source E_a is not involved in these operations, and therefore does not affect the volt-second characteristics of stages 10 and 20 insofar as they function as pulse-formers for their respective succeeding stages.

The auxiliary source E_a only affects the operation in which the pulse-former output coil N5 injects a pulse 14 into the counter input coil CN1, CN2, CN3. Represented in FIG. 1 as a battery of variable voltage E_a tentatively connected across leads 32a and 62, the auxiliary source is connected in series with the pulse-former output coil N5 and the counter input coil CN1, CN2, CN3. The series path may be traced from E_a negative over leads 62 and 64, pulse-former output coil N5, lead 66, interstage transistor Q103, counter input coil CN1, CN2, CN3, and back over leads 32c and 32a to E_a positive. Thus the voltage E_a augments by a selected amount the voltage which is applied by coil N5 as an input to counter stage 20 during the duration of the output pulse 14 provided by the pulse-former stage 10. Thus the pulse duration remains constant, but the pulse amplitude is increased. This increases the total volt-second energy input per pulse by E_a times the pulse duration. As a result a higher value of E_a causes core 20 to saturate after fewer pulses 14, i.e., it produces a lower count. A lower value of E_a has the opposite effect, i.e., it produces a higher count. When E_a equals zero, the count is a maximum for the polarities shown in the drawing. Thus no power is wasted, because no more power is drawn from the auxiliary source E_a than is necessary to lower the count when that is desired. In practical embodiments of the invention, count ranges from 1 to 10 and greater are easily achieved in this manner. Furthermore, if the polarity of the source E_a were reversed so as to reduce the amplitude of the pulses 14, then the count would be increased.

The interstage transistor Q103 is normally turned off and thus blocks the voltage E_a from the coils N5 and CN1, CN2, CN3. It is only when a pulse 14 occurs, turning on transistor Q103, that power can be drawn from E_a through the core windings.

ADJUSTABLE VOLTAGE SOURCE

The additional volt-second content added to each pulse 14 by the auxiliary power source is equal to E_a times the pulse duration. Thus the amount of added volt-second product will vary as a function of this pulse duration. For this reason, it is desirable to hold the pulse duration constant. A principal source of variation in the duration of the output pulses 14 is variation in voltage of the principal power source E. Therefore it is desirable that this source E be regulated. It is also desirable that the variable auxiliary source E_a be regulated so that the same increment of voltage E_a is always added to the pulses 14 for any given setting of this voltage.

Furthermore, for a given setting of the variable voltage E_a the ratio between E and E_a may change with varying conditions. Whenever one of these levels varies relative to the other, the stability of the count is affected. A mathematical explanation of this fact will now be given, since it will be helpful in understanding the novel method by which this invention compensates for this effect and maintains the stability of the count.

The counting modulus n of stage 20 equals ϕ_{22} , the total flux excursion required to drive core 22 from negative saturation to positive saturation, divided by ϕ_{14} , the incremental flux excursion produced by a single pulse 14. This gives us the equation $n = \phi_{22} / \phi_{14}$. The latter quantity ϕ_{14} may be evaluated, starting with the basic equation of magnetic induction, $e = -Nd\phi/dt$, which states that the voltage e induced in a winding equals minus N , the number of turns in the winding, times $d\phi/dt$, the time rate of flux change. When this expression is rewritten $d\phi = edt/N$ and integrated over the time duration of one pulse 14, the result is the equation

$$\phi_{14} = -E_{CN123} t_{14} / N_{CN123}$$

which states that the incremental flux excursion ϕ_{14} equals minus E_{CN123} , the voltage across windings CN1, 2, and 3, times t_{14} , the pulse duration, divided by N_{CN123} , the number of turns in windings CN1, 2, and 3. From FIG. 1 it can be seen that E_{CN123} equals E_{N5} , the output voltage developed across winding N5, plus E_a , the auxiliary voltage, plus a negligibly small drop across transistor Q103 when it is conducting. Thus as a good approximation, $E_{CN123} = E_{N5} + E_a$. When this expression is substituted in the previous equation we get $\phi_{14} = -(E_{N5} + E_a) t_{14} / N_{CN123}$. If the basic induction equation $e = -Nd\phi/dt$ is rewritten $dt = -Nd\phi/e$ and integrated over the time duration of one pulse 14, then the result is $t_{14} = -N_{N3} \phi_{11} / E$, which states that the pulse duration t_{14} equals minus the number of turns N_{N3} in the pulse-former reset winding N3, times the total flux excursion ϕ_{11} when pulse-former core 11 is reset from positive to negative saturation, divided by the voltage applied to the winding N3 during reset, which in FIG. 1 is seen to be equal to E less the negligible drop across Q102 when it is conducting. Substituting this expression for t_{14} in the equation previously derived for ϕ_{14} gives $\phi_{14} = (E_{N4} + E_a) N_{N3} \phi_{11} / N_{CN123} E$. Then substituting this last expression for ϕ_{14} in the original equation for the counting modulus n gives

$$n = \phi_{22} N_{CN123} E / (E_{N5} + E_a) N_{N3} \phi_{11}$$

Several of the terms included in the foregoing equation are constants under certain operating conditions. At a given temperature, the total core flux excursions ϕ_{22} and ϕ_{11} are fixed for a given pair of cores 22 and 11. The numbers of winding turns N_{CN123} and N_{N3} are also fixed for a given pair of windings CN1, 2, 3 and N3. Therefore, the count n is a function of E, E_{N5} , and E_a . E_{N5} is dependent upon E because the voltage induced in winding N5 occurs in response to the reset pulse which source E sends through the winding N2. Therefore the count n is a function of E and E_a , and if the relationship between these two quantities changes then the count changes. For the sake of count stability, therefore, it is desirable to hold constant the ratio of E and E_a . There-

fore a preferred power supply circuit for use with this counter would not only regulate both E and E_a , but would also maintain the relationship between them.

In accordance with this invention, a power supply circuit of this type is shown in FIG. 2. The leads 62, 32a, and 38 of the circuit in FIG. 1 are to be connected to terminals A, G' and B respectively of the power supply circuit in FIG. 2. Terminal B provides a common positive level, and is connected by a bus 150 directly to the positive terminal B' of an unregulated DC supply.

The negative side of the circuit has two parts, a fixed power supply 143 which supplies the voltage E, and an adjustable power supply 168 which supplies the voltage E_a . Looking first at section 148 of the circuit, the negative side of the fixed principal operating voltage E is derived from a bus 152 which goes from the negative terminal A' of the unregulated DC supply to a series regulating transistor Q2. The output of this transistor is applied over a bus 154 to the output terminal G'. The transistor Q2 is controlled so that a regulated potential of E exists across the terminals B and G'. The varying Q2 base signal necessary for exerting this control is provided by a sensing and amplifying transistor Q1. For voltage regulation purposes, the emitter of Q1 is clamped at a reference potential determined by Zener diode CR3. The base of transistor Q1 is connected to a potential determined by a resistive voltage divider R2, P1, R3 placed across the output buses 150 and 154. Consequently, as the output voltage across these buses varies, this variation is sensed by Q1 and an amplified error signal is supplied to Q2 to correct the output voltage, variation. This circuit as so far described will be recognized as a well known type of voltage regulator circuit.

Potentiometer P1 allows for initial adjustment of the Q1 base voltage to a desired operating point. The fixed resistors R2 and R3 need only be sufficiently accurate to roughly set the limits of the range of operation. Therefore wide-tolerance, low-cost components R2 and R3 may be employed, and any inaccuracies caused by these components can be cancelled by factory adjustment of the potentiometer P1. This simple adjustment need only be made once, after which P1 requires no further attention and the device may be sealed or potted prior to shipment from the factory.

Looking next at section 168 of the circuit, the negative side of the variable auxiliary voltage E_a is derived from another negative bus 170 and another regulator circuit which operates similarly to the one just described. Bus 170 goes from the negative source terminal A' to a series regulating transistor Q110. The output of this transistor is taken over a bus 172 to terminal A. A sensing and amplifying transistor Q111 varies the Q110 base signal in such manner that the voltage across the buses 150 and 172 is regulated at a level equal to E_a plus E. The resulting voltage across terminals A and G' is therefore E_a , as required.

As a key novel feature of this circuit, the emitter of Q111 is returned over a lead 174 to the same reference potential determined by the Zener diode CR3 previously discussed. In this way the single regulator CR3 is used to control both the circuit 143 which supplies the fixed voltage E and the circuit 168 which supplies the variable voltage E_a . Therefore, the Zener regulation for these two voltage levels automatically stays in track, and for any given setting of E_a the relationship between E and E_a is maintained. This circuit is advantageous because it promotes stability of the selected count, and also because the use of one Zener diode instead of two is a cost-saving feature.

The base of the transistor Q111 is connected to sense the potential determined by a resistive voltage divider. The divider is connected across the output buses 150 and 172 so that the sensed potential varies with the output voltage on these buses to provide an error signal. However, in order to allow for adjustment of the count there

is a choice of several voltage dividers such as R126, P101, R125, and R140, P108, R141. There is one such voltage divider for each value of the count n which can be selected. A manual multi-position switch 200 is employed to select which one of the voltage dividers shall be connected to the base of Q111. This determines the count n . Since it is wasteful of power to leave all the voltage dividers connected across the output buses 150 and 172 when only one of them can be used at any time, another multi-position switch 202 is ganged with switch 200 and is arranged in such manner that it connects to the power bus 172 only the one voltage divider which is then connected to the base of Q111. Each voltage divider again comprises a pair of fixed, low-cost, wide-tolerance resistors such as R126, R125 and R140, R141, which serve to roughly set the limits of operation for each particular setting of the count n . Within that range more accurate adjustment of the Q111 base voltage to the desired operating point for each count is achieved by means of potentiometers such as P101 and P108. Again, this has the cost-saving advantage of allowing simple factory adjustment to compensate for errors resulting from the wide tolerances. In addition, the settings for the various values of the count n are made individually on their respective potentiometers P101 through P108. Consequently no potentiometer adjustment is necessary each time the customer changes the count. As a result, the potentiometers can be finally set at the factory and the units sealed or potted prior to shipment. In view of the stepwise adjustment of the count provided by the switch 200, and the individual factory-sealed adjustments provided for each count setting by the respective potentiometers P101 through P108, the customer is able to switch in a simple manner from one optimum discrete count setting to another, without danger of setting the counter in any intermediate conditions wherein the count might be ambiguous.

The description of these circuits 148 and 168 is intended to apply also to portions of the circuits of FIGS. 4 through 6, where to facilitate comparison similar reference characters are used except for certain distinguishing prefixes and suffixes.

MULTI-STAGE HIGH COUNT DEVICE

Consideration will now be given to the manner in which multiple counting stages in accordance with this invention may be interconnected in a novel manner to achieve higher counts than are possible with a single stage. Simply connecting two or more stages in cascade permits the selection of only those counts which are equal to the products of the available counting moduli of the individual stages. In order to avoid this limitation the stages are interconnected in the manner generally indicated by FIG. 3. This block diagram shows the general outlines of a system capable of counting up to any integer in the range from one to nine hundred ninety-nine. The system comprises three separate sections: a units counting section, a tens counting section, and a hundreds counting section. The units counting section comprises an adjustable counter U20 which counts from one to nine. The tens counting section includes a fixed decade counter AF20T which counts to ten, and an adjustable multiplier counter A20T which is adjustable to count from one to nine. The setting of the counter A20T determines to what multiple of ten the tens section will count, hence the term "multiplier" counter. The hundreds counting section also includes a fixed counter AF20H plus an adjustable one to nine multiplier counter A20H. In order to provide a basic fixed count of one hundred for this section at minimum cost, the two fixed decade counters AF20T (of the tens counting section) and AF20H (of the hundreds counting section) may be connected in cascade to count up to one hundred whenever this section is in use. The details of this connection are described below. Starting with this basic count of one hundred, the adjustable multiplier

counter A20H determines the multiple of one hundred to which the section will count.

A pulse-former unit U10 receives the count input and applies its formed output pulses to the counters U20 and AF20T of both the units and tens counting sections. However only the particular counting units which are activated at any given moment respond to these pulses. In order to turn the counter units on and off as required, their respective power inputs are applied through "and" gates 286, 288T, 290T, 288H, and 290H. Therefore, these gates must be enabled in particular combinations in order to permit power to be applied to the desired counters. To accomplish this, each counting section includes one flip-flop U296, A296T, or A296H of the units, tens, and hundreds counting sections respectively.

In order to explain the operation of this invention, a typical counting operation will now be described. For the moment it will be assumed that the selected count is a number between 100 and 999, and it will be further assumed that none of the digits of this number equals zero. Initially, the units flip-flop U296 is set, while the tens flip-flop A296T and the hundreds flip-flop A296H are in their reset condition. The set condition of the units flip-flop U296 enables the gate 286, which activates the counter U20 of the units counting section. The reset condition of the other two flip-flops disables the gates 288T, 290T, 288H, and 290H, which in turn disables the counters AF20T and A20T of the tens section and AF20H and A20H of the hundreds section respectively. Therefore at this time only the units counting section can respond to the pulse-former U10 and only units are counted.

After counting the desired units number of inputs, counter U20 provides an output which resets the units flip-flop 296, disabling the gate 286 to disable the units counter U20. This output also sets the tens flip-flop A296T, as a result of which the gates 288T and 290T are enabled, to activate the counters AF20T and A20T respectively of the tens counting section. The hundreds counting section remains off. Thus only the tens section is on, and therefore tens are counted as the fixed decade counter AF20T responds to the output of the pulse-former U10. The output of the fixed counter AF20T is cascaded with the adjustable one to nine multiplier counter A20T to count the desired multiple of ten. Thus the tens count is added to the previously completed units count.

When the tens counting operation is completed the output of counter A20T resets the tens flip-flop A296T to shut off the tens counting section. This output also sets the hundreds flip-flop A296H. The resulting set output from this flip-flop enables the gate 288T which is associated with the fixed decade counter AF20T of the tens counting section, and also enables the gates 288H and 290H which are associated with the decade counter AF20H and adjustable counter A20H respectively of the hundreds counting section. The adjustable counter A20T of the tens section is not turned on. Hence this operation amounts to partial activation of the tens counting section together with total activation of the hundreds counting section. At this time, the units section remains off. Thus only the three counters AF20T, AF20H, and A20H are now activated to form the hundreds counting chain. The first two of these are fixed decade counters which are connected together in cascade to count up to 100. When the decade counter AF20T is activated, it responds to the output of the pulse-former U10 just as it did for the tens counting operation. Each tens output from the counter AF20T is applied to the decade counter AF20H which is now also activated. Each hundreds output from counter AF20H is cascaded to the adjustable one to nine multiplier counter A20H to count the desired multiple of 100. The output from counter A20H constitutes the count output of the system. It represents the sum of the units digit plus the tens count plus the hundreds count. This output is also used to reset the hundreds flip-flop A296H

in order to terminate the activation of the hundreds counting chain at the end of the system counting cycle.

The count output of the system is applied to a terminating module which responds by energizing or picking a relay to provide the desired power output upon attaining the predetermined count. The terminating module also provides a restoring output which serves the function of returning the entire counting system to the proper condition for the start of the next counting cycle. In FIG. 3 the restorer function is illustrated as consisting primarily of the operation of setting the units flip-flop U296 once again. However, in subsequent more detailed description of this counting system it will be seen that the restoring function involves certain other operations which become important when the selected count has some digits equal to zero.

As a concrete example of the counting operation just described, suppose that the selected modulus of the system is the prime number 967, which would not be attainable with a counting system limited to moduli which equaled the product of the individual counting moduli to which the separate stages could be adjusted. In order to achieve this count with the present system, it is only necessary to set the adjustable counter U20 of the units counting section to count the units digit 7, set the adjustable counter A20T of the tens counting section to count the tens digit 6, and the adjustable counter A20H of the hundreds section to count the hundreds digit 9. The first seven pulses are counted by the counter U20. After that the tens counters AF20T and A20T combine to count the next tens times six or sixty pulses. Following this the counters AF20T, AF20H, and A20H combine to count the next 100 times 9 or 900 pulses. In this way the system counts the total of 7 plus 60 plus 900, or 967 pulses all together.

MODULAR CONSTRUCTION

In a practical high count device according to this invention, certain features in addition to those shown in FIG. 3 are required to meet the problems presented by the presence of one or more zeroes in the higher or lower orders of the desired count. The detailed circuitry of such a practical embodiment is illustrated in FIGS. 4 through 8. These drawings also serve to show the manner in which such a counting system may be conveniently constructed in modular form to allow the customer the greatest choice of counting ranges at the lowest production cost. FIGS. 4 through 7 show the four different types of modules required, while FIG. 8 shows the interconnections between modules of these types necessary for creating a hundreds range counting system. FIG. 5 shows a units module which comprises the units counting section of FIG. 3 plus certain associated circuitry. FIG. 6 shows an adder module which comprises the tens counting section of FIG. 3 plus certain associated circuitry. In order to constitute a hundreds range counting system, a second adder module identical with the first one is connected in the system, and when all the modules are connected as shown in FIG. 8 the second adder module comprises the hundreds counting section of FIG. 3 plus certain additional circuitry. The terminating module of FIG. 3 is shown in full circuit detail in FIG. 7. FIG. 4 shows a power supply module which contains various components that are common to the power supplies of all the other modules in the system.

One of the principal advantages of the system to be described is the fact that by an appropriate selection and arrangement of the modules just mentioned, the system can be arranged for different count ranges. If a customer wishes only to be able to adjust the count within a range of, for example, one to ten, then a simple counter device in accordance with FIG. 1 plus an appropriate power supply in accordance with FIG. 2 and any appropriate output circuit will suffice. When the customer desires a system capable of achieving a higher count in accordance

with the principles illustrated in FIG. 3, the more extensive circuitry of FIGS. 4 to 8 would be employed. With this latter type of system, four modules can be arranged as shown in FIG. 11 to achieve a count which is adjustable over the range from one to ninety-nine, or five modules can be arranged in the manner shown by FIG. 8 to achieve a count which is adjustable in the range from one to nine hundred ninety-nine. This permits the customer to economize by purchasing only so many modules as are required for the desired count range.

A comparison of FIGS. 11 and 8 shows that the difference between the smaller and larger systems is that the tens range system has only one adder module, while the hundreds range system has two adder modules. This invention contemplates that the two adder modules shall be identical in circuitry for minimal production cost. This requires that each module must have the capability of functioning in any one of three ways: as the adder module of a tens range counting system, as the tens adder module of a hundreds range counting system, or as the hundreds adder module in a hundreds range counting system.

Each of the individual modules will now be described in detail. As this description progresses, it will be helpful to refer back to the previous description of FIGS. 1 and 2. Such reference will be facilitated by the scheme of reference characters which clearly shows the correspondence between components in the various drawings. It will also be helpful to correlate the lettered terminals of the various modules of FIGS. 4 through 8 with corresponding circuit points in the schematic diagrams of FIGS. 1 and 2, and also with the operations indicated in the block diagrams of FIGS. 3, 9 and 10. This is facilitated by a scheme of reference characters which clearly points out the correspondence between these terminals and their related circuit points and logical operations.

POWER SUPPLY MODULE (FIG. 4)

This module supplies certain operating voltages for all the other modules. For the purposes of description the circuit may be divided into two parts, a DC source 360, and a fixed output voltage regulator PS148.

D.C. source 360.—The first part of the circuit, DC source 360, is a conventional power supply front end which receives the usual 117 volt, single phase, 60 cycle AC input and provides an unregulated DC output. The AC input is applied across terminals 362 and 364 through an on-off switch SW-1 and a fuze FU-1 to the primary of a transformer T1. A pilot light PL-1 is shunted across the transformer primary. The transformer secondary output is full-wave rectified by a pair of diodes CR1 and CR2, and filtered by a capacitor C1.

Fixed regulator PS148.—This circuit corresponds to the fixed power supply 148 of FIG. 2. Its function is to supply the fixed regulated voltage E. The positive voltage on lead PS150 is brought out to the terminal PSB. This represents the common positive side of all voltages employed by the counting system. The negative unregulated potential on lead PS152 passes through the series regulating transistor PSQ2 and is then delivered as the regulated voltage E negative over lead PS154 to terminal PSG. Sensing and controlling transistor PSQ1 controls the regulating transistor PSQ2, and has its base connected to the potentiometer PSP1 which forms a voltage divider along with resistors PSR2 and PSR3. A Zener diode PSCR3 provides the fixed emitter reference potential for PSQ1. An additional smoothing capacitor C2 is connected across the output terminals PSG and PSB. The Zener reference voltage is brought out over a lead PS174 to a power supply module output terminal PSZ, so as to make this same reference voltage available to all other modules in the counting system. The unregulated negative voltage is similarly made available at a power supply module output terminal PSA, for use by all the other modules in the system.

From FIG. 8 it can be seen that the voltage on power supply module output terminal PSA is connected to units

module terminal UA, tens adder module terminal AAT, hundreds adder module terminal AAH, and terminating module terminal TA. Similarly, terminal PSB is connected to terminals UB, ABT, ABH, and TB. Terminal PSG is connected to terminals UG, AGT, AGH, and TG. The reference voltage terminal PSZ is connected to terminals UZ, AZT, and AZH.

UNITS MODULE (FIG. 5)

This module includes the pulse-former U10, the adjustable units counter U20, the gate 286, and the flip-flop U296. It also includes an adjustable power supply circuit U168, which corresponds to circuit 168 of FIG. 2, for supplying the adjustable count-selecting voltage E_a . The operating voltages which this module receives from the power supply module are the fixed voltage E negative which is connected to terminal UG, an unregulated negative voltage connected to terminal UA, and the common positive side of both these voltages which is connected to terminal UB.

Pulse-former U10.—The positive side of the count input to the pulse-former U10 is applied to an input terminal UF and lead U30. The negative side is applied to another input terminal UG and a lead U32. This latter terminal is also the input point for the fixed E negative supply voltage. As previously described in connection with FIG. 1, the pulse-former U10 includes an input transistor PFQ101 and an input winding PFN1 linking the core U11. After the core has been driven past saturation a sensing winding PFN2 turns on a resetting transistor PFQ102 to send a surge of current through the resetting winding PFN3 which also links the core U11. During the flow of resetting current the formed pulse output of circuit U10 is induced in a main output winding PFN5 which also links core U11. This output is applied to the adjustable counter U20 over leads U64 and U66. Collector current for transistor PFQ101 is supplied from positive input terminal UB over lead U38, resistor PFR102, and winding PFN1, and is returned over leads U32d and U32 to the fixed E negative terminal UG.

One to nine counter U20.—The negative side of the formed pulse output from circuit U10 is applied over lead U66 to the emitter of the interstage transistor UQ103. The positive side of this output is applied over lead U64 to the base resistor UR105 of transistor UQ103. Since UQ103 is of the NPN type, this voltage serves to render the transistor conductive. At this point a series circuit is created starting with the adjustable E_a voltage supplied by circuit U168 over lead U62, and continuing over lead U64 and through winding PFN5, lead U66, transistor UQ103, and input windings UN1, UN2, and UN3 wound on the core U22 of the adjustable counter circuit U20. The return side of this series circuit goes over leads U32c and U32 to the fixed E negative potential on terminal UG. Thus, as in FIG. 1, the adjustable voltage E_a which exists between the terminal UG and the lead U62 is placed in series with the main output winding PFN5 of the pulse-former and the input winding UN1, UN2, UN3 of the counter, so as to augment the voltage of the formed pulses and thus alter the count in accordance with this invention.

Adjustable power supply U168.—Lead U62 is maintained at the adjustable voltage level E_a negative by means of the adjusting and regulating circuit U168. The unregulated negative voltage applied to the units module input terminal UA is applied over a lead U170 to the gate 286. When this gate is enabled the unregulated negative voltage is allowed to pass via a lead U170' to the series regulating transistor UQ110 of circuit U168. The emitter output voltage of UQ110 is delivered over a lead U172 to which the counter supply lead U62 is connected. For regulation purposes the transistor UQ110 is governed by a sensing and controlling transistor UQ111. The latter draws its emitter reference voltage over a lead U174 from a units module input terminal UZ which in turn is connected to the reference voltage terminal PSZ of the power

supply module of FIG. 4. Thus, just as in the circuit of FIG. 2, this reference voltage is drawn from the same Zener diode PSCR3 of FIG. 4. As previously noted, this feature saves component expense and also helps to keep the fixed E and adjustable E_a voltages in track with each other over varying operating conditions.

The base of the sensing and controlling transistor UQ111 is selectively connectable by means of a manual selector switch U200 to the appropriate one of several alternative voltage levels in order to determine the count setting for the adjustable counter U20. These individual voltages are provided by respective individual voltage-dividers connected across the negative lead U172 and a positive supply lead U150 which is returned to the positive input terminal UB. There is one such voltage-divider for each of the nine available count settings of the counter U20 from one through nine. For example, in order to provide a count of nine the voltage-divider UR140, UP108, UR141 is employed. The center tap of potentiometer UP108 is labeled "nine." This indicates that it corresponds to the nine count setting. It also indicates that this center tap should be understood to be connected to the terminal labeled "nine" of the count selector switch U200. The other voltage-dividers for count settings three through eight are similarly labeled and connected. The voltage-divider UR126, UP101, UR127 for the count setting of two is explicitly connected to the two count terminal of switch U200 as a specific example of this type of connection.

The voltage-divider for a count of one is somewhat different. Since a counter operated in a one to one count division ratio is quite stable, the bias voltage setting for operating in this mode is not particularly critical. Therefore it is feasible to employ a voltage-divider consisting simply of a pair of fixed, wide-tolerance resistors UR124 and UR125 to set this biasing level. A lead 384 connects the junction between these two resistors directly to the one count terminal of switch U200.

Another and similar switch U202 is ganged with the switch U200 so that both switches always select the same numbered terminal. Switch U202 serves to connect to the positive lead U150 only the particular one of the voltage-dividers which is then being tapped by the base of the transistor UQ111.

Gate 286.—The negative input to the adjustable power supply U168 is switched on or off by the gate 286, which comprises the gating transistor Q113. The negative voltage on terminal UA and lead 170 must pass through Q113 to reach lead U170'. In order to render Q113 conductive switching current must be applied to its base over a lead 396, which is connected through a resistor R114 and a lead 404 to the collector of the set transistor Q107 of flip-flop U296. When the flip-flop is set Q107 conducts, and part of its collector current flows through flip-flop output lead 404, resistor R114, lead 396, and the base-emitter path of gating transistor Q113 to turn on Q113 and thus enable the gate 286.

Flip-flop 296.—This circuit comprises a set transistor Q107 and a reset transistor Q106. Both transistors draw positive emitter power from the lead U150 through a limiting resistor R118 which is bypassed by a coupling capacitor C108. The collectors of Q106 and Q107 are returned to the negative lead U170 through respective resistors R109 and R113. Since Q106 and Q107 are both of the PNP type, each requires negative base bias for switching on, while positive base drive turns them off. Also, when either transistor is switched on its collector potential rises owing to the drop across the respective collector resistors R109 and R113. For bistable operation in which one and only one of the two flip-flop transistors conducts at any time, the collector output of transistor Q107 is coupled to the base of Q106 through the network R112, C107. Similarly, the collector of Q106 is coupled to the base of Q107 through the network R110, C106. As a result of this cross coupling, when either transistor turns

on its positive going collector voltage is applied to the base of the other transistor, turning that other transistor off.

When the set transistor Q107 is conducting, the flip-flop may be reset by applying a positive pulse over input lead U56a, diode CR105, and coupling network R111, C103 to the base of the conducting set transistor Q107. This pulse turns Q107 off, whereupon its collector voltage drops and allows the base of the reset transistor Q106 to go sufficiently negative so that Q106 turns on. The feedback from the collector of Q106 to the base of Q107 keeps Q107 turned off.

In order to set the flip-flop once again, a positive pulse is applied over input lead 556 and diode CR109 to the base of the conducting reset transistor Q106. This has the effect of turning off Q106, and allowing Q107 to turn back on. The collector of Q107 then feeds back to the base of Q106 to keep Q106 turned off.

Units counting operation.—When the units module first begins to count, the flip-flop U296 is initially in the set condition. Consequently part of the collector output current of transistor Q107 flows over output lead 404, resistor R114, lead 396, the base-emitter path of the gating transistor Q113 and lead 170 to negative supply terminal UA. This current turns on Q113 and thus enables gate 286. As a result, the negative supply on terminal UA and lead U170 passes through gating transistor Q113 and over lead U170' to the adjustable power supply circuit U168. Consequently the selected E_a negative voltage is made available by circuit U168 over lead U62 to the adjustable counter U20, and this counter becomes activated. Therefore the units module becomes effective to count the selected units number of input pulses.

We shall continue for the time being to assume that no digit in the selected count is equal to zero. The input pulses supplied to the pulse-former circuit U10 are acted on by it, and the resulting formed pulses developed in the main output winding PFN5 are applied to the counter U20. When U20 reaches the desired units count an output indicative of that fact is developed across an auxiliary output winding UN4. The side of this winding which is more negative when the output is induced therein, is connected directly to the lead U38 to be clamped at the power supply potential of terminal UB. The other side of auxiliary output winding UN4 goes positive when an output is induced therein, and this side is connected to a lead U56' and then to a flip-flop reset input lead U56a. Thus the positive output pulse from winding UN4 is applied to reset the flip-flop U296. When the flip-flop resets, output current from the collector of set transistor Q107 is no longer available, and the gating transistor Q113 therefore turns off. As a result the negative supply on the lead U170 no longer passes through gate 286 to the adjustable power supply circuit U168. As a result activating voltage is no longer supplied by circuit U168 to the counter U20 over lead U62. Thus the units counter U20 is inactivated at the end of the units count.

Shift to tens counting.—The positive output from winding UN4 which is delivered over lead U56' is also applied through diode CR107 and coupling network R119, C104 to a units module output terminal UX. This positive pulse is connected to the appropriate input terminal of the tens adder module to shift the counting system over to tens counting, as will be described below.

ADDER MODULE (FIG. 6)

Each adder module comprises a fixed decade counter AF20 which may function as either the counter AF20T of the tens counting section or AF20H of the hundreds counting section. Similar dual capabilities characterize certain other components of the adder module, including the gate 288 which controls the flow of power to the fixed counter AF20, the one to nine adjustable counter A20, the adjustable power supply circuit A168 which provides the adjustable voltage E_a to the circuit A20, the gate 290 which controls the flow of power from cir-

cuit A168 to circuit A20, the flip-flop A296 which enables the gates to activate the adder module, and an amplifier 482 which amplifies the output of flip-flop A296 to provide adequate power for enabling gates 288 and 290.

Various other components of the adder module such as the various lettered input and output terminals and the switch 205 may also function either as part of a tens adder module or a hundreds adder module. Therefore to clarify matters, in FIGS. 3 and 8 through 11, as well as at certain places in the specification, the suffix T is used to designate a particular circuit or component in its capacity as part of a tens adder module while the suffix H is used to designate the same circuit or component in its capacity as part of a hundreds adder module.

The adjustable counter A20 is identical with the units counter U20. The fixed decade counter AF20 is almost identical with counters previously described, the only difference being the fact that the base resistor R201 of its input transistor Q201 is not returned to a source of adjustable auxiliary voltage E_a as in the case of the adjustable counters described herein. Instead, the base resistor R201 is connected through a lead AF64 and a gate circuit 288 to a source of fixed E negative potential on the adder module input terminal AG. The adjustable power supply A168 is identical to the circuit U168 of the units module. Here again the sensing and controlling transistor Q211 draws its emitter reference potential over a lead A174 from an adder module input terminal AZ which in turn is connected to the reference potential output terminal PSZ of the power supply module of FIG. 4. This and all other intermodule connections are shown in FIGS. 8 and 11. The adder module flip-flop A296 is almost identical with the units flip-flop U296, the only difference being that circuit A296 has two additional reset input leads 557 and 559.

Adder module operation.—The operation of this module will first be considered without regard to whether it is functioning as a tens or hundreds counting section. Operation of the module is initiated when a positive set input pulse is applied to the flip-flop lead A556. This sets the flip-flop A296 by turning off the reset transistor Q206 and turning on the set transistor Q207. When Q207 turns on its collector voltage goes high and provides an output on the lead A404 to the amplifier circuit 482. This output voltage on lead A404 causes base-emitter current to flow through the first stage Q208 of amplifier 482. Q208 then turns on, drawing current from the positive lead A150 through R221 and R220, Q208 and CR210 to the negative lead A170. Emitter-base current of the second stage Q209 also flows from positive lead A150 through CR211, R220, Q208, and CR210 to the negative lead A170. This current switches on the second stage Q209 of the amplifier 482. As a result, output current from the amplifier 482 flows in the form of Q209 collector current along a lead 510, resistors R208 and R207, and a lead 526 to the negative lead A170. Part of this amplifier output current branches off to the gate 288, flowing through diode CR204, resistor R205, and the base-emitter path of gating transistor Q205 to the negative adder module supply terminal AG. This current serves to switch on the transistor Q205 to enable gate 288. The output current of amplifier 482 also branches off from the junction of resistors R208 and R207 along a lead 530 and then through the base-emitter path of transistor Q212 and over lead A62' to the negative lead A172. This provides switching current for the transistor Q212 so as to enable the gate 290. Gate 290, when enabled, makes the adjustable E_a negative voltage on lead A172 available over leads A62' and A62 to the adjustable counter A20. Gate 288, when enabled, makes the fixed E negative voltage on adder module input terminal AG available over lead AF62 to the base resistor R201 of the input transistor Q201 of the fixed counter AF20. Thus, when the flip-flop A296 is set, it energizes the amplifier 482 which in turn enables the gates 288 and 290, and these then activate the counters AF20 and A20 respectively.

When the fixed counter AF20 is activated the positive side of its input pulses are applied to the terminal AG' and then over a lead AF64 and through resistor R201 to the base of the input transistor Q201. The negative side of the input is applied to terminal AF and over lead AF66 to the emitter of Q201.

Tens counting operation.—The positive shift pulse output from terminal UX of the units module is connected to the input terminal AQT of the tens adder module. This input then travels over a lead 601T to the wiper arm of a switch A203T. Since we are still assuming that the tens digit exceeds zero, the pulse must then emerge on a lead 603 which is connected to the set input lead A556T of the flip-flop A296T. This sets the flip-flop of the tens adder module and shifts the counting system over to tens counting operation. The flip-flop set output on lead A404T energizes the amplifier 482T which in turn enables gates 288T and 290T to activate the counters AF20T and A20T respectively.

While the pulse-former U10 was receiving the desired units number of pulses, the units counter U20 was activated and responded to pulse-former outputs developed in the main output winding PFN5. After counting of the units number of pulses, the counter U20 is shut off in the manner previously described, and it no longer responds even though the pulse-former U10 continues to receive input pulses and to develop an output voltage across its main output winding PFN5. From this point on, only the output voltage developed across an auxiliary winding PFN4 will play any part in the operation of the counting system for the remainder of the counting cycle.

The positive-going side of the output from winding PFN4 is connected over a lead U64' to a units module output terminal UJ. The negative-going side of this output is connected over a lead U66' to terminal UH. This units module output terminal UH is connected to the tens adder module input terminal AFT so that the negative side of the pulse input is applied over a lead AF66 to the emitter of input transistor Q201 of the fixed counter AF20T. The positive units module output terminal UJ is connected to the tens adder module input terminal AG'T so that the positive side of the input is applied over lead AF64 to the base resistor R201 of the input transistor Q201. Thus the pulses from the pulse-former U10 serve to open the input transistor Q201 and to pass through Q201 to be counted by circuit AF20 in the manner previously described. It will be seen that circuit AF20 is a fixed counter because of the fact that its input windings AFN1, AFN2, AFN3 are returned over lead AF32c to a fixed voltage, the fixed E negative voltage which lead A32 derives from the adder module input terminal AGT. The fixed counter AF20 is designed to count exactly ten pulses.

For every ten pulses counted by the circuit AF20T, an output is developed across its main output winding AFN5. The negative side of this output is applied over a lead AF54 to the emitter of the interstage transistor Q203. The positive side of the output is applied over a lead AF56 to the base resistor R203 of Q203. Thus, these pulses open up Q203 and pass through it to be counted by the adjustable counter A20. The number of pulses counted by circuit A20 before it produces an output is determined by the selected voltage applied to it over lead A62 by adjustable power supply circuit A168 and gate 290. When the desired multiple of ten has been counted by circuit A20T, an output is developed across its auxiliary winding AN4 and applied over leads A56' and A56a to reset the tens flip-flop A296T. The reset of the flip-flop terminates the tens counting operation. The output on lead A56' also is applied through diode CR207 and network R219, C204 to a tens adder module output terminal AXT. This tens adder module output serves to shift the system over to hundreds counting operation.

Hundreds counting operation.—The positive shift output from the tens adder module terminal AXT is con-

nected to the hundreds adder module input terminal APH. From there it goes over a lead 605H to the set input lead A556H of the hundreds flip-flop A296H. This causes the flip-flop A296H to be set, which in turn energizes amplifier 482H. The output current from the amplifier on lead 510 enables the gates 288H and 290H to activate the counters AF20H and A20H in the manner previously described. The output current also branches off over a lead 607 to a hundreds module output terminal AMH. This terminal is connected to an input terminal ANT of the tens adder module. Consequently, output current from the amplifier 482H flows through diode CR203T and the resistor R205T and through the base-emitter path of gating transistor Q205T to the negative terminal AGT. This turns on gating transistor Q205T to enable gate 288T of the tens adder module. Gate 288T then activates the fixed decade counter AF20T for partial activation of the tens adder module. This enables the fixed decade counter of the tens module to join with the fixed decade counter of the hundreds module in forming a hundreds counting chain when the hundreds module is activated. When the tens adder module is partially activated in this manner, the gate 290T and its associated counter A20T are not turned on. In particular, the current from terminal ANT flowing through CR203T to enable the gate 288T is blocked by diode CR204T from flowing through resistor R208T and lead 530T to the base of transistor Q212T of gate 290T.

With the tens module fixed counter AF20T once again activated, the formed pulses from the units module circuit U10 applied to the tens module input terminals AFT and AGT are again counted by the circuit AF20T in the manner previously described. This time however, circuit AF20T counts the formed pulses for the purpose of counting hundreds instead of tens. The tens counting output from the main winding AFN5T is applied to the now inactive tens counter A20T. Therefore pulses from this winding are not counted by the inactive counter. However the auxiliary output winding AFN4T also produces output pulses for the counter AF20T. The positive side of this output is connected over a lead AF56' to a tens module output terminal AJT. This in turn is connected to the hundreds module input terminal AG'H so that the positive side of the output is applied over lead AF64H to the base resistor R201H of the input transistor Q201H of the hundreds fixed counter AF20H. The negative side of the output from winding AFN4T is applied over a lead AF54'T to a tens modules output terminal AHT. This is connected to a hundreds module input terminal AFH, so that the negative side of the output is applied over lead AF66H to the emitter of Q201H. These pulses are counted by circuit AF20H in the manner previously described, and the outputs developed across winding AFN5H are applied to the hundreds counter A20H over leads AF54H and AF56H in the manner previously described.

When the desired number of multiples of one hundred has been counted, circuit AF20H develops an output across its auxiliary winding AN4H. The side of this winding which goes more negative when the output is developed therein is connected over a lead A38H to be clamped at the power supply potential of terminal ABH. The side of the winding which goes more positive when the output is induced therein is connected over a lead A56' to the flip-flop reset input lead A56a. This resets the hundreds flip-flop A296H to terminate the hundreds counting cycle. At the same time, an output is also developed across the main winding AN5H. The side of this winding which goes more negative when the output is induced therein, is connected over a lead A54H to be clamped at the negative potential on lead A170H. The side of the winding which goes more positive at this time is connected over a lead A56H to a switch 205H. Still assuming that none of the digits are equal to zero, the output thus applied to switch 205H will emerge over a lead 570 to a hundreds module

output terminal ASH. The output from this terminal represents the counting system output which triggers the terminating module.

TERMINATING MODULE (FIG. 7)

The positive-going count output from terminal ASH is connected to input terminal TS of the terminating module. The positive pulse is then coupled through C301 to the base resistor R302 of the first stage Q301 of an output amplifier circuit 580. This causes base biasing current to flow through the emitter of Q301 and the emitter diode CR302 to a lead 590 which is connected to the terminating module negative power supply input terminal TA. A back-poled diode CR301 is connected between C301 and the negative lead 590 to clip any input pulses of excessive amplitude. The base drive to Q301 causes this transistor to turn on. Current then flows from the terminating module positive power supply input terminal TB over a lead 700, through a manual restore switch 582, a terminal TW, a lead 702, resistors R307 and R306, transistor Q301, and diode CR302 to the negative lead 590. Switching current for the second stage Q302 of this amplifier then branches off through diodes CR307, the emitter-base path of the second stage transistor Q302, and then on through R306, Q301, and CR302 to negative lead 590. This switching current turns on the amplifier second stage Q302, causing it to draw collector current through CR307, Q302, load resistor R304, output terminal TE, and a relay coil 350 to the negative lead 590. The energization of relay coil 350 is the useful output of the counting device of this invention. A back-poled diode CR303 is connected across the relay coil 350 for the purpose of dropping inductive kickback spikes generated when the coil current is terminated.

The output amplifier 580 also serves as a pulse-stretcher circuit which energizes the relay coil 350 for a predetermined time which is longer than the duration of the count output pulse applied to terminal TS. Initially the count output pulse turns on the first stage Q301, which then turns on the second stage Q302. However, Q302 then feeds back to latch Q301 in its conducting condition for a predetermined time. As Q302 turns on a feedback path is established from the collector of Q302 through R305 and C302 to the base resistor R302 of the first stage Q301. This feedback connection provides base biasing current to sustain the conduction of Q301 during the time that feedback current flows through C302. When C302 finally charges, the feedback current can no longer flow through this capacitor, and since the input pulse on terminal TS has already terminated, the first stage Q301 is allowed to turn off. This deprives the second stage Q302 of its base biasing current, causing Q302 to turn off also. C302 then discharges through R305, R304, the relay coil 350, lead 590, and R301. By discharging through the relay coil 350, C302 prolongs the period of relay energization even further. Thus, the energization of relay coil 350 is prolonged for a time that is determined by the time constant of C302 and its various associated resistances through which it is charged and discharged.

The operation of the output amplifier and pulse-stretcher circuit 580 has been described with the operating mode switch 648 open as illustrated. If it is desired that the relay coil 350 be energized for an indefinite time, it is only necessary to close the operating mode switch 648 and the circuit will then operate in a maintained mode instead of the momentary mode described above. With switch 648 closed, the Q302 collector current feedback through R305 finds a permanent path through R303, terminal TD, switch 648 and terminal TC to the base resistor R302 of the first stage Q301. This permanent feedback path is not blocked by the charging of capacitor C302. Therefore the circuit 580 continues to energize the relay coil 350 until the operating mode switch 648 is manually opened.

Circuit 642 is energized each time that the output amplifier 580 is fired, and serves the purpose of resetting

the entire counting system. It does this by providing a first output which resets all the magnetic cores of all the counters in the system, and a second output which restores all the flip-flops in the system to the appropriate condition for the start of the next counting cycle. When the output amplifier 580 turns on, a positive signal is coupled from the collector of the second stage Q302 through capacitor C303 to the base resistor R308 of a first core-resetting stage Q303. Base drive current then flows through the base-emitter path of Q303 and through diode CR305 to the negative lead 590. A diode CR304 connected between the negative lead 590 and the junction of C303 and R308 serves the purpose of limiting signals of excessive amplitude. The base drive causes the first stage Q303 to turn on. Current then flows from the terminating module positive power supply terminal TB through a lead 704, resistors R311 and R310, Q303, and CR305 to the negative lead 590. Switching current is also drawn for the second core-resetting stage Q304. This current flows from positive lead 704 through diode CR306, the emitter-base circuit of Q304, and then through R310, Q303, and CR305 to the negative lead 590. This causes the second stage Q304 to turn on and draw current from positive lead 704 through CR306 and Q304 to the core-resetting output terminal TL. From there the current path continues to hundreds module terminal ALH, through a winding AN6H which resets the core 222H, a winding AFN6H which resets the core 211H, and then to a hundreds module output terminal AYH. This part of the circuit causes the current to reset the cores of the hundreds counters A20H and AF20H. The current path is then traced from hundreds module output terminal AYH to the tens module input terminal ALT. In its course through the tens module the current flows through a winding AN6T to reset the core 222T, and a winding AFN6T to reset the core 211T. Thus the cores of the tens counters A20T and AF20T are also reset. The current emerges from the tens module output terminal AYT and proceeds to a units module input terminal UY. Upon entering the units module the current flow proceeds through a winding UN6 to reset the core U22 of the units counter U20. The return path for the current is over a lead 706, a resistor R107, and a diode CR103 to the negative lead U170 of the units module. Resetting of the pulse-former core U11 in this manner is not necessary, since the pulse-former U10 always resets its own core completely on every operating cycle. More specifically, for every input pulse received by the circuit U10, the core U11 is saturated, and then reset to produce the formed output pulse. However the cores U22, 211, and 222 of the counter circuits require anywhere from one to nine or ten pulses to perform a full operating cycle culminating in resetting of the core. Therefore in the event of a spurious pulse it is possible for one of these cores to be left in an intermediate condition. It is in order to avoid having any counting core in an intermediate condition at the start of a counting cycle that the output from terminating module TL is used to reset the counting cores at the conclusion of each count.

Whenever the first core-resetting stage Q303 is operated, it thereafter operates the last two stages Q306 and Q305 of circuit 642. These stages then provide an output at terminal TR which serves to restore the flip-flops of all modules to the appropriate conditions for the start of the next counting cycle. Q303 turns on at the same time that the output stage Q302 of the amplifier 580 turns on. When this happens, the collector voltage of Q303 goes low. Then during the entire pulse-stretching interval of the output amplifier 580, Q302 remains on, Q303 also remains on, and the collector voltage of Q303 remains low. At the end of the pulse-stretching interval of circuit 580, Q302 turns off, allowing Q303 to turn off also, and the collector potential of Q303 then rises to its former level. This causes a positive spike to be coupled through a differentiating capacitor C304 to the base of the first

flip-flop restoring stage Q306, to turn on this stage. Thus, it is seen that flip-flop restoring operation is not initiated until the relay-energizing function of circuit 580 and the core-resetting function of the stages Q303 and Q304 have been terminated. This prevents any change in the state of the flip-flops U296, A296T, and A296H from occurring until after the present condition of these flip-flops has been continued right through to the end of the counting cycle.

Upon receiving the positive spike from differentiating capacitor C304, the first flip-flop restoring stage Q306 turns on and draws current from the positive lead 704 through resistors R313 and R312, Q306, and diodes CR308 to the negative lead 590. Base current to switch on the second flip-flop restoring stage Q305 then also flows from the positive lead 704 through the emitter-base path of Q305, R312, Q306, and CR308 to the negative lead 590. This causes the second stage Q305 to turn on. When Q305 is on, it provides a very low impedance between the positive lead 704 and the terminating module output terminal TR. Thus a high potential is applied to terminal TR and this potential is in turn communicated to the units module input terminal UR and then over a lead 710 to the set input lead 556 of the units flip-flop U296. This positive pulse applied to the set input lead sets the flip-flop U296 and thus restores it to the proper condition for the start of the next counting cycle. The positive pulse applied to lead 710 is also communicated through a diode CR108 to a switch U203. Still assuming that all the digits in the selected count exceed zero, this positive potential will emerge over a lead 712 to the units module output terminal UP.

The pulse then proceeds to a tens module input terminal AUT and is applied to the reset input lead 559T of the tens flip-flop A296T. This causes the tens flip-flop to be reset, which is the proper condition for the start of the next counting cycle.

The tens module terminal AUT is also connected to a hundreds module input terminal AKH. Accordingly a positive pulse is also delivered via terminal AKH to reset input lead 557H to reset the hundreds flip-flop A296H. This puts the hundreds flip-flop in the proper condition for the start of the next counting cycle.

Manual reset.—Switch 582 can be operated manually to reset the counting device at any time that it is desired to do so, even during a counting cycle. Normally the positive power on terminating module terminal TB is applied over lead 700 through the manual reset switch 582 to the terminating module terminal TW and over lead 702 to the output amplifier 580. The switch 582 is spring-biased to this position. Upon being manually depressed switch 582 diverts the positive power to terminating module terminal TV. From there it proceeds over a lead 720 and a resistor R314 to the base of the first stage Q303 of the restoring circuit 642. When this connection is made the first stage Q303 turns on, and triggers stages Q304, Q306, and Q305 of the restoring circuit 642 in the manner previously described. Circuit 642 then delivers an output from terminating module terminal TL for resetting the counter cores, and an output from terminating module terminal TR for restoring the flip-flops U296, A296T, and A296H. The operator may wish to reset the counter manually in the middle of a counting cycle if he realizes that some sort of error has been made and that therefore the count should be started over again. In this case the counting cycle would be interrupted with some of the counting cores U22, 211T, 222T, 211H, and 222H remaining in an intermediate remanent state. The core-resetting output from terminal TL is designed to prevent this from happening.

ZERO OPERATION

Until now the operation of the counting system has been described on the assumption that none of the digits in the selected count are equal to zero. Now however we shall consider how the system operates when one or more of the digits in the selected count is equal to zero. In the

discussion which follows, and in the accompanying figures, the units, tens, and hundreds digits may be referred to as U, T, and H respectively.

Higher order zero.—This aspect of counter operation will be described in connection with FIGS. 5 through 9. The counting system output for triggering the output amplifier 580 of the terminating module always comes to the terminating module terminal TS from the hundreds module terminal ASH and a lead 570H which is connected to the wiper arm of switch 205H. This switch is ganged with the hundreds module count-selecting switch A200H. Whenever the hundreds digit H exceeds zero, the switch 205H is connected to the appropriate one of its count terminals 1 through 9. As a result, the counting system output is derived from the output lead A56H coming from the hundreds multiplier counter A20H. In this case, the terminating module is not triggered until the counter has gone through its units counting cycle, its tens counting cycle, and its hundreds counting cycle all in turn.

If H equals zero, however, the switch 205H is connected to its zero count terminal so that the counting system output is derived over a lead 730H from a hundreds module input terminal ATH. This terminal is connected to a tens module output terminal AST, and then over a lead 570T to the wiper arm of the switch 205T. If the tens digit T exceeds zero, then, as previously explained in connection with switch 205H of the hundreds adder module, switch 205T of the tens adder module will select the appropriate one of the one through nine count terminals. As a result, the counting system output will be derived over a lead A56T coming from the tens adjustable multiplier counter A20T. In this case, the terminating module will be triggered after the counting system has gone through only its units counting cycle and its tens counting cycle. The hundreds digit being zero, the hundreds counting cycle is eliminated from the effective operating chain by the fact that the switches 205H and 205T derive the counting system output directly from the tens module.

If T also equals zero, i.e., if there is more than one zero in the higher orders of the count, then the process of connecting back to derive the counting system output from a preceding module is repeated once again. In this case switch 205T selects its zero count terminal and thus derives the counting system output over a lead 730T from the tens module input terminal ATT. This terminal is connected to the units module output terminal US to derive the counting system output from the lead U56 coming from the units adjustable counter U20. In this case, the terminating module is triggered as soon as the counter has gone through its unit counting cycle. Since both T and H equal zero, the tens and hundreds modules do not take any part in the operation of the system during this counting cycle.

Lower order zero.—This aspect of counter operation will be described in connection with FIGS. 5 through 8 and 10. The problem of one or more zeros in the lower orders of the selected count is handled by routing the flip-flop restoring output from terminating module TR in such a manner that the three flip-flops U296, A296T, and A296H are restored in a particular pattern of set and reset so as to eliminate from the counting chain those modules of the lower orders which have a zero count. The manner in which the units flip-flop 296 is set and the tens flip-flop A296T and the hundreds flip-flop A296H are both reset by the flip-flop restoring pulse when all the digits exceed zero, has already been described. When U equals zero, the flip-flop restoring output from terminating module terminal TR to units module terminal UR and lead 710 is still applied to set input lead 556 to set the units flip-flop U296. This means that the units counter U20 will begin to count at the start of the next counting cycle even though U equals zero. However, counter U20 will be effectively removed from the counting chain by virtue of the fact that one of the higher

order counters will also be activated at the start of this same counting cycle, without waiting, as it normally does, to start its count after the units counter U20 has finished counting.

The activation of one of the higher order counters simultaneously with the units counter U20 is achieved by selecting an appropriate set-reset pattern in restoring the higher order flip-flops A296T and A296H. The switch U203 is ganged with the units module count selector switch U200. When U exceeds zero the switch U203 is connected to the appropriate one of its count terminals 1 through 9. As a result, the flip-flop restoring pulse from lead 710 and diode CR108 is routed out over lead 712 in the manner previously described to reset the tens flip-flop A296T and the hundreds flip-flop A296H. But when U equals zero the switch U203 connects to its zero count terminal so that the flip-flop restoring pulse from diode CR108 is routed out over a lead 740 to the units module terminal UX. From there the pulse goes to a tens module input terminal AQT and then over lead 601T to the switch A203T. This switch is ganged with the adder module count selector switch A200 so that when T exceeds zero the switch A203T selects the appropriate one of its one through nine count terminals and thus causes the flip-flop restoring pulse to be routed out over a lead 603T to the set input lead A556T of the tens flip-flop A296T. As a result, the tens flip-flop A296T is set at the start of the counting cycle along with the units flip-flop U296. Accordingly the tens counting part of the counting cycle begins at the very start of the cycle, thus effectively eliminating the units counter from the counting chain when U equals zero. However, when T exceeds zero the hundreds counting module must wait its normal turn and not begin counting until after the tens counting cycle has been completed. For this reason, the flip-flop restoring pulse on lead 603T is also applied over a lead 605T to a tens module output terminal APT. From there it goes to a hundreds module input terminal AUH and is applied to the reset input lead 559H to reset the hundreds flip-flop A296H. With this flip-flop in the reset condition, the hundreds module waits in the normal manner until the tens count has been finished and the hundreds count can be started by setting the hundreds flip-flop A296H in the manner previously described.

If U and T are both zero, then the switch A203T will connect to its zero count terminal. As a result, the flip-flop restoring pulse on lead 601T is routed out over a lead A740T to a tens module output terminal AXT. From there the flip-flop restoring pulse goes to a hundreds module input terminal APH and then over a lead 605H to the set input lead A556H of the hundreds flip-flop A296H. This sets the hundreds flip-flop so that the hundreds module begins counting immediately at the start of the counting cycle as is required when both U and T are equal to zero. When the counting system is operating in this mode there is no flip-flop restoring pulse going from the T equals zero terminal of switch A203T to the tens flip-flop A296T. This is because it does not make any difference what the condition of the tens flip-flop may be. As long as the hundreds flip-flop A296H is set and the hundreds module begins counting right from the start of the counting cycle, both the units module and the tens module are effectively cut out of the counting chain regardless of the condition of their flip-flops U296 and A296T.

Because of the fact that the three flip-flops U296, A296T, and A296H are restored to the proper condition for the next counting cycle by means of the restoring pulse generated at the end of the previous cycle, one important precaution must be observed. If the counting system is set for a given count, upon completing that count it will be restored to the correct condition for counting to that same number again on the next cycle. If, before the start of the next cycle, the operator decides to select a different count, he must first manipulate the count selector switches

U200, A200T, and A200H to select the units, tens, and hundreds digits respectively of the new count. Then he must operate the manual reset switch 582 to initiate the flip-flop restoring operation previously described so that the three flip-flops will be re-organized into the set-reset pattern which is appropriate for the newly selected count, and not remain in the pattern appropriate for the counting modulus employed in the last counting cycle.

As a final word regarding zero operation, it will be observed that the switch U200 of the units module includes a jumper lead 750 between its zero and one count terminals, and the switch U202 also has a jumper lead 752 which is similarly connected. Similar jumper leads A750 and A752 may be observed in the switches A200 and A202 of the adder modules. The purpose of these jumper leads is simply to make sure that the sensing and governing transistors UQ111 and Q211 are provided with base bias to prevent them from running away even though the associated counting circuitry is set for a zero count. The simplest way to do this is simply to connect the zero count terminals of the selector switches to the one count terminals of these switches so that the adjustable power supply circuits U168 and A168 are in the same condition for a zero count as they are for a one count. Specifically, the base of UQ111 is connectable from the zero count terminal of switch U200 over the jumper lead 750 to the one count terminal of switch U200 and then over lead 384 to the voltage divider UR124, UR125. At the same time the aforesaid voltage divider is connected from the one count terminal of switch U202 over the jumper lead 752 to the zero count terminal of switch U202 so that it is connected to the source of positive potential provided by lead U150. The connections for the adder module adjustable power supply circuits A168 are identical to those just described for the units module. It will be appreciated that putting any one of the counters in the one count condition even though zero count operation is intended, does not make any difference since zero count operation is actually achieved by cutting that particular counter out of the counting chain when its modulus is to be zero.

TENS RANGE SYSTEM

A tens range counting system (one to ninety-nine) may be made from a single adder module in conjunction with a units module, a terminating module, and a power supply module. The interconnections between these modules, and the operating features of such a system, are summarized in FIG. 11 in the same way that the interconnections and operating features of a hundreds range counting system are shown in FIG. 8. The single adder module of this system is connected to the units module in the same manner that the tens adder module is connected to the units module in the higher range counting system of FIG. 8. On the other hand, the adder module of FIG. 11 is connected to the terminating module in the same manner that the hundreds adder module is connected to the terminating module in the higher range counting system of FIG. 8. Except for the shorter counting range achieved, the operation of this system is identical in all respect with the operation of the hundreds range system previously described.

Along with all the other noted advantages of the counting systems of this invention, the arrangements shown permit the customer to buy only as many adder modules as is necessary to suit his particular counting range requirements. If a customer first buys a single adder module, tens range counting system, and later on finds that he requires a hundreds range counting system, it is only necessary to purchase an additional adder module identical with the first one.

What has been described is a preferred embodiment and is presently believed to be the best mode of practicing the invention, but it will be clear to those skilled in this art that many modifications may be made without

departing from the principles of the invention. Accordingly this description is intended merely as an illustrative example, the broader scope of the invention being stated in the appended claims.

The invention claimed is:

1. A counter comprising:
 - a counting stage having an input circuit, said counting stage requiring a given volt-second energy content input to said input circuit to switch from one state to the opposite state; and
 - a voltage source connected in series with a pulse source in said input circuit, the voltage of said voltage source being selectively adjustable within the range wherein the volt-second energy content of individual pulses supplied to said input circuit is less than said given volt-second energy content, whereby the modulus of said stage can be changed by adjustment of said voltage source.
2. A counter as defined in claim 1, wherein said counter includes a saturable reactor core, and wherein said input circuit is a winding on said core.
3. A counter as defined in claim 1, further comprising means for restoring said counting stage to said one state.
4. A counter as defined in claim 2, further comprising means for restoring said core to said one state.
5. A counter as defined in claim 1, wherein said voltage source is connected to aid said pulse source to increase the net voltage supplied to said input circuit.
6. A counter as defined in claim 1, wherein said voltage source is connected to oppose said pulse source to decrease the net voltage applied to said input circuit.
7. A counter comprising:
 - a counting stage including an input circuit for receiving pulses from a source, the modulus of said counting stage being a function of the voltage-second content of inputs to said circuit;
 - and an auxiliary source of EMF connected to be in series with said input circuit and said pulse source to alter the net voltage applied to said input circuit during said pulses whereby the volt-second content of the inputs to said circuit is altered to change the modulus of said counting stage;
 - said counter including an electronic switch connected to substantially prevent the application of said auxiliary EMF to said counting stage input circuit between pulses from said source, said electronic switch being responsive to pulses from said source to permit application to said input circuit during said pulses, of the algebraic sum of the voltages of said pulse source and said auxiliary source.
8. An adjustable counter comprising:
 - a pulse source including an output circuit;
 - a counting stage including an input circuit, the modulus of said counting stage being a function of the volt-second content of inputs to said circuit;
 - an electronic switch including a controlled circuit and a controlling circuit;
 - and adjustable auxiliary source of EMF;
 - said pulse source, said electronic switch controlled circuit, said counting stage input circuit, and said auxiliary source all being connected in a series circuit for said auxiliary source and said pulse source to apply substantially the resultant of their respective voltages to the remainder of said series circuit to selectively alter the net voltage applied to said counting stage input circuit so that the volt-second contents of inputs to said circuit is altered to change the modulus of said counting stage;
 - said electronic switch controlling circuit being connected to said pulse source;
 - said electronic switch controlling circuit being at a potential between outputs from said pulse source whereby to cause said electronic switch to block the application of the voltage of said auxiliary source to said counting stage input circuit;

- said electronic switch controlling circuit being biased by outputs from said pulse source to cause said electronic switch to permit substantially the net voltage of said pulse source and said auxiliary source to be applied to said counting stage input circuit.
9. An adjustable counting system including a lower order zero circuit, comprising:
 - a plurality of counting sections normally operating in successive additive relation for counting the respective orders of a selected multi-digit number;
 - means for selecting a desired individual count for a lower order counting section, said means having a zero selection condition and at least one non-zero selection condition;
 - respective enabling means including respective bistable devices settable for activating said counting sections;
 - means for restoring said bistable devices to respective conditions appropriate for the start of the next counting cycle, said restoring means including:
 - means connected to set the appropriate one of said bistable devices to activate said lower order counting section;
 - means responsive to the selection of a non-zero count for said lower order section to cause said restoring means to reset the appropriate ones of said bistable devices to inactivate all higher order counting sections whereby to postpone operation thereof until after operation of said lower order section to maintain said additive relation relative thereto;
 - and means responsive to the selection of a zero count for said lower order section to cause said restoring means to set the appropriate one of said bistable devices to activate the next higher order counting section above said lower order section at the start of said next counting cycle whereby to remove the lower order count from the sum attained by said counting system.
10. An adjustable counting system including a lower order zero circuit, comprising:
 - a plurality of counting sections normally operating in successive additive relation for counting the respective orders of a selected multi-digit number, and producing an output upon counting up to said number;
 - means for selecting a desired individual count for a lower order counting section, said means having a zero selection condition and at least one non-zero selection condition;
 - respective enabling means including respective bistable devices settable for activating said counting sections;
 - restoring means responsive to said output to restore said bistable devices to respective conditions appropriate for the start of the next counting cycle, said restoring means including:
 - means connected to set the appropriate one of said bistable devices to activate said lower order counting section;
 - means responsive to the selection of a non-zero count for said lower order section to cause said restoring means to reset the appropriate ones of said bistable devices to inactivate all higher order counting sections whereby to postpone operation thereof until after operation of said lower order section to maintain said additive relation relative thereto;
 - and means responsive to the selection of a zero count for said lower order section to cause said restoring means to set the appropriate one of said bistable devices to activate the next higher order counting section above said lower order section at the start of said next counting cycle whereby to remove the lower order count from the sum attained by said counting system.
11. An adjustable counting system including a lower order zero circuit, comprising:

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a plurality of counting sections normally operating in successive additive relation for counting the respective orders of a selected multi-digit number, and producing an output upon counting up to said number;

means for selecting a desired individual count for a lower order counting section, said means having a zero selection condition and at least one non-zero selection condition;

respective enabling means including respective bistable devices settable for activating said counting sections; restoring means responsive to said output to restore said bistable devices to respective conditions appropriate for the start of the next counting cycle, said restoring means including:

means connected to set the appropriate one of said bistable devices to activate said lower order counting section;

means responsive to the selection of a non-zero count for said lower order section to cause said restoring means to reset the appropriate ones of said bistable devices to inactivate all higher order counting sections whereby to postpone operation thereof until after operation of said lower order section to maintain said additive relation relative thereto;

and means responsive to the selection of a zero count for said lower order section to cause said restoring means to set the appropriate one of said bistable devices to activate the next higher order counting section above said lower order section at the start of said next counting cycle whereby to remove the lower order count from the sum attained by said counting system;

said last-named means being further responsive to the selection of a zero count for said lower order section to cause said restoring means to reset the appropriate ones of said bistable devices to inactivate any higher order counting sections above the said next higher order section whereby to postpone operation thereof until after operation of said next higher order section to maintain said additive relation relative thereto.

12. The invention of claim 11, further comprising manually operable means for triggering said restoring means at any desired time.

13. An adjustable counting system including a higher order zero circuit, comprising:

a plurality of sections for counting respective orders of a multi-digit number, said sections producing respective outputs when reaching their respective counts;

said sections having respective output means;

said sections of an order above the lowest order in said system having respective input means and respective switching means and being selectively adjustable to choose their respective counts;

the said input means of said sections each being connected to receive signals from the said output means of the next lower order section;

said switching means of each counting section being operable in response to selection of a non-zero count for such section to transmit the said count output of such section to the said output means of such section whereby the count output of the highest order non-zero-selecting counting section is made available at the said input means of the next higher order counting section;

said switching means of each section being operable in response to selection of a count of zero for such section so that any signal applied to the said input means of such section is transmitted to the said output means of said section whereby said highest order non-zero-selecting counting section output is

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routed through all of said higher order zero-selecting counting sections to the said output means of the highest order counting section in said system.

14. An adjustable counting system comprising:

a plurality of sections for counting respective orders of a multi-digit number;

at least one of said sections being adjustable to choose the count thereof;

said adjustable section including a counting stage having an input circuit for receiving pulses from a source, the modulus of said counting stage being a function of the volt-second content of inputs to said circuit;

said adjustable section further including means for connecting a selectively adjustable auxiliary voltage in series with said input circuit and said pulse source to alter the net voltage applied to said input circuit during said pulses whereby the volt-second content of the inputs to said circuit is altered to permit adjustment of the modulus of said counting stage;

and means for enabling said counting sections at different times, including means for gating the application of said auxiliary voltage to said input circuit whereby to activate said counting stage.

15. For use in a modular counting system, an adder module capable of functioning at any one of a plurality of order positions in said system, comprising:

a fixed counter;

means for connecting said fixed counter to receive inputs from circuitry preceding said adder module;

means connecting said fixed counter to supply outputs to circuitry following said adder module;

an adjustable counter cascaded with said fixed counter;

means for supplying outputs from said adjustable counter to circuitry following said adder module;

bistable means for activating said fixed and adjustable counters when in a first stable condition;

means for connecting said bistable means to receive an input from circuitry preceding said adder module for switching said bistable means to said first stable condition to activate said adder module to perform a count;

said adjustable counter being connected to apply count outputs therefrom to switch said bistable means to a second stable condition to de-activate said adder module and to activate circuitry following said adder module at the end of the count performed by said adder module;

output means for supplying a partial activation signal to circuitry preceding said adder module when said bistable means is in said first stable condition;

and input means for receiving a partial activation signal from circuitry following said adder module and applying said signal to activate said fixed counter.

16. An adder module as in claim 15 wherein:

said adjustable counter output means includes a circuit receiving said adjustable counter output, an adder module output terminal, and higher order zero switching means connecting said circuit to apply said output to said terminal in response to selection of a count greater than zero for said adjustable counter;

and said adder module comprises an input terminal; said higher order zero switching means connecting said input terminal to said output terminal in response to selection of a count of zero for said adjustable counter.

17. An adder module as in claim 15 further comprising:

a lead connected for switching said bistable means to said first stable condition;

an input-output terminal connected to said switching lead;

a pair of input terminals each connected to switch said bistable means to said second stable condition;

lower order zero switching means including a movable contact;
 an input terminal connected to said movable contact;
 said switching means operating in response to selection of a count greater than zero for said adjustable counter to connect said movable contact to said switching lead and said input-output terminal;
 and an output terminal;
 said switching means operating in response to selection of a count of zero for said adjustable counter to

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connect said movable contact to said output terminal.

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