(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
2 May 2008 (02.05.2008)

PCT

(10) International Publication Number
WO 2008/050171 A1

(51) International Patent Classification:
H03G 7/08 (2006.01) *H03M 1/18* (2006.01)

(21) International Application Number:
PCT/IB2006/002988

(22) International Filing Date: 25 October 2006 (25.10.2006)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **SENSITIVE OBJECT** [FR/FR]; 8 rue Danjou, 92100 Boulogne-Billancourt (FR).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **BENHAMOUDA, Franck** [FR/FR]; 26 quater Rue Pierre Curie, F-78370 Plaisir (FR). **ING, Ros, Kiri** [FR/FR]; 11 rue de Chaligny, F-75012 Paris (FR). **LINOTTE, Jean-Michel** [FR/FR]; 1-3 rue du Tage, F-75013 Paris (FR).

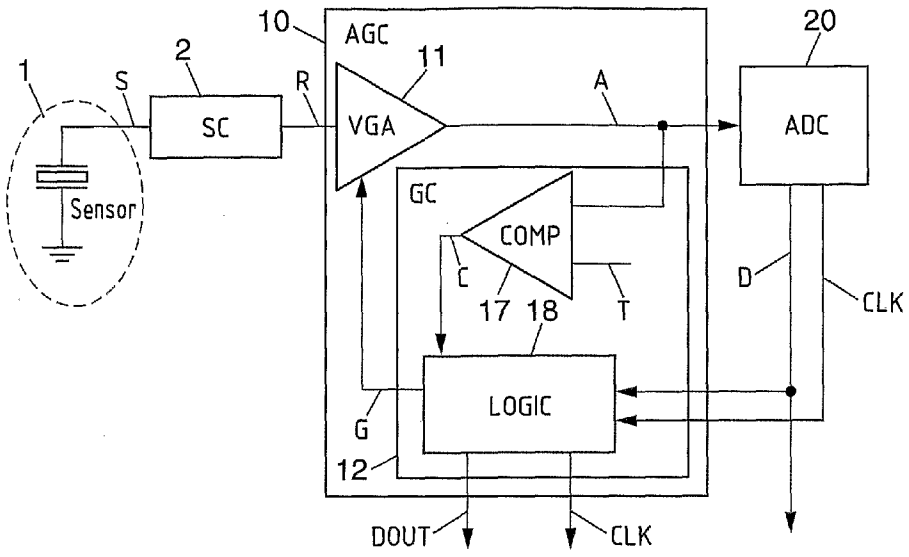
(74) Agents: **BURBAUD, Eric** et al.; Cabinet Plasseraud, 52, rue de la Victoire, Cedex 9, F-75440 Paris (FR).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(54) **Title:** AUTOMATIC GAIN CONTROL CIRCUIT, SYSTEM INCLUDING SUCH CIRCUIT AND METHOD FOR ATUOMATIC GAIN CONTROL



(57) **Abstract:** An automatic gain control circuit including a variable gain amplifier (11) adapted to receive a received signal (R) and to output an amplified signal (A) to an analog to digital converter (20), and a gain controller (12) which is connected to said variable gain amplifier (11) for receiving said amplified signal (A) and for controlling a gain of said variable gain amplifier (11). The gain controller (12) is adapted to determine an occurrence of a threshold event each time the amplified signal (A) has reached a predetermined threshold, decrease the gain of the variable gain amplifier (11) at each occurrence of a threshold event, measure a delay since the last threshold event, increase the gain of the variable gain amplifier (11) if the delay is greater than a delay specified value and if the gain of the variable gain amplifier (11) is not maximum.

WO 2008/050171 A1

Automatic gain control circuit, system including such circuit and method for automatic gain control.

FIELD OF THE INVENTION

The present invention concerns an automatic gain control (AGC) circuit, a system including such circuit and a method for automatic gain control.

BACKGROUND OF THE INVENTION

The present invention concerns more precisely an automatic gain control (AGC) circuit including:

- a variable gain amplifier (VGA) adapted to receive a received signal and to output an amplified signal to an analog to digital converter (ADC),
- and a gain controller (GC) which is connected to said variable gain amplifier for receiving said amplified signal and for controlling a gain of said variable gain amplifier.

When the received signal is coming for instance from a vibration sensor, the received signal can be an impulsive signal with variations in amplitude of several orders of magnitude.

Generally, low input gain and high resolution analog to digital converters (ADC) are used to convert such received signal. But when the received signal is an impulsive signal, it is necessary to tune an important margin between the ADC full scale input voltage range and the received signal maximum voltage. That is why most of time, the amplified signal has a very small amplitude and is noisy. Moreover, the use of high resolution ADC is costly.

Another way is to use an automatic gain control (AGC) circuit in front of the ADC. An AGC refers to a circuit which gain varies substantially depending on the magnitude of the received signal so as to maintain the amplified signal level substantially constant. As described

is US-5 606 284, the AGC circuit comprises at least one analog amplifier for the received signal which is automatically controlled by an analog feedback signal. Unfortunately amplified signal must be integrated in the feedback loop to produce the VGA gain control voltage. Thus, time constant must be sufficiently large and such AGC circuit is not well adapted to impulsive signals with lots of variations in amplitudes.

OBJECTS AND SUMMARY OF THE INVENTION

An object of the present invention is to solve this problem by providing an efficient circuit for automatic gain control that does not require an integrator circuit.

To this effect, the gain controller is adapted to:

- determine an occurrence of a threshold event each time the amplified signal has reached a predetermined threshold,
- decrease the gain of the variable gain amplifier at each occurrence of a threshold event,
- measure a delay since the last threshold event,
- increase the gain of the variable gain amplifier if the delay is greater than a delay specified value and if the gain of the variable gain amplifier is not maximum.

Thanks to this regulation of the gain of the VGA, it is possible to anticipate received signal amplitude change even during first impulses and it is possible to get a constant signal-to-noise ration (SNR) in spite of change of received signal magnitude. Moreover, the cost of the VGA and the gain controller is relatively low and supposed lower than a high resolution ADC which has a variable quantization noise.

In preferred embodiments of the automatic gain control circuit proposed by the invention, one and/or the other of the following features may optionally be incorporated:

- the gain controller is adapted to command the

change of gain of the variable gain amplifier between two samples of the analog to digital converter conversion;

- the gain controller is adapted to send via a serial bus a first digital value given by the analog to digital converter and a second digital value representing the gain of the variable gain amplifier;

- at each occurrence of a threshold event and if the gain of the variable gain amplifier is not minimum, the gain controller decreases the gain of the variable gain amplifier by a factor multiple of two;

- at each occurrence of a threshold event and if the gain of the variable gain amplifier is not minimum, the gain controller decreases the gain of the variable gain amplifier by a predetermined value depending on the absolute difference between two successive first digital value;

- if the delay is greater than a delay specified value and if the gain of the variable gain amplifier is not maximum, the gain controller increases the gain of the variable gain amplifier by a factor multiple of two;

- the gain controller is a programmable logic device;

- the automatic gain control circuit is an application specific integrated circuit;

- the gain controller is able to manage two channels, with two analog to digital converters and two variable gain amplifiers, each of then in one or two circuits;

- variable gain amplifier is further composed of an inverting amplifier with a digital potentiometer.

Another object of the invention is a system including an automatic gain control circuit, further including an analog to digital converter connected to said automatic gain control circuit for receiving said amplified signal from said variable gain amplifier.

The system may further include a vibration sensor

connected to said variable gain amplifier, wherein said received signal is received by said variable gain amplifier from said vibration sensor.

Another object of the invention is to provide an efficient method for automatic gain control of a variable gain amplifier amplifying a received signal and outputting an amplified signal comprising the steps of:

- determining an occurrence of a threshold event each time the amplified signal has reached a predetermined threshold,
- decreasing the gain of the variable gain amplifier at each occurrence of a threshold event,
- measuring a delay since the last threshold event,
- increasing the gain of the variable gain amplifier if the delay is greater than a delay specified value and if the gain of the variable gain amplifier is not maximum.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the invention will be apparent from the following detailed description of one of its embodiments given by way of non-limitating example, with reference to the accompanying drawings. In the drawings:

- Figure 1 is a block diagram of an automatic gain control (AGC) circuit according to the invention;
- Figure 2 is a block diagram of a variable gain amplifier (VGA);
- Figure 3 represents a receiving signal;
- Figure 4 represents the amplified signal of the received signal of figure 3.

MORE DETAILED DESCRIPTION

In figure 1, a sensor 1 is producing a sensor signal S, for example representing vibrations of an object. In that case, the sensor could be a piezoelectric element. This sensor signal S is imputed in a signal conditioning

(SC) circuit 2 which can be composed at least of a filter to reduce high frequency noise of sensor signal S and is outputting a received signal R. The automatic gain control (AGC) circuit 10 receives said received signal R to produce an amplified signal A, which is converted into digital data D by an analog to digital converter (ADC) 20.

For example, the ADC 20 may be a Texas Instruments PCM1803 which is a high-performance, low-cost, single-chip stereo analog to digital converter. In that case, the ADC 20 is able to give to the AGC circuit 10 a clock signal CLK for synchronization of serial audio digital data D and a left-right signal LRCLK for defining if current converted data D is from the left or right input channel. These additional signals are useful for the AGC circuit 10 to synchronize with ADC and to identify each sample.

The automatic gain control (AGC) circuit 10 is at least composed of a variable gain amplifier (VGA) 11 and a gain controller (GC) 12.

The VGA may be developed as exposed in figure 2. It is an inverting amplifier 13, eventually with signal centered on Vcc/2, which is half of amplifier supply voltage Vcc. This amplification stage uses three resistors: an input resistor 14 (of resistance Ra), a first feedback resistor 15 (of resistance r) and a second feedback resistor 16 (of resistance Rb). First and second feedback resistors 15, 16 are connected in series. Then, the gain of inverting amplifier 13 is given by the following formula:

$$\text{Gain} = -\frac{Rb + r}{Ra} \qquad (1)$$

This kind of simple inverting amplifier permits to get a large range of gain by tuning its resistors values.

Second feedback resistor 16 is a programmable variable resistor, also called a digital potentiometer. An example of that kind of resistor is the Analog Devices AD5162 which is a dual 256-position Serial Peripheral Interface (SPI) digital potentiometer. The SPI bus is a 4-wire synchronous serial communications interface used by

many microprocessor peripheral chips for connecting at a relatively low speed. This SPI bus can be used in the AGC to communicate a digital gain value G from the Gain Controller (GC) 12 to the Variable Gain Amplifier (VGA) 11.

In the case of a 8-bit digital potentiometer, like the AD5162, the digital gain value G can take any integer value between zero and 255. The resistance value Rb of the second feedback resistor 16 is given by a simple linear formula:

$$Rb = \frac{G}{256}.Re + Rw \qquad (2)$$

Where Re is the end to end resistance value (maximum resistance value) and Rw is the wiper contact resistance (the minimum resistance value).

The first feedback resistor 15 of the inverting amplifier 13 can help to compensate the wiper resistance Rw effect. Thus, it may be possible to have real evolutions of the gain of inverting amplifier 13 by factors of two, for instance:

The gain controller (GC) is detailed in figure 1 and is itself composed of a signal comparator 17 and a logic circuit 18.

The signal comparator 17 is comparing the amplified signal A to a threshold T, and outputting the binary comparison signal C.

In the general case with a non centered amplified signal A, the comparator 17 is comparing the amplified signal A to thresholds T1 and T2. If amplified signal A is greater than threshold T1 or lower than threshold T2 the comparison signal C will be in the true state represented by a Vcc voltage of comparison signal C, otherwise the comparison signal C will be in the false state represented by a zero or ground voltage.

In practice, only one threshold T is used to define the comparison signal C. In case of a centered signal around zero volts, the comparison signal C is determined as in the general case above with T1 equal to T and T2 equal

to -T. In case of a centered signal around Vcc/2 volts, the comparison signal C is determined as in the general case above with T1 equal to Vcc/2+T and T2 equal to Vcc/2-T.

Figures 1, 3 and 4 are representing a block diagram and signals with centered signal around zero volt, and related description is based on a centered signal around zero volt.

The logic circuit 18 is using the comparison signal C and the ADC digital data D and ADC clock signal CLK to provide the said digital gain value G for the VGA 11 and to provide a completed digital data DOUT and a clock signal CLK to a user circuit (not shown) such as a microcontroller or a microprocessor or a digital signal processor (DSP).

The logic circuit 18 can be made by using several logic gate circuits connected together, or by using a Programmable Logic Device (PLD) such as a PAL device (Programmable Logic Array) or a GAL device (Generic Array Logic) or a CPLD device (Complex Programmable Logic Device) or a FPGA device (Field-Programmable Gate Array), or by using an Application Specific Integrated Circuit (ASIC), or any device of the like to implement all the bellow described logic. These PLD are programmed by using a language called Hardware Description Language (HDL). The ASIC can eventually integrate all or any of all the functions of the AGC circuit 10, e.g. including the signal SC circuit 2, the VGA circuit 11, the GC circuit 12 and the ADC circuit 20. Then, for high production volumes, ASIC design may be more cost effective than PLD design.

At initialisation, the logic circuit 18 is setting the gain value G of the VGA at the maximum value (e.g. 255, in case of a 8-bit digital potentiometer).

Then, the logic circuit 18 is determining an occurrence of a threshold event each time the amplified signal A has reached the predetermined threshold T, that is to say, each time the comparison signal C is equal to true state.

For each threshold event, the logic circuit 18 decreases the gain of the VGA by decreasing its output gain value G (e.g. the gain is decreased by a factor of two in changing the digital gain value G).

The logic circuit 18 also measures the delay since last threshold event. This can be done by simply counting samples since last true state of comparison signal C. In case of the use of PCM1803 stereo ADC, the logic circuit 18 only need to count the rising edges of left-right signal LRCLK.

If the gain of the VGA is not maximum (e.g. 255) and if the measured delay is greater than a specified value ΔT, the logic circuit 18 increases the gain of the VGA by increasing the digital gain value G (e.g. the gain is increased by a factor of two in changing the digital gain value G).

If a new threshold event happens before the measured delay becomes greater than said specified value ΔT, the logic circuit 18 decreases the gain of the VGA by decreasing its output gain value G and the delay is simply initialized to zero value. Then, the gain of the VGA can be increased a first time after a delay of ΔT if no threshold event occurs and a second time after a delay of $2.\Delta T$ if no threshold event occurs. Another way to do this is to initialize the delay to a zero value when the gain of the VGA is firstly increased. In that case, if the gain of the VGA can be increased a second time after a delay of ΔT if no threshold event occurs (since last initialization of delay).

The logic circuit 18 is providing to a user circuit a completed digital data DOUT which is merging the digital data D from ADC and the digital gain value G of VGA, so that the user microprocessor circuit can calculate the real value of received signal R. In case of two channels (with two ADCs or a two channel ADC), the logic circuit 18 is also managing all these devices and providing a completed

digital data DOUT merging the digital data D of left channel, gain value G of VGA of left channel, digital data D of right channel, gain value G of VGA of right channel, and providing a LRCLK signal for defining if current data in DOUT is from the left or right input channel.

In a second embodiment of the invention, the gain of the VGA 11 may be increased or decreased by a predetermined factor value, which could be for instance two or four or a multiple of two.

In a third embodiment of the invention, the logic circuit 18 is calculating the absolute difference DIFF between two successive digital data D from ADC 20, at each occurrence of a threshold event:

$$DIFF = abs(D(n) - D(n-1)) \quad (3)$$

Where:

. T is a sampling period of the ADC,

. n is referring to sampling instant nT,

. n-1 is referring to the previous sampling instant (n-1)T,

. D(n) is the digital data D from ADC 20 at instant nT,

. D(n-1) is the digital data D from ADC 20 at instant (n-1)T.

If the absolute difference DIFF is lower than a predetermined value the gain is decreased by a first factor, for example of two, else the gain is decreased by a second factor higher than said first factor, for example of four.

Thanks to this third embodiment of the invention, the gain of the VGA 11 is automatically decreased by a predetermined factor value and the gain of the VGA 11 is simply and well adapted to amplified signal A evolution.

Figure 3 represents the typical amplified signal A from the vibration sensor 1 without the automatic gain amplifier of the invention, looking like an impulse response of a vibration structure with a first high impulse

and following smaller and smaller oscillation amplitudes. Speed of decreasing of the oscillation amplitude depends at least on damping characteristics of the vibration structure. As it can be seen on figure 3, it can be difficult to keep this amplified signal A bellow threshold T, and after two or three oscillations amplified signal A becomes very small. That type of signal leads to saturation problems and then to poor signal-to-noise ratio.

For example, between A1 and A2 and between A3 and A4, the amplified signal A exceeds threshold level T, with a high risk of saturation and non linearity of amplifier.

Figure 4 represents the same amplified signal A with the automatic gain amplifier of the invention. When the signal reach threshold level T at A1, then the gain controller 12 decrease the VGA 11 gain and the signal is falling down, staying bellow threshold T level. After a predetermined delay ΔT, the amplified signal A is at A5 and the gain controller 12 is increasing back the gain of the VGA 11, producing another step in the signal now following the unmodified signal. This example is demonstrating how the AGC 10 is keeping amplified signal A bellow the threshold T.

The ACG of the invention is continuously adapting variable gain amplifier gain value to keep the signal bellow threshold and with a maximum amplification. That is why the signal-to-noise ration (SNR) of amplified signal is kept as constant and as high as possible. With these devices and method it is possible to get a precise analog-to-digital conversion of received signal, at a lower cost than with a high resolution analog to digital converter.

CLAIMS

1. An automatic gain control circuit including:

- a variable gain amplifier (11) adapted to receive a received signal (R) and to output an amplified signal (A) to an analog to digital converter (20),

- and a gain controller (12) which is connected to said variable gain amplifier (11) for receiving said amplified signal (A) and for controlling a gain of said variable gain amplifier (11),

wherein the gain controller (12) is adapted to:

- determine an occurrence of a threshold event each time the amplified signal (A) has reached a predetermined threshold,

- decrease the gain of the variable gain amplifier (11) at each occurrence of a threshold event,

- measure a delay since the last threshold event,

- increase the gain of the variable gain amplifier (11) if the delay is greater than a delay specified value and if the gain of the variable gain amplifier (11) is not maximum.

2. An automatic gain control circuit according to claim 1, wherein the gain controller (12) is adapted to command the change of gain of the variable gain amplifier (11) between two samples of the analog to digital converter conversion.

3. An automatic gain control circuit according to anyone of claims 1 and 2, wherein the gain controller (12) is adapted to send via a serial bus a first digital value given by the analog to digital converter and a second digital value representing the gain of the variable gain amplifier (11).

4. An automatic gain control circuit according to anyone of claims 1 to 3, wherein at each occurrence of a threshold event and if the gain of the variable gain amplifier (11) is not minimum, the gain controller (12)

decreases the gain of the variable gain amplifier (11) by a factor multiple of two.

5. An automatic gain control circuit according to claim 3, wherein at each occurrence of a threshold event and if the gain of the variable gain amplifier (11) is not minimum, the gain controller (12) decreases the gain of the variable gain amplifier (11) by a predetermined value depending on the absolute difference between two successive first digital value.

6. An automatic gain control circuit according to anyone of claims 1 to 5, wherein if the delay is greater than a delay specified value and if the gain of the variable gain amplifier (11) is not maximum, the gain controller (12) increases the gain of the variable gain amplifier (11) by a factor multiple of two.

7. An automatic gain control circuit according to anyone of claims 1 to 6, wherein the gain controller (12) is a programmable logic device (PLD).

8. An automatic gain control circuit according to anyone of claims 1 to 6, wherein the automatic gain control circuit (10) is an application specific integrated circuit (ASIC).

9. An automatic gain control circuit according to anyone of claims 1 to 8, wherein the gain controller (12) is able to manage two channels, with two analog to digital converters and two variable gain amplifiers (11), each of then in one or two circuits.

10. An automatic gain control circuit according to anyone of claims 1 to 9, wherein the variable gain amplifier (11) is further composed of an inverting amplifier (13) with a digital potentiometer (16).

11. A system including an automatic gain control circuit (10) as claimed in anyone of the preceding claims, further including an analog to digital converter (20) connected to said automatic gain control circuit (10) for receiving said amplified signal (A) from said variable gain

amplifier (11).

12. A system as claimed in claim 11, further including a vibration sensor (1) connected to said variable gain amplifier (11), wherein said receiving signal (R) is received by said variable gain amplifier (11) from said vibration sensor (1).

13. A method for automatic gain control of a variable gain amplifier (11) amplifying a received signal (R) and outputting an amplified signal (A) comprising the steps of:

- determining an occurrence of a threshold event each time the amplified signal (A) has reached a predetermined threshold,
- decreasing the gain of the variable gain amplifier (11) at each occurrence of a threshold event,
- measuring a delay since the last threshold event,
- increasing the gain of the variable gain amplifier (11) if the delay is greater than a delay specified value and if the gain of the variable gain amplifier (11) is not maximum.

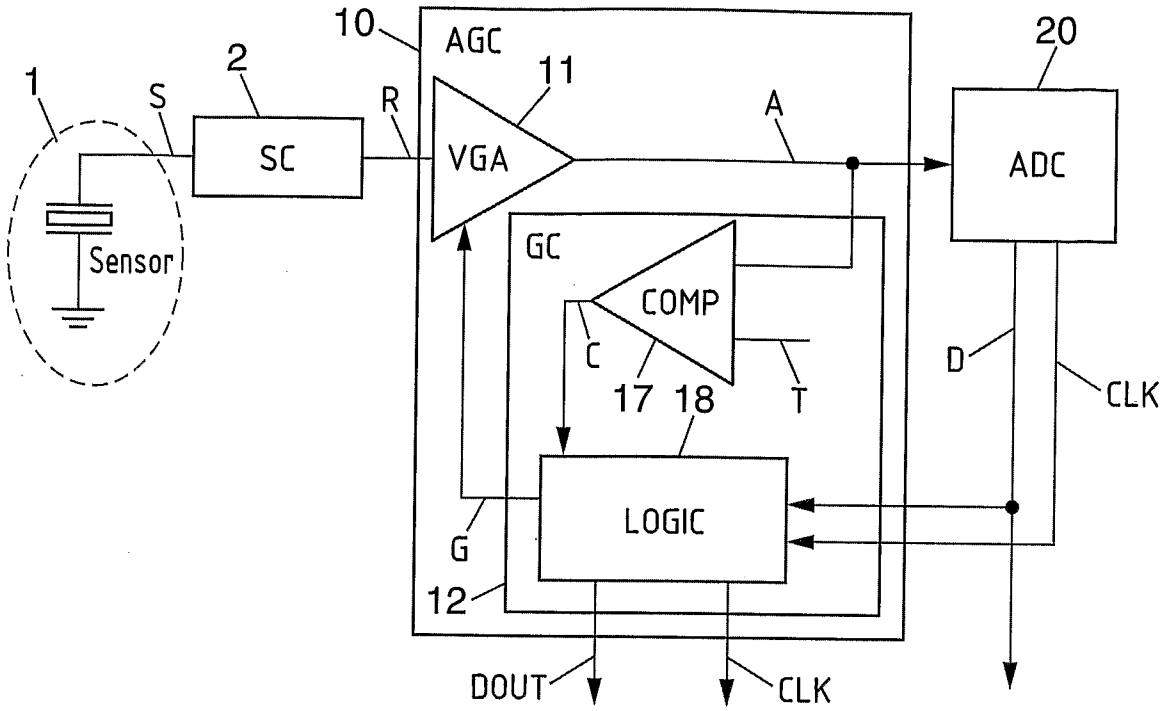

10
AGC
20
1
S
2
R
11
A
SC
VGA
ADC
Sensor
GC
COMP
C
D
CLK
17
18
T
LOGIC
G
12
DOUT
CLK

FIG. 1

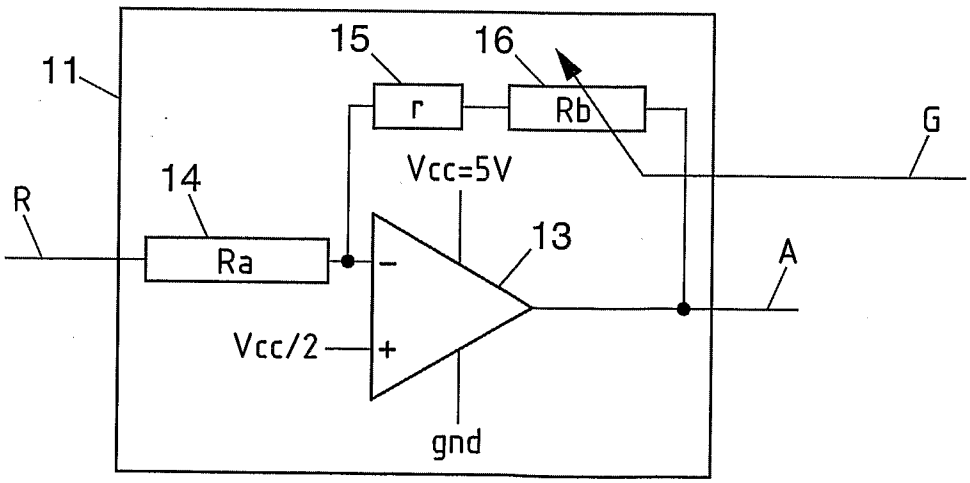

11
15
16
r
Rb
G
Vcc=5V
14
R
13
Ra
A
Vcc/2
gnd

FIG. 2

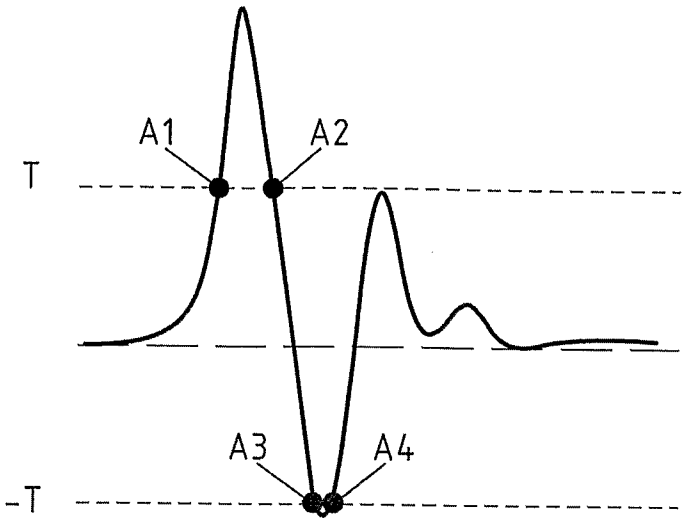


FIG. 3

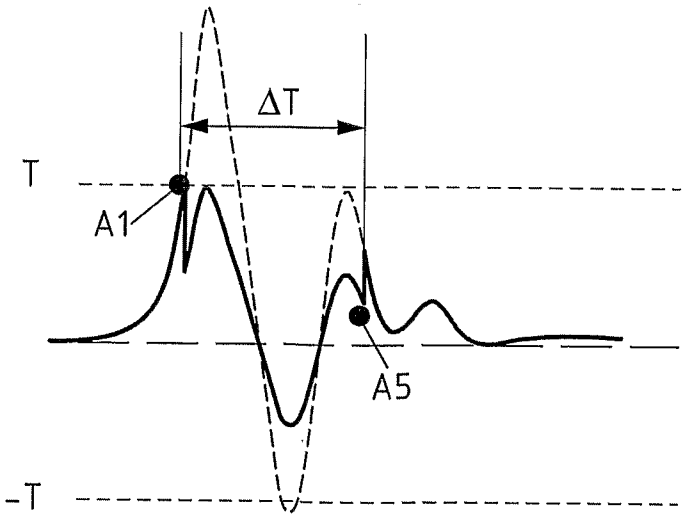


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2006/002988

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03G7/08 H03M1/18

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M H03G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 929 150 A (ERICSSON TELEFON AB L M [SE]) 14 July 1999 (1999-07-14) paragraphs [0031] - [0033]; figures 2b,4	1-13
X	EP 0 604 295 A1 (ALCATEL RADIOTELEPHONE [FR] ALSTHOM CGE ALCATEL [FR]) 29 June 1994 (1994-06-29) column 5, line 48 - column 6, line 58; figures 1,2A,2B	1-13
A	EP 0 803 977 A (SONY CORP [JP]) 29 October 1997 (1997-10-29) the whole document	1-13

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 June 2007	16/07/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	FRITZSCHE, H

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2006/002988

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0929150 A	14-07-1999	NONE	
EP 0604295 A1	29-06-1994	AT 160657 T	15-12-1997
		AU 668243 B2	26-04-1996
		AU 5262793 A	07-07-1994
		DE 69315417 D1	08-01-1998
		DE 69315417 T2	19-03-1998
		ES 2109455 T3	16-01-1998
		FI 935755 A	24-06-1994
		FR 2699768 A1	24-06-1994
		JP 6276171 A	30-09-1994
		NO 934737 A	24-06-1994
EP 0803977 A	29-10-1997	JP 9289426 A	04-11-1997
		US 5929706 A	27-07-1999