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W. J. MORLOCK

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GAIN CONTROL CIRCUITS

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2 Sheets-Sheet 1

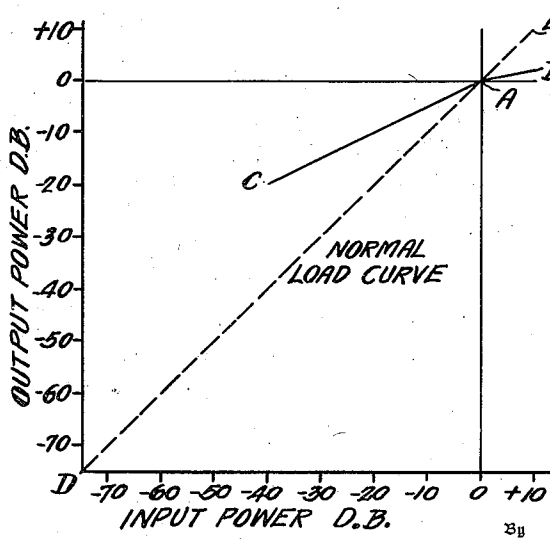
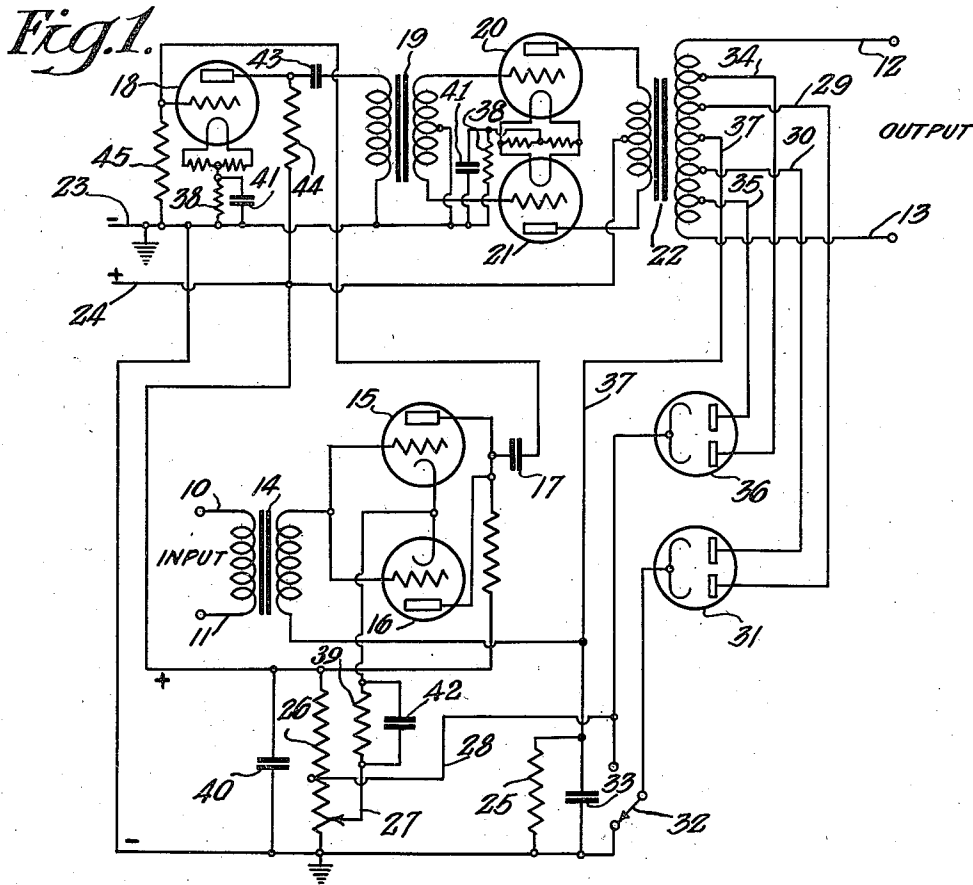


Fig. 2.

Inventor
William J. Morlock
J. S. Saff
 Attorney

June 10, 1941.

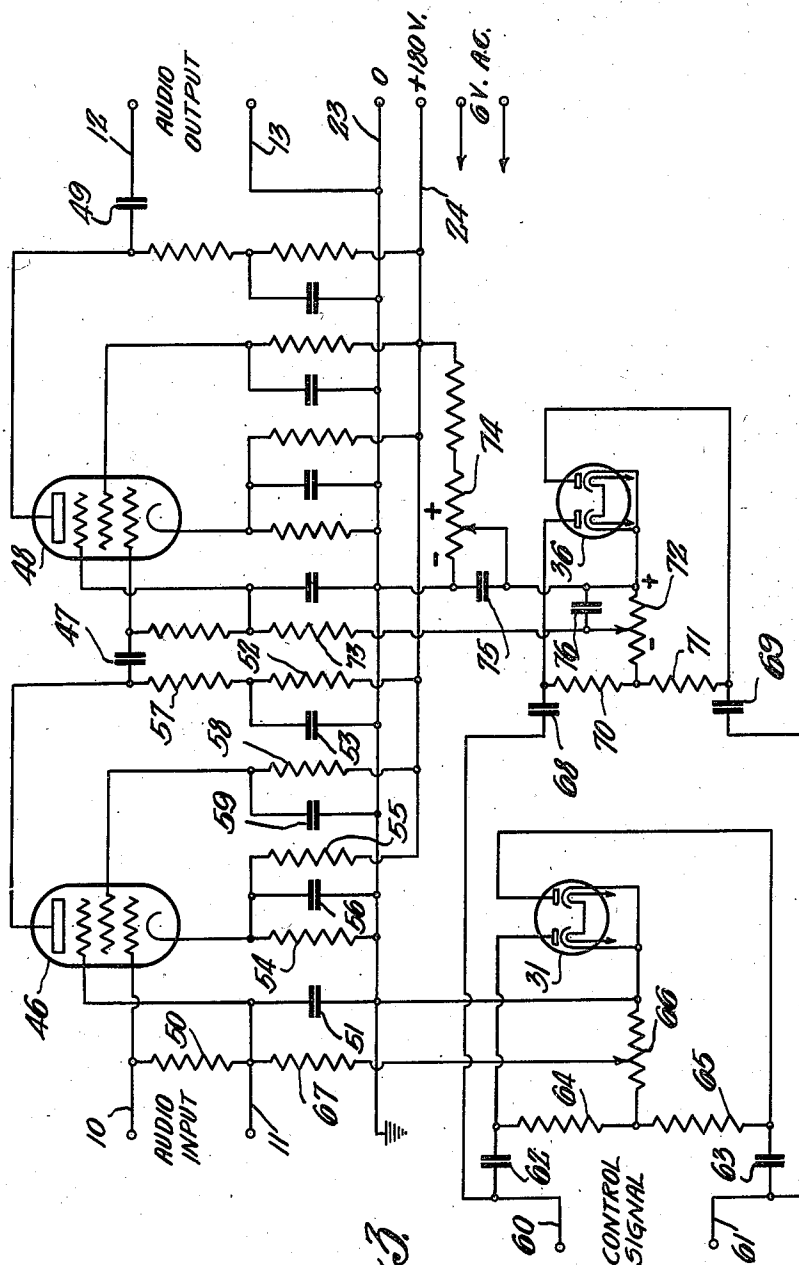
W. J. MORLOCK

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2 Sheets-Sheet 2



Inventor

William J. Morlock

Gruff

Attorney

UNITED STATES PATENT OFFICE

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GAIN CONTROL CIRCUITS

William J. Morlock, Collingswood, N. J., assignor
to Radio Corporation of America, a corporation
of Delaware

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4 Claims. (Cl. 179—171)

This invention relates to gain control circuits such as are applicable to public announcement and other radio or audio frequency amplifying systems, and has for its principal object the provision of an improved circuit and method of operation whereby a higher average acoustical output may be obtained from an amplifier without increased rating and without overload from excessive signal input.

In accordance with the present invention, there are provided a plurality of gain control circuits one of which gradually compresses the output as the signal level increases up to a point near the normal rating of the amplifier and another of which rapidly compresses the output beyond this point. Under these conditions, signals of a very low level are highly amplified, the amplifier gain decreases as the input signal level increases, a higher average acoustic output is realized without increasing the peak rating of the equipment, and the output at high signal level is compressed to an extent which prevents overloading.

The invention will be better understood from the following description considered in connection with the accompanying drawings and its scope is indicated by the appended claims.

Referring to the drawings—

Figure 1 is a wiring diagram of an amplifying system to which the invention is applied.

Figure 2 is an explanatory diagram relating to the operation of the system of Fig. 1, and

Figure 3 is a wiring diagram of a resistance coupled amplifier system involving the invention.

The system of Fig. 1 includes input terminals 10—11 and output terminals 12—13 between which signals are transmitted through an amplifying channel including a coupling transformer 14, a pair of parallel connected tubes 15—16 which are of the exponential characteristic type, a coupling capacitor 17, a single tube stage 18, a coupling transformer 19, a push-pull stage 20—21 and a coupling transformer 22. Power for operating these various stages of the amplifying channel is derived from the direct current supply terminals 23 and 24, the negative side of this power supply line being grounded. It should be understood that the parallel connected tubes 15—16 and the push-pull connected tubes 20—21 may be replaced by a single triode without altering the operation of the system.

The input circuit of the tubes 15—16 includes (1) the secondary winding of the transformer 14 through which the signal is applied, (2) a resistor 25 through which a gradually increasing volume compression potential and an anti-overload bias derived through a lead 28 are applied and (3) a bleeder resistor 26 from a part of which a bias is derived through the lead 28 to a diode 36.

The volume compression bias potential of the resistor 25 is derived from the secondary winding of the transformer 22 through relatively low voltage leads 29—30, a diode 31 and a switch 32 and the lead 37. A capacitor 33 is connected in shunt to the resistor 25 for timing the action of this volume control circuit.

The anti-overload bias of the resistor 25 is derived from the relatively high voltage secondary leads 34—35 through a diode 36, the lead 28, the lower section of the resistor 26 and the lead 37. Since this overload control circuit includes the lower section of the resistor 26, it is subjected to a bias potential which allows current to flow through the diode 36 only when the signal output attains a predetermined high value.

It should be noted that the resistor 26 and the cathode lead resistors 38 and 39 are shunted by signal by-pass capacitors 40, 41 and 42 and that a direct current stopping condenser 43 is provided in the signal output circuit of the amplifier stage 18 which is also provided with an output resistor 44 and an input resistor 45.

Fig. 2 illustrates the characteristic operation of the system of Fig. 1, the point 0 being taken as the reference point of the curves D—E, C—A and A—B. The curve D—E will be recognized as the normal characteristic load curve plotted with amplifier input as abscissae and with amplifier output as ordinates. Otherwise stated, the curve D—E is the normal load curve of the amplifier in the absence of the volume compression and anti-overload control circuits.

The curve C—A is the amplifier load characteristic resulting from the bias potential produced in the resistor 25 of the volume compression circuit 29—30, 31 and 37. Thus, a part of the output signal is fed to the diode 31, this signal is rectified by the diode 31 and the rectified current flows through the resistor 25. This current will begin flowing at a signal level at least —40 db. below the normal input signal of the amplifier, this signal being represented by the reference numeral 0. A bias voltage is produced in the resistor 25 which forms a part of the input circuit of the amplifier 15—16. This amplifier has an exponential characteristic which permits a variation of amplification by changing its grid bias voltage. It is thus apparent that the amplification of this amplifier will vary with the potential drop of the resistor 25 and it will amplify less as the signal output level increases. Otherwise stated, the volume is compressed as the output signal level increases.

The curve A—B is the amplifier load characteristic resulting from the bias potential produced in the resistor 25 by the anti-overload or relatively high compression circuit 34—35, 36 and 37. The diode 36 has applied to its cathode

a bias potential derived from the lower section of the bleeder resistor 26 through the lead 28. This bias potential is adjusted to equal the signal output voltage applied to the diode 36 when the amplifier is delivering its rated output. As the signal output voltage applied to the diode must exceed the value of the bias potential before rectification occurs, it follows that no current is delivered through the diode 36 until the amplifier delivers its normal output. This point is indicated at A. At this point, the overload control circuit begins to function to add more current to that flowing through the resistor 25, thus increasing the bias potential and producing a more rapid compression of the amplifier output.

The system of Fig. 3 accomplishes the same result as the system of Fig. 1 but differs therefrom in that the volume compression and overload bias potentials are applied to different stages of a resistance coupled amplifying channel. This channel includes signal input terminals 10—11 and signal output terminals 12—13 which are interconnected through an amplifier 46, a coupling capacitor 47, an amplifier 48 and a coupling capacitor 49.

It will be noted that the amplifiers 46 and 48 are of the pentode type and that power for operating the amplifying channel is derived from the power supply terminals 23—24. The input signal is applied to a resistor 50 which has its upper terminal connected to the control grid of the amplifier 46 and its lower terminal grounded for alternating current through a capacitor 51. Anode-cathode potential is applied to the amplifier 46 from a filter resistor 52 and capacitor 53 through an output resistor 57, a bleeder resistor 54—55 partly shunted by a capacitor 56 being provided for producing a constant bias potential in the amplifier input circuit. The screen grid potential of the amplifier 46 is derived from a filter resistor 58 and capacitor 59. The similar connections of the amplifier 48 will be understood without detailed explanation.

From the output circuit of the amplifying channel is derived a control signal which is applied to the control circuit terminals 60 and 61.

Connected to the terminals 60 and 61 through coupling capacitors 62 and 63 and resistors 64 and 65 is a diode double wave rectifier 31 provided with a cathode lead resistor 66 from which a volume compression bias potential is applied through a resistor 67 to the control and suppressor grids of the amplifier stage 46. The application of this bias potential to both the grids is advantageous in that it makes the amplifier 46 operate with an exponential type of load characteristic.

Also coupled to the control terminals 60 and 61 through capacitors 68 and 69 and resistors 70 and 71 is a diode double wave rectifier 36 provided with a cathode lead resistor 72 from which overload bias potential is applied through a resistor 73 to the control and suppressor grids of the amplifier stage 48. For the purpose of preventing the flow of current through the rectifier 36 from affecting the input of the amplifier 48 until the amplifier output has attained normal value, an adjustable part of a bleeder resistor 74 shunted by a capacitor 75 is interposed in the input circuit. The resistor 72 is shunted by a timing capacitor 76.

The operation of the system of Fig. 3 is the same as that of Fig. 1, the double diode 31 func-

tioning to gradually compress the output as the signal level increases and the double diode 36 functioning to prevent overloading of the output circuit.

I claim as my invention:

1. The combination of an amplifier provided with input and output circuits, a resistor connected in said input circuit, means for deriving from said output circuit and producing in said resistor a bias potential whereby the gain of said amplifier is gradually reduced as the signal level increases to its normal value, means for deriving from said output circuit and producing in said resistor a bias potential whereby the gain of said amplifier is reduced more rapidly when the signal level exceeds its normal value, and means for preventing the production of said latter bias potential until said signal level has attained its normal value.

2. The combination of an amplifier provided with input and output circuits, a resistor connected in said input circuit, means for deriving from said output circuit and producing in said resistor a bias potential whereby the gain of said amplifier is gradually reduced as the signal level increases to its normal value, means for deriving from said output circuit and producing in said resistor a bias potential whereby the gain of said amplifier is reduced more rapidly when the signal level exceeds its normal value, and means for timing the relation of the gain controlling action of said bias potentials on said input circuit.

3. In a signal amplifying channel including a plurality of amplifying stages, the combination of an amplifying tube in an initial stage having an amplification control circuit, means providing a signal output impedance for said amplifying channel to which said amplification control circuit is connected, means providing low signal voltage and high signal voltage output connections on said impedance means on opposite sides of said last-named connection, a rectifier for each of said low voltage and high voltage output connections, a common output resistor for said rectifiers, said amplifier tube having a cathode and said resistor being connected between the cathode and said amplification control circuit, and means providing a delayed potential in circuit with the rectifiers for the high signal voltage output connection of a value to prevent operation of the high voltage rectifiers until the amplifying channel delivers a normal signal output level.

4. In an audio frequency amplifier, the combination of an initial amplifying stage comprising an amplifying tube having a cathode and an amplification control electrode, an output transformer for said amplifier having a secondary provided with low and high signal potential output connections and a connection common thereto for said control electrode, a biasing resistor connected between said last-named connection and the cathode, a rectifier connected between each of said low and high signal voltage output connections and said resistor whereby said resistor provides a common output potential means for said rectifiers, and means providing a fixed source of delay potential in circuit with said high signal potential rectifiers having a potential value such that said high signal voltage rectifiers are rendered inoperative until a predetermined normal signal output level is attained.

WILLIAM J. MORLOCK.