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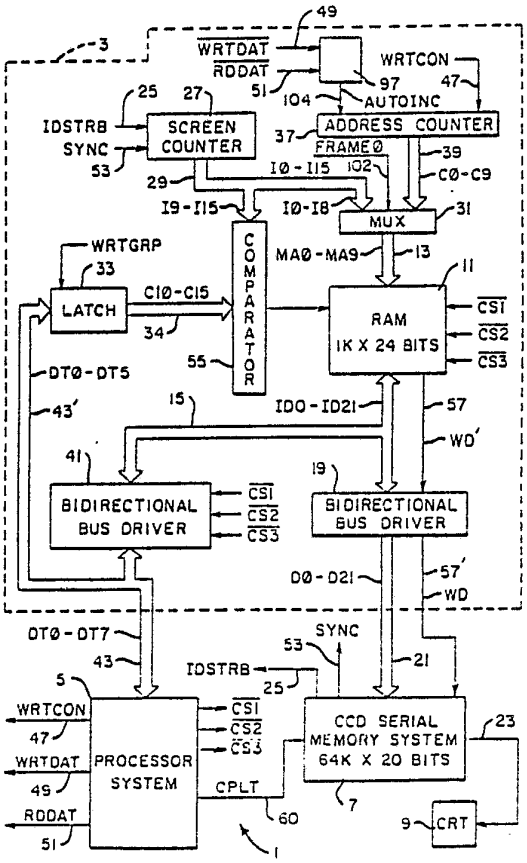
(54) Title: DATA TRANSFER SYSTEM

(57) Abstract

A buffer memory system for effecting parallel transfer of data between an eight-bit processor (5) and a large continually recirculating serial memory (7) includes a 1024 word by 20 bit static random access memory (RAM) (11). Twenty data terminals of the serial RAM (7) are coupled by means of first bi-directional driver circuitry (19) to corresponding terminals of the static RAM (11). Three groups of the data terminals of the static RAM (11) are sequentially multiplexed onto a data bus of the processor (5). Control circuitry responsive to control signals produced by the processor (5) and the serial memory includes first (37) and second (27) counters, outputs of which are applied to the static RAM (11) to enable the processor (5) to write information into and read information out of the static RAM (11) and to enable the serial memory (7) to write information into and read inforamtion out of the static RAM (11),



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DATA TRANSFER SYSTEM

Technical Field

This invention relates to a data transfer system for transferring data between a processor and a memory system.

Background Art

Low cost charge coupled devices (CCDs) may be utilized to implement serial memories for storing information to be outputted to and displayed on video and associated scanning circuitry. CCDs are dynamic in nature and must be continually recirculated at a minimum shift rate to ensure refreshing of each memory cell to avoid loss of stored data. As is well known, the scanning circuitry for cathode ray tube display systems ordinarily continuously scans the screen area in order to provide a continuous display. Consequently, information to be displayed on the CRT screen must be serially inputted to the scanning circuitry at a rate which is synchronized with the scanning rate. It is desirable to utilize CCD memory devices (which are relatively low cost memory devices) operating in synchronization with the scanning circuitry of a CRT display system.

Disclosure of the Invention

It is an object of the present invention to provide a system and method capable of economically effecting rapid transfer of parallel formatted data with a recirculating serial memory system.

According to the present invention, there is provided a data transfer system for transferring data between a processor and a memory system, characterized by buffer memory means, first transfer means coupled to said processor and to said buffer memory means, first addressing means arranged to produce a first sequence of address signals effective to store in said buffer

memory means the data transferred by said first transfer means from said processor, second transfer means coupled to said buffer memory means and to said memory system, and second addressing means arranged to produce, in response to timing signals provided by said memory system, a second sequence of address signals effective to read out stored data from said buffer memory means to said second transfer means for application to said memory system.

According to another aspect of the present invention, there is provided a method for transferring data between a processor and a memory system, characterized by the steps of providing data words derived from said processor, transmitting said data words to buffer memory means under the control of first addressing means, incrementing second addressing means in accordance with timing signals provided by said memory system, and transmitted the data stored in said buffer memory means to said memory system in accordance with addresses provided by said second addressing means.

It should be understood that a relatively large number of bits (approximately 1.3 million bits) must be temporarily stored in order to effect display of information on the cathode ray tube of a conventional video display system. It is frequently desirable to be able to print out this stored information, which also is being displayed on a CRT of the video display system. Further, it frequently is desirable to be able to perform diagnostic operations on a serial memory utilized to store data (which subsequently is serially outputted to a cathode ray tube video display system) without utilizing complex circuitry (referred to as decompression circuitry) used in conjunction with interfacing a dynamic serial RAM to a parallel processor.

It will be appreciated that the described embodiment of the invention provides an interface memory system and method for effecting use of a processor to

control writing parallel formatted data into a recirculating serial memory and reading data in a parallel format out of the recirculating serial memory.

Brief Description of the Drawings

Fig. 1 is a block diagram of the interface memory system of the present invention.

Figs. 2A and 2B, inclusive, show a detailed block diagram of one portion of the interface memory system of Fig. 1.

Figs. 3A and 3B, inclusive, show a detailed block diagram of another portion of the memory interface system of Fig. 1.

Figs. 4A-C, inclusive, show a detailed block diagram of another portion of interface memory system of Fig. 1.

Fig. 5 is a detailed block diagram of another portion of the interface memory system of Fig. 1.

Figs. 6A-C, inclusive, show a detailed block diagram of another portion of the interface memory system of Fig. 1.

Fig. 7 is a timing diagram useful in describing the operation of interface memory system of Fig. 1; and

Fig. 8 is a diagram showing the manner in which Figs. 1A-B, Figs. 3A-B, Figs. 4A-C, and Figs. 6A-C are arranged to form the logic circuitry.

Best Mode for Carrying Out the Invention

Referring now to Fig. 1, reference number 1 designates a video display system including a cathode ray tube (CRT) display terminal 9, a charge coupled device (CCD) serial memory system 7 (including associated control and scanning circuitry), a processor system 5 (including a memory and control circuitry) and an interface memory system 3, also referred to as a buffer memory system or a loader memory system. Buffer memory system 3 interfaces between processor system 5

and CCD serial memory system 7 (hereinafter referred to simply as CCD memory system 7) to effect both writing of information from processor system 5 into CCD memory system 7 and reading of data stored in CCD memory system 7.

CCD memory system 7 includes a CCD memory which includes 65,536 (commonly known in the art as 64K) twenty bit words. The 65,536 words continually circulate in synchronization with the above-mentioned scanning circuitry. The scanning circuitry produces scanning signals on conductor 23, which scanning signals are inputted to CRT display device 9, hereinafter referred to as CRT 9. It should be noted that the CCD memory portion of CCD memory system 7 "continuously" recirculates by shifting information contained therein at a minimum frequency to avoid loss of stored information by "refreshing" each CCD cell. Processor system 5 is connected to buffer memory system 3 by means of bidirectional eight bit data bus 43, which is referred to herein as the "processor bus", and which includes conductors DT0-DT7. Processor system 5 produces a number of control signals, including a write control signal WRTCON on conductor 47, a write data signal WRTDAT on conductor 49 and a read data signal RDDAT on conductor 51. Processor system 5 also produces a signal CPLT on conductor 60. The signal CPLT is a "hand-shake" signal which notifies CCD memory system 7 that buffer memory 3 has been filled and is ready to transmit a block of data into CCD memory system 7.

CCD memory system 7 is connected to interface memory system 3 by means of a 22 bit bidirectional bus 21, hereinafter referred to as the "image data bus". Image data lines 21 include conductors D0-D21. CCD memory system 7 produces a data strobe signal IDSTRB on conductor 25. The IDSTRB and SYNC signals are shown in Fig. 7. The SYNC signal on conductor 53 is produced with every occurrence of a vertical synchronization signal which is applied to cathode ray tube 9. Synchronization signals produced by CRT scanning circuitry

are well-known to those skilled in the art, and need not be discussed further herein. The IDSTRB signal is a signal which includes 512 "bursts" of 64 pulses in synchronization with the SYNC signal for each loading or unloading of a static RAM 11, subsequently described.

Data is clocked into CRT 9 from CCD memory system 7 at a 60 MHz. rate. The above-mentioned scanning circuitry causes the data to be outputted to CRT 9 during a scan from the top to the bottom of the CRT screen every 16.6 milliseconds. During the 16.6 milliseconds, the even numbered lines on CRT 9 are scanned. During the following 16.6 millisecond interval, the odd numbered lines of the CRT screen are scanned. Processor system 5 produces a FRAME 0 signal (shown in Fig. 7) which is applied to conductor 102 in Figs. 1 and 5. The FRAME 0 signal is at a logical "zero" during scanning of the even numbered lines of CRT 9 and is at a logical "one" during scanning of the odd numbered lines of CRT 9. (The time required for the CRT beam to move from the bottom of the CRT screen to the top of the CRT screen to make another pass is referred to as the "vertical blank time".)

During the horizontal scanning of the CRT screen, the CCD memory portion of CCD memory system 7 is clocked (i.e., undergoes a data shift) 64 times, followed by a horizontal blanking interval of approximately 9 microseconds; this is repeated during scanning of the 512 even lines and the 512 odd lines of CRT 9. During each horizontal blanking interval, one pulse of the SYNC signal appears on conductor 53. Each time the data in CCD memory undergoes a shift, another pulse of IDSTRB appears on conductor 25. Therefore, 512 "bursts" of IDSTRB pulses occur after each SYNC pulse, as indicated in the timing diagram in Fig. 7.

There are 64 twenty bit words of information displayed on each horizontal scan line of CRT 9. Static RAM 11 contains 1024 (commonly known in the art as 1K)

twenty bit words. This is the amount of information which can be displayed on 16 lines of the CRT 9, and represents 1/64 of the total amount of data which can be displayed on the entire screen of CRT 9.

Referring still to Fig. 1, the 1024 words of static RAM 11 are addressed by means of 10 address inputs MA0-MA9 transmitted via address bus 13 from a multiplexer circuit (MUX) 31. Twenty-two data terminals of static RAM 11 are connected to a 22 bit bidirectional data bus 15, (hereinafter referred to as the "memory data bus"). Twenty two conductors included in memory data bus 15 are designated ID0-ID21. (It should be noted that in the described embodiment of the invention, conductors ID20 and ID21 (Fig. 6C) are not used). The 22 conductors of bidirectional data bus 15 are connected to corresponding ones of a first group of input/output terminals of bidirectional bus driver circuitry 19, (hereinafter referred to simply as bus driver circuitry). A signal WD' is produced on another data terminal of static RAM 11, which data terminal is connected to conductor 57. Conductor 57 is connected to bidirectional bus driver circuitry 19.

Bus driver circuitry 19 includes a second group of input/output terminals connected to image data bus conductors D0-D21, which are connected to CCD serial memory system 7 for transferring 20-bit data words between CCD memory system 7 and bidirectional bus driver circuitry 19. A signal WD (corresponding to WD') is transmitted from bidirectional bus driver circuitry 19 to CCD memory system 7 on conductor 57'.

Bidirectional bus driver circuitry 41 (hereinafter referred to simply as "bus driver circuitry 41") includes first and second groups of input/output terminals. The conductors of memory data bus 15 are respectively connected to corresponding ones of the first group of input/output terminals of bus driver circuitry 41. As subsequently explained with reference

to Fig. 3A, there are three separately packaged groups of individual bus driver circuits contained in bus driver circuitry 41; the three groups are sequentially enabled in response to three control signals $\overline{CS1}$, $\overline{CS2}$, and $\overline{CS3}$. Only four bits of the third eight bit word contain video data; a fifth bit contains a write control bit to determine the level of the WD' and WD signals. The three remaining bits of the third eight bit word are blank. Also, when data is read from static RAM 11 by processor system 5, the three sections or bytes of the 20 bit words outputted onto memory data bus 43 are sequentially routed via the above mentioned three groups of bus drivers to conductors DT0-DT7 in response to $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$.

The three control signals $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ are also inputted to static RAM 11 to enable three corresponding 1024 word by eight bit sections of static RAM 11 to receive the above mentioned eight bit words multiplexed via bus driver circuitry 41 from processor system 5 to static RAM 11, as subsequently explained.

Six of the conductors of processor bus 43, which conductors are designated by reference numeral 43' in Fig. 1, are connected to inputs of a six bit latch circuit 33, (hereinafter referred to as "group latch" 33). The outputs of group latch 33 are connected by bus 34 to inputs of comparator circuitry 55; the conductors of bus 34 are designated C10-C15. Interface memory system 3 includes a screen counter 27, which is a 16 bit counter. Screen counter 27 is reset by the SYNC signal on conductor 53 from CCD memory system 7 and is incremented by the IDSTRB signal on conductor 25 from CCD memory system 7. The outputs of screen counter 27 are connected to a bus 29, which includes conductors I0-I15. Conductors I0-I8 of bus 29 are connected to a first group of inputs of a multiplexer circuit 31. Conductors I9-I14 are connected to respective ones of a first set of inputs of comparator 55. Respective

ones of a second set of inputs of comparator 55 are connected to conductors C10-C15 of bus 34 (which is connected to outputs of group latch 33).

An address counter 37 produces a ten bit address on bus 39, which includes conductors C0-C9. Conductors C0-C9 are connected to a second group of inputs of multiplexer 31. Address counter 37, which is required to address 1024 word static RAM 11, is incremented by the AUTOINC signal, which is shown on conductor 104 in Fig. 4B by one-shot circuit 97.

The above-mentioned 10 bits outputted onto conductors I0-I8 by screen counter 27 along with the FRAME 0 signal enable the CCD memory system 7 to "address" static memory 11, and the 10 bits C0-C9 outputted by address counter 37 enable processor system 5 to "address" static RAM 11. Therefore, depending upon the type of operation being executed, processor system 5 either addresses static RAM 11 to write new information into it or read information out of it (a "processor bus operation") or processor system 5 signals CCD memory system 7 to produce the IDSTRB signal, which causes screen counter 27 to be incremented while other control signals cause static RAM 11 to be accessed at the addresses produced on conductors I0-I8 of bus 29. This causes information stored in static RAM 11 to be transferred to CCD memory system 7 or causes information stored in CCD memory system 7 to be written into static RAM 11 (the latter two operations being referred to as "image bus operations").

Before explaining in detail the operation of video display system 1, it may be helpful to describe in detail an actual implementation of the interface memory system 3 of Fig. 1.

Figs. 2A-B, 3A-B, 4A-C, 5, and 6A-C in combination constitute a detailed block diagram of the interface memory system 3 shown in Fig. 1. Static RAM 11 and bidirectional bus driver circuitry 19 are shown

in Figs. 6A-C. Static RAM 11 is implemented by means of six Intel 2114-2 static random access memory integrated circuits, each of which are organized as 1024 words by four bits. In Figs. 6A-C, the six static random access memory integrated circuits are designated by reference numerals 11A, 11B, 11C, 11D, 11E and 11F. Integrated circuit random access memory (RAM) devices 11A and 11B are selected by means of the previously mentioned $\overline{CSI}$ signal applied to conductor 61A. Similarly, integrated circuit RAM devices 11C and 11D are selected in response to $\overline{CS2}$ on conductor 61B, and integrated circuits RAM devices 11E and 11F are selected in response to $\overline{CS3}$ on conductor 61C.

The 24 data outputs of RAM devices 11A-11F are connected, respectively, to corresponding ones of conductors ID0-ID21 of memory bus 21. One of the unused data outputs of integrated circuit RAM device 11F is utilized to conduct the previously mentioned WD' signal.

Bus driver circuitry 19 includes three integrated circuit bidirectional three state driver devices designated in Figs. 6A-C by reference numerals 19A, 19B and 19C. Devices 19A, 19B and 19C are implemented by means of Texas Instruments 74LS245 Universal Bidirectional Bus Driver Integrated Circuits. (It should be noted that in the drawings, certain lead numbers of the integrated circuits identified herein by a manufacturer's part number are indicated, in order to make it completely clear how such integrated circuits are interconnected. However, manufacturer's part numbers and lead numbers have been omitted herein for conventional logic gates shown in the drawings).

The memory data bus terminals ID0-ID21 are connected, respectively, to individual ones of a first group of bidirectional data terminals of bus driver integrated circuits 19A, 19B and 19C as shown in Figs. 6A-C. Each of a second group of bidirectional data terminals of bus driver integrated circuits 19A, 19B and

19C are connected, respectively, to image data bus conductors D0-D21. The direction of transfer of information in bus driver circuits 19A-19C is determined by the read image data bus signal RDIDB produced on conductor 63. Conductor 63 is conducted to lead No. 1 of each of integrated circuit bus drivers 19A, 19B and 19C.

Each of integrated bus driver circuits 19A, 19B and 19C has a three state output driver connected, respectively, to each of the data terminals of that integrated circuit. The output drivers can be caused to assume a high impedance state by means of a signal applied to leads 19 of the respective bus driver circuits 19A, 19B and 19C. Lead 19 of each of bus driver circuits 19A-19C is connected to conductor 65. Conductor 65 is connected to the output of an AND gate 67, which has its outputs connected, respectively, to a conductor to which a "read image data bus" signal $\overline{\text{RDIDB}}$ is applied and to a conductor to which a "write image data bus" signal $\overline{\text{WRIDB}}$ is applied. Since negative logic signals are applied to the inputs of AND gate 67, AND gate 67 performs a "logical ORing" function, so that a read image data bus command or a write image data bus command causes the bus driver circuitry 19 to be "enabled"; otherwise, the bus driver circuits contained in block 19 (Fig. 1) assume high output impedance configurations.

The WD (write data) signal on conductor 57' is produced by logically ANDing the write image data bus signal WRIDB and the ENAB signal with the WD' signal via gates 63A, 63B and 63C. The purpose of the WD signal is to allow transfer of all information stored in static RAM 11 to be transmitted via image data bus 21 to CCD memory system 7 while only allowing a portion of that data to actually be written into CCD serial memory system 7. (This capability allows a check verification system in which the video display system 1 is utilized to obtain an image of a signature on a check

to be verified by means of a video camera and display the image on the CRT screen adjacent to an authorized signature previously retrieved from a computer memory and displayed on the screen without re-writing the signature data into the CCD memory).

The static memory address inputs MA0-MA9 shown in Figs. 6A-C are connected, respectively, to leads A0-A9 of each of memory integrated circuits 11A-11F.

Lead 10 of each of integrated RAM circuits 11A-11F is a write input terminal of that RAM circuit. The write signal applied thereto is produced by a logic circuit including NAND gate 69A, AND gates 69B and 69C and AND gate 69D.

Bus driver circuitry 41 of Fig. 1 is implemented by means of three 74LS245 integrated circuits designated by reference numerals 41A, 41B and 41C in Fig. 3A. Each of a first group of input/output terminals of each of bus driver circuits 41A-41C is respectively connected to certain ones of conductors DT0-DT7 of processor data bus 43. More specifically, DT0 is connected to the A1 terminal of each of bus driver circuits 41A, 41B and 41C. Similarly, DT1 is connected to the A2 terminal of each of bus driver circuits 41A-C, etc.

A second group of input/output terminals of bus driver circuit 41A are connected, respectively, to conductors ID0-ID7 of memory data bus 15; each of a corresponding group of input/output terminals of bus driver circuit 41B is connected, respectively, to conductors ID8-ID15 of memory data bus 15; and each of a corresponding group of input/output terminals of bus driver circuit 41C is connected, respectively, to conductors ID16-ID23 of memory data bus 15.

A signal RDCCB applied to conductor 71 in Fig. 3A controls the direction of data transfer for bi-directional bus driver circuits 41A-41C, and causes data to be transferred from processor data bus 43 to static

RAM 11 if RDCCB is at a logical "one" and causes the direction of data transfer to be in the opposite direction if RDCCB is at logical "zero".

Driver 41A is enabled by signal $\overline{CS1}$ via gates 42A, 42B, 42C, and 42D; driver 41B is enabled by signal $\overline{CS2}$ via gates 42E, 42F, 42G, and 42H; driver 41C is enabled by signal $\overline{CS3}$ via gates 42J, 42K, 42L, and 42M. The logic circuitry connected to lead 19 of each of bi-directional bus driver circuits 41A-41C causes all of the input/output terminals of each of bus driver circuit 41A-41C to assume a high impedance state via gates 44A and 44B if either a "read image data bus" ($\overline{RDIDB}$) or a "write image data bus" ($\overline{WRIDB}$) operation occurs, or via gate 44C if either a read data ($\overline{RDDAT}$) operation or a write data ($\overline{WRDAT}$) operation occurs.

Group latch circuit 33 of Fig. 1 can be implemented by means of a Texas Instruments LS174 six bit integrated circuit latch, designated by reference numeral 33 in Fig. 4C.

Screen counter 27 of Fig. 1 can be implemented by means of four Texas Instruments 74LS161 integrated circuit counters, designated by reference numerals 27A, 27B, 27C and 27D in Fig. 4B. Each of counters 27A-27D is reset by a signal $\overline{SYNC}$, which is the logical complement of the SYNC signal produced on conductor 53 in Fig. 1. The clock inputs of each of counter circuits 27A-27D are connected to conductor 73. The clock (CLK) input of each of counter circuits 27A-27B receives a clock signal produced in response to IDSTRB via gates 20A, 20B, and 20C (Fig. 4A).

The outputs of counters 27A-27D are connected, respectively, to conductors I0-I15 of bus 29. Conductors I0-I8 along with the FRAME 0 signal are connected to inputs of multiplexer circuitry 31, which can be implemented by means of Texas Instruments 74LS157 Quad 2-to-1 line multiplexer (MUX) integrated circuits 31A, 31B and 31C, as shown in Fig. 5. The multiplexer se-

lection is controlled by signals $\overline{\text{RDIDB}}$ and $\overline{\text{WRIDB}}$ via a NAND gate 31D. The signal FRAME 0 is applied to multiplexer circuit 31B via gates 102A and 102B. Conductors I9-I14 are connected to respective ones of a first group of comparison inputs of comparators 55A and 55B of Fig. 5. Comparators 55A and 55B can be implemented by means of Texas Instruments LS 85 four bit comparator integrated circuits, as shown in Fig. 5.

Each of a second group of comparison inputs of comparator circuits 55A and 55B is connected to a respective one of outputs C10-C15 of group latch 33 (previously described with reference to Fig. 3A).

Address counter 37 of Fig. 1 is implemented by means of three integrated circuit counter circuits designated by reference numeral 37A, 37B and 37C (Fig. 4C) which counter circuits can be implemented by means of Texas Instruments LS161 four bit synchronous counters with synchronous clear inputs. The outputs labeled C0-C9 of address counter circuits 37A-37C are connected to corresponding inputs of multiplexer circuits 31A-31C of Fig. 3B. The write control signal WRTCON on conductor 47' clears address counters 37A-C. Address counters 37A-C are incremented in response to the occurrence of either a WRDAT pulse or a RDDAT pulse produced by processor system 5, which WRDAT and RDDAT pulses produce the AUTOINC signal previously mentioned.

Referring now to Figs. 2A and 2B, control circuitry (not shown in the block diagram of Fig. 1) is disclosed. Processor system 5 generates additional address and control signals, including address signals A0, A1, and A2 applied to inputs A, B and C of a three-line to eight-line decoder circuit 75 implemented by means of a Texas Instruments 74LS138 integrated circuit. The outputs of decoder circuit 75 produce a plurality of control signals, including a write control signal $\overline{\text{WRTCON}}$ on conductor 77', a write group signal $\overline{\text{WRTGRP}}$ on conductor 78' and a write data signal $\overline{\text{WRTDAT}}$ on con-

ductor 79'. The logical complements of each of the foregoing signals are produced on conductors 77, 78, and 79 as the signals are transmitted through inverters 65, 67, and 69 respectively. The WRTDAT pulses are produced once during every processor write cycle, and the RDDAT pulses are produced once during every processor read cycle.

Other control signals produced by processor system 5 include an address valid signal AVAL, a master select signal MSEL and a board select signal BSEL all of which are applied to inputs of a NAND gate 81. The output of gate 81 is transmitted via an inverter 81A to inputs of two NAND gates 82A and 82B. A write signal WRT produced by processor system 5 is applied to another input of gate 82B via an inverter 83, and a $\overline{\text{POLL}}$ signal is applied to the third input of NAND gate 82B. The output of gate 82B is applied via an inverter 84A to flip-flops 84B and 84C to produce a data valid signal DVALT on conductor 90. Flip-flop 84C is controlled by a processor signal COMPR and a reset signal $\overline{\text{RES}}$ via gates 93A and 93B. A data valid signal DVAL and the WRT signal are also applied to inputs of gate 82A. The output of gate 82A is applied to flip-flops 58A and 58B to produce the signals COMPT and $\overline{\text{COMPT}}$ at the outputs of flip-flop 58B, assuming the processor system is not "busy".

A second three-line to eight-line decoder circuit 85 receives address inputs A0, A1, and A2, and produces a control signal $\overline{\text{RDSTAT}}$ on conductor 86 and a control signal $\overline{\text{RDDAT}}$ on conductor 87 in response to A0, A1, and A2 and several of the above-mentioned control signals produced by processor system 5.

An eight bit octal three state latch implemented by means of a Texas Instruments 74LS374 and designated by reference numeral 89 in Fig. 2B has its eight inputs connected to conductors DT0-DT7 of processor data bus 43. Latch 89 stores memory commands loaded therein by processor system 5, four of the

outputs of latch 89 being connected to conductors, 89', 90', 91', and 92'. A "read processor bus" signal $\overline{\text{RDCCB}}$ is produced on conductor 89'. A "write processor data bus" signal $\overline{\text{WRCCB}}$ is produced on conductor 90'. The previously mentioned "read image data" bus signal $\overline{\text{RDIDB}}$ is produced on conductor 91'. The previously mentioned "write image data bus" signal $\overline{\text{WRIDB}}$ is produced on conductor 92'. The complements of these memory commands are generated by transmitting the $\overline{\text{WRIDB}}$ signal to an inverter 92A, the $\overline{\text{RDIDB}}$ signal to an inverter 91A, transmitting the $\overline{\text{WRCCB}}$ signal to an inverter 90A, and transmitting the $\overline{\text{RDCCB}}$ signal to an inverter 89A.

The operation of the above-described interface system will be best understood if the main control signals and the four above-mentioned memory commands are understood. The MSEL signal applied to AND gate 81 of Fig. 2A indicates that processor system 5 has access to processor bus 43. The WRT signal applied to inverter 83 of Fig. 2A is a command which is utilized to generate the $\overline{\text{WRTCON}}$ signal on conductor 78'. WRTCON is utilized to clock latch 89 of Fig. 2B to load four basic direction signals RDCCB, WRCCB, RDIDB, and WRIDB. $\overline{\text{WRTCON}}$ is utilized in Figs. 4A and B to initialize the sequencing circuitry which produces $\overline{\text{CS1}}$, $\overline{\text{CS2}}$ and $\overline{\text{CS3}}$. In Figs. 4A and B, the three D-type flip-flops 96A, 96B and 96C and associated logic gates 93A and 93B cooperate to produce a serial counter which is incremented via gate 96D in response to a $\overline{\text{WRDAT}}$ (write data) or a $\overline{\text{RDDAT}}$ (read data) signal produced by processor system 5. The outputs of the three D-type flip-flops 96A, 96B and 96C are applied to the inputs of three gates 95A, 95B, and 95C (which are enabled via flip-flop 99A and gate 99B) by means of a multiplexer (MUX) circuit 101. Multiplexer circuit 101 can be implemented by means of a Texas Instruments 74LS157 2-to-1 line multiplexer integrated circuit. Multiplexer circuit 101 is enabled if a "processor bus operation" is being performed, i.e., if both $\overline{\text{RDIDB}}$ and

$\overline{\text{WRIDB}}$ equals logic "one" via gate 95D. Logic circuit 97, which can be implemented by means of a Fairchild 9602 "one-shot" flip-flop, produces a clock signal designated AUTOINC on conductor 104. The signal AUTOINC is utilized to clock address counters 37A-C (Fig. 4C) once in response to each RDDAT or WRDAT pulse produced by processor system 5.

The above-mentioned four direction signals produced by processor system 4 cause interface memory system 3 to perform the following functions. The RDCCB signal causes bus driver circuitry 41 to transfer data on processor bus 43 (Fig. 3A) to memory data bus 15 in three consecutive bytes, whereby they are written into static RAM 11. The WRCCB direction signal causes bus driver circuitry 41 to transfer 20 bits of data from memory data bus 15 in three consecutive bytes onto processor bus 43. Execution of the WRCCB and RDCCB commands are referred herein to as "processor bus operations". The $\overline{\text{WRIDB}}$ direction signal causes bus driver circuitry 19 to transfer data on memory data bus 15 to image data bus 21 (Fig. 6A). These twenty bits of data then are written into twenty bits of CCD memory system 7 in response to the IDSTRB signal. The $\overline{\text{RDIDB}}$ signal causes bus driver circuitry 19 to transfer data outputted by CCD memory system 7 onto image data bus 21 via bus driver circuitry 19 to memory data bus 15 (Fig. 6A) whereby that data is written into static RAM 11.

The basic operation of the system shown in the block diagram of Fig. 1 is as follows. First, a six bit "group number" is written into group latch 33 from processor system 5. The above described control signals (WRTCON, RDCCB, WRTGRP, WRDAT and RDDAT) are then produced by processor system 5 to cause data to be transmitted from processor system 5 to bidirectional bus driver 41. Three thousand seventy two (3072) eight bit bytes then are transmitted from processor system 5 on conductors DT0-DT7 of bidirectional processor bus 43 to

bus driver 41. Each group of three bytes of data form a single 20-bit word, only four bits of the third byte of each group being utilized as data, the fifth bit of the third byte containing information used to generate the WD' and WD signals as seen from Fig. 6C. The $\overline{CSI}$ signal causes the first byte to be loaded into the first 8 bits of the location of static RAM 11 addressed by address counter 37. The second byte of each three byte group is conducted from bidirectional bus driver circuitry 41 onto the next eight bits of bidirectional memory bus 15 by means of $\overline{CS2}$. Similarly, the third byte of each three byte group is routed to 1024 word by eight bit integrated circuit memory devices 11E and 11F of static RAM 11 in response to $\overline{CS3}$.

CCD memory system 7 contains 65,536 20-bit words. Therefore, 16 bits are required to address each word in CCD serial memory system 7, ten of which are produced by address counter 37 to address static RAM 11 as subsequently explained, the other six bits required to address CCD memory system 7 includes outputs C10-C15 of group latch 33. Outputs C0-C9 of address counter 37 of Fig. 1 are used to generate memory address inputs MA0-MA9.

After static RAM 11 is completely loaded by 1024 twenty bit words in the manner described above, the situation is that the CCD serial memory system 7 is simply recirculating at its usual rate. In response to the CPLT signal produced on conductor 60 by processor system 5, the CCD serial memory system outputs the SYNC signal on conductor 53 at the beginning of every vertical retrace signal, as previously described. After each SYNC pulse, 512 IDSTRB pulses are produced on conductor 25, as indicated in Fig. 5. In response to the IDSTRB pulses, screen counter 27 produces sequential addresses on conductors I0-I15 to address static RAM 11 and to transfer data from static RAM 11 to CCD serial memory system 7. In order to accomplish this, bits I0-I8 along with the FRAME 0 signal are inputted to multiplexers

31A-C in order to produce the address inputs MA0-MA9 for static RAM 11 and bits I10-I15 are compared by comparators 55 A and B with the contents of group latch 33. The memory enable signal ENAB is produced, causing static RAM 11 to output data at the address corresponding to the group number stored in group latch 33 when bits I9-I15 match the group number. This sequence continues 32 times, until all of the 1024 twenty bit words stored in static RAM 11 have been loaded into CCD memory system 7, which includes latch circuitry which temporarily "snaps-up" the twenty bit words.

It should be understood that data stored in CCD memory system 7 is broken up into 64 groups. The group number stored in group latch 33 represents one of these 64 groups. Thus, during execution of the above described operations, the group latch number determines which of the 64 groups is involved. Processor system 5 determines the group by loading the six bit group number into group latch 33 by means of the WRTGRP signal generated on conductor 78 in Fig. 2A (as a result of decoding instruction commands produced on address conductors A0, A1 and A2 of processor system 5).

The WD signal generated in response to the "WD information bit" of static RAM 11 (by means of the circuitry shown at the top of Fig. 6C) enables processor system 5 to write new information into a selected twenty bit word in the CCD serial memory system 7. This capability is necessary, since it is not always desired to replace an entire stored block of data (1024 words by twenty bits) during a particular interface memory reading or writing operation. Interface memory system 3 always transmits 1024 twenty bit words to CCD serial memory system 7 during an interface memory write operation, and utilizes the WD signal to control how much of that information actually gets written into the CCD memory system 7.

In order to transfer information stored in CCD memory system 7 to processor system 5, a set of

operations which are essentially the reverse of the foregoing set of operations are performed. Processor system 5 sets up the above-described control signals to transfer data outputted onto conductors D0-D21 of image data bus 21 as the CCD memory circulates. Processor system 5 causes the group number of the selected group of 1024 twenty bit words stored in CCD memory system 7 to be written into group latch 33. The SYNC and IDSTRB pulses cause screen counter 27 to stay in synchronization with the circulating data in CCD memory system 7, and when the first twenty bit word of the selected group appears on image data bus 21, the resulting match between I9-I15 and the outputs C10-C15 of group latch 33 enables static memory 11 to begin receiving the selected 1024 word groups. When the entire selected group has been written into static RAM 11, the CCD memory system sends a handshake signal CPLT to processor system 5, causing multiplexer 31 to switch address inputs MA0-MA9 of static RAM 11 from bus 29 to bus 39, and address counter 37 is then incremented in response to RDDAT signals from processor system 5 to effect outputting successive twenty bit words of the selected group of data from static RAM 11 onto memory data bus 15. Each such twenty bit word is transferred, one byte at a time, to processor bus 43 in response to $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$.

CLAIMS:

1. Data transfer system for transferring data between a processor (5) and a memory system (7), characterized by: buffer memory means (11); first transfer means (41) coupled to said processor (5) and to said buffer memory means (11); first addressing means (37) arranged to produce a first sequence of address signals effective to store in said buffer memory means (11) the data transferred by said first transfer means (41) from said processor (5); second transfer means (19) coupled to said buffer memory means (11) and to said memory system (7); and second addressing means (27) arranged to produce, in response to timing signals provided by said memory system (7), a second sequence of address signals effective to read out stored data from said buffer memory means (11) to said second transfer means (19) for application to said memory system (7).

2. Data transfer system according to claim 1, characterized in that said first addressing means includes a first counter (37); in that said second addressing means includes a second counter (27); and in that said first and second counters (37, 27) are coupled to a multiplexer circuit (31) coupled to said buffer memory means (11).

3. Data transfer system according to claim 2, characterized in that said first counter (37) is incremented in response to signals provided by said processor (5).

4. Data transfer system according to claim 3, characterized in that said second addressing means includes a storage device (33) arranged to store a group address provided by said processor (5), and comparison means (55) coupled to said storage device (33)

4. (concluded)
and to said second counter (27) and adapted to compare said group address with a portion of each address provided by said second counter (27), said comparison means (55) providing a memory enable signal for enabling said buffer memory means (11) to output stored data.

5. Data transfer system according to claim 4, characterized in that said buffer memory means (11) is arranged to store a first number of words each having a second number of bits and in that said processor (5) is coupled to said first transfer means (41) by a processor bus (43) having a third number of conductors less than said second number, said first transfer means (41) being effective to transfer data, in successive groups each including said third number of bits, to corresponding groups of data terminals of said buffer memory means (11).

6. Data transfer system according to claim 5, characterized in that said processor (5) is adapted to provide a signal to said memory system (7) representing that data storage in said buffer memory means (11) is complete.

7. Data transfer system according to claim 6, characterized in that said memory system is adapted to shift the data stored therein and is further adapted to receive from said second transfer means (19) a group of bits equal in number to said second number each time a shifting of data occurs.

8. Data transfer system according to claim 7, characterized in that said memory system is a charge coupled device containing a plurality of words each having said second number of bits.

9. Data transfer system according to claim 8, characterized in that said words stored in said buffer memory means (11) are associated with respective write control bits effective to determine whether or not the associated word is written into said memory system (7).

10. Data transfer system according to claim 9, characterized in that said processor (5) is adapted to control the production of first and second direction signals, said first direction signal controlling said first transfer means (41) to be operative to transfer data from said processor (5) to said buffer memory means (11) and said second direction signal controlling said second transfer means (19) to be operative to transfer data from said buffer memory means (11) to said memory system (7).

11. Data transfer system according to claim 10, characterized in that said processor (5) is adapted to control the production of third and fourth direction signals, said third direction signal controlling said second transfer means (19) to be operative to transfer data from said memory system (7) to said buffer memory means (11) and said fourth direction signal controlling said first transfer means (41) to transfer data from said buffer memory means (11) to said processor (5).

12. Data transfer system according to any one of the preceding claims, characterized in that said buffer memory means includes a random access memory (11).

13. A method for transferring data between a processor (5) and a memory system (7), characterized by the steps of providing data words derived from said processor (5), transmitting said data words to buffer memory means (11) under the control of first addressing

13. (concluded)
means (37), incrementing second addressing means (27) in accordance with timing signals provided by said memory system (7), and transmitting the data stored in said buffer memory means (11) to said memory system (7) in accordance with addresses provided by said second addressing means (27).

14. A method according to claim 13, characterized by the step of comparing a portion of the contents of a counter (27) included in said second addressing means with a group address provided by said processor (5) to provide a memory enable signal for enabling said buffer memory means (11).

FIG. 1

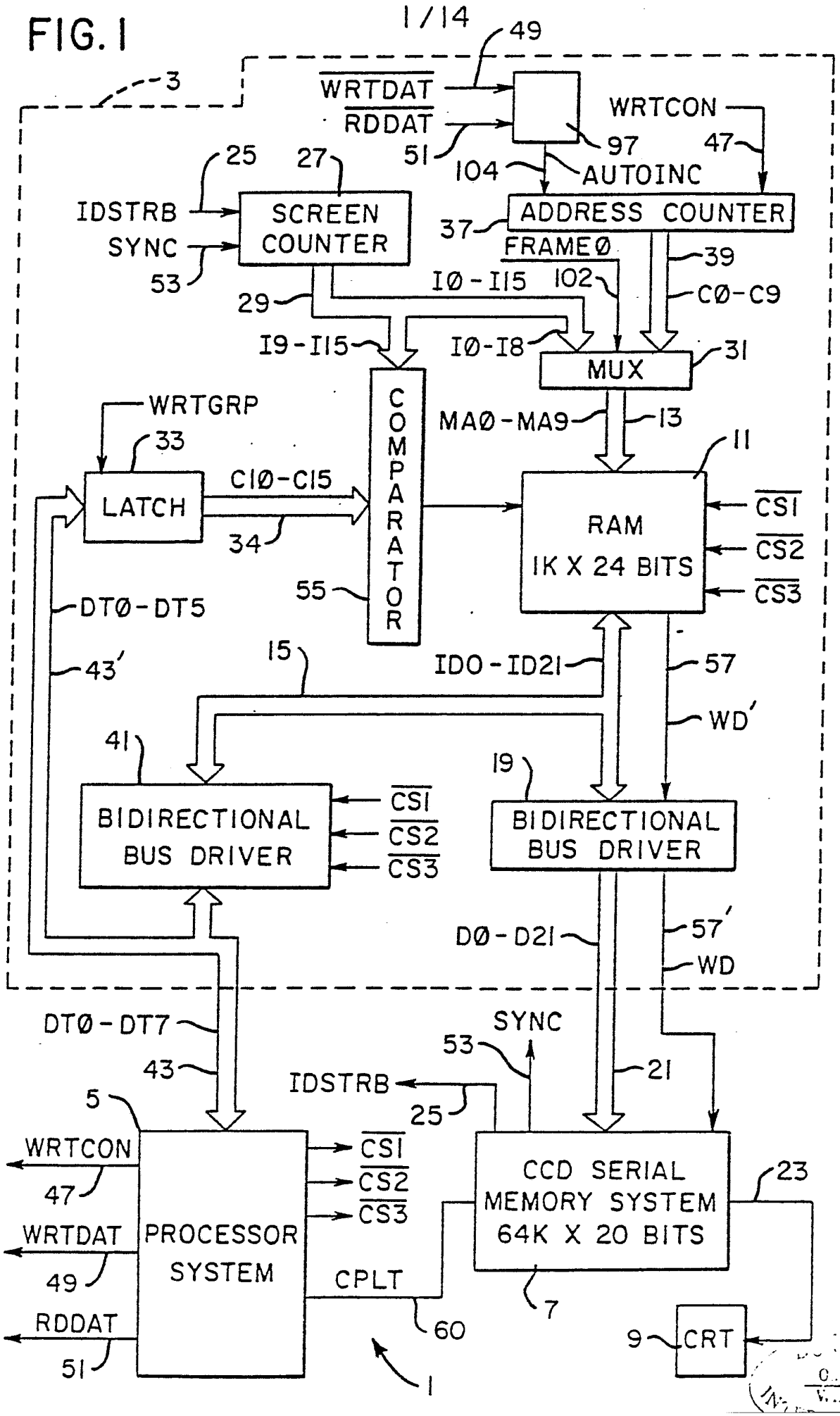
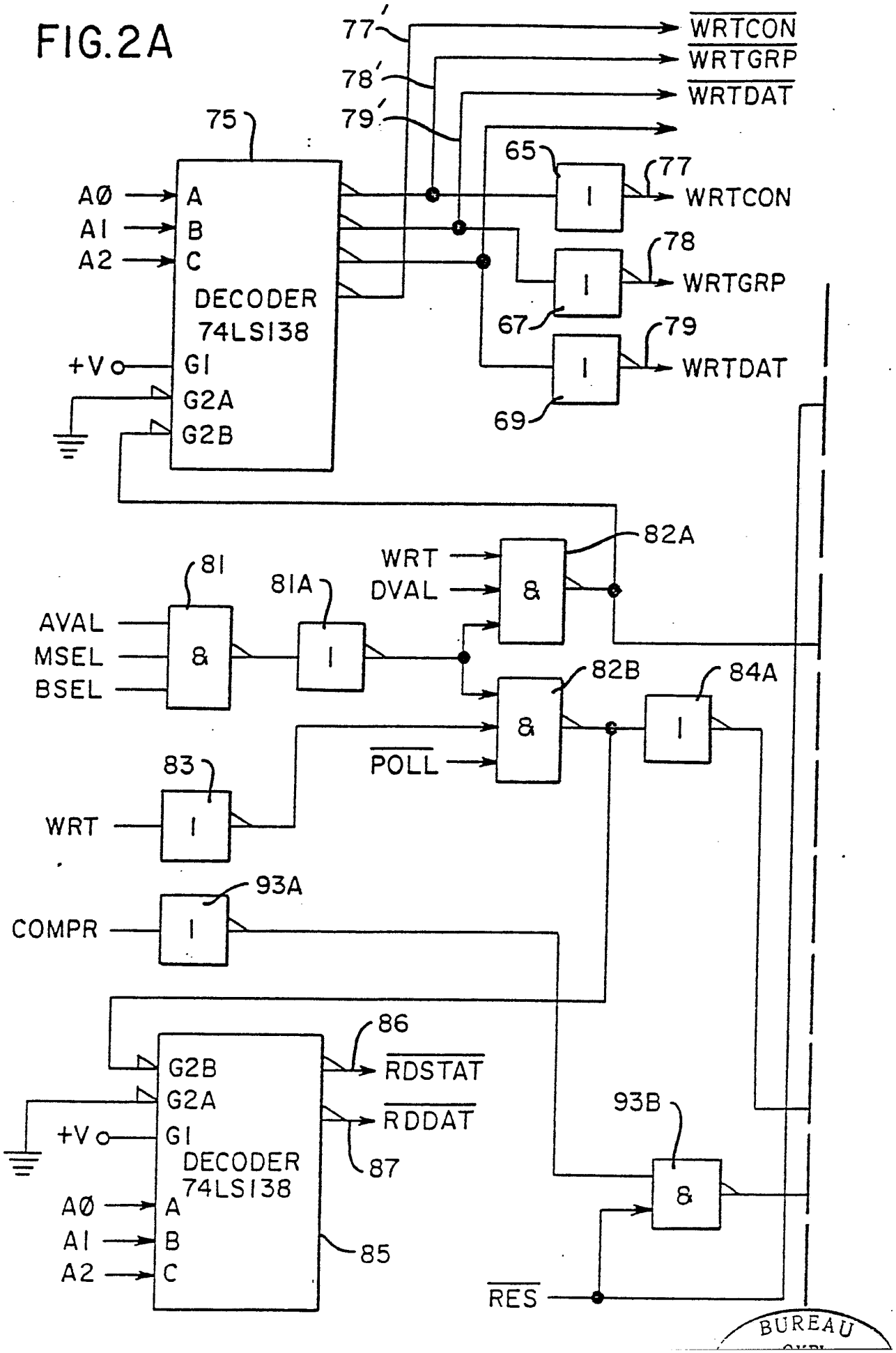

1/14
3
49
WRTDAT
RDDAT
51
97
WRTCON
47
104
AUTOINC
25
27
IDSTRB
SYNC
53
SCREEN COUNTER
ADDRESS COUNTER
37
FRAME0
39
I0-I15
102
C0-C9
29
I9-I15
I0-I8
MUX
31
WRTGRP
33
LATCH
C10-C15
34
COMPARATOR
MA0-MA9
13
11
RAM
1K X 24 BITS
CS1
CS2
CS3
55
DT0-DT5
43'
15
ID0-ID21
57
WD'
41
19
BIDIRECTIONAL BUS DRIVER
BIDIRECTIONAL BUS DRIVER
D0-D21
57'
WD
DT0-DT7
43
SYNC
53
21
IDSTRB
25
5
WRTCON
47
WRTDAT
49
RDDAT
51
PROCESSOR SYSTEM
CPLT
60
CCD SERIAL MEMORY SYSTEM
64K X 20 BITS
23
7
9
CRT
1

FIG.2A


77'
78'
79'
WRTCON
WRTGRP
WRTDAT
75
65
77
A0
A1
A2
A
B
C
DECODER
74LS138
+V
G1
G2A
G2B
1
WRTCON
78
WRTGRP
67
79
WRTDAT
69
82A
WRT
DVAL
&
81
81A
AVAL
MSEL
BSEL
&
1
82B
84A
&
1
POLL
83
WRT
1
93A
COMPR
1
86
G2B
G2A
+V
G1
DECODER
74LS138
A0
A1
A2
A
B
C
RDSTAT
RDDAT
87
85
93B
&
RES

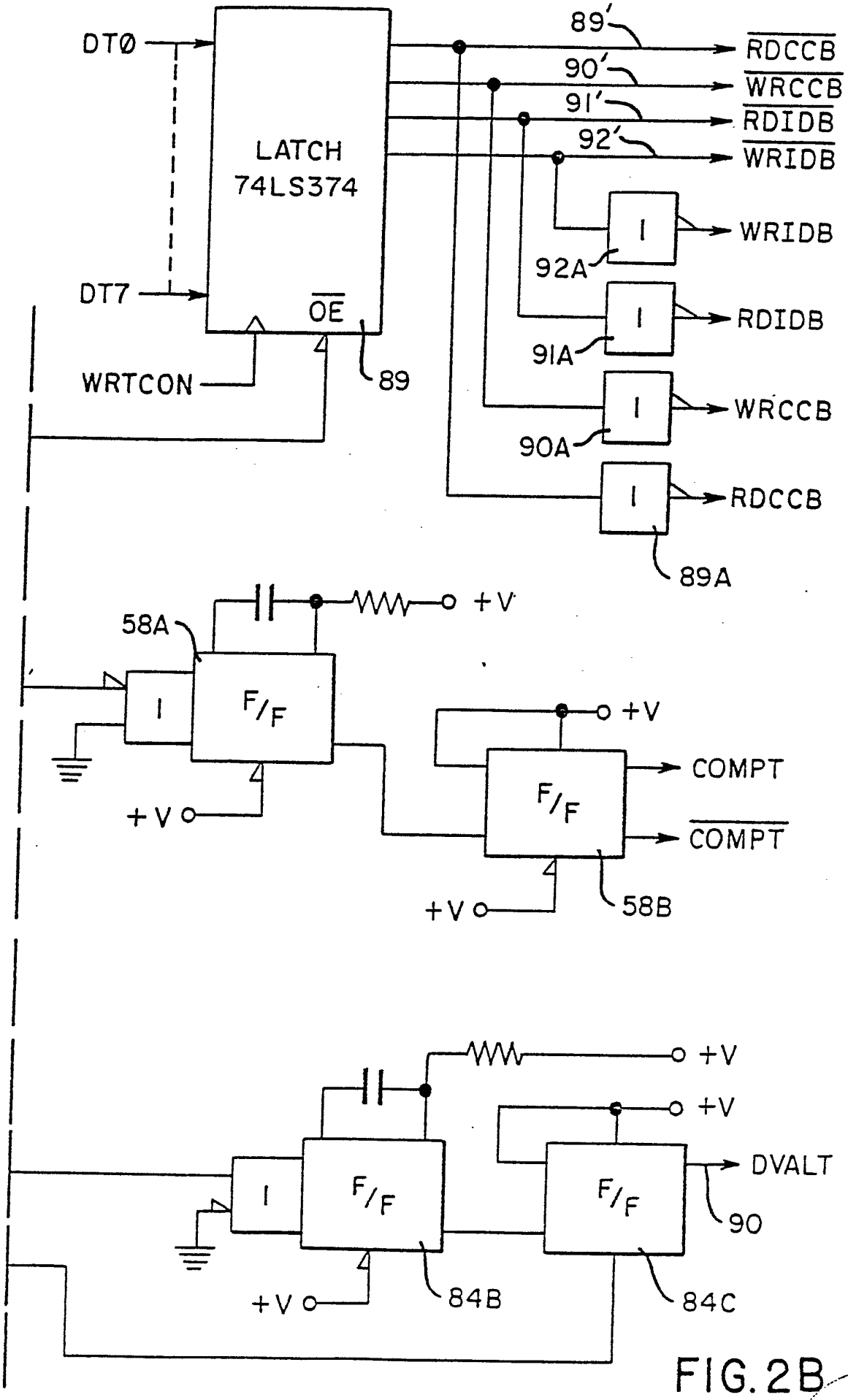


FIG. 2B

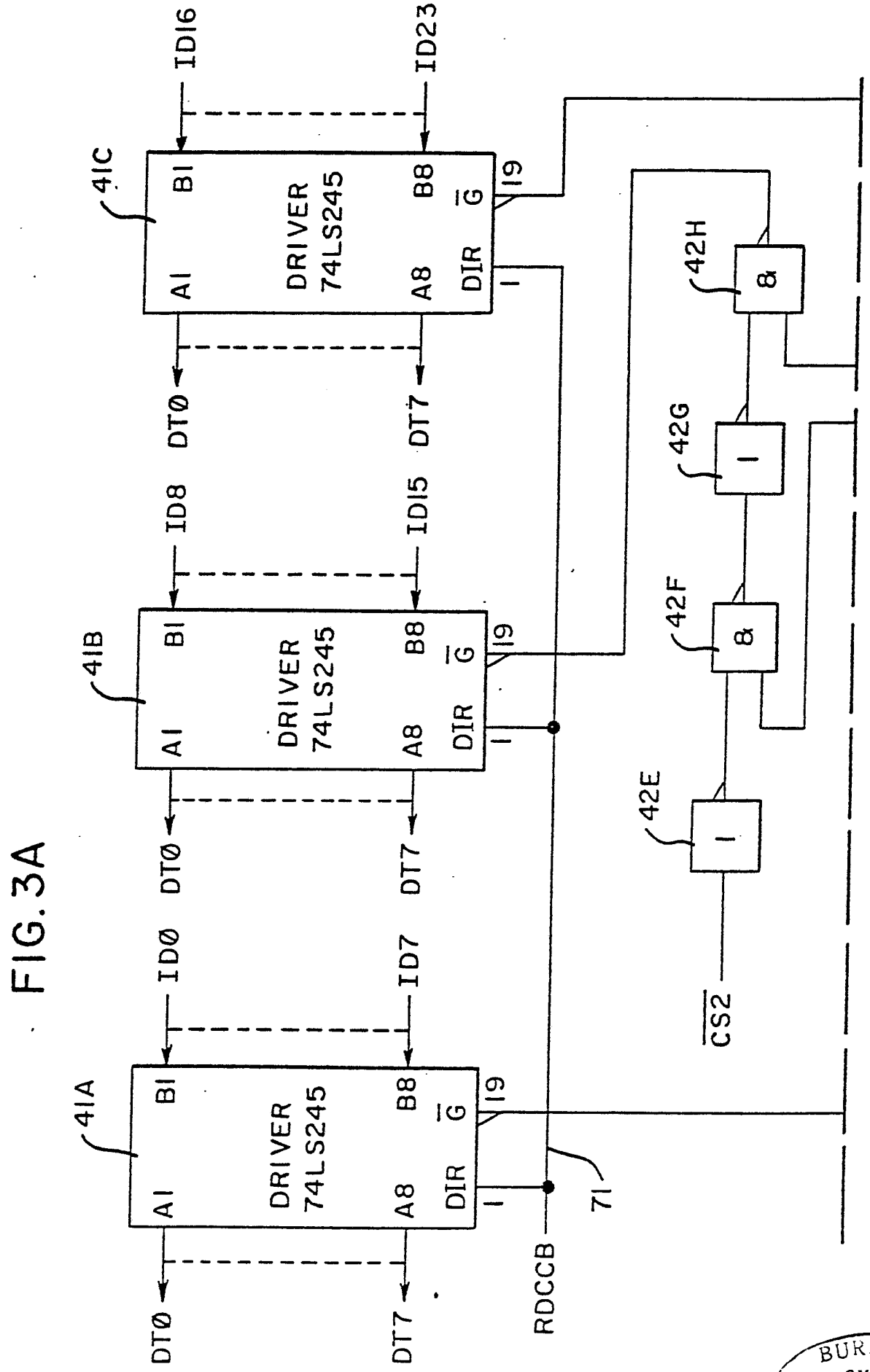


FIG. 3A

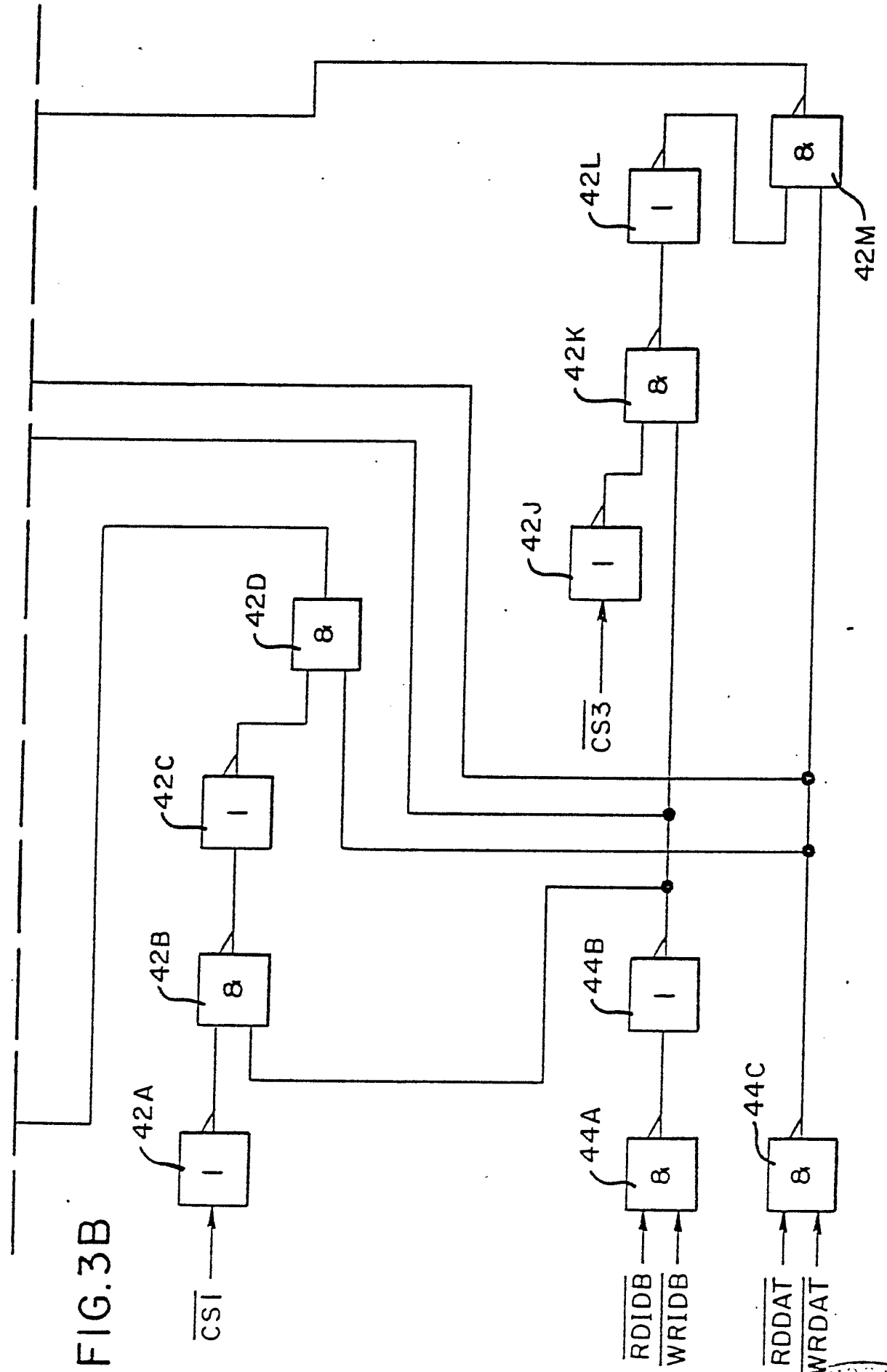


FIG. 3B

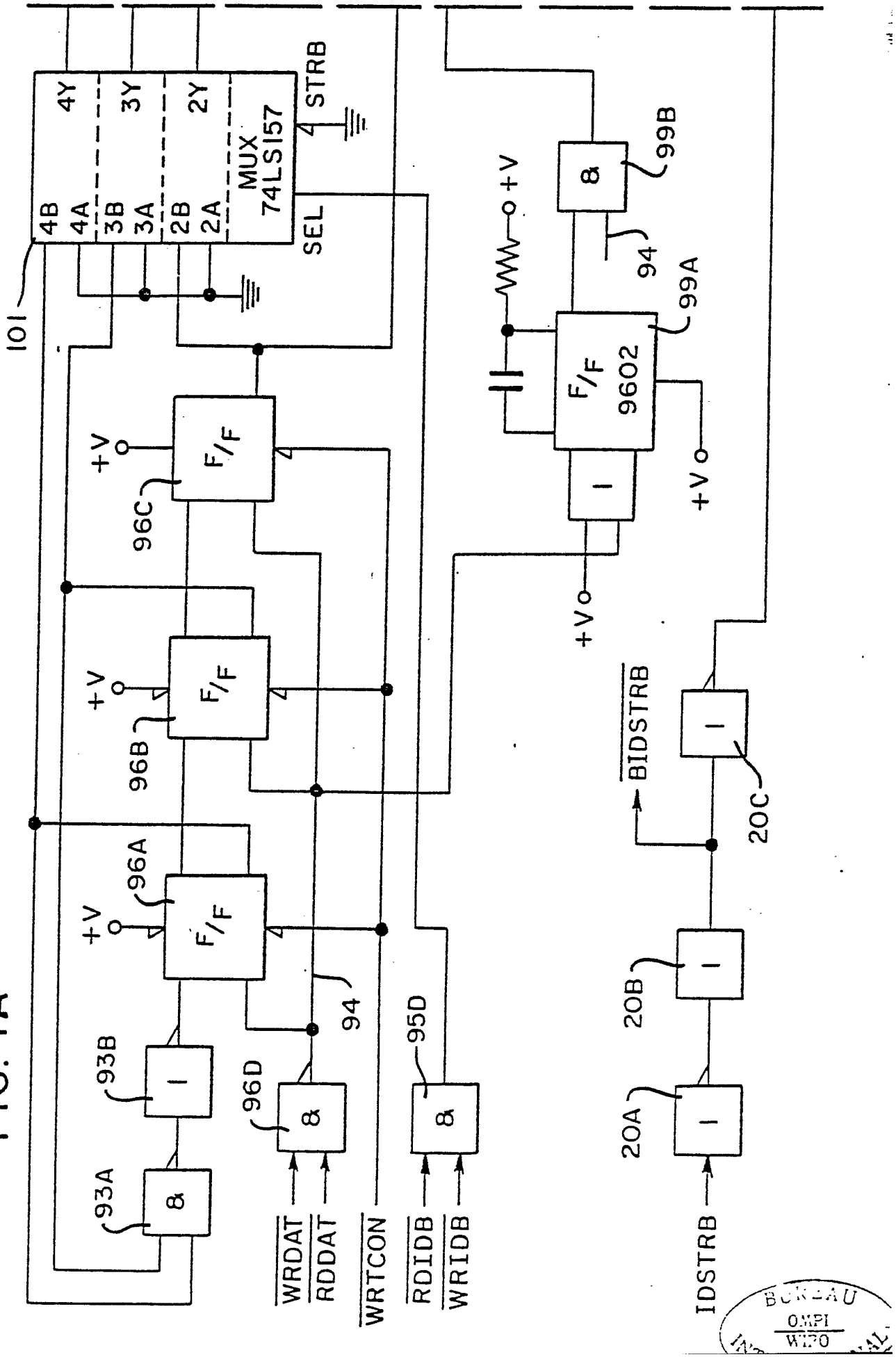


FIG. 4A

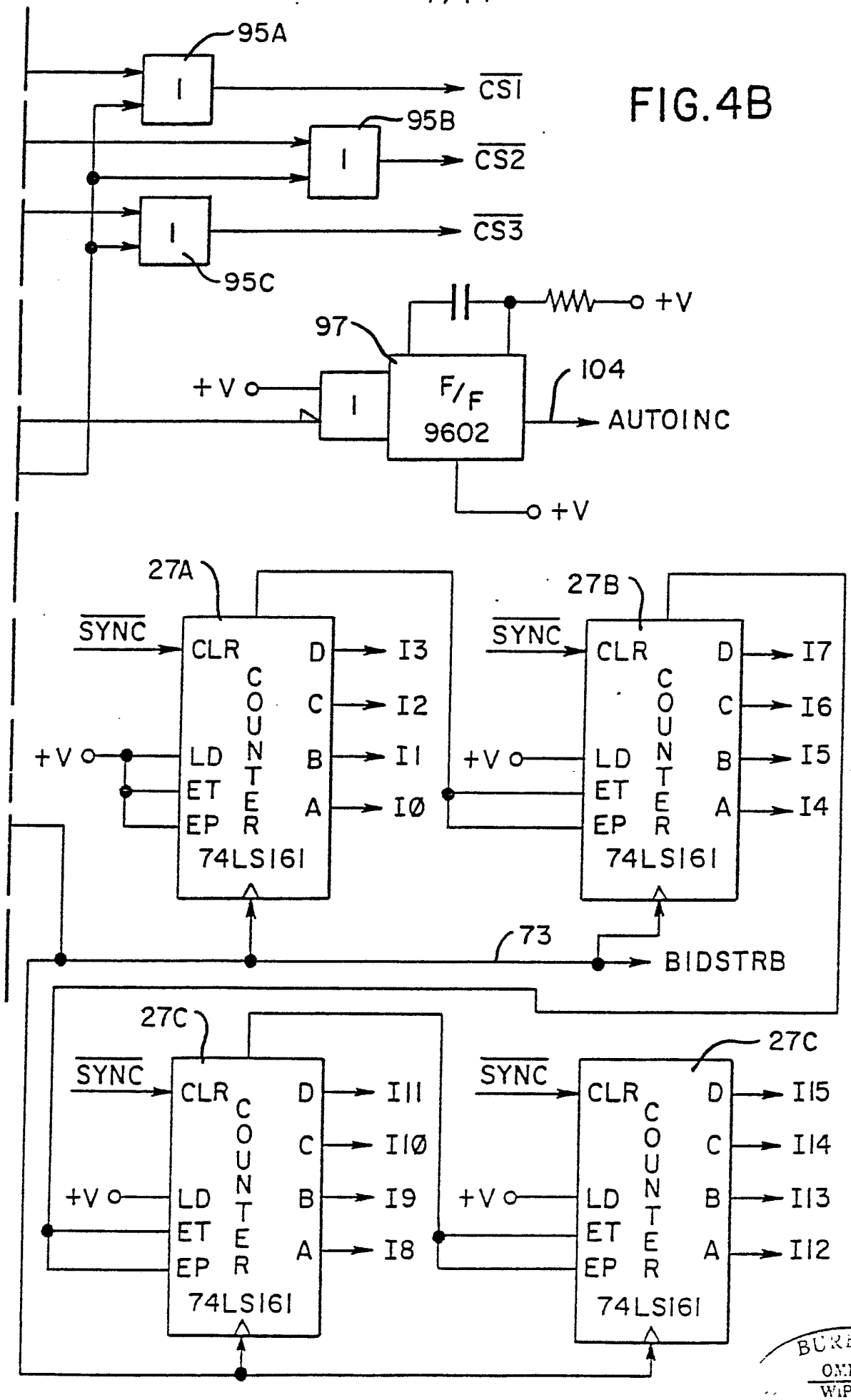


FIG.4B

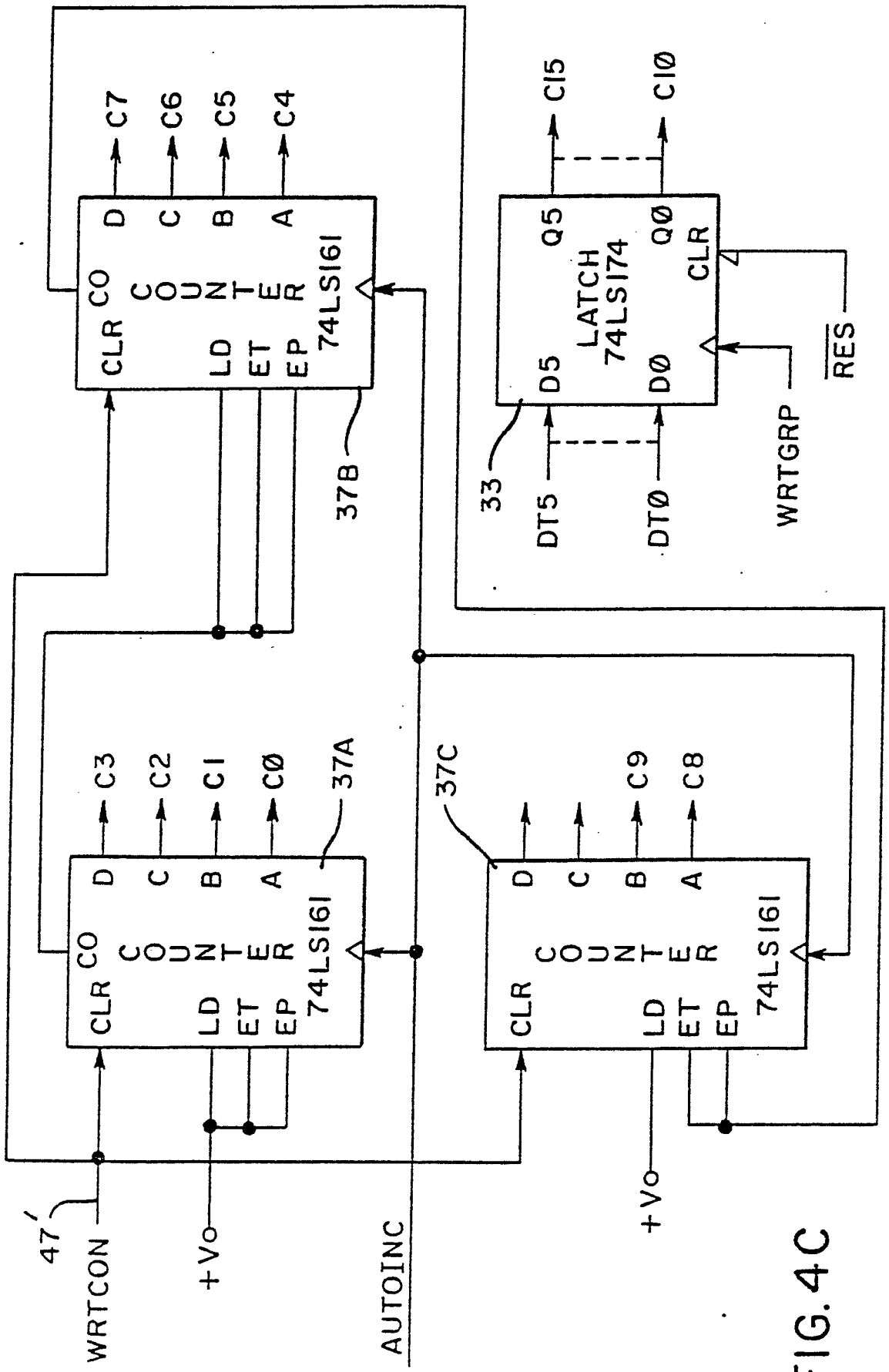


FIG. 4C

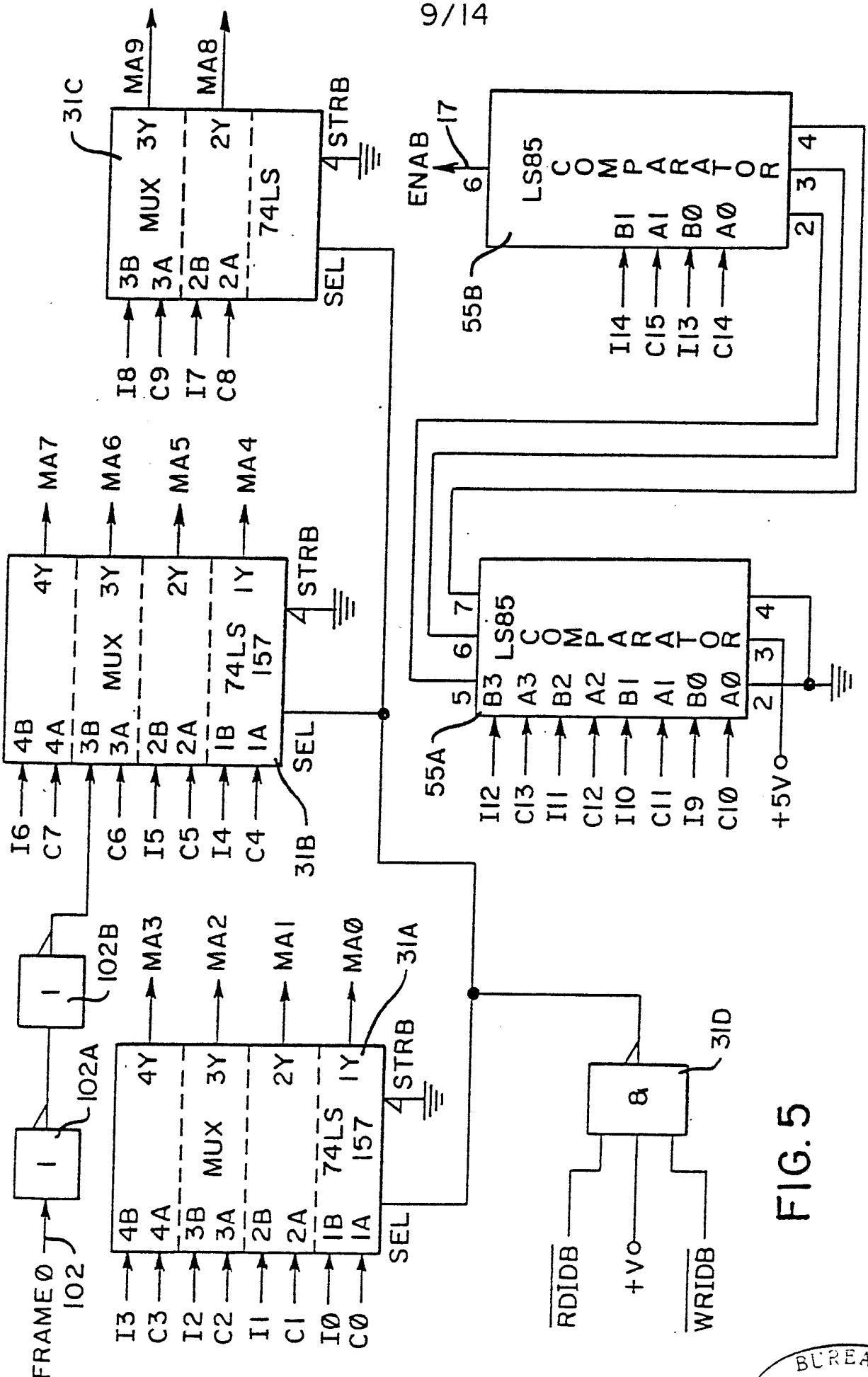


FIG. 5

FIG.6A

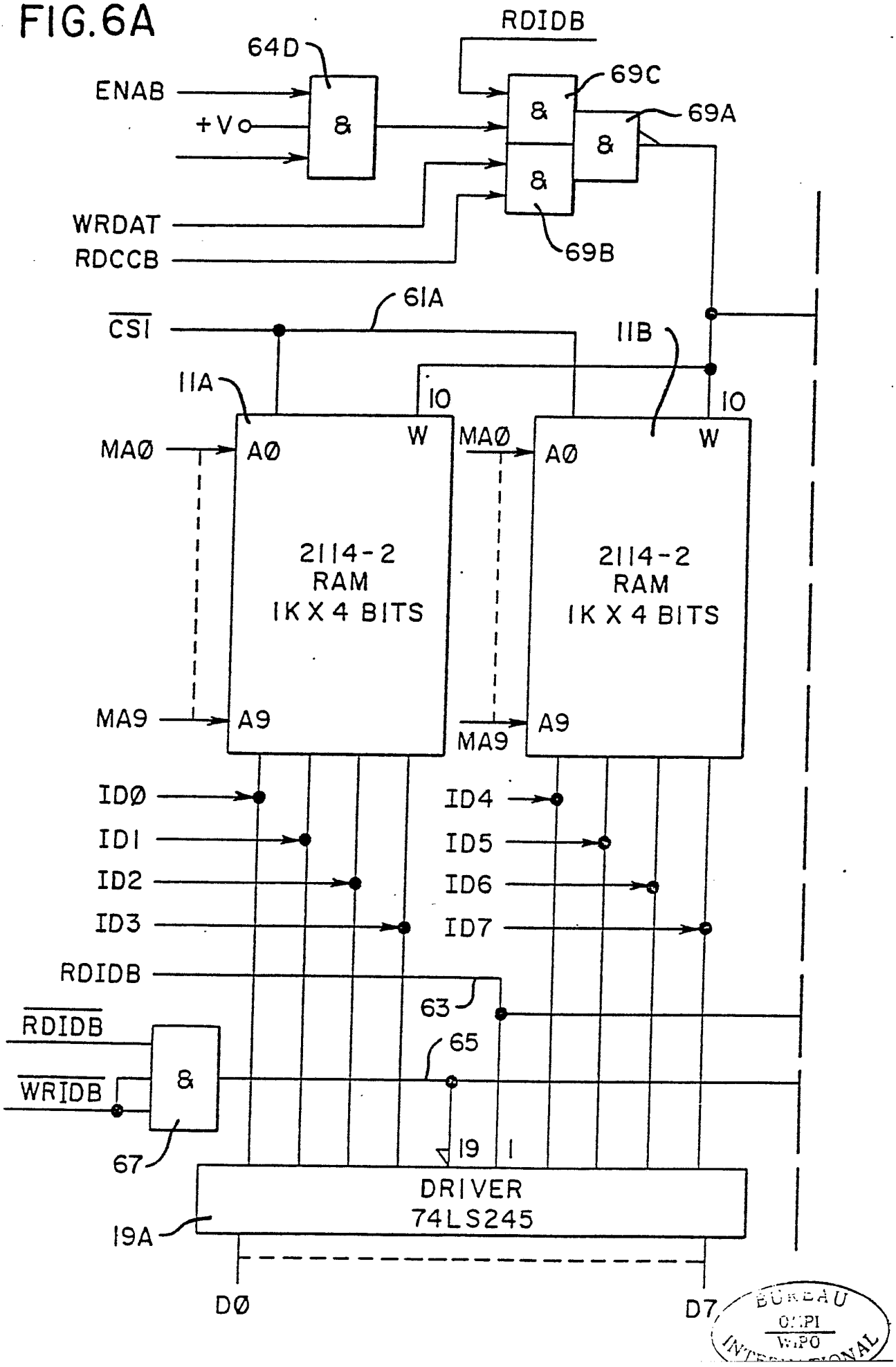


FIG. 6B

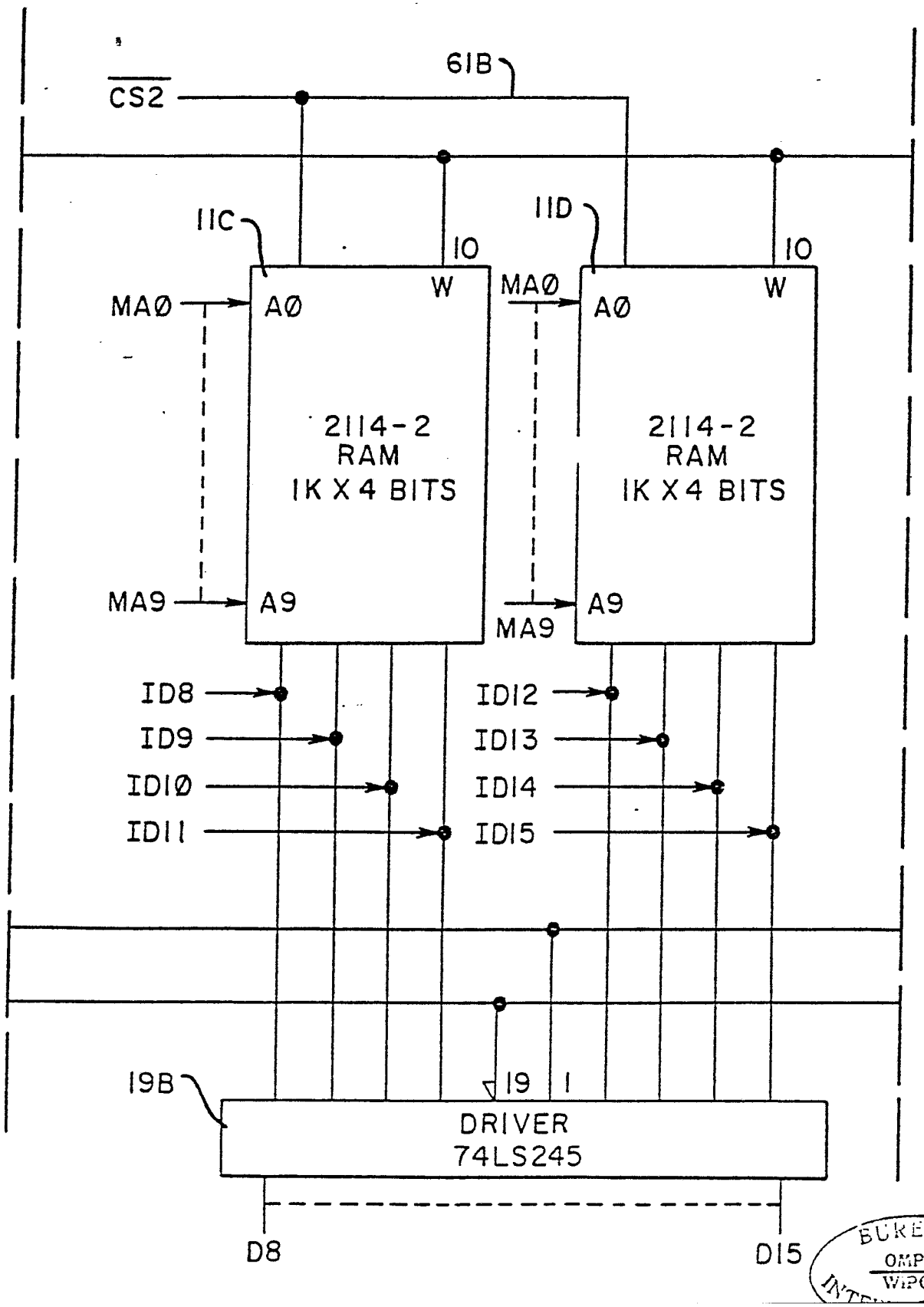


FIG. 6C

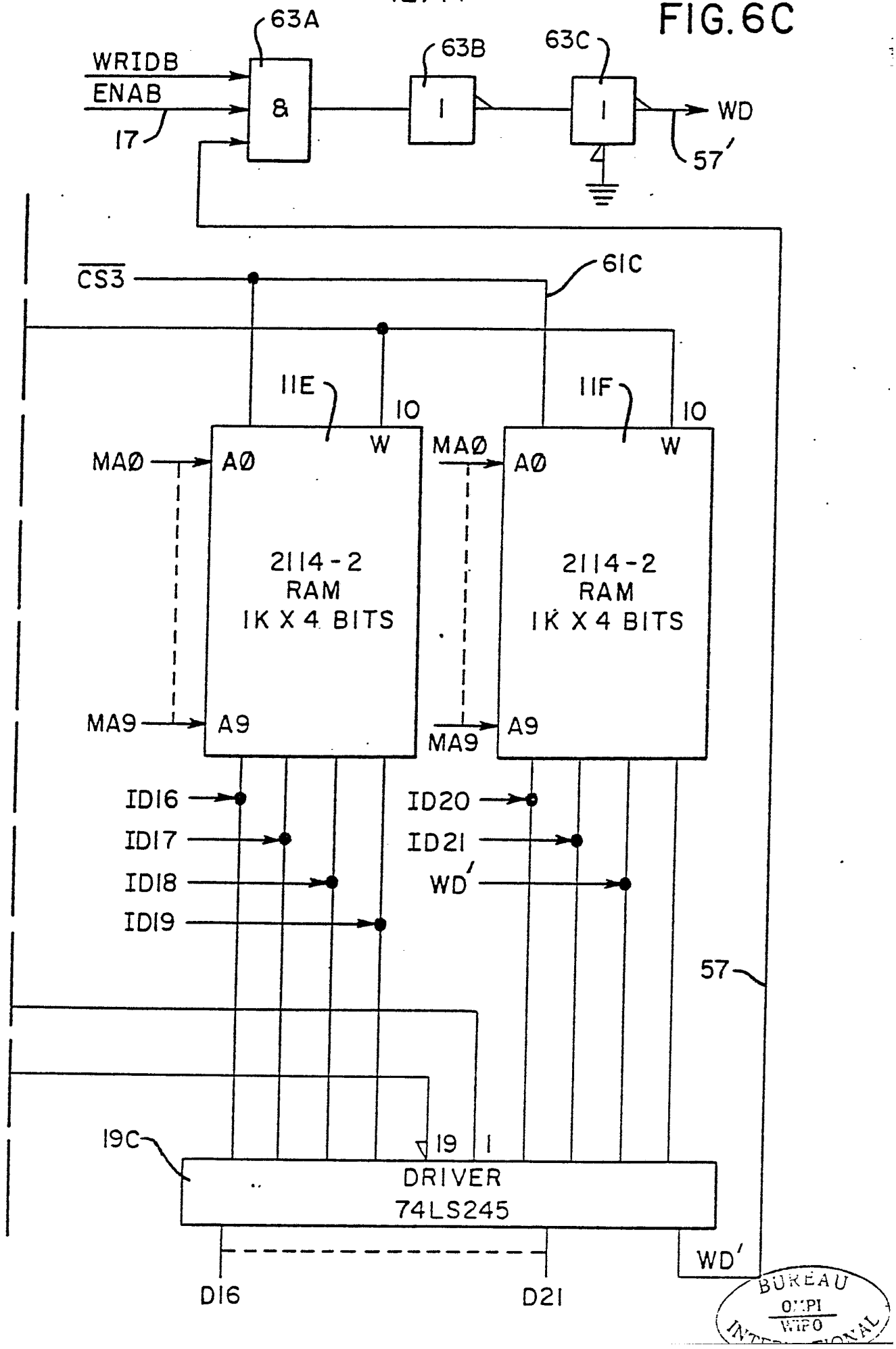
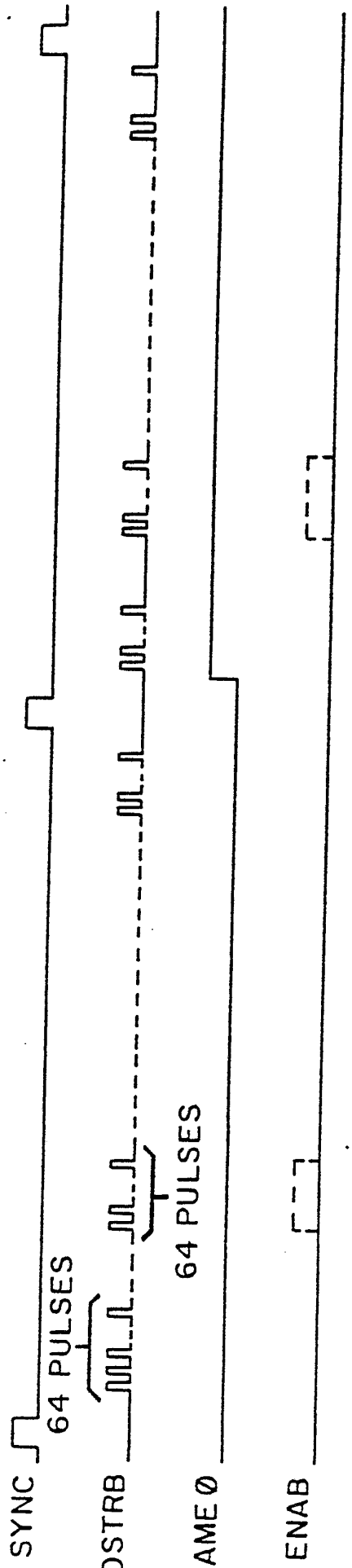


FIG. 7



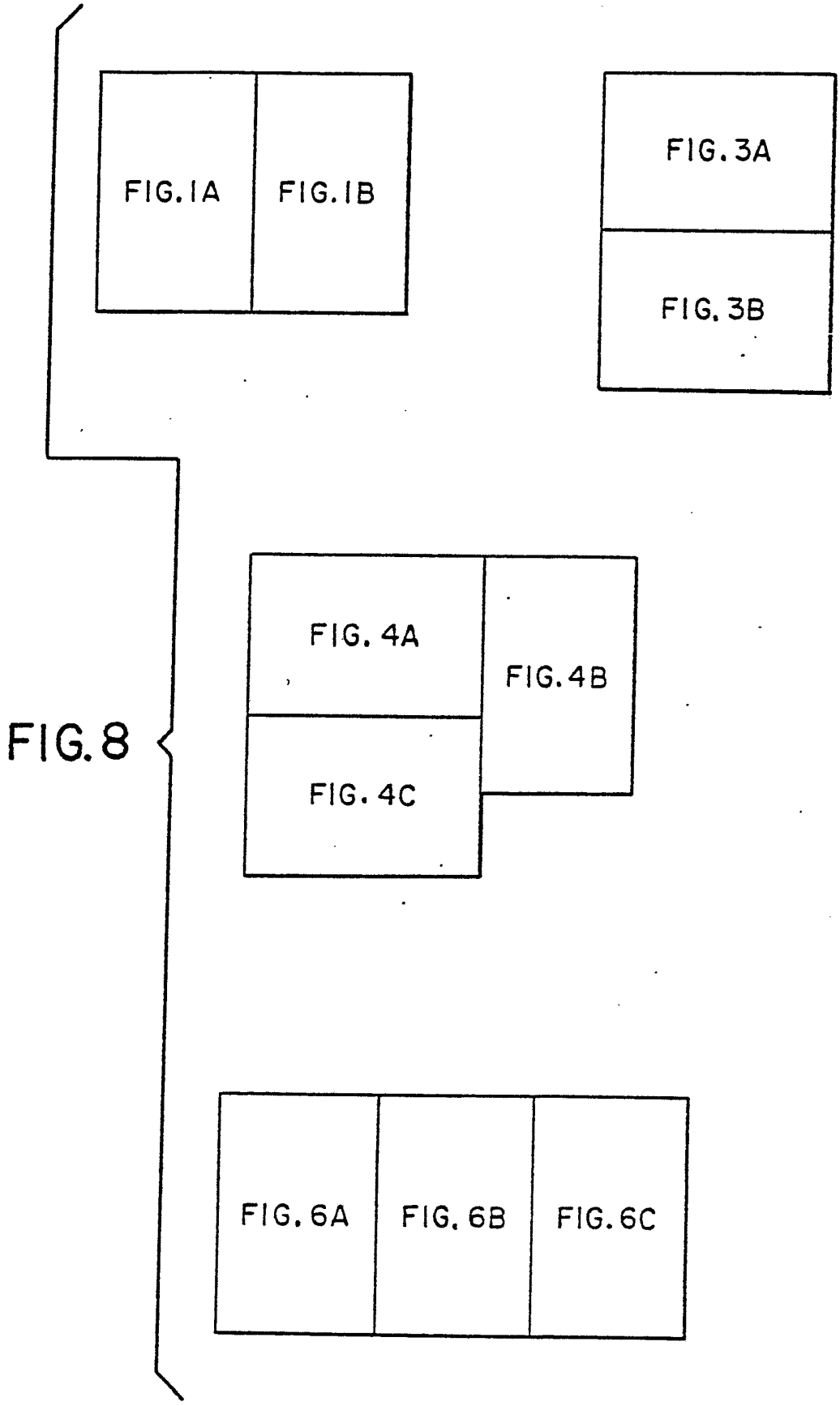


FIG. 8

INTERNATIONAL SEARCH REPORT

International Application No PCT/US81/01431

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.[3] GO 6F. 13/00
U.S. CL. 364/900

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	364/200,900,518,521-22 340/750,798-803 365/73,78,183,222

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	US,A, 3,930,238, Published 30 DECEMBER 1975 Mc Leod, Jr et al----------	--1-7,13-14
p X	US,A, 4,276,609 Published 30 JUNE 1981 Patel----------	--1-14
X	US,A, 4,099,258, Published 4 JULY 1978 Parsons----------	--1-14
A	US,A, 4,117,473, Published 26 SEPTEMBER 1978 Haberger, Jr. et al----------	--1-7,13-14
P X	US,A, 4,290,105 Published 15 SEPTEMBER 1981 CICHELLI et al----------	--1-14
p X	US,A, 4,232,376, Published 4 NOVEMBER 1980 DION et al----------	--1-14
A	US,A, 4,197,590, Published 8 APRIL 1980 SUKONICK et al----------	--1-6

* Special categories of cited documents: [15]

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"L" document cited for special reason other than those referred to in the other categories

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but on or after the priority date claimed

"T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention

"X" document of particular relevance

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
31 DECEMBER 1981	12 JAN 1982
International Searching Authority [1]	**Signature of Authorized Officer** [20]
ISA/US	A.E. WILLIAMS/ G.D. SHAW

Form PCT/ISA/210 (second sheet) (October 1977)