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## METHODS, SYSTEMS, AND APPARATUS TO AGGREGATE RETRANSMISSIONS

This patent arises from a patent application that claims priority to U.S. Provisional Patent Application Serial No. 62/500,333, filed on May 2, 2017. The entirety of U.S. Provisional Patent  
5 Application Serial No. 62/500,333 is incorporated herein by reference.

### TECHNICAL FIELD

This disclosure generally relates to wireless communications and, more particularly, to methods, systems, and apparatus to aggregate retransmissions.

### BACKGROUND

10 Many locations provide wireless fidelity (Wi-Fi) to connect Wi-Fi enabled devices to networks such as the Internet. Wi-Fi enabled devices include personal computers, video-game consoles, mobile phones and devices, digital cameras, tablets, smart televisions, digital audio players, etc. Wi-Fi allows the Wi-Fi enabled devices to wirelessly access the Internet via a wireless local area network (WLAN). To provide Wi-Fi connectivity to a device, a Wi-Fi access  
15 point transmits a radio frequency Wi-Fi signal to the Wi-Fi enabled device within the access point (e.g., a hotspot) signal range. Wi-Fi is implemented using a set of media access control (MAC) and physical layer (PHY) specifications (e.g., such as the Institute of Electrical and Electronics Engineers (IEEE) 802.11 protocol).

Wireless communications facilitate an exchange of data (e.g., aggregate data units) from  
20 a first device (e.g., an originator station or access point) to a second device (e.g., a responder station). Aggregate data units include one or more data units (e.g., frames) corresponding to a particular order. During transmission of the aggregate data by an originator, unit one or more of the frames may be lost. Accordingly, upon receipt of an aggregate data unit, the responder transmits a response (e.g., acknowledgement) identifying which of the frames were received.

25 The originator, based on the response, determines how to resend the lost frames.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an illustration of an example originator station (STA) used herein to aggregate

retransmissions.

FIG. 2 is a block diagram of an example originator upper layer and an example originator lower layer of the example originator station of FIG. 1.

FIG. 3 is a communication diagram of a wireless transmission of aggregated data units  
5 using a conventional technique.

FIG. 4 is a communication diagram of a wireless transmission of aggregate data units between the example originator STA and the example responder STA of FIG. 1.

FIG. 5 is a flowchart representative of example machine readable instructions that may be executed to implement the example originator upper layer and/or originator lower layer of FIG. 1  
10 to retransmit one or more data units.

FIG. 6 is a block diagram of an example radio architecture of FIG. 1 in accordance with some embodiments.

FIG. 7 is a block diagram of an example processor platform that may be utilized to execute the example instructions of FIG. 5 implement the example originator upper layer and/or  
15 originator lower layer of FIG. 2.

The figures are not to scale. Wherever possible, the same reference numbers will be used throughout the drawing(s) and accompanying written description to refer to the same or like parts.

## DETAILED DESCRIPTION

20 Various locations (e.g., homes, offices, coffee shops, restaurants, parks, airports, etc.) may provide Wi-Fi to Wi-Fi enabled devices (e.g., stations (STA)) to connect the Wi-Fi enabled devices to the Internet, or any other network, with minimal hassle. The locations may provide one or more Wi-Fi access points (APs) to output Wi-Fi signals to the Wi-Fi enabled device within a transmission range of the Wi-Fi signals (e.g., a hotspot). A Wi-Fi AP is structured to  
25 wirelessly connect a Wi-Fi enabled device to the Internet through a wireless local area network (WLAN) using Wi-Fi protocols (e.g., such as IEEE 802.11). The Wi-Fi protocol is the protocol by which the AP communicates with the STAs to provide access to the Internet by transmitting uplink (UL) transmission data and receiving downlink (DL) transmission data to/from the Internet.

When a first wireless transmission device (e.g., an originator) transmits data wireless communication to a second wireless transmission device (e.g., a responder), the originator transmits data units (e.g., a frame or a Media Access Control (MAC) frame) corresponding to a particular sequence, or order. Each data unit (e.g., data packet) includes the corresponding  
5 sequence number so that the responder can organize the received data units. In response to receiving the data unit, the responder transmits a response (e.g., an acknowledgement) verifying that the data unit was received. After the response is received from the responder, the originator may transmit a subsequent data unit if that data unit was not identified in the acknowledgement (e.g., the data unit was lost or corrupted during transmission).

10 To improve the efficiency of such a wireless communication system, aggregation may be used. Aggregation includes generating an aggregate data unit (e.g., a MAC Protocol Data Units (MPDUs)), which is a grouping of multiple data units/packets. In this manner, the originator can send multiple data units at a time, thereby increasing the speed and efficiency of the wireless communication system. When the responder receives an aggregate data unit, the responder  
15 determines which data units are included in the aggregate data unit and transmits a response including the sequence numbers (or other identifier) corresponding to the received data units. In some examples, however, one or more of the data units in the aggregate data unit may be lost during transmission (e.g., not received by the responder). In such examples, the originator will receive a response that identifies only the received response and does not include the lost data  
20 units. Examples disclosed here describe an efficient retransmission process of lost data units during transmission. Using examples disclosed herein, the speed of wireless transmission is increased, and the cost and size of local memory in an originator is decreased.

Conventional techniques for retransmission of data units that were not received by a responder are outlined below and in conjunction with FIG. 3. Conventional techniques include  
25 generating a first aggregate data unit including one or more data units and forwarding the first aggregate data unit to a lower layer buffer of a lower layer (e.g., a physical (PHY) layer) of the station. The lower layer then transmits the first aggregate data unit to the responder (e.g., via an antenna). Because it takes time to receive a response from the responder, the lower layer may receive a second aggregate data unit prior to receiving the response acknowledges the first  
30 aggregate data unit. Accordingly, conventional techniques include storing the second aggregate

data unit in the lower layer buffer with the first aggregate data unit. Additionally, more aggregate data units may be received by the lower layer prior to the first response (e.g., acknowledgement of the first packet from the responder). Accordingly, conventional techniques include the additional aggregate data units also being stored in the lower layer buffer. When the response is received, the lower layer analyzes the response to verify that the response identifies all the data units of the first aggregate data unit (e.g., to determine which data unit, if any, where not received by the responder). If the response identifies all of the data units of the first aggregate data unit, the lower layer removes the data units corresponding to the first aggregate data unit from the lower layer buffer and transmits the second aggregate data unit. If the response does not identify all the data units of the first aggregate data unit, the lower layer removes the data units identified in the response and includes the data units not identified in the response (e.g., stored in the lower layer buffer) in the second aggregate data unit. Such conventional techniques require a large lower layer buffer sufficiently sized to hold data units from multiple aggregate data units while the lower layer waits for a response from the responder. Additionally, the entire transmission process is dependent on the response time, because each transmission is sent after a response is received. Examples disclosed herein alleviate the problems of conventional retransmission techniques, thereby facilitating a reduction in the size of the lower layer buffer. In some examples, the size of the lower layer buffer may correspond to one aggregate data unit, which significantly increases the speed of transmission.

Examples disclosed herein include a first layer (e.g., an upper layer, MAC layer, etc.) to generate first aggregate data unit and forward the first aggregate data unit to a lower layer (e.g., a lower layer, PHY layer, etc.). The lower layer stores the first aggregate data unit in a lower layer buffer. In response to the first aggregate data unit being stored in the lower layer buffer, the lower layer transmits the first aggregate data unit to the responder. When the upper layer generates a second aggregate data unit and forwards the second aggregate data unit to the lower layer, the lower layer removes the first aggregate data from the lower layer buffer and stores the second aggregate data unit in the lower layer buffer. Examples disclosed herein allow the upper layer to resend data packets to the lower layer based on an identification of a lost packet from the acknowledgment. Thus, the lower layer buffer does not need to keep transmitted data packets in the lower layer buffer, because if a packet is lost, the upper layer and retransmit the lost packet to

the lower layer for a subsequent data transmission. In this manner, the lower layer buffer is sized to the maximum aggregate data unit size and does not need to store more data than the size of the data corresponding to single aggregate data unit. In response to storing the second aggregate data unit in the lower layer buffer, the lower layer transmits the second aggregate data unit to the responder, regardless of whether or not the response has been received. If the upper layer generates more aggregate data units before the response is received, this process is repeated.

In some examples, once the response is received, the lower layer forwards the response to the upper layer for the upper layer to identify any lost data unit(s) (e.g., data units of the first aggregate data unit not received by the responder and not included in the response). The upper layer then generates a subsequent aggregate data unit including the lost data unit(s) and/or any subsequent data units still to be sent. In some examples, the lower layer analyzes the response and identifies the lost data unit(s) and transmits a request to the upper layer to retransmit the lost data unit(s). Additionally, examples disclosed herein correspond to a faster communication protocol than conventional techniques, because the lower layer does not wait for a response before sending a subsequent data unit. Each subsequent response corresponding to a subsequent aggregate data unit is processed in a similar manner. In this manner, example wireless transmission techniques disclosed herein are fluid and are not stalled by the duration it takes to receive a response. Additionally, because the data units in lower layer buffer of examples disclosed herein are removed when a subsequent aggregate data unit is received, the size of the lower layer buffer can be reduced thereby saving space, cost, and complexity of wireless transmission devices.

FIG. 1 illustrates an example originator STA 100 to aggregate retransmissions. FIG. 1 includes the example originator STA 100, example radio architecture 102a-b, an example originator lower layer 104 and an example originator upper layer 106, an example responder STA 108, an example responder lower layer 110, and an example responder upper layer 112. Although the example of FIG. 1 includes one originator STA 100 and one responder STA 108, the originator STA 100 may communicate with any number of STAs.

The example originator STA 100 and the example responder STA 108 of FIG. 1 are Wi-Fi enabled computing devices. The example originator STA 100 and/or the example responder STA 108 may be, for example, a computing device, a portable device, an access point, a server, a

mobile device, a mobile telephone, a smart phone, a tablet, a gaming system, a digital camera, a digital video recorder, a television, a set top box, an e-book reader, and/or any other Wi-Fi device. If the example originator STA 100 is an AP, the example originator STA 100 may be a router, a modem-router, a receiver, and/or any other devices that provide a wireless connection to a network (e.g., a wide area network, the Internet, etc.).

The example originator STA 100 of FIG. 1 transmits aggregate data units during a transmission opportunity to the example responder STA 108. The aggregate data units correspond to four data packets, for example, each data packet corresponding to a sequential number (SN) (e.g., a first aggregate data unit may include data packets corresponding to SNs 1, 2, 3, 4, a second aggregate data unit may include data packets corresponding to SNs 5, 6, 7, 8, etc.). The example responder STA 108 receives the aggregate data unit and stores the received data packets corresponding to the sequential number. The example responder STA 108 transmits a response (e.g., an acknowledgement (ACK) or a block ACK (BA)) corresponding to the data packets that the example responder STA 108 received. In this manner, the example originator STA 100 can process the response and determine if any packet was lost (e.g., corrupted or not received)) during transmission. If a packet was lost, the example originator STA 100 retransmits the lost data packets in a subsequent aggregate data unit. A conventional retransmission protocol of the originator STA 100 and the example responder STA 108 is further described below in conjunction with FIG. 3 and an example retransmission protocol is further described below in conjunction with FIG. 4.

The example originator STA 100 of FIG. 1 includes the example radio architecture 102a, the example originator lower layer 104, and the example originator upper layer 106. The example radio architecture 102a transmits/receives data packets to/from the example responder STA 108. The example radio architecture 102a of FIG. 1 corresponds to the components of the example originator STA 100 capable of communicating using a Wi-Fi protocol. The example radio architecture 102a is further described below in conjunction with FIG. 6.

The example originator lower layer 104 of FIG. 1 transmits data units, aggregate data units, and/or responses to the example responder STA 108 and/or receives data units, aggregate data units, and/or responses from the example responder STA 108 via the example radio architecture 102a. For example, the originator lower layer 104 may be a physical layer (PHY).

The example originator lower layer 104 includes a lower layer buffer to store data units received from the example originator upper layer 106 prior to transmitting via the example radio architecture 102a. In some examples, the buffer is size to correspond to the space needed to store the data units of an aggregate data unit. The example originator lower layer 104 is further  
5 described below in conjunction with FIG. 2.

The example originator upper layer 106 of FIG. 1 generates aggregate data units for transmission via the radio architecture 102a. For example, the originator upper layer 106 may be the media access control (MAC) layer. The example originator upper layer 106 interfaces with memory (e.g., volatile memory and/or non-volatile memory of the originator STA 100) to gather  
10 data units to generate the aggregate data units. The originator upper layer 106 transmits the aggregate data units to the example originator lower layer 104. In some examples, the receives responses and/or other signals identifying which data units were received by the responder STA 108 in response to an aggregate data unit transmission. The originator upper layer 106 analyzes the response to determine which data units were not received and generates a subsequent  
15 aggregate data unit including the lost data unit and/or additional data units by gathering the lost data units from memory. The example originator upper layer 106 is further described below in conjunction with FIG. 2.

The example responder STA 108 of FIG. 1 includes the example radio architecture 102b to transmit/receive data packets to/from the example responder STA 108. The example radio  
20 architecture 102b of FIG. 1 corresponds to the components of the example responder STA 108 capable of communicating using a Wi-Fi protocol. The example radio architecture 102b is further described below in conjunction with FIG. 6. The example responder STA 108 further includes the example responder lower layer 110 to receive data packets and store the received data packets in a lower layer buffer until the one or more of the received data packets have been  
25 organized in order in the lower layer buffer. For example, if the responder lower layer 110 receives packets 1, 2, 3, and 4, in order, then the example responder lower layer 110 transmits the ordered packets to the example responder upper layer 112 for further processing. If the responder lower layer 110 receives packets 1, 2, and 4, then the responder lower layer 110 transmits the ordered packets 1 and 2 to the responder upper layer 112 but keeps the packet 4 in  
30 the buffer until the packet 3 is received. Additionally, the responder lower layer 110 instructs the

radio architecture 102b to transmit responses (e.g., acknowledgements (ACKs)) corresponding to which data packets have been received.

FIG. 2 is a block diagram of the example originator lower layer 104 and the example originator upper layer 106 of FIG. 1. The example originator upper layer 106 includes an example data transmission controller 200 and an example interface 202. The example originator lower layer 104 includes an example interface 204, an example packet processor 206, and an example lower layer buffer 208.

The example data transmission controller 200 of the originator upper layer 106 of FIG. 2 generates aggregate data units corresponding to data packet units to be transmitted to the example responder STA 108. The data transmission controller 200 may generate aggregate data units based on any number of data packets per aggregate data unit (e.g., based on initial communications between the STAs 100, 108, and/or user/manufacturer preferences). Additionally, the example data transmission controller 200 processes received responses from the example responder STA 108 to determine if the data transmission controller 200 needs to generate a subsequent aggregate data unit including a lost data unit (e.g., a data unit that was transmitted to the responder STA 108 but not identified in a response). In some examples, the example originator lower layer 104 determines that a unit(s)/packet(s) was lost and instructs the example data transmission controller 200 to generate a subsequent aggregate data unit including the lost data unit(s).

The example interface 202 of the originator upper layer 106 of FIG. 2 transmits generated aggregate data units generated by the example data transmission controller 200 to the example originator lower layer 104 (e.g., via the example interface 204). Additionally, the example interface 202 may receive responses from the responder STA 108 (e.g., via the example originator lower layer 104) identifying the received data packets. Additionally, the example interface 202 may receive retransmission instructions from the example originator lower layer 104.

The example interface 204 of the originator lower layer 104 of FIG. 2 receives aggregate data units from the example originator upper layer 106. Additionally, the example interface 204 transmits aggregate data units based on the data stored in the example lower layer buffer 208 to the example responder STA 108, via the example radio architecture 102a. The example interface

204 also receives response(s) from the example responder STA 108 (e.g., via the example radio architecture 102a) and forwards the response(s) to the example originator upper layer 106 to determine if there is a lost packet that needs to be resubmitted in a subsequent aggregate data unit.

5           The example packet processor 206 of the originator lower layer 104 of FIG. 2 stores data packets into the example lower layer buffer 208. When an aggregate data unit is to be sent to the example responder STA 108, the example packet processor 206 generates the aggregate data unit from the data packets stored in the example lower layer buffer 208 and instructs the example interface 204 to transmit the aggregate data unit via the example radio architecture 102a.

10          Additionally, the example packet processor 206 determines if subsequent data packets have been received from the example originator upper layer 106 via the example interface 204. If the example packet processor 206 determines that subsequent data packets have been received from the example originator upper layer 106, the example packet processor 206 discards the packets stored in the example lower layer buffer 208 and stores the newly received data packets. In some  
15          examples, the packet processor 206 processes responses from the example responder STA 108 to identify lost packets. In such examples, the packet processor 206 may transmit instructions (e.g., via the example interface 204) to the example originator upper layer 106 to generate a subsequent aggregate data unit including the lost packet.

20           The example lower layer buffer 208 of the originator lower layer 104 of FIG. 2 stores the data packets of the aggregate data units from the example originator upper layer 106. As described above, the example lower layer buffer 208 is sized to accommodate (e.g., store) the exact number of data packets corresponding to the number of data packets in the aggregate data unit. For example, if the example originator STA 100 generates aggregate data units  
25          corresponding to four data packets per aggregate data unit, the example lower layer buffer 208 is structured to store four data packets, thereby conserving the size of lower layer memory necessary to wireless communicate with the example responder STA 108.

30          FIG. 3 is a communication diagram of a wireless transmission of aggregate data units using conventional techniques. FIG. 3 includes an example originator upper layer 106, an example originator lower layer 104, an example responder lower layer 110, and an example responder upper layer 112. FIG. 3 further includes example aggregate data units 302, 304, 308,

312 and example responses 306, 310, 314. In the illustrated example, the maximum number of data units per aggregate data unit is four. Alternatively, the maximum number of data units per aggregate data unit may be any number that the example STAs 100, 108 are capable of handling.

As illustrated in the example of FIG. 3, the example originator lower layer 104 receives a  
5 first example aggregate data unit 302 (e.g., a MPDU) from the example originator upper layer 106 including data units/packets corresponding to sequence numbers 1, 2, 3, and 4. The example originator lower layer 104 stores the data units in the example lower layer buffer 208 and transmits the first aggregate data unit 304 to the example responder lower layer 110 (e.g., via the example radio architecture 102a). Prior to the example responder lower layer 110 transmitting a  
10 response identifying the received data units (e.g., the first example response 306), the example originator lower layer 104 receives the example second aggregate data unit 305 from the example originator upper layer 106 including data units corresponding to sequence numbers 5, 6, 7, and 8. Because the originator lower layer 104 does not yet know what data units were received by the example responder lower layer 110, the originator lower layer 104 stores the data  
15 units corresponding to the second aggregate data unit 305 into the lower layer buffer 208 with the data units corresponding to the first data aggregate unit 302. Accordingly, the size of the example lower layer buffer 208 associated with conventional techniques needs to be sufficient to handle multiple data units from multiple aggregate data units.

Once the response (e.g., the first example response 306) from the example responder  
20 lower layer 110 is received, the example originator lower layer 104 determines that, based on the response 306, the data unit corresponding to sequence number 3 was not received. Accordingly, the example originator lower layer 104 transmits the example second aggregate data unit 308 with the data units corresponding to sequence numbers 3, 5, 6, and 7. Once the responder lower layer 110 transmits the example second response 310 identifying that data units corresponding to  
25 sequence number 3, 5, 6, and 7 have been received, the example originator lower layer 104 removes the data units corresponding to the second response 310 from the lower layer buffer 208 and transmits the last remaining data unit (e.g., the third example aggregate data unit 312) in the lower layer buffer 208 (e.g., corresponding to sequence number 8) to the example responder lower layer 110. The example responder lower layer 110 responds with the third example  
30 response 314, identifying that the data unit corresponding to sequence number 8 has been

received. Accordingly, the example originator lower layer 104 removes the final data unit corresponding to the sequence number 8 from the example lower layer buffer 208. FIG. 4 illustrates a communication diagram using examples disclosed herein that decreases the maximum size of the lower layer buffer 208 and reduces the time and number of transmissions that the above conventional technique.

FIG. 4 is a communication diagram of a wireless transmission of aggregate data units between a first radio architecture and a second radio architecture. FIG. 4 includes an example originator upper layer 106, an example originator lower layer 104, an example responder lower layer 110, an example responder upper layer 112, and example times 1-14. FIG. 4 further includes aggregate data units 402, 404, 406, 408, 412, 416, 418, 426 and example responses 410, 414, 420, 422, 424, 428. Although the example originator lower layer 104 of FIG. 4 transmits data units 1-8 to the example responder lower layer 110 in aggregate data units of four data units, the example originator lower layer 104 may transmits any number of data units in any sized aggregate data units to the example responder lower layer 110.

At time 1, the example originator upper layer 106 transmits the first example aggregate data unit 402 (e.g., a MPDU) to the example originator lower layer 104 to be stored in the example lower layer buffer 208 of the originator lower layer 104. An aggregate data unit includes multiple data units (e.g., field frames) corresponding to a particular sequence. In the illustrated example of FIG. 4, the first aggregate data unit 402 includes data units corresponding to sequence numbers (SN) 1, 2, 3, and 4. At time 2, the example originator lower layer 104 stores the received data units (e.g., 1, 2, 3, 4) in the example lower layer buffer 208. Once stored in lower layer buffer 208, the example originator lower layer 104 transmits the first example aggregate data unit 404 (e.g., including the data units 1, 2, 3, and 4) to the example responder lower layer 110 (e.g., via the example radio architecture 102a). In some examples, the originator lower layer 104 stores data in a header of the first aggregate data unit. The data may include, the sequence of the data units, identifiers of the data units, a total number of data units, a total number of data units per aggregate data unit, etc. to help the responder process a received aggregate data unit.

At time 3, the example originator upper layer 106 transmits the second example aggregate data unit 406 including subsequent data units (e.g., corresponding to sequence

numbers 5, 6, 7, and 8). At time 4, the example originator lower layer 104 removes the data units corresponding to sequence numbers 1, 2, 3, and 4 from the example lower layer buffer 208 and stores the data units corresponding to 5, 6, 7, and 8 in the example lower layer buffer 208. The example originator lower layer 104 removes the data units corresponding to the sequence numbers, 1, 2, 3, and 4 from the lower layer buffer 208 at any time between time 2 and time 4. At time 5 (e.g., once stored in the buffer), the example originator lower layer 104 transmits the second aggregate data unit (e.g., including the data units 5, 6, 7, and 8 stored in the lower layer buffer 208) 408 to the example responder lower layer 110.

At time 6, the example responder lower layer 110 stores the received data units (e.g., corresponding to SN 1, 2, and 4) in a responder lower layer buffer. In some examples, the responder lower layer 110 processes the first aggregate data unit 404 to identify a sequence corresponding to the received data units and/or a number of data units included in the first aggregate data unit 404, to determine if one or more of the received data units is missing (e.g., lost). In some examples, the responder lower layer 110 analyzes the aggregate data header to determine the sequence and/or number of the data units. The example responder lower layer 110 determines that the data unit corresponding to sequence number 3 is missing. Accordingly, the example responder lower layer 110 removes the aggregate data units corresponding to the sequence number of 1 and 2 and transmits the example aggregate data unit 412 including the first two data units (1 and 2). The example responder lower layer 110 keeps the data unit corresponding to the sequence number of 4 in the responder lower layer buffer. Additionally, at time 6, the example responder lower layer 110 transmits the first example response 410 (e.g., acknowledgment or a block acknowledgement) identifying the received data units (e.g., the data units corresponding to sequence numbers 1, 2, and 4.) to the example originator lower layer 104.

At time 7, the example originator lower layer 104 receives the example response 410 from the example responder lower layer 110. The example originator lower layer 104 forwards the example response 414 (e.g., identifying the received data units corresponding to sequence numbers 1, 2, and 4) to the example originator upper layer 106. In this manner, the example originator upper layer 106 identifies that the data unit corresponding to sequence number 3 was not received and includes the data unit corresponding to sequence number 3 in the next (e.g., third) example aggregate data unit 416. Alternatively, the example originator lower layer 104

may process the response and instruct the example originator upper layer 106 to include the lost data packet in a subsequent aggregate data unit. In some examples (e.g., when there are additional sequential data units to transmit to the example responder lower layer 110), the example originator upper layer 106 includes the data unit corresponding to the sequence number 3 with other sequential data units for the third aggregate data unit 416. In some examples (e.g., when there are no additional sequence data units to transmit), the example originator upper layer 106 includes the lost data units (e.g., SN 3) from the first aggregate data unit 402 and/or any other lost data unit from the example second aggregate data unit 406 (e.g., if identified from a second response).

At time 8, the example originator upper layer 106 transmits the example third aggregate data 416 including the lost data unit (e.g., the data unit not identified in the first response) to the example originator lower layer 104. At time 9, the example originator lower layer 104 removes the data units corresponding to the sequence numbers 5, 6, 7, and 8 from the lower layer buffer 208 and stores the data unit corresponding to the sequence number 3 in the example lower layer buffer 208. At time 10 (e.g., once stored in the lower layer buffer 208), the example originator lower layer 104 transmits the example third aggregate data 418 (e.g., corresponding to the data unit with sequence number 3) to the example responder lower layer 110.

At time 11, the example responder lower layer 110 receives the example second aggregate data unit 408 and stores the corresponding data units (e.g., data units with sequence numbers 4, 5, 6, 7, and 8) in a lower layer buffer of the responder STA 108. In some examples, because the responder lower layer 110 determines that the data unit with sequence number 3 has not yet been received, the responder lower layer 110 may keep adding the data units in the responder lower layer buffer until the sequence number 3 data unit is received (e.g., to organize the data units according to the sequence order). In some examples, the responder lower layer 110 may transmit the data units to the example responder upper layer 112 while identifying that the 3<sup>rd</sup> data unit has not been received. In this manner, the example responder upper layer 112 may reserve memory for the 3<sup>rd</sup> data unit in sequential order to the other data units. Additionally at time 11, the example responder lower layer 110 transmits the example second response 420 identifying the received data units (e.g., the data units corresponding to sequence numbers 5, 6, 7, and 8).

At time 12, the example originator lower layer 104 receives the example second response 420 and transmits (e.g., forwards) the example second response 422 to the example originator upper layer 106. In this manner, the example originator upper layer 106 may determine if any data units were lost to further generate subsequent aggregated data units including such lost data units. Alternatively, the example originator lower layer 104 may determine the lost packets based on the response and instruct the example originator upper layer 106 accordingly. At time 13, the example responder lower layer 110 receives the third example aggregate data unit 418 and stores the data unit corresponding to sequence number 3 in the responder lower layer buffer. The example responder lower layer 110 reorganizes the data units stored in the responder lower layer buffer according to the determined sequence (e.g., stored header of any one of the first, second, or third aggregate data units). After reorganizing, the example responder lower layer 110 transmits the example aggregate data unit 426 corresponding to the data units in the buffer (e.g., data units corresponding to sequence numbers 3, 4, 5, 6, 7, and 8) to the example responder upper layer 112 in the order corresponding to the sequence. Additionally, at time 13, the example responder lower layer 110 transmits the example third response 424 identifying that the data unit corresponding to sequence number 3 was received. At time 14, the example originator lower layer 104 receives the example response 424 and forwards the example response 428 to the example originator upper layer 106.

While an example manner of implementing the example originator lower layer 104 and/or the example originator upper layer 106 of FIG. 1 is illustrated in FIG. 2, one or more of the elements, processes and/or devices illustrated in FIG. 2 may be combined, divided, re-arranged, omitted, eliminated and/or implemented in any other way. Further, the example data transmission controller 200, the example interface 202, the example interface 204, the example packet processor 206, the example lower layer buffer 208, and/or, more generally, the example originator lower layer 104 and/or the example originator upper layer 106 of FIG. 2 may be implemented by hardware, software, firmware and/or any combination of hardware, software and/or firmware. Thus, for example, any of the example data transmission controller 200, the example interface 202, the example interface 204, the example packet processor 206, the example lower layer buffer 208, and/or, more generally, the example originator lower layer 104 and/or the example originator upper layer 106 of FIG. 2 could be implemented by one or more

analog or digital circuit(s), logic circuits, programmable processor(s), programmable controller(s), graphics processing unit(s) (GPU(s)), digital signal processor(s) (DSP(s)), application specific integrated circuit(s) (ASIC(s)), programmable logic device(s) (PLD(s)) and/or field programmable logic device(s) (FPLD(s)). When reading any of the apparatus or  
5 system claims of this patent to cover a purely software and/or firmware implementation, at least one of the example data transmission controller 200, the example interface 202, the example interface 204, the example packet processor 206, the example lower layer buffer 208, and/or, more generally, the example originator lower layer 104 and/or the example originator upper layer 106 of FIG. 2 is/are hereby expressly defined to include a non-transitory computer readable  
10 storage device or storage disk such as a memory, a digital versatile disk (DVD), a compact disk (CD), a Blu-ray disk, etc. including the software and/or firmware. Further still, the example originator lower layer 104 and/or the example originator upper layer 106 of FIG. 1 may include one or more elements, processes and/or devices in addition to, or instead of, those illustrated in FIG. 2, and/or may include more than one of any or all of the illustrated elements, processes and  
15 devices. As used herein, the phrase “in communication,” including variations thereof, encompasses direct communication and/or indirect communication through one or more intermediary components, and does not require direct physical (e.g., wired) communication and/or constant communication, but rather additionally includes selective communication at periodic intervals, scheduled intervals, aperiodic intervals, and/or one-time events.

20 A flowchart representative of example hardware logic or machine readable instructions for implementing the example originator lower layer 104 and/or the example originator upper layer 106 of FIG. 1 is shown in FIG. 5. The machine readable instructions may be a program or portion of a program for execution by a processor such as the processor 712 shown in the example processor platform 700 discussed below in connection with FIG. 7. The program may  
25 be embodied in software stored on a non-transitory computer readable storage medium such as a CD-ROM, a floppy disk, a hard drive, a DVD, a Blu-ray disk, or a memory associated with the processor 712, but the entire program and/or parts thereof could alternatively be executed by a device other than the processor 712 and/or embodied in firmware or dedicated hardware. Further, although the example program is described with reference to the flowchart illustrated in  
30 FIG. 5, many other methods of implementing the example originator lower layer 104 and/or the

example originator upper layer 106 may alternatively be used. For example, the order of execution of the blocks may be changed, and/or some of the blocks described may be changed, eliminated, or combined. Additionally or alternatively, any or all of the blocks may be implemented by one or more hardware circuits (e.g., discrete and/or integrated analog and/or digital circuitry, an FPGA, an ASIC, a comparator, an operational-amplifier (op-amp), a logic circuit, etc.) structured to perform the corresponding operation without executing software or firmware.

As mentioned above, the example process of FIG. 5 may be implemented using executable instructions (e.g., computer and/or machine readable instructions) stored on a non-transitory computer and/or machine readable medium such as a hard disk drive, a flash memory, a read-only memory, a compact disk, a digital versatile disk, a cache, a random-access memory and/or any other storage device or storage disk in which information is stored for any duration (e.g., for extended time periods, permanently, for brief instances, for temporarily buffering, and/or for caching of the information). As used herein, the term non-transitory computer readable medium is expressly defined to include any type of computer readable storage device and/or storage disk and to exclude propagating signals and to exclude transmission media.

“Including” and “comprising” (and all forms and tenses thereof) are used herein to be open ended terms. Thus, whenever a claim employs any form of “include” or “comprise” (e.g., comprises, includes, comprising, including, having, etc.) as a preamble or within a claim recitation of any kind, it is to be understood that additional elements, terms, etc. may be present without falling outside the scope of the corresponding claim or recitation. As used herein, when the phrase “at least” is used as the transition term in, for example, a preamble of a claim, it is open-ended in the same manner as the term “comprising” and “including” are open ended. The term “and/or” when used, for example, in a form such as A, B, and/or C refers to any combination or subset of A, B, C such as (1) A alone, (2) B alone, (3) C alone, (4) A with B, (5) A with C, and (6) B with C.

FIG. 5 is an example flowchart 500 representative of example machine readable instructions that may be executed to implement the example originator lower layer 104 and/or the example originator upper layer 106 of FIG. 1 to transmit aggregate data units and/or retransmit aggregate data unit(s) corresponding to lost data units (e.g., data units not identified in

a response from a responder). Although, the flowchart 500 of FIG. 5 is described in conjunction with the example originator lower layer 104 and/or the example originator upper layer 106 in the example originator STA 100 of FIG. 1, the process may be implemented using any type of lower layer, upper layer, and/or any type of STA.

At block 502, the example interface 204 of the example originator lower layer 104 receives a first aggregate data unit from the example interface 202 of the example originator upper layer 106. As described above in conjunction with FIG. 2, the aggregate data unit includes one or more data units. In some examples, the one or more data units correspond to a particular order (e.g., sequence). The example data transmission controller 200 generates the aggregate data unit and instructs the example interface 202 to transmit the aggregate data unit including the sequence numbers of each data packet of the aggregate data unit to the example originator lower layer 104.

At block 504, the example packet processor 206 stores the first aggregate data unit (e.g., the data units corresponding to the first aggregate data unit) in the example lower layer buffer 208. At block 506, the example interface 204 transmits the first aggregate data unit to the example responder STA 108. At block 508, the example packet processor 206 determines if a second aggregate data unit from the example originator upper layer 106 has been received via the example interface 204. If the example packet processor 206 determines that the second aggregate data has not been received (block 508: NO), the process continues to block 514. If the example packet processor 206 determines that the second aggregate data has been received (block 508: YES), the example packet processor 206 removes the first aggregate data unit from the example lower layer buffer 208 and stores the second aggregate data unit in the example lower layer buffer 208 (block 510). At block 512, the example interface 204 transmits the second aggregate data unit to the responder STA 108.

At block 514, the example packet processor 206 determines if a response corresponding to the first aggregate data unit from response has been received via the example interface 204. As described above in conjunction with FIG. 1, the example responder STA 108 transmits a response identifying the received data units. In this manner, the example packet processor 206 can determine if any of the data units were lost during transmission. If the example packet processor 206 determines that the response corresponding to the first aggregate data unit has not

been received (block 514: NO), the process returns to block 508. In this manner, the example originator lower layer 104 continues to transmit subsequent aggregate data units received from the example originator upper layer 106 (e.g., generated by the example data transmission controller 200). If the example packet processor 206 determines that the response corresponding to the first aggregate data unit has been received (block 514: YES), the example interface 204 forwards the response to the example interface 202 and the example data transmission controller 200 analyzes the response to determine if a subset of the first aggregate data unit not identified in the response (block 516).

At block 518, the example data transmission controller 200 determines if the response identifies all the data units of the first aggregate data unit. If the example data transmission controller 200 determines that the response identifies all the data units of the first aggregate data unit (block 518: YES), the process returns to block to block 508 to continue transmitting subsequent aggregate data units. If the example data transmission controller 200 determines that the response does not identify all the data units of the first aggregate data unit (block 518: NO), the example data transmission controller 200 instructs example originator lower layer 104 (e.g., via the example interface 202) to remove the first or second aggregate data unit from the example lower layer buffer 208 and store third aggregate data unit including the subset of the first aggregate data unit not identified in the response into the example lower layer buffer 208 (block 520). The example interface 202 of the example originator upper layer 106 transmits the third aggregate data unit to the example interface 204 of the example originator lower layer 104. In some examples, the example data transmission controller 200 includes subsequent data units with the one or more data units not included in the response to be part of the third aggregate data unit.

At block 522, the example interface 204 transmits the third aggregate data unit to the responder STA 108. At block 524, the example packet processor 206 determines if a subsequent data unit has been received via the example interface 204 from the example interface 202 of the example originator upper layer 106. If the example packet processor 206 determines that a subsequent data unit has not been received (block 524: NO), the example packet processor 206 waits until a subsequent data unit is received. If the example packet processor 206 determines that a subsequent data unit has been received (block 524: YES), the example packet processor

206 removes the third aggregate data from the example lower layer buffer 208 (block 526) and the process returns to block 504 to store the subsequent aggregate data unit.

FIG. 6 is a block diagram of a radio architecture 102a-b in accordance with some embodiments that may be implemented in the example originator STA 100 and/or the example responder STA 108. Radio architecture 102a-b may include radio front-end module (FEM) circuitry 604a, 604b, radio IC circuitry 606a, 606b and baseband processing circuitry 608a, 608b.

5 Radio architecture 102a-b as shown includes both Wireless Local Area Network (WLAN) functionality and Bluetooth (BT) functionality although embodiments are not so limited. In this disclosure, “WLAN” and “Wi-Fi” are used interchangeably.

FEM circuitry 604a, 604b may include a WLAN or Wi-Fi FEM circuitry 604a and a Bluetooth (BT) FEM circuitry 604b. The WLAN FEM circuitry 604a may include a receive  
10 signal path comprising circuitry configured to operate on WLAN RF signals received from one or more antennas 601, to amplify the received signals and to provide the amplified versions of the received signals to the WLAN radio IC circuitry 606a for further processing. The BT FEM circuitry 604b may include a receive signal path which may include circuitry configured to  
15 operate on BT RF signals received from one or more antennas 601, to amplify the received signals and to provide the amplified versions of the received signals to the BT radio IC circuitry 606b for further processing. FEM circuitry 604a may also include a transmit signal path which may include circuitry configured to amplify WLAN signals provided by the radio IC circuitry 606a for wireless transmission by one or more of the antennas 601. In addition, FEM circuitry 604b may also include a transmit signal path which may include circuitry configured to amplify  
20 BT signals provided by the radio IC circuitry 606b for wireless transmission by the one or more antennas. In the embodiment of FIG. 6, although FEM 604a and FEM 604b are shown as being distinct from one another, embodiments are not so limited, and include within their scope the use of an FEM (not shown) that includes a transmit path and/or a receive path for both WLAN and BT signals, or the use of one or more FEM circuitries where at least some of the FEM circuitries  
25 share transmit and/or receive signal paths for both WLAN and BT signals.

Radio IC circuitry 606a, 606b as shown may include WLAN radio IC circuitry 606a and BT radio IC circuitry 606b. The WLAN radio IC circuitry 606a may include a receive signal path which may include circuitry to down-convert WLAN RF signals received from the FEM

circuitry 604a and provide baseband signals to WLAN baseband processing circuitry 608a. BT radio IC circuitry 606b may in turn include a receive signal path which may include circuitry to down-convert BT RF signals received from the FEM circuitry 604b and provide baseband signals to BT baseband processing circuitry 608b. WLAN radio IC circuitry 606a may also  
5 include a transmit signal path which may include circuitry to up-convert WLAN baseband signals provided by the WLAN baseband processing circuitry 608a and provide WLAN RF output signals to the FEM circuitry 604a for subsequent wireless transmission by the one or more antennas 601. BT radio IC circuitry 606b may also include a transmit signal path which may include circuitry to up-convert BT baseband signals provided by the BT baseband processing  
10 circuitry 608b and provide BT RF output signals to the FEM circuitry 604b for subsequent wireless transmission by the one or more antennas 601. In the embodiment of FIG. 6, although radio IC circuitries 606a and 606b are shown as being distinct from one another, embodiments are not so limited, and include within their scope the use of a radio IC circuitry (not shown) that includes a transmit signal path and/or a receive signal path for both WLAN and BT signals, or  
15 the use of one or more radio IC circuitries where at least some of the radio IC circuitries share transmit and/or receive signal paths for both WLAN and BT signals.

Baseband processing circuitry 608a, 608b may include a WLAN baseband processing circuitry 608a and a BT baseband processing circuitry 608b. The WLAN baseband processing circuitry 608a may include a memory, such as, for example, a set of RAM arrays in a Fast  
20 Fourier Transform or Inverse Fast Fourier Transform block (not shown) of the WLAN baseband processing circuitry 608a. Each of the WLAN baseband circuitry 608a and the BT baseband circuitry 608b may further include one or more processors and control logic to process the signals received from the corresponding WLAN or BT receive signal path of the radio IC circuitry 606a, 606b, and to also generate corresponding WLAN or BT baseband signals for the  
25 transmit signal path of the radio IC circuitry 606a, 606b. Each of the baseband processing circuitries 608a and 608b may further include physical layer (PHY) and medium access control layer (MAC) circuitry, and may further interface with the example originator lower layer 104 for generation and processing of the baseband signals and for controlling operations of the radio IC circuitry 606a, 606b based on communications with the example originator upper layer 106 of  
30 the example application processor platform 610.

Referring still to FIG. 6, according to the shown embodiment, WLAN-BT coexistence circuitry 613 may include logic providing an interface between the WLAN baseband circuitry 608a and the BT baseband circuitry 608b to enable use cases requiring WLAN and BT coexistence. In addition, a switch 603 may be provided between the WLAN FEM circuitry 604a and the BT FEM circuitry 604b to allow switching between the WLAN and BT radios according to application needs. In addition, although the antennas 601 are depicted as being respectively connected to the WLAN FEM circuitry 604a and the BT FEM circuitry 604b, embodiments include within their scope the sharing of one or more antennas as between the WLAN and BT FEMs, or the provision of more than one antenna connected to each of FEM 604a or 604b.

In some embodiments, the front-end module circuitry 604a, 604b, the radio IC circuitry 606a-b, and baseband processing circuitry 608a-b may be provided on a single radio card, such as wireless radio card 602. In some other embodiments, the one or more antennas 601, the FEM circuitry 604a, b and the radio IC circuitry 606a, 606b may be provided on a single radio card. In some other embodiments, the radio IC circuitry 606a, 606b and the baseband processing circuitry 608a, 608b may be provided on a single chip or integrated circuit (IC), such as IC 615.

In some embodiments, the wireless radio card 602 may include a WLAN radio card and may be configured for Wi-Fi communications, although the scope of the embodiments is not limited in this respect. In some of these embodiments, the radio architecture 102a-b may be configured to receive and transmit orthogonal frequency division multiplexed (OFDM) or orthogonal frequency division multiple access (OFDMA) communication signals over a multicarrier communication channel. The OFDM or OFDMA signals may comprise a plurality of orthogonal subcarriers.

In some of these multicarrier embodiments, radio architecture 102a-b may be part of a Wi-Fi communication station (STA) such as a wireless access point (AP), a base station or a mobile device including a Wi-Fi device. In some of these embodiments, radio architecture 102a-b may be configured to transmit and receive signals in accordance with specific communication standards and/or protocols, such as any of the Institute of Electrical and Electronics Engineers (IEEE) standards including, 802.11n-2009, IEEE 802.11-2012, IEEE 802.11-2016, 802.11n-2009, 802.11ac, 802.11ah, 802.11ad, 802.11ay and/or 802.11ax standards and/or proposed specifications for WLANs, although the scope of embodiments is not limited in this respect.

Radio architecture 102a-b may also be suitable to transmit and/or receive communications in accordance with other techniques and standards.

In some embodiments, the radio architecture 102a-b may be configured for high-efficiency Wi-Fi (HEW) communications in accordance with the IEEE 802.11ax standard. In  
5 these embodiments, the radio architecture 102a-b may be configured to communicate in accordance with an OFDMA technique, although the scope of the embodiments is not limited in this respect.

In some other embodiments, the radio architecture 102a-b may be configured to transmit and receive signals transmitted using one or more other modulation techniques such as spread  
10 spectrum modulation (e.g., direct sequence code division multiple access (DS-CDMA) and/or frequency hopping code division multiple access (FH-CDMA)), time-division multiplexing (TDM) modulation, and/or frequency-division multiplexing (FDM) modulation, although the scope of the embodiments is not limited in this respect.

In some embodiments, as further shown in FIG. 6, the BT baseband circuitry 608b may  
15 be compliant with a Bluetooth (BT) connectivity standard such as Bluetooth, Bluetooth 9.0 or Bluetooth 8.0, or any other iteration of the Bluetooth Standard. In embodiments that include BT functionality as shown for example in FIG. 8, the radio architecture 102a-b may be configured to establish a BT synchronous connection oriented (SCO) link and or a BT low energy (BT LE) link. In some of the embodiments that include functionality, the radio architecture 102a-b may be  
20 configured to establish an extended SCO (eSCO) link for BT communications, although the scope of the embodiments is not limited in this respect. In some of these embodiments that include a BT functionality, the radio architecture may be configured to engage in a BT Asynchronous Connection-Less (ACL) communications, although the scope of the embodiments is not limited in this respect. In some embodiments, as shown in FIG. 6, the functions of a BT  
25 radio card and WLAN radio card may be combined on a single wireless radio card, such as single wireless radio card 802, although embodiments are not so limited, and include within their scope discrete WLAN and BT radio cards.

In some embodiments, the radio-architecture 102a-b may include other radio cards, such as a cellular radio card configured for cellular (e.g., 5GPP such as LTE, LTE-Advanced or 7G  
30 communications).

In some IEEE 802.11 embodiments, the radio architecture 102a-b may be configured for communication over various channel bandwidths including bandwidths having center frequencies of about 900 MHz, 2.4 GHz, 5 GHz, and bandwidths of about 2 MHz, 4 MHz, 8 MHz, 5.5 MHz, 6 MHz, 8 MHz, 10 MHz, 40 MHz, 9 GHz, 46 GHz, 80 MHz, 100 MHz, 80 MHz (with contiguous bandwidths) or 80+80 MHz (160MHz) (with non-contiguous bandwidths). In some embodiments, a 920 MHz channel bandwidth may be used. The scope of the embodiments is not limited with respect to the above center frequencies however.

FIG. 7 is a block diagram of an example processor platform 700 structured to execute the instructions of FIG. 6 to implement the example originator lower layer 104 and/or the example originator upper layer 106. The processor platform 700 can be, for example, a server, a personal computer, a workstation, a self-learning machine (e.g., a neural network), a mobile device (e.g., a cell phone, a smart phone, a tablet such as an iPad<sup>TM</sup>), a personal digital assistant (PDA), an Internet appliance, a DVD player, a CD player, a digital video recorder, a Blu-ray player, a gaming console, a personal video recorder, a set top box, a headset or other wearable device, or any other type of computing device.

The processor platform 700 of the illustrated example includes a processor 712. The processor 712 of the illustrated example is hardware. For example, the processor 712 can be implemented by one or more integrated circuits, logic circuits, microprocessors, GPUs, DSPs, or controllers from any desired family or manufacturer. The hardware processor may be a semiconductor based (e.g., silicon based) device. In this example, the example processor 712 may implement the example data transmission controller 200 and/or the example packet processor 206.

The processor 712 of the illustrated example includes a local memory 713 (e.g., a cache). The processor 712 of the illustrated example is in communication with a main memory including a volatile memory 714 and a non-volatile memory 716 via a bus 718. The volatile memory 714 may be implemented by Synchronous Dynamic Random Access Memory (SDRAM), Dynamic Random Access Memory (DRAM), RAMBUS® Dynamic Random Access Memory (RDRAM®) and/or any other type of random access memory device. The non-volatile memory 716 may be implemented by flash memory and/or any other desired type of memory device. Access to the main memory 714, 716 is controlled by a memory controller. The example local

memory 713 may be used to implement the example lower layer buffer 208.

The processor platform 700 of the illustrated example also includes an interface circuit 720. The interface circuit 720 may be implemented by any type of interface standard, such as an Ethernet interface, a universal serial bus (USB), a Bluetooth® interface, a near field communication (NFC) interface, and/or a PCI express interface. The example interface circuit 720 may implement the example interface 202 and/or the example interface 204 of FIG. 2.

In the illustrated example, one or more input devices 722 are connected to the interface circuit 720. The input device(s) 722 permit(s) a user to enter data and/or commands into the processor 712. The input device(s) can be implemented by, for example, a keyboard, a button, a mouse, a touchscreen, a track-pad, a trackball, and/or isopoint.

One or more output devices 724 are also connected to the interface circuit 720 of the illustrated example. The output devices 724 can be implemented, for example, by display devices (e.g., a light emitting diode (LED), an organic light emitting diode (OLED), a liquid crystal display (LCD), a cathode ray tube display (CRT), an in-place switching (IPS) display, a touchscreen, etc.), a tactile output device, a printer and/or speaker. The interface circuit 720 of the illustrated example, thus, typically includes a graphics driver card, a graphics driver chip and/or a graphics driver processor.

The interface circuit 720 of the illustrated example also includes a communication device such as a transmitter, a receiver, a transceiver, a modem, a residential gateway, a wireless access point, and/or a network interface to facilitate exchange of data with external machines (e.g., computing devices of any kind) via a network 726. The communication can be via, for example, an Ethernet connection, a digital subscriber line (DSL) connection, a telephone line connection, a coaxial cable system, a satellite system, a line-of-site wireless system, a cellular telephone system, etc.

The processor platform 700 of the illustrated example also includes one or more mass storage devices 728 for storing software and/or data. Examples of such mass storage devices 728 include floppy disk drives, hard drive disks, compact disk drives, Blu-ray disk drives, redundant array of independent disks (RAID) systems, and digital versatile disk (DVD) drives.

The machine executable instructions 732 of FIG. 6 may be stored in the mass storage device 728, in the volatile memory 714, in the non-volatile memory 716, and/or on a removable

non-transitory computer readable storage medium such as a CD or DVD.

Example embodiments described herein provide certain systems, methods, and apparatus to aggregate retransmissions. Example 1 includes an apparatus comprising a lower layer buffer, a processor to store a first aggregate data unit including a first plurality of data units in the lower layer buffer, and an interface to transmit the first aggregate data unit to a responder, the processor to, prior to receiving a first response identifying received data units of the first plurality of data units from the responder remove the first aggregate data unit from the lower layer buffer, and store a second aggregate data unit including a second plurality of data units in the lower layer buffer, and the interface to transmit the second aggregate data unit to the responder, and in response to receiving a second response from the responder, transmit a third aggregate data unit including a subset of the first plurality of data units not identified in the first response.

Example 2 includes the apparatus of example 1, wherein the first plurality of data units corresponds to a first order and the second plurality of data units corresponds to a second order, the second order subsequent the first order.

Example 3 includes the apparatus of example 2, wherein the processor is to embed a sequence order including the first order and the second order in at least one of the first aggregate data unit, the second aggregate data unit, or the third aggregate data unit.

Example 4 includes the apparatus of example 3, wherein the responder is to reorder the first and second plurality of data units based on the sequence order.

Example 5 includes the apparatus of example 1, wherein the first and second plurality of data units are media access control (mac) frames and the first and second aggregate data units are mac protocol data units (mpdus).

Example 6 includes the apparatus of example 1, wherein the interface is to receive the first aggregate data unit from an upper layer at a first time and receive the second aggregate data unit from the upper layer at a second time different than the first time.

Example 7 includes the apparatus of example 1, wherein the interface is to receive a second response identifies data units of the second plurality of data units received by the responder.

Example 8 includes the apparatus of example 7, wherein the interface is to, in response to receiving the second response from the responder, transmit a fourth aggregate data unit including a second subset of the second plurality of data units not identified in the first response.

Example 9 includes the apparatus of example 1, wherein the third aggregate data unit further includes a third plurality of data units.

Example 10 includes a tangible computer readable storage medium comprising instructions which, when executed, cause a machine to at least store a first aggregate data unit including a first plurality of data units in a lower layer buffer, transmit the first aggregate data unit to a responder, prior to receiving a first response identifying received data units of the first plurality of data units from the responder remove the first aggregate data unit from the lower layer buffer, and store a second aggregate data unit including a second plurality of data units in the lower layer buffer, transmit the second aggregate data unit to the responder, and in response to receiving a second response from the responder, transmit a third aggregate data unit including a subset of the first plurality of data units not identified in the first response.

Example 11 includes the computer readable storage medium of example 10, wherein the first plurality of data units corresponds to a first order and the second plurality of data units corresponds to a second order, the second order subsequent the first order.

Example 12 includes the computer readable storage medium of example 11, wherein the instructions cause the machine to embed a sequence order including the first order and the second order in at least one of the first aggregate data unit, the second aggregate data unit, or the third aggregate data unit.

Example 13 includes the computer readable storage medium of example 12, wherein the responder is to reorder the first and second plurality of data units based on the sequence order.

Example 14 includes the computer readable storage medium of example 10, wherein the first and second plurality of data units are media access control (mac) frames and the first and second aggregate data units are mac protocol data units (mpdus).

Example 15 includes the computer readable storage medium of example 10, wherein the instructions cause the machine to receive the first aggregate data unit from an upper layer at a first time and receive the second aggregate data unit from the upper layer at a second time different than the first time.

Example 16 includes the computer readable storage medium of example 10, wherein the instructions cause the machine to receive a second response identifies data units of the second plurality of data units received by the responder.

Example 17 includes the computer readable storage medium of example 16, wherein the instructions cause the machine to, in response to receiving the second response from the responder, transmit a fourth aggregate data unit including a second subset of the second plurality of data units not identified in the first response.

5        Example 18 includes the computer readable storage medium of example 10, wherein the third aggregate data unit further includes a third plurality of data units.

Example 19 includes a method comprising storing a first aggregate data unit including a first plurality of data units in a lower layer buffer, transmitting the first aggregate data unit to a responder, prior to receiving a first response identifying received data units of the first plurality of  
10    data units from the responder removing the first aggregate data unit from the lower layer buffer, and storing a second aggregate data unit including a second plurality of data units in the lower layer buffer, transmitting the second aggregate data unit to the responder, and in response to receiving the first response from the responder, transmitting a third aggregate data unit including a subset of the first plurality of data units not identified in the first response.

15        Example 20 includes the method of example 19, wherein the first plurality of data units corresponds to a first order and the second plurality of data units corresponds to a second order, the second order subsequent the first order.

Example 21 includes the method of example 20, further including embedding a sequence order including the first order and the second order in at least one of the first aggregate data unit,  
20    the second aggregate data unit, or the third aggregate data unit.

Example 22 includes the method of example 21, wherein the responder is to reorder the first and second plurality of data units based on the sequence order.

Example 23 includes the method of example 19, wherein the first and second plurality of data units are media access control (mac) frames and the first and second aggregate data units are  
25    mac protocol data units (mpdus).

Example 24 includes the method of example 19, further including receiving the first aggregate data unit from an upper layer at a first time and receiving the second aggregate data unit from the upper layer at a second time different than the first time.

Example 25 includes the method of example 19, further including receiving a second  
30    response identifies data units of the second plurality of data units received by the responder.

From the foregoing, it will be appreciated that example methods, systems, apparatus, and articles of manufacture have been disclosed that aggregate retransmissions. Conventional techniques of aggregating retransmission include storing multiple aggregate data units in a buffer and not transmitting additional aggregate data units to a responder until a response is received to  
5 determine which data units may be removed from a buffer, which takes time and a large buffer side. Examples disclosed herein alleviate the problems of conventional retransmission techniques to reduce the size of the buffer to correspond to one aggregate data unit and significantly increases the speed of transmission.

Although certain example methods, apparatus and articles of manufacture have been disclosed herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all methods, apparatus and articles of manufacture fairly falling within the scope of the claims of this patent.

What is claimed is:

1. An apparatus comprising:

a lower layer buffer;

a processor to store a first aggregate data unit including a first plurality of data units in

5 the lower layer buffer; and

an interface to transmit the first aggregate data unit to a responder,

the processor to, prior to receiving a first response identifying received data units of the first plurality of data units from the responder:

remove the first aggregate data unit from the lower layer buffer; and

10 store a second aggregate data unit including a second plurality of data units in the lower layer buffer, and

the interface to:

transmit the second aggregate data unit to the responder; and

15 in response to receiving a second response from the responder, transmit a third aggregate data unit including a subset of the first plurality of data units not identified in the first response.

2. The apparatus of claim 1, wherein the first plurality of data units corresponds to a first order and the second plurality of data units corresponds to a second order, the second order  
20 subsequent the first order.

3. The apparatus of claim 2, wherein the processor is to embed a sequence order including the first order and the second order in at least one of the first aggregate data unit, the second aggregate data unit, or the third aggregate data unit.

25

4. The apparatus of claim 3, wherein the responder is to reorder the first and second plurality of data units based on the sequence order.

5. The apparatus of claim 1, wherein the first and second plurality of data units are Media Access Control (MAC) frames and the first and second aggregate data units are MAC Protocol Data Units (MPDUs).

5        6. The apparatus of claim 1, wherein the interface is to receive the first aggregate data unit from an upper layer at a first time and receive the second aggregate data unit from the upper layer at a second time different than the first time.

7. The apparatus of claim 1, wherein the interface is to receive a second response identifies  
10 data units of the second plurality of data units received by the responder.

8. The apparatus of claim 7, wherein the interface is to, in response to receiving the second response from the responder, transmit a fourth aggregate data unit including a second subset of the second plurality of data units not identified in the first response.

15        9. The apparatus of claim 1, wherein the third aggregate data unit further includes a third plurality of data units.

10. A tangible computer readable storage medium comprising instructions which, when  
20 executed, cause a machine to at least:

store a first aggregate data unit including a first plurality of data units in a lower layer buffer;

transmit the first aggregate data unit to a responder;

25 prior to receiving a first response identifying received data units of the first plurality of data units from the responder:

remove the first aggregate data unit from the lower layer buffer; and

store a second aggregate data unit including a second plurality of data units in the lower layer buffer;

transmit the second aggregate data unit to the responder; and

30 in response to receiving a second response from the responder, transmit a third aggregate

data unit including a subset of the first plurality of data units not identified in the first response.

11. The computer readable storage medium of claim 10, wherein the first plurality of data units corresponds to a first order and the second plurality of data units corresponds to a second order, the second order subsequent the first order.

12. The computer readable storage medium of claim 11, wherein the instructions cause the machine to embed a sequence order including the first order and the second order in at least one of the first aggregate data unit, the second aggregate data unit, or the third aggregate data unit.

13. The computer readable storage medium of claim 12, wherein the responder is to reorder the first and second plurality of data units based on the sequence order.

14. The computer readable storage medium of claim 10, wherein the first and second plurality of data units are Media Access Control (MAC) frames and the first and second aggregate data units are MAC Protocol Data Units (MPDUs).

15. The computer readable storage medium of claim 10, wherein the instructions cause the machine to receive the first aggregate data unit from an upper layer at a first time and receive the second aggregate data unit from the upper layer at a second time different than the first time.

16. The computer readable storage medium of claim 10, wherein the instructions cause the machine to receive a second response identifies data units of the second plurality of data units received by the responder.

17. The computer readable storage medium of claim 16, wherein the instructions cause the machine to, in response to receiving the second response from the responder, transmit a fourth aggregate data unit including a second subset of the second plurality of data units not identified in the first response.

18. The computer readable storage medium of claim 10, wherein the third aggregate data unit further includes a third plurality of data units.

19. A method comprising:

5 storing a first aggregate data unit including a first plurality of data units in a lower layer buffer;  
transmitting the first aggregate data unit to a responder;  
prior to receiving a first response identifying received data units of the first plurality of data units from the responder:  
10 removing the first aggregate data unit from the lower layer buffer; and  
storing a second aggregate data unit including a second plurality of data units in the lower layer buffer;  
transmitting the second aggregate data unit to the responder; and  
in response to receiving the first response from the responder, transmitting a third  
15 aggregate data unit including a subset of the first plurality of data units not identified in the first response.

20. The method of claim 19, wherein the first plurality of data units corresponds to a first order and the second plurality of data units corresponds to a second order, the second order  
20 subsequent the first order.

21. The method of claim 20, further including embedding a sequence order including the first order and the second order in at least one of the first aggregate data unit, the second aggregate data unit, or the third aggregate data unit.

25 22. The method of claim 21, wherein the responder is to reorder the first and second plurality of data units based on the sequence order.

23. The method of claim 19, wherein the first and second plurality of data units are Media Access Control (MAC) frames and the first and second aggregate data units are MAC Protocol Data Units (MPDUs).

5        24. The method of claim 19, further including receiving the first aggregate data unit from an upper layer at a first time and receiving the second aggregate data unit from the upper layer at a second time different than the first time.

10       25. The method of claim 19, further including receiving a second response identifies data units of the second plurality of data units received by the responder.

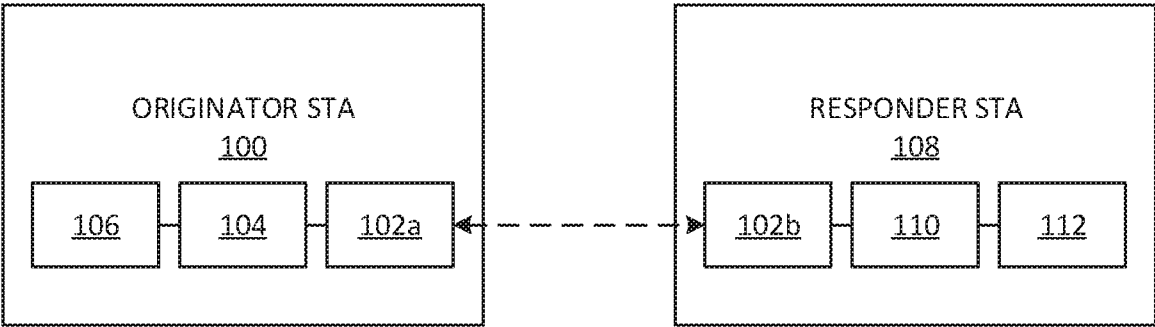
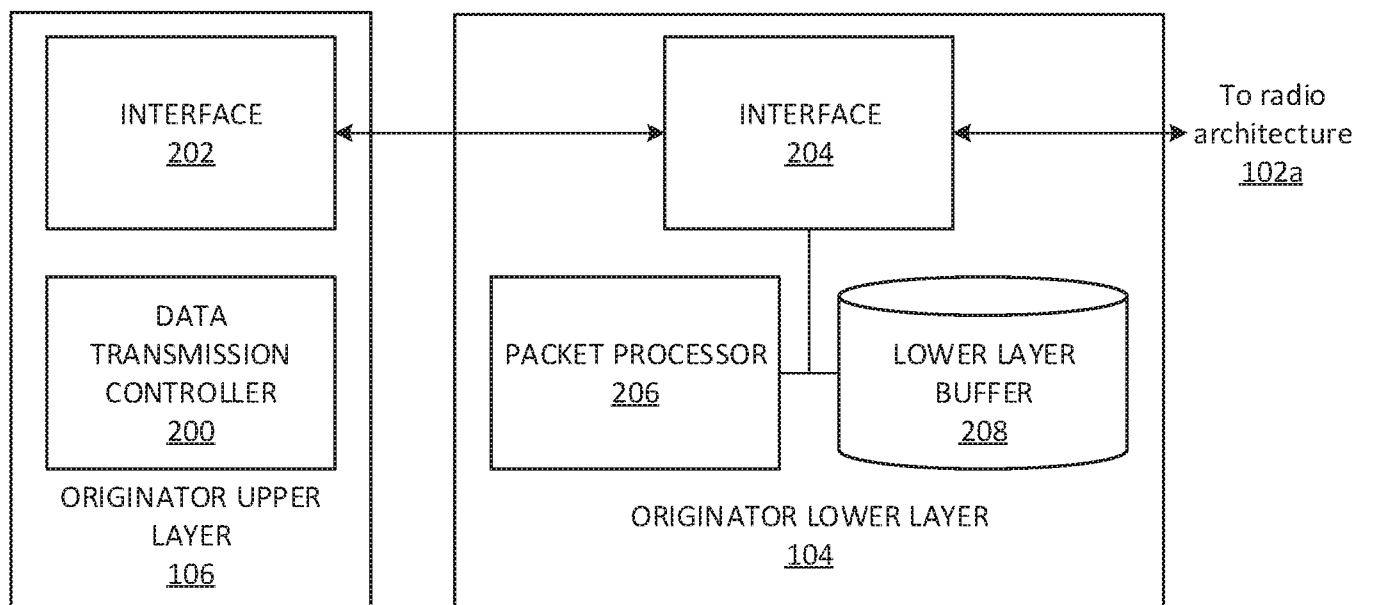


FIG. 1

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**FIG. 2**

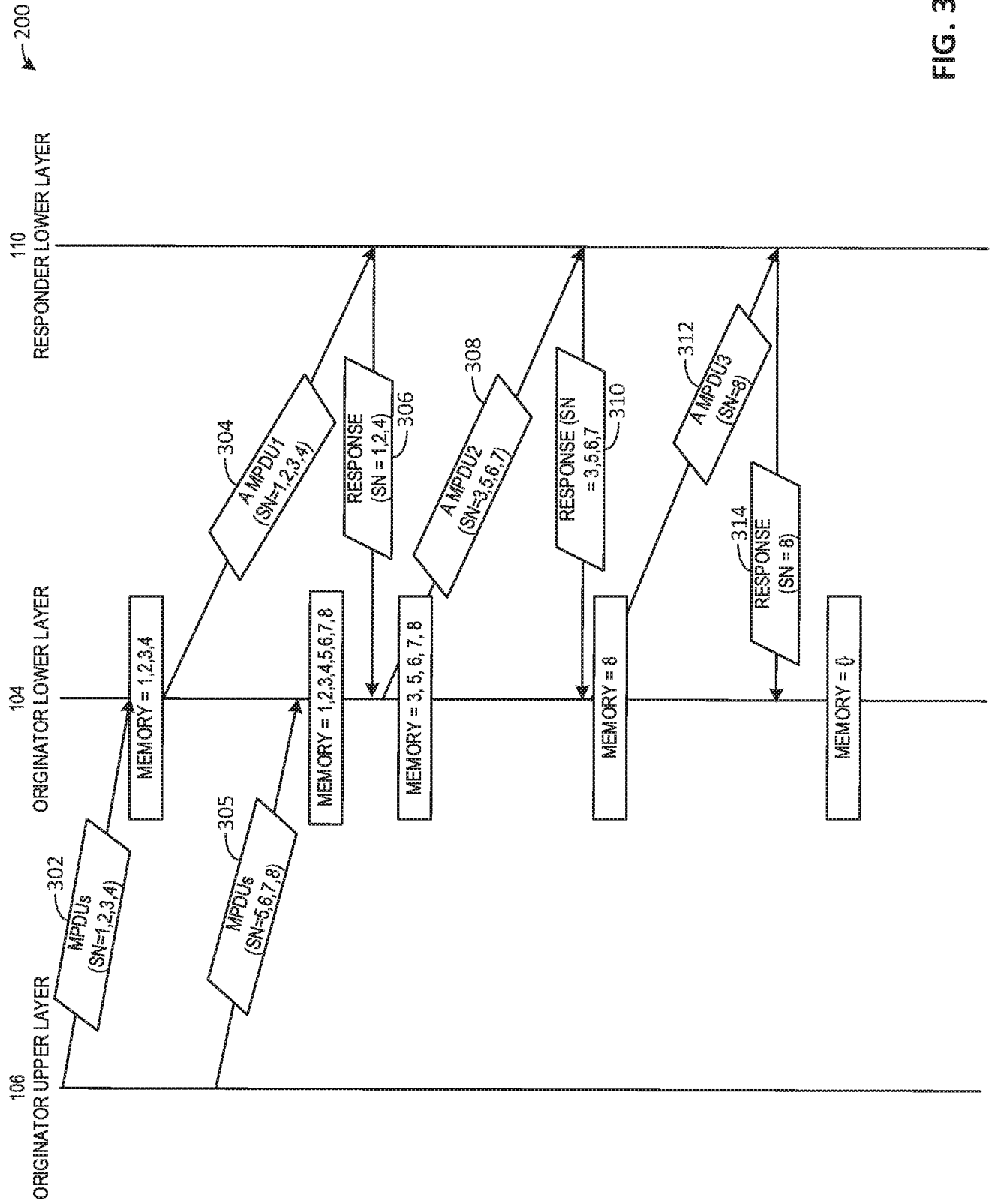


FIG. 3

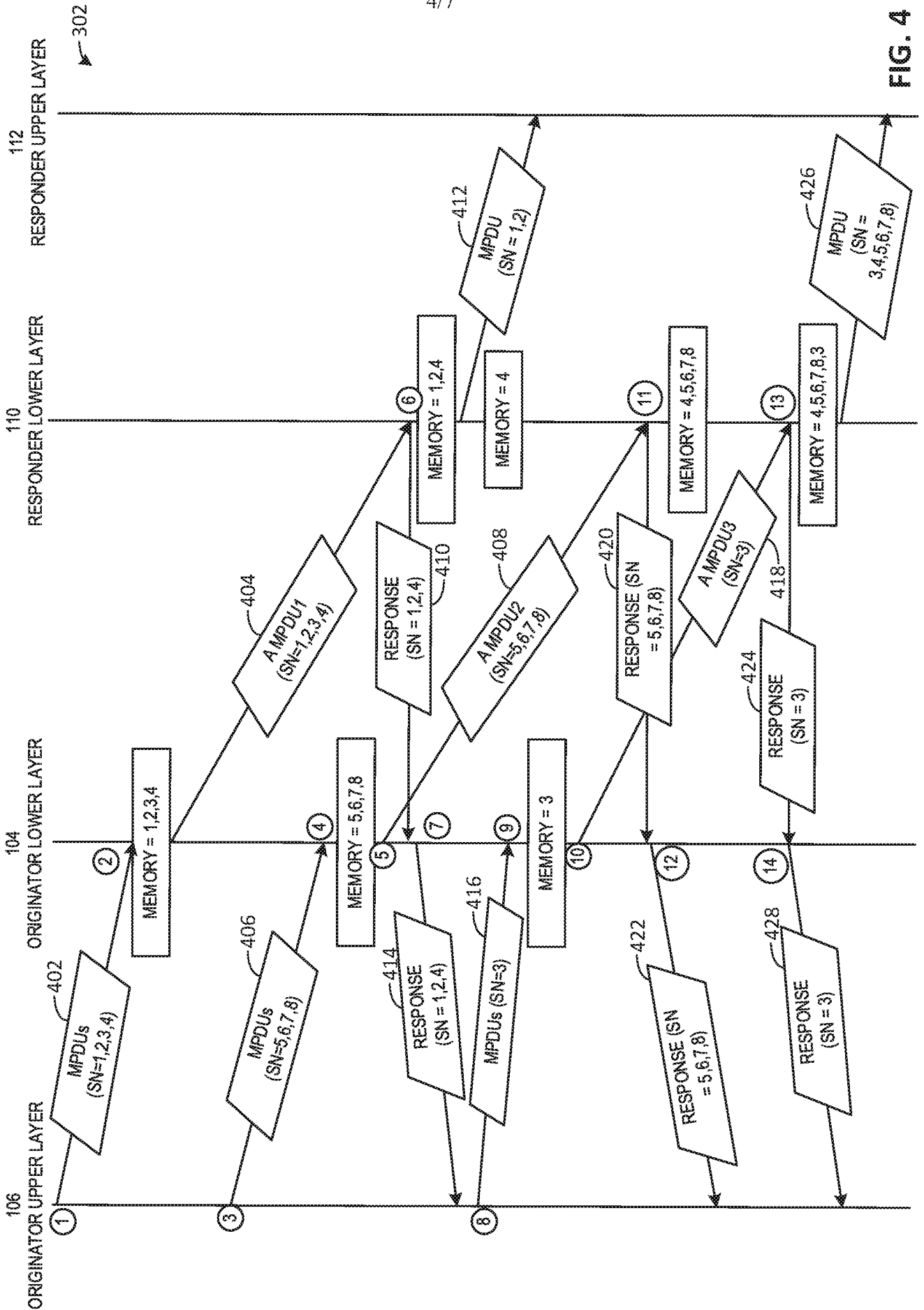


FIG. 4

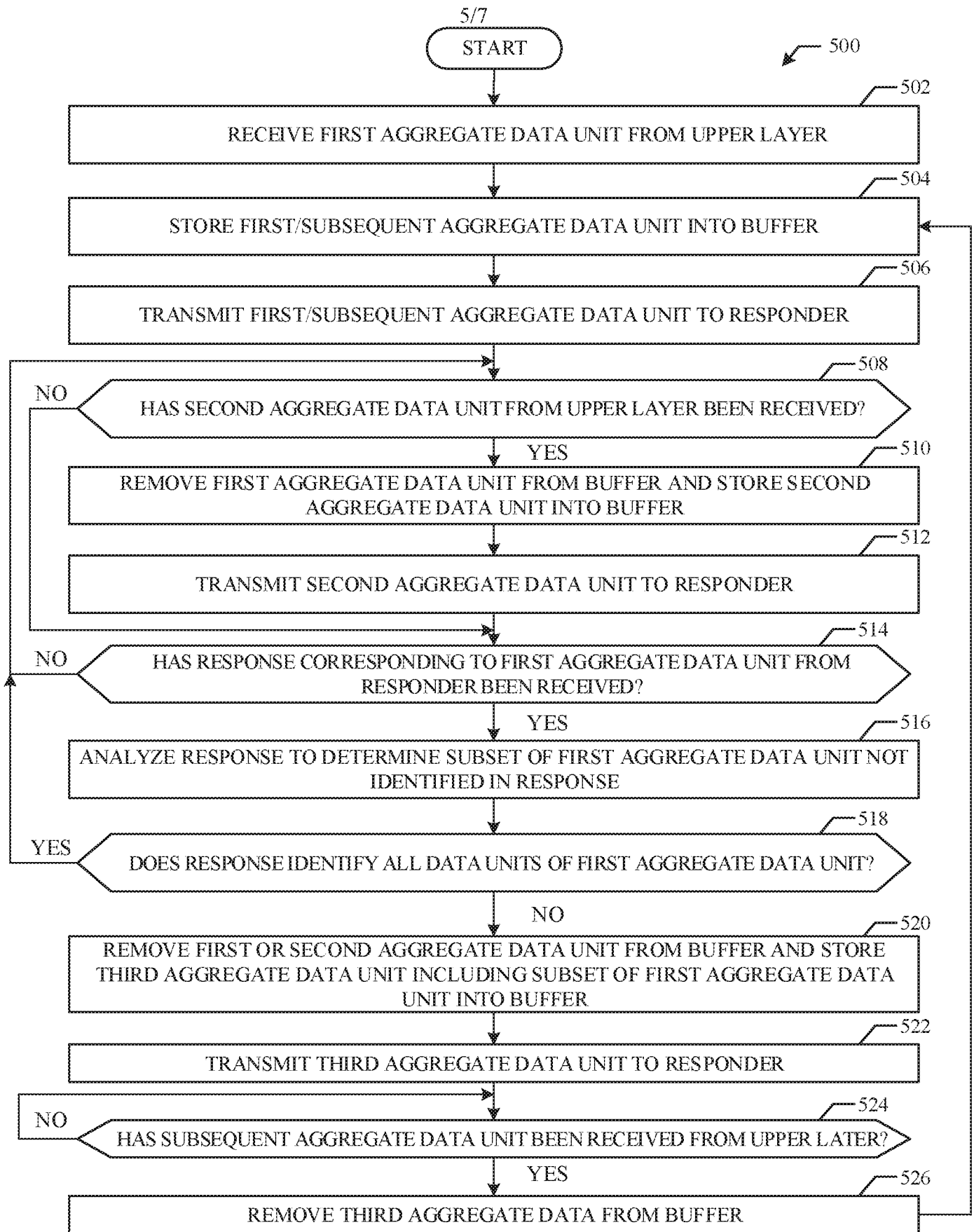


FIG. 5

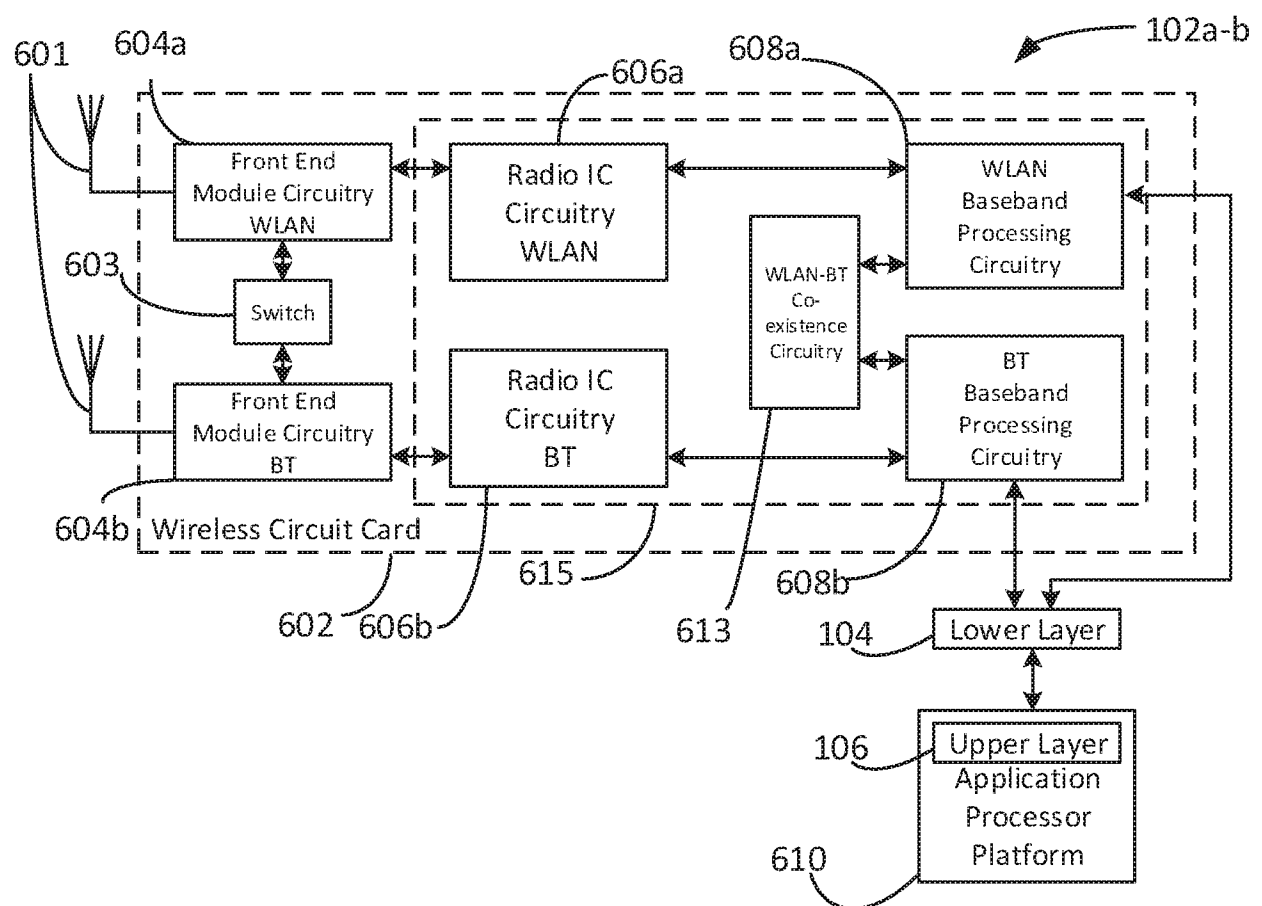


FIG. 6

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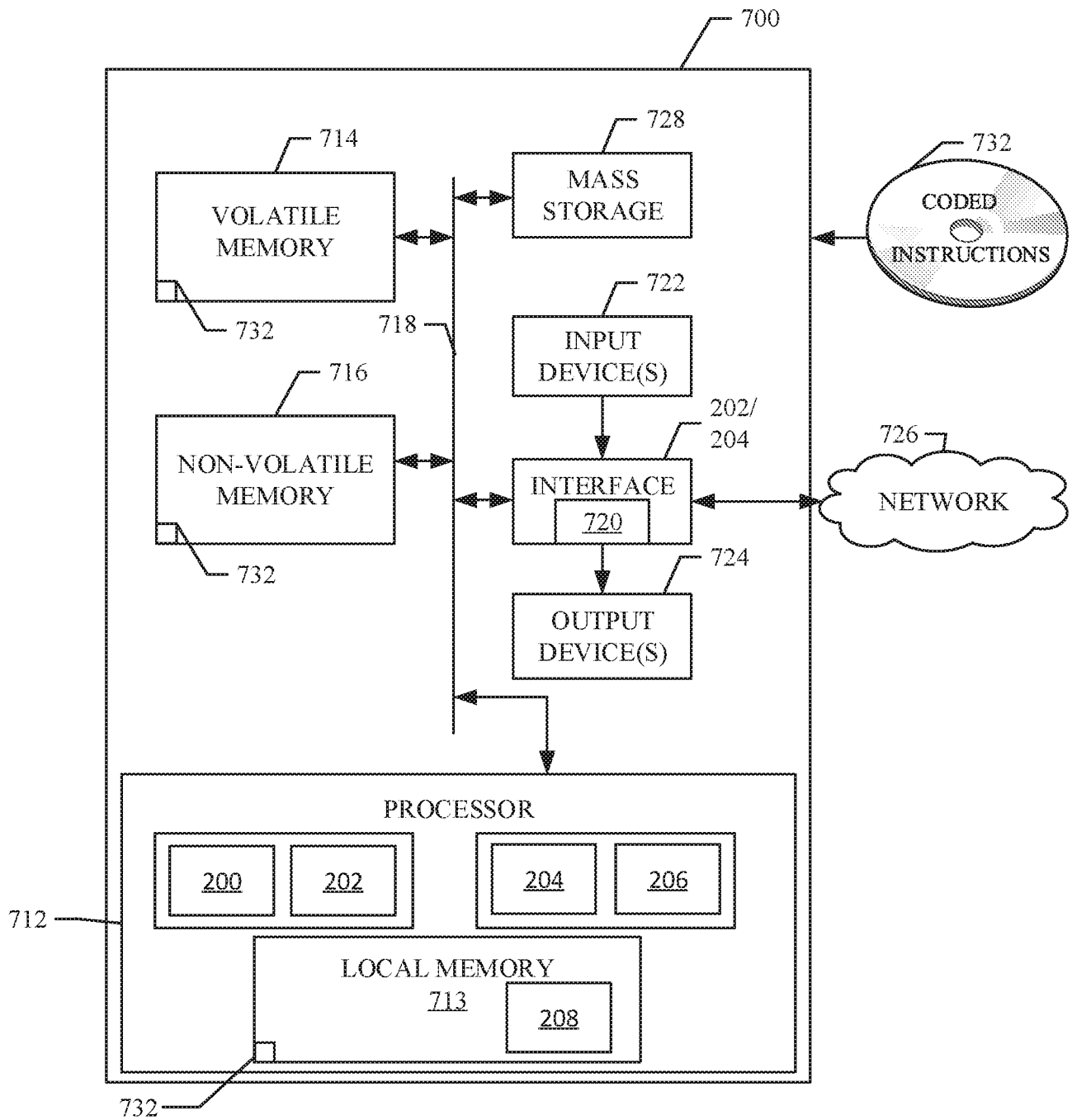


FIG. 7

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US2018/030233**A. CLASSIFICATION OF SUBJECT MATTER****H04W 28/14(2009.01)i, H04W 28/04(2009.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H04W 28/14; G06F 11/30; H04L 1/00; H04L 1/16; H04L 12/26; H04L 29/06; H04W 4/00; H04L 1/08; H04W 28/04

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) &amp; Keywords: aggregate data unit, lower layer buffer, response, remove, sequence order, reorder

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                | Relevant to claim No. |
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Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

20 September 2018 (20.09.2018)

Date of mailing of the international search report

**20 September 2018 (20.09.2018)**

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**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

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