A vehicle includes a magnetic sensor comprising a plurality of layers including a substrate having circuitry, at least one conductive layer to interconnect the circuitry, and an insulator layer to electrically insulate the at least one conductive layer. First and second conductive layers are generally parallel to the substrate with a dielectric layer disposed between the first and second conductive layers such that the first and second conductive layers and the dielectric layer form a capacitor. A first terminal is electrically connected to the first conductive layer and a second terminal is electrically connected to the second conductive layer.
BEGIN

FORM FIRST AND SECOND LAYERS OVER SUBSTRATE

DEPOSIT INTERLAYER DIELECTRIC

PATTERN DIELECTRIC AND OPEN CONNECTIONS TO BOND PADS

DEPOSIT FIRST CONDUCTIVE LAYER FOR CAPACITOR

DEPOSIT AND PATTERN CAPACITOR DIELECTRIC

DEPOSIT SECOND LAYER OF CAPACITOR

APPLY PASSIVATION LAYER

END

FIG. 5
VEHICLE HAVING A SENSOR WITH CAPACITOR ON CHIP

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Divisional application of U.S. patent application Ser. No. 11/279,780 filed on Apr. 14, 2006, which is hereby incorporated herein by reference in its entirety.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH

[0002] Not Applicable.

BACKGROUND

[0003] As is known in the art, there are a variety of sensors that are useful for particular applications. For example, magnetic sensors are useful to detect movement, such as rotation, of an object of interest. Typically, Hall-effect sensors require a discrete decoupling capacitor component placed on or near the sensor to enhance EMC (Electromagnetic Compatibility) and reduce so-called long-wire noise problems. However, external capacitors incur added cost and processing at the individual device level. External capacitors also increase the total package size if the capacitor resides on the leadframe or requires an additional printed circuit board.

SUMMARY

[0004] The present invention provides a magnetic sensor including an on chip capacitor formed from first and second conductive layers and a dielectric layer disposed over a substrate. With this arrangement, the need for an external decoupling capacitor may be eliminated. While the invention is primarily shown and described in conjunction with particular layer stack ups, devices and configurations, it is understood that the invention is applicable to circuits in general in which it is desirable to provide a capacitive impedance.

[0005] In one aspect of the invention, a magnetic sensor comprises a plurality of layers including a substrate including circuitry, at least one conductive layer to interconnect the circuitry, an insulator layer to electrically insulate the at least one conductive layer. First and second conductive layers are disposed over the substrate, and a dielectric layer is disposed between the first and second conductive layers such that the first and second conductive layers and the dielectric layer form a capacitor. The sensor further includes a first terminal electrically connected to the first conductive layer and a second terminal electrically connected to the second conductive layer.

[0006] In another aspect of the invention, a method includes forming a first conductive layer over a substrate containing circuitry, forming a dielectric layer over the first conductive layer, and, forming a second conductive layer over the dielectric layer such that the first conductive layer, the dielectric layer, and the second conductive layer form a first capacitor. A first terminal can be coupled to the first conductive layer and a second terminal can be coupled to the second conductive layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The foregoing features of this invention, as well as the invention itself, may be more fully understood from the following description of the drawings in which:

[0008] FIG. 1A is a top view of a sensor having an on chip capacitor in accordance with an exemplary embodiment of the invention;

[0009] FIG. 1B is a cross-sectional view of the sensor of FIG. 1A taken along line A-A;

[0010] FIGS. 2A and 2B show a two-wire magnetic sensor having an on chip capacitor;

[0011] FIG. 3 is a pictorial top view of a three-wire magnetic sensor having an on chip capacitor;

[0012] FIG. 4 is a schematic diagram of a sensor having multiple on chip capacitors; and

[0013] FIG. 5 is a flow diagram showing an exemplary sequence of steps to fabricate a sensor having an on chip capacitor.

DETAILED DESCRIPTION

[0014] FIGS. 1A-B show an exemplary embodiment of a magnetic sensor 100 having an on chip capacitor 102 in accordance with the present invention. In the illustrated embodiment, the sensor 100 is a two-wire Hall effect type sensor having a VCC terminal 104 and a ground terminal 106. The capacitor 102 can be provided as a decoupling capacitor between the VCC terminal 104 and the ground terminal 106, for example. As described more fully below, the capacitor 102 can be coupled to a VCC cap terminal 108, which is at the same potential as the VCC terminal 104 in an exemplary embodiment. The VCC cap terminal 108 and the VCC terminal 104 can be electrically coupled using any suitable technique, such as wire bonding. This arrangement allows breakdown testing. In alternative embodiments, Vcc and Vcc cap bond pads could be combined to form a single pad.

[0015] A first metal layer 116 is disposed on the substrate 116 and an optional second layer 118, which is sandwiched between first and second insulating layers 120, 122, is disposed over the first metal layer 116. The first and second metal layers 116, 118 provide, for example, interconnection and routing for the device layer 112. The first and second insulating layers 120, 122 can be provided, for example, as interlayer dielectric and/or passivation layers.

[0016] First and second conductive layers 124, 126 are separated by a dielectric material 128 to form the on-chip capacitor 102 above the substrate. The capacitor 102 is covered by a further insulating layer 130. In an exemplary embodiment, the capacitor 102 is separated, and electrically isolated, from the second metal layer 118 by the second insulating layer 122.

[0017] In an exemplary embodiment, a substrate 110, e.g., silicon, includes an integrated circuit (IC) in layers 112, 116, 120, 118, and/or 122 in which circuitry is formed in a manner well known to one of ordinary skill in the art. The device layer 112 can include a Hall element 114 that forms part of the magnetic sensor 100. The device layer may include various layers necessary to form an integrated
circuit, including, but not limited to, implant or doped layers, polysilicon, epi layers, oxide, or nitride layers.

[0018] While a particular layer stack up is shown and described, it is understood that other embodiments having different layering orders and greater and fewer metal and other layers are within the scope of the invention. In addition, additional conductive layers can be added to form additional capacitors to meet the needs of a particular application.

[0019] As shown in FIG. 2A, for the illustrated two-wire sensor, a sense resistor Rsense can be coupled between the ground terminal 106 and a ground connection, or as shown in FIG. 2B, the sense resistor Rsense can be coupled between the VCC terminal 104 and the power supply. This enables measurement of the sensor 100 output in the form of current changes in response to a positional displacement of a magnetic object of interest. By providing an on chip capacitor, the need for an external decoupling capacitor for the sensor may be eliminated.

[0020] In another embodiment shown in FIG. 3, a three-wire magnetic sensor 200 includes an on chip capacitor 202 with a Vout terminal 204 to provide a sensor output signal. The sensor 200 of FIG. 3 has some similarity with the sensor 100 of FIGS. 1A-1C, where like reference numbers indicate like elements.

[0021] It is understood that higher breakdown voltage requirements for the capacitor may limit the amount of capacitance that can be provided by the on chip capacitor. Lower breakdown voltage requirements may increase the amount of capacitance that can be provided. Factors that determine the characteristics of the on chip capacitor 102 include, for example, die size, metal layer area, conductive layer area, dielectric material, selected breakdown voltage, layer spacing, geometry, and others.

[0022] A variety of dielectric materials for the capacitor 166 can be used including, but not limited to; silicon nitride, silicon oxide, e.g. silicon dioxide, Tantalum oxide, Aluminum oxide, ceramics, glass, mica, polymers (e.g. Mylar), KAPTON, polyimides (e.g. Pyralin by HD Microsystems), benzocyclobutene (BCB, e.g. Cyclotene by Dow Chemical), and polynorbornene (e.g., Avatrel by Promerus). Inorganic dielectrics may be preferable for some applications based on their higher dielectric constant and the ability to create uniform thin films in the sub-micron range; e.g. 3,000 to 5,000 Angstroms in thickness.

[0023] These same dielectrics may be used where appropriate for interlayer dielectric, or final passivation materials. In the case of the interlayer dielectric, it may be advantageous to select a material that planarizes well, and has a low dielectric constant for use between the second metal layer 118 and the conductive layer 124. This should reduce any unwanted coupling of signals from lines on the metal layer 118 to the conductive layer 124, which may, for example, be a ground plane.

[0024] A variety of suitable materials can be used to provide the device layer for the sensor including silicon, gallium arsenide, silicon on insulator (SOI), and the like. In addition, various materials can be used to provide the metal layers and the conductive layers, which form the capacitor. Exemplary metal and conductive layer materials include copper, aluminum, alloys and/or other suitable metals.

[0025] In general, for a die size of about 2.5 to 3 mm², the on chip capacitor provides in the order of 400 pF. For a larger die, e.g., about 5 mm², the capacitor provides in the order of 800 pF. In exemplary embodiments, the capacitor provides a capacitance from about 100 pF to about 1,500 pF for a substrate ranging in size from about 1 mm² to about 10 mm².

[0026] In one particular embodiment, the first and second conductive layers 124, 126 (FIG. 1B) have dimensions of 2.3 mm². The dielectric material is silicon nitride having a thickness ranging of approximately 3,000 Å to about 5,000 Å. This arrangement provides a breakdown voltage of about at least 50V with a capacitance of about 300 pF to about 500 pF.

[0027] A Hall sensor having an on chip capacitor of about 100 pF to about 1,500 pF and at least 50V breakdown voltage is well suited for many vehicle applications, such as anti-lock brake sensors (ABS), linear position sensors, angle sensors, transmission sensors, cam sensors, and crank sensors.

[0028] In general, the first and second conductive layers 124, 126 (FIG. 1B) forming the capacitor 102 cover from about thirty percent to about ninety percent of the die area. The capacitor 102 may be above the die where above refers to some degree of overlap between generally parallel planes formed by the die and the conductive layers of the capacitor.

[0029] In one embodiment, the first and second layers cover an area of about eighty percent of the die area. Such a capacitor would provide a capacitance on the order of 400 pF, which can provide additional EMC protection to the circuitry on the die. In some devices, in the order of 200 pF may be sufficient for EMC or long-wire protection. In such a case the area required by the capacitor is not as large, and may be on the order of fifty percent of the total die area. In general, the capacitor can be sized to meet the needs of a particular application.

[0030] As used herein, the term die refers to a substrate, which may be a semiconductor or a semiconductor layer on an insulator, for example SOI substrates, with its associated circuits or electronic device elements. The circuits on the die may include semiconductor devices, for example diodes, and transistors, and passive devices, for example a resistor, inductor, or capacitor.

[0031] As shown in FIG. 4, the second conductive layer 304 can be separated to form multiple capacitors, shown as first and second capacitors 306, 308 provided the first conductive layer 302 is at the same potential for both. It would also be apparent that the first conductive layer 302 could also be split to form separate capacitors, although it may require the addition of a bonding pad depending on the application. The first capacitor 306 provides a decoupling capacitor between the VCC cap terminal 108 and ground 106. The second capacitor 308 is coupled between a Vout cap terminal 310 and ground 106. A Vout terminal 204, which can be coupled to the Vout cap terminal 310 via wire-bond, provides a sensor output signal for a three-wire magnetic sensor, for example.

[0032] It is understood that the apportionment of the first and second conductive layers 302, 304 can be made to achieve capacitance requirements for a particular application. In addition, the first and second conductive layers can
be split to form any practical number of capacitors above the die. Such multiple capacitor configurations may be useful for applications that require more than two-wires; for example a three-wire part with power, ground, and independent output pins.

[0033] FIG. 5 shows an exemplary sequence of steps to fabricate a sensor having an on-chip capacitor. In general, fabrication of the integrated capacitor is performed after an integrated circuit process is performed, which may also be referred to as the base process.

[0034] In step 400, first and second metal layers are formed over a substrate. In one particular embodiment, the base process includes two metal layers for interconnection and routing and a final passivation. It may be desirable to change the final passivation on the base process, which may typically include an oxide and nitride layer. After the second metal layer, in step 402 an interlayer dielectric is deposited. Again, this is the place where the final passivation would be performed in the base process. The interlayer dielectric can be an oxide, nitride, or organic dielectric such as a polyimide, or BCB. A material such as BCB has advantages in that it planarizes the underlying substrate well and allows a flat surface for the subsequent capacitor deposition. In step 404, the interlayer dielectric is then patterned to open connections to the bond pads in the underlying integrated circuit.

[0035] In step 406, a conductive layer is then deposited on the wafer and patterned to form one of the capacitor electrodes. In the illustrated embodiment, the lower capacitor electrode is connected to the ground bonding pad, but not any other portions of the underlying circuit. In some cases it may be desirable to have the lower capacitor layer on the other bonding pads of the integrated circuit, although these pads are not connected to the capacitor electrode. In step 408, the capacitor dielectric is deposited and patterned. The dielectric material may be silicon nitride, or other suitable material. In step 410, the second conductive layer of the capacitor is deposited on the wafer and patterned to form the top electrode of the capacitor. The upper layer of the capacitor may be connected to the Vcc pad of the integrated circuit, or it may be its own bonding pad. Having the upper layer of the capacitor as an independent pad allows the dielectric breakdown to be tested during the final test of the integrated circuit with an on-chip capacitor. In step 412, a final passivation layer is applied to the integrated circuit with the capacitor and pattern openings for the bonding pads.

[0036] It is understood that a variety of suitable fabrication processes can be used to form a sensor having an on-chip capacitor including, but not limited to, bipolar, DMOS, bi-CMOS, CMOS, and processes and combinations of these and other processes.

[0037] While exemplary embodiments contained herein discuss the use of a Hall effect sensor, it would be apparent to one of ordinary skill in the art that other types of magnetic field sensors may also be used in place of or in combination with a Hall element. For example the device could use an anisotropic magnetoresistance (AMR) sensor and/or a Giant Magnetoresistance (GMR) sensor. In the case of GMR sensors, the GMR element is intended to cover the range of sensors comprised of multiple material stacks, for example: linear spin valves, a tunneling magnetoresistance (TMR), or a colossal magnetoresistance (CMR) sensor. In other embodiments, the sensor includes a buck bias magnet.

[0038] Having described exemplary embodiments of the invention, it will now become apparent to one of ordinary skill in the art that other embodiments incorporating their concepts may also be used. The embodiments contained herein should not be limited to disclosed embodiments but rather should be limited only by the spirit and scope of the appended claims. All publications and references cited herein are expressly incorporated herein by reference in their entirety.

What is claimed is:

1. A vehicle, comprising:
   a sensor, comprising:
   a substrate including circuitry;
   at least one conductive layer to interconnect the circuitry;
   an insulator layer to electrically insulate the at least one conductive layer;
   first and second conductive layers generally parallel to the substrate;
   a dielectric layer disposed between the first and second conductive layers such that the first and second conductive layers and the dielectric layer form a capacitor; and
   first and second terminals, wherein the first terminal is electrically connected to the first conductive layer and the second terminal is electrically connected to the second conductive layer.

2. The vehicle according to claim 1, wherein the capacitor overlaps with at least thirty percent of an area of the substrate.

3. The vehicle according to claim 1, wherein the first and second conductive layers are divided to form a further capacitor.

4. The vehicle according to claim 1, wherein the capacitor provides a capacitance from about 100 pF to about 1,500 pF for a substrate ranging in size from about 1 mm² to about 10 mm².

5. The vehicle according to claim 1, wherein the sensor includes a Hall sensor.

6. The vehicle according to claim 5, wherein the Hall sensor is a two-wire Hall sensor.

7. The vehicle according to claim 1, wherein the first terminal is adapted for coupling to a voltage supply terminal.

8. The vehicle according to claim 7, wherein the second terminal is adapted for coupling to a ground terminal.

9. The vehicle according to claim 1, wherein the sensor includes a buck bias magnet.

10. The vehicle according to claim 1, wherein the sensor includes an AMR sensor.

11. The vehicle according to claim 1, wherein the sensor includes a GMR sensor.

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