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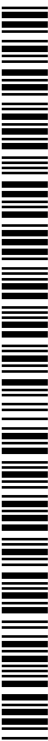

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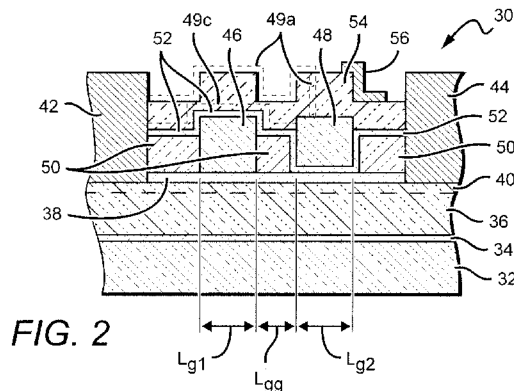

FIG. 2

(57) **Abstract**: A transistor device including a field plate is described. One embodiment of such a device includes a field plate separated from a semiconductor layer by a thin spacer layer. In one embodiment, the thickness of spacer layer separating the field plate from the semiconductor layers is less than the thickness of spacer layer separating the field plate from the gate. In another embodiment, the non- zero distance separating the field plate from the semiconductor layers is about 1500A or less. Devices according to the present invention can show capacitances which are less drain bias dependent, resulting in improved linearity.

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RECESSED FIELD PLATE TRANSISTOR STRUCTURES

This application is a continuation-in-part of and claims the benefit of U.S. Patent Application Serial No. 13/913,490, filed on June 9, 2013 and entitled "Cascode Structures for GaN HEMTs," which is fully incorporated by reference herein in its entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to cascode structures and particularly to dual-gate transistors having an insulating layer below one gate. The present invention also relates to transistors including a field plate and particularly to transistors having a field plate relatively near the semiconductor layers.

Description of the Related Art

[0002] Materials such as silicon (Si) and gallium arsenide (GaAs) have found wide application in semiconductor devices for low power and, in the case of Si, low frequency applications. However, these more familiar semiconductor materials may not be well-suited for high power and/or high frequency applications, for example, due to their relatively small bandgaps (1.12 eV for Si and 1.42 for GaAs at room temperature) and relatively small breakdown voltages.

[0003] In light of the difficulties presented by Si and GaAs, interest in high power, high temperature and/or high frequency applications and devices has focused on wide

bandgap semiconductor materials such as silicon carbide (2.996 eV for alpha SiC at room temperature) and the Group III nitrides (e.g., 3.36 eV for GaN at room temperature). These materials, typically, may have higher electric field breakdown strengths and higher electron saturation velocities as compared to GaAs and Si.

[0004] A device of particular interest for high power and/or high frequency applications is the High Electron Mobility Transistor (HEMT), which is also known as a modulation doped field effect transistor (MODFET). In a HEMT device, a two-dimensional electron gas (2DEG) may be formed at the heterojunction of two semiconductor materials with different bandgap energies. The smaller bandgap material may have a higher electron affinity than the wider bandgap material. The 2DEG is an accumulation layer in the undoped smaller bandgap material and can contain a relatively high sheet electron concentration, for example, in excess of 10^{13} carriers/cm^2. Additionally, electrons that originate in the wider bandgap semiconductor may transfer to the 2DEG, allowing a relatively high electron mobility due to reduced ionized impurity scattering. This combination of relatively high carrier concentration and carrier mobility can give the HEMT a relatively large transconductance and may provide a performance advantage over metal-semiconductor field effect transistors (MESFETS) for high-frequency applications.

[0005] HEMTs fabricated in the gallium nitride/aluminum gallium nitride (GaN/AlGaN) material system can generate large amounts of RF power due to a combination of material characteristics, such as relatively high breakdown fields,

relatively wide bandgaps, relatively large conduction band offset, and/or relatively high saturated electron drift velocity. A major portion of the electrons in the 2DEG may be attributed to polarization in the AlGaN.

[0006] Different types of HEMTs in the GaN/AlGaN system have been demonstrated. For example, U.S. Pat. Nos. 5,192,987 and 5,296,395 describe AlGaN/GaN HEMT structures and methods of manufacture. In addition, U.S. Pat. No. 6,316,793, to Sheppard et al., which is commonly assigned with the present application, describes a HEMT device having a semi-insulating silicon carbide substrate, an AlN buffer layer on the substrate, an insulating GaN layer on the buffer layer, an AlGaN barrier layer on the GaN layer, and a passivation layer on the AlGaN active structure. Moreover, U.S. Patent Application Publication No. U.S.2005/0170574 to Sheppard et al., which is also commonly assigned, describes a HEMT device including a protective layer and/or a low damage recess fabrication technique which may reduce damage to the semiconductor in the gate region of the transistor that can occur during an anneal of the ohmic contacts of the device.

[0007] Electron trapping and the resulting difference between DC and RF characteristics can be a limiting factor in the performance of these devices. Silicon nitride (SiN) passivation has been employed to alleviate this trapping problem resulting in high performance devices with power densities over 10W/mm at 10 Ghz. For example, commonly assigned U.S. Patent No. 6,586,781 to Wu et al. discloses methods and structures for reducing the trapping effect in GaN-based transistors. However, due to the high electric

fields existing in these structures, charge trapping can still be a concern.

[0008] Field plates have been used to enhance the performance of GaN-based HEMTs at microwave frequencies and have exhibited performance improvement over non-field-plated devices [See S. Kamalkar and U.K. Mishra, *Very High Voltage AlGaN/GaN High Electron Mobility Transistors Using a Field Plate Deposited on a Stepped Insulator,* Solid State Electronics 45, (2001), pp. 1645-1662]. Many field plate approaches have involved a field plate connected to the gate of the transistor with the field plate on top of the drain side of a channel. This can result in a reduction of the electric field on the gate-to-drain side of the transistor, thereby increasing breakdown voltage and reducing the high-field trapping effect. However, transistors with gate-to-drain field plates can exhibit relatively poor reliability performance, particularly at class C (or higher class) operation where the electric field on the source side of the gate becomes significant.

[0009] It is well known that field plate approaches involving connecting the field plate to the source offer a reduction in gate-to-drain capacitance C_{gd}, which consequently can enhance the gain. In addition to minimizing capacitance, one goal in some applications is to improve linearity (i.e., the degree of proportionality between input and output) and reduce the drain bias dependence of the capacitance. While GaN-based HEMTs generally display good linearity, in some applications further improvement is desired (e.g., high power RF or and/or communication applications).

[0010] FIG. 1A shows a prior art transistor 10 having a field plate 28 connected to a source 22. The transistor 10 also includes a gate 26 which is on a barrier layer 18 and arranged between the source 22 and a drain 24, and within an insulating spacer layer 21. The barrier layer 18 is on a layer sequence including a 2DEG 20, a buffer layer 16, and a substrate 12. FIG. 1B is a chart showing the capacitance C_{gd} as a function of drain voltage V_d for a structure similar to the transistor 10. While this structure can have a reduced capacitance C_{gd} compared to structures without a field plate, the capacitance C_{gd} can still show a large dependence on the bias of the drain 24 as shown by FIG. 1B and shows a linearity with room for improvement.

[0011] One method of minimizing feedback capacitance while also improving linearity involves multi-stage arrangements. Transistors such as HEMTs can be combined in a two-stage cascode arrangement (using two of the same or different transistors). Some cascode arrangements including an initial non-field-plated common source stage and a second field-plated common gate stage are described in the commonly assigned U.S. Pat. No. 7,126,426 to Mishra et al. and entitled "Cascode Amplifier Structure Including Wide Bandgap Field Effect Transistor With Field Plates," which is fully incorporated by reference herein in its entirety. These devices can obtain the benefits of the field plate with little detrimental impact due to the feedback capacitance caused by the use of the field plate.

[0012] Multi-stage arrangements can also be achieved within a single dual-gate transistor, such as those described in U.S. Pat. No. 5,514,992 to Tanaka et al. In a dual-gate

cascode transistor, the drain-to-source connection of a two transistor arrangement is replaced by the portion of the transistor between the two gates. FIG. 1C shows a prior art HEMT 11 with a dual-gate cascode arrangement including many of the same elements as the transistor 10 (like reference numerals are used to indicate like elements). The HEMT 11 includes a first stage gate 26 and a second stage gate 29 which are on the barrier layer 18 and arranged between the source 22 and drain 24. The second gate 29 can act as a shield for the first gate 26, and thus can reduce the feedback capacitance between the first gate 26 and drain 24, can reduce the drain voltage dependence of the capacitance, and can improve linearity.

[0013] In prior art dual-gate arrangements such as that shown in FIG. 1C, the first and second stages have the same threshold voltage. If the second gate in such an arrangement is grounded, then the current flow can be limited. Because of this, the second stage must be DC biased so as to avoid limiting the maximum current of the device. Some such devices are described in U.S. Pub. No. 2007/0290762 to Lin et al. However, separately biasing the second stage leads to added complexity and cost.

SUMMARY OF THE INVENTION

[0014] The present invention provides transistor structures with a field plate nearer the active semiconductor layers than prior art structures. One embodiment of a transistor according to the present invention includes a plurality of semiconductor layers and a gate between a source and a

drain. The transistor comprises a field plate separated from a gate by a thicker portion of spacer layer and separated from the semiconductor layers by a thinner portion of spacer layer.

[0015] Another embodiment of a transistor according to the present invention comprises a spacer layer shaped to define an aperture, and a field plate at least partially within the aperture.

[0016] Yet another embodiment of a transistor according to the present invention comprises a spacer layer that separates a field plate from both semiconductor layers and a gate. The spacer layer has a thickness less than or equal to about 1500Å.

[0017] These and other further features and advantages of the invention would be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] FIG. 1A is a cross-sectional view of one embodiment of a prior art transistor;

[0019] FIG. 1B is a graph of gate-to-drain capacitance as a function of drain voltage in a prior art transistor;

[0020] FIG. 1C is a cross-sectional view of another embodiment of a prior art transistor;

[0021] FIG. 2 is a cross-sectional view of one embodiment of a transistor according to the present invention;

[0022] FIG. 3 is a plan view of the transistor shown in FIG. 2;

[0023] FIG. 4 is a cross-sectional view of another embodiment of a transistor according to the present invention;

[0024] FIG. 5 is a cross-sectional view of another embodiment of a transistor according to the present invention;

[0025] FIG. 6 is a cross-sectional view of another embodiment of a transistor according to the present invention;

[0026] FIG. 7 is a cross-sectional view of another embodiment of a transistor according to the present invention;

[0027] FIG. 8 is a cross-sectional view of another embodiment of a transistor according to the present invention;

[0028] FIG. 9 is a cross-sectional view of another embodiment of a transistor according to the present invention;

[0029] FIG. 10 is a cross-sectional view of another embodiment of a transistor according to the present invention;

[0030] FIG. 11 is a cross-sectional view of another embodiment of a transistor according to the present invention;

[0031] FIG. 12 is a cross-sectional view of another embodiment of a transistor according to the present invention;

[0032] FIG. 13 is a cross-sectional view of another embodiment of a transistor according to the present invention;

[0033] FIG. 14 is a cross-sectional view of another embodiment of a transistor according to the present invention;

[0034] FIG. 15 is a cross-sectional view of another embodiment of a transistor according to the present invention;

[0035] FIG. 16 is a cross-sectional view of another embodiment of a transistor according to the present invention; and

[0036] FIG. 17 is a cross-sectional view of another embodiment of a transistor according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0037] The present invention provides structures, such as a dual-gate transistor or HEMT cascode structure, that provide lower feedback capacitance and improved linearity

at reduced complexity and cost. These structures, such as a GaN-based dual-gate HEMT, can provide high voltage, high current, and high gain operation with improved linearity. The present invention is generally directed to cascode structures wherein a second stage gate is separated from the barrier layer by a relatively thin spacer layer, causing the second stage to have a more negative threshold voltage than the first stage. In one embodiment, the second stage includes a cavity in a spacer layer which exposes the active region; a thin spacer layer is deposited over the active region, and the second stage gate fills the remainder of the cavity. The second stage gate can then be grounded, such as through a connection to the source, and the need for separately biasing the second stage gate is eliminated.

[0038] The present invention also provides transistor structures with a field plate placement which can improve the linearity of the transistor. Embodiments of the present invention are generally directed to transistor structures where a field plate is separated from the barrier layer by a relatively short distance, such as a relatively thin spacer layer. In some embodiments, the field plate can be separated from the active semiconductor layers by one spacer layer, while a thicker spacer layer can be maintained between the field plate and the gate. In another embodiment, a spacer layer can have variable thickness, with a relatively thin thickness between the field plate and the active semiconductor layers and a thicker thickness between the field plate and the gate. In some embodiments, the field plate can be placed in an aperture within a spacer layer in order to lessen the distance between the

field plate and the semiconductor layers. In some embodiments, the field plate can be separated from the semiconductor layers by a non-zero distance of about 1500Å or less.

[0039] It will be understood that when an element or layer is referred to as being "on", "connected to", "coupled to" or "in contact with" another element or layer, it can be directly on, connected or coupled to, or in contact with the other element or layer or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly on," "directly connected to", "directly coupled to" or "directly in contact with" another element or layer, there are no intervening elements or layers present. Likewise, when a first element or layer is referred to as being "in electrical contact with" or "electrically coupled to" a second element or layer, there is an electrical path that permits current flow between the first element or layer and the second element or layer. The electrical path may include capacitors, coupled inductors, and/or other elements that permit current flow even without direct contact between conductive elements. Further, terms such as "insulating" for example, can refer to materials that are fully insulating, semi-insulating, or that can be either.

[0040] It is also understood that, although the ordinal terms first, second, third, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a

second element could be termed a first element, without departing from the scope of the present invention.

[0041] Furthermore, relative terms, such as "lower" or "bottom" and "upper" or "top," may be used herein to describe the relationship of one element to another as illustrated in the drawings. It is understood that relative terms are intended to encompass different orientations of the device in addition to the orientation depicted in the drawings. For example, if the device in one of the drawings is turned over, features described as being on the "lower" side of an element would then be oriented on "upper" side of that element. The exemplary term "lower" can therefore describe both lower and upper orientations, depending of the particular orientation of the device. Similarly, if the device in one of the drawings is turned over, elements described as "below" or "beneath" other elements would then be oriented above those other elements. The exemplary terms "below" or "beneath" can therefore describe both an orientation of above and below.

[0042] The terminology used in the description of the invention herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used in the description of the invention and the appended claims, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It is also understood that the term "and/or" as used herein refers to and encompasses any and all possible combinations of one or more of the associated listed items.

It will be further understood that the terms "comprises" and "comprising," when used in this specification, specify the presence of stated steps, operations, features, elements, and/or components, but do not preclude the presence or addition of one or more other steps, operations, features, elements, components, and/or groups thereof.

[0043] Embodiments of the invention are described herein with reference to cross-section illustrations that are schematic illustrations of idealized embodiments of the invention. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments of the invention should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. The regions illustrated in the drawings are schematic in nature, and their shapes are not intended to illustrate the actual shape of a region of a device and are not intended to limit the scope of the invention unless explicitly stated otherwise. Further, lines that appear straight, horizontal, or vertical in the below drawings for schematic reasons will often be sloped, curved, non-horizontal, or non-vertical. Further, while the thicknesses of elements are meant to be schematic in nature. For example, a thickness of a field plate may be completely within an aperture or the thickness of the field plate may be such that the field plate completely fills the aperture.

[0044] Unless otherwise defined, all terms used in disclosing embodiments of the invention, including technical and scientific terms, have the same meaning as commonly understood by one of ordinary skill in the pertinent art and are not necessarily limited to the specific definitions known at the time of the present invention. Accordingly, these terms can include equivalent terms that are created after such time. It is further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the present specification and in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0045] FIG. 2 shows one embodiment of a HEMT 30 according to the present invention that is preferably Group-III nitride based, although other material systems can also be used. It should be noted that while the term HEMT is used herein for simplicity, the elements and concepts of the disclosed embodiments can be applied to many different types of transistors, including but not limited to Metal Semiconductor Field Effect Transistors (MESFETs) and Metal Oxide Semiconductor Heterostructure Field Effect Transistors (MOSHFETs). Group III nitrides refer to those semiconductor compounds formed between nitrogen and the elements in the Group III of the periodic table, usually aluminum (Al), gallium (Ga), and indium (In). The term also refers to ternary and tertiary compounds such as AlGaN and AlInGaN.

[0046] The HEMT 30 can comprise a substrate 32 which can be made from silicon carbide, sapphire, spinet, ZnO, silicon, gallium nitride, aluminum nitride, or any other material or combinations of materials capable of supporting growth of a Group-III nitride material. A nucleation layer 34 can be formed on the substrate 32 to reduce the lattice mismatch between the substrate 32 and the next layer in the HEMT 30, although this nucleation layer is not mandatory. The nucleation layer 34 can be approximately 1000 angstroms (Å) thick, although other thicknesses can be used. The nucleation layer 34 can comprise many different materials, with a suitable material being $Al_zGa_{1-z}N$ ($0<=z<=1$), and can be formed on the substrate 32 using known semiconductor growth techniques such as Metal Organic Chemical Vapor Deposition (MOCVD), Hydride Vapor Phase Epitaxy (HVPE), or Molecular Beam Epitaxy (MBE).

[0047] The substrate 32 can be made of many different materials with a suitable substrate being a 4H polytype of silicon carbide, although other silicon carbide polytypes can also be used including 3C, 6H and 15R polytypes. Silicon carbide has a much closer crystal lattice match to Group III nitrides than sapphire and results in Group III nitride films of higher quality. Silicon carbide also has a very high thermal conductivity so that the total output power of Group III nitride devices on silicon carbide is not limited by the thermal dissipation of the substrate (as may be the case with some devices formed on sapphire). Also, the availability of silicon carbide substrates provides the capacity for device isolation and reduced parasitic capacitance that make commercial devices possible. SiC substrates are available from Cree, Inc., of

Durham, North Carolina and methods for producing them are set forth in the scientific literature as well as in a U.S. Pat. Nos. Re. 34,861 to Davis et al.; 4,946,547 to Palmour et al.; and 5,200,022 to Kong et al.

[0048] The formation of a nucleation layer 34 can depend on the material used for the substrate 32. For example, methods of forming a nucleation layer 34 on various substrates are taught in U.S. Patents 5,290,393 to Nakamura and 5,686,738 to Moustakas, each of which are incorporated by reference as if fully set forth herein. Methods of forming nucleation layers on silicon carbide substrates are disclosed in U.S. Patents 5,393,993 to Edmond et al., 5,523,589 to Edmond et al., and 5,739,554 to Edmond et al., each of which is incorporated herein by reference as if fully set forth herein.

[0049] The HEMT 30 can further comprise a buffer layer 36 which can have high resistivity formed on the nucleation layer 34. The buffer layer 36 can comprise doped or undoped layers of Group III-nitride materials with a preferred buffer layer 36 made of a Group III-nitride material such as $Al_xGa_yIn_{(1-x-y)}N$ ($0<=x<=1$, $0<=y<=1$, $x+y<=1$). Other materials can also be used for the buffer layer 36 such as GaN that is approximately 0.5-20μm thick, and part or all of the buffer layer can be doped with Fe.

[0050] A barrier layer 38 is formed on the buffer layer 36 with the buffer layer 36 being sandwiched between the barrier layer 38 and the nucleation layer 34. Like the buffer layer 36, the barrier layer 38 can comprise doped or undoped layers of Group III-nitride materials. The barrier layer can be made of one or multiple layers of $Al_xGa_{1-x}N$ or

$Al_xIn_yGa_{1-x-y}N$, where each of x and y ranges from 0-1 with exemplary values being 0, 0.2, 0.4, 0.5, 0.6, 0.8, and 1, and x and y can be a function of depth such that the barrier layer 38 can be a graded layer. A 2DEG channel layer 40 can be induced at the heterointerface between the buffer layer 36 and the barrier layer 38, and the buffer layer 36, 2DEG channel layer 40 and barrier layer 38 can generally form the HEMT active region.

[0051] Exemplary HEMT structures are illustrated in U.S. Patent Nos. 6,316,793 to Sheppard et al., 6,586,781 to Wu et al., 6,548,333 to Smith and U.S. Published Patent Application Nos. 2002/0167023 to Prashant et al., and 2003/0020092 to Parikh et al., each of which is incorporated by reference as though fully set forth herein. Other nitride based HEMT structures are illustrated in U.S. Patents 5,192,987 to Kahn et al. and 5,296,395 to Kahn et al., each of which is incorporated herein by reference as if fully set forth herein. The buffer and barrier layers 36,38 can be made using the same methods used to grow the nucleation layer 34. Electric isolation between the devices can be accomplished through mesa etch or ion implementation outside the active HEMT.

[0052] Source and drain electrodes 42, 44 can be formed in contact with the barrier layer 38. Electric current can flow between the source and drain electrodes 42, 44 through the 2DEG channel layer 40 between the buffer layer 36 and the barrier layer 38 when a gate is biased at the appropriate level. The formation of source and drain electrodes 42, 44 is described in detail in the patents and publications referenced above.

[0053] A first stage gate 46 can be formed on the barrier layer 38, and can be at least partially surrounded by and within an aperture of a first spacer layer 50. The first spacer layer 50 can be many different thicknesses, with some exemplary layers being between 100nm and 2000nm. A second stage gate 48 can also formed on the barrier layer 38 and within an aperture in the first spacer layer 50.

[0054] The gates 46,48 can have many different lengths (L_{g1} and L_{g2}), with suitable gate lengths ranging from 10nm to 1000nm or approximately 500nm, although other gate lengths can also be used. In one embodiment, L_{g1} is shorter than L_{g2}; in another embodiment, the gate lengths are equal; in another embodiment, L_{g1} is longer than L_{g2}. In the embodiment shown, the gates 46,48 can be side by side, which can reduce parasitic capacitance. The gates 46,48 can be separated by a distance L_{gg}, which allows the second gate 48 to shield the first gate 46 as previously described. The distance L_{gg} can be many different values, with exemplary distances being between 10nm and 2000nm. In some embodiments L_{gg} can range from 600nm to 1200nm which can provide easier fabrication, and in some embodiments L_{gg} can be approximately 900nm.

[0055] As best shown in the combination of FIG. 2 and FIG. 3, a plan view of the FIG. 2 embodiment, the first gate 46 can be contacted at a first gate contact 47. In a preferred embodiment, the second gate 48 can be connected to the source 42, although other connections including various ground connections are possible. This connection can be achieved in a number of manners. FIG. 3 shows two such manners, although other manners are possible. The second

gate 48 can be connected to the source 42 by a series of conductive vias and/or buses 49a, which run through and/or on a third spacer layer 54 if such a layer is present. The third spacer layer 54 can be many different thicknesses, with one suitable range of thicknesses being approximately 100nm to 1000nm and another suitable range being approximately 150nm to 500nm, and in some embodiments the second spacer layer 54 can be 300nm thick. The third spacer layer 54 can cover all of the active region between the drain 44 and source 42, can cover just the portion of the active region between either edge of the second gate 48 and the source 42, can cover just the portion of the active region between the furthest edge of a field plate 56 and the source 42 if such a field plate is present (to be discussed below), or can cover only the surface of the active region needed to support conductive buses (e.g., strips with only a width necessary to support such buses).

[0056] The buses of the via/bus system 49a can be on the topmost surface of the HEMT 30. One or more buses can be used, with the FIG. 2 embodiment including two buses. The greater the area covered by the buses, the greater the unwanted capacitance that can be introduced by the buses. The buses can have a sufficient number and width so that current effectively spreads between the source 42 and the second gate 48 while not covering too much of the HEMT active region. In one embodiment, the buses of the via/bus system 49a cover less than all of the HEMT active region. In one embodiment, the second gate 48 and source 42 are connected by a conductive path, such as the via/bus system 49a, covering less than all of the topmost surface of the HEMT 30, in this case the third spacer layer 54.

[0057] In one embodiment, the second gate 48 can be connected to the source 42 by a conductive path 49b running outside the active region of the HEMT 30. In the FIGs. 2 and 3 embodiment, the conductive path 49b is on the side opposite the gate contact 47, although in other embodiments the conductive path can be on the same side as the gate contact 47, or there can be two or more conductive paths running on one or both sides of the HEMT 30. Conductive paths running outside the active region can be used in many different embodiments, but can be particularly useful in embodiments where a spacer layer does not cover the active region between the second gate 48 and the source 42 (e.g., an embodiment without the third spacer layer 54).

[0058] Another connection manner can include a via/bus system 49c. The system 49c can include one or more buses which run on the surface of the second spacer layer 52. If present, the third spacer layer 54 can then cover the buses 49c. HEMTs according to the present invention can include one or multiple of the conductive paths 49a,49b,49c shown in the FIGs. 2 and 3 embodiment, or can include other connection means.

[0059] In the FIG. 2 embodiment of the present invention, a second spacer layer 52 can be between the second stage gate 48 and the barrier layer 38. The second spacer layer 52 can comprise many different insulating materials, including but not limited to dielectrics. The second spacer layer 52 can comprise the same or different materials than the first spacer layer 50. Some exemplary materials for spacer layers 50,52,54 include, but are not limited to, SiN, SiO_2, Si, Ge,

MgO_x, MgN_x, ZnO, SiN_x, SiO_x, TiO_x, and combinations or layer sequences thereof.

[0060] As previously discussed, in prior art dual gate HEMTs the second gate must be separately DC biased, which can lead to excessive expense and complexity. By including the second spacer layer 52, the threshold voltage of the second gate 48 can be made different than that of the first gate 46, and in one embodiment can be more negative than the threshold voltage of the first gate 46. Because of this, the second gate 48 can be DC grounded, such as through connecting the second gate 48 to the source 42 as described above. This can eliminate the need for separate biasing of the second gate 48, and thus can eliminate at least some of the cost and manufacturing difficulty of prior art devices. Devices with a layer such as the second spacer layer 52 can also exhibit improved linearity and lower capacitance than prior art HEMTs and/or cascode structures.

[0061] The thickness of the second spacer layer 52 can be chosen such that feedback capacitance remains nearly constant over a wide range of drain voltages, while at the same time not limiting the maximum current flow of the device. An insulator that is too thick can lead to inadequate shielding of the first stage and large drain voltage dependence, while an insulator that is too thin can limit the maximum current (and therefore RF power). The second spacer layer 52 can have many different thicknesses. In some embodiments, the thickness can be determined based on the dielectric constant of the material. In some embodiments, the non-zero thickness of the second spacer

layer 52 is equal to or less than about 1500Å and/or ranges from 50Å to 1500Å. In other embodiments, the non-zero thickness is equal to or less than 800Å and/or ranges from 100Å to 800Å. In another embodiment, the thickness is approximately 300Å to 600Å and/or about 400Å. One embodiment of a second spacer layer 52 according to embodiments of the present invention is a 100Å to 800Å and/or approximately 400Å layer of SiN, SiO_2, or a combination thereof. Another embodiment of a second spacer layer 52 according to embodiments of the present invention is an 800-1500Å layer of TiO_x, which has a higher dielectric constant.

[0062] The HEMT 30 can be fabricated in many different ways. The first spacer layer 50, second spacer layer 52, and third spacer layer 54 can be deposited using many deposition methods including but not limited to those deposition methods previously mentioned, with preferred methods being plasma chemical vapor deposition (PCVD) and atomic layer deposition (ALD). In one preferred method, the first spacer layer 50 is deposited over the entire top surface between the source 42 and drain 44, and the apertures in which the gates will be deposited are formed, such as by using reactive ion etching (RIE). The first gate 46 can then be formed before the deposition of the second spacer layer 52 over the entire top surface of the HEMT 30 between the source 42 and drain 44. Alternatively, the second spacer layer 52 can be deposited only in the region of the second aperture in which the second gate 48 will be formed, such as depositing the second spacer layer 52 such that it only covers the exposed surface of the barrier layer 38 or only covers the exposed surface of the barrier

layer 38 and the side walls of the aperture. The second gate 48 can then be formed in the same aperture as the second spacer layer 52. The third spacer layer 54 can then be formed over the entire top surface of the HEMT 30 between the source 42 and drain 44, or can be deposited selectively in the areas described above.

[0063] As previously discussed, one or more field plates can optionally be used and can enhance device performance. Devices according to the present invention, such as the device shown in FIG. 2, are compatible with many different field plate arrangements. Some such field plate arrangements are discussed, for example, in the commonly assigned U.S. Pub. Nos. 2005/0253167, 2005/0253168, and 2006/0202272 to Wu et al., which are all fully incorporated by reference herein in their entirety. In the embodiment of FIGs. 2 and 3, a field plate 56 can be included on the third spacer layer 54 and can overlap the second gate 48. In other embodiments, the HEMT can include a space between the edge of the field plate and the edge of the second gate, or the field plate can cover the entire second gate. Examples of such field plate arrangements are described in the previously mentioned publications. In one embodiment, the field plate can be over the second gate 48 and/or between the second gate 48 and the drain 44. This can minimize the electric field at the edge of the second gate 48. Similar concepts are described in the commonly assigned U.S. Pat. No. 2005/0051800. In other arrangements, a field plate is provided between the source 42 and the first gate 46, over the first gate 46, and/or between the first and second gates 46,48. These field plates can also be used in

combination with field plates over the second gate 48 and/or between the second gate 48 and the drain 44.

[0064] In a preferred embodiment, the field plate 56 can be connected to the source 42, although other arrangements are contemplated. The field plate 56 can be connected using structures similar to the conductive structure 49a,49b. For example, the field plate 56 can be connected to the source 42 by conductive buses covering less than all of the third spacer layer 54, a conductive path running outside the active region of the HEMT 30, a combination thereof, or many other conductive structures. Source-connected field plates with examples of appropriate conductive structures are described, for example, in U.S. Pub. No. 2005/0253167. Additionally, the HEMT 30 can include more than one field plate. In one such arrangement, each of the multiple field plates can be either at least partially over the second gate or between the second gate and the drain. Some appropriate multiple field plate structures are described, for example, in U.S. Pub. No. 2005/0253168.

[0065] While the gates 46,48 shown in FIG. 2 are shown as rectangular, many different gate shapes are possible. FIG. 4 shows an embodiment of an HEMT 60 according to the present invention that includes a T-shaped first gate 66. The gate 66 includes overhanging sections 66a. The area below the overhanging sections 66a can be left empty, can be partially or entirely filled by a portion of the first spacer layer 61, or can be partially or entirely filled by another material or layer. In the FIG. 4 embodiment, this area can be entirely filled by a portion of the first spacer layer 61. The device 60 with the T-shaped gate 66

can be particularly adapted for high frequency operation. Gate length is an important device dimension in determining device speed, and with high frequency devices gate length is typically shorter. Shorter gate length can lead to high resistance that can negatively impact high frequency operation. By including the overhanging sections 66a, the upper portion of the gate 66 has a larger cross-section than the lower portion. This can result in lower resistance and enhanced gate conductance.

[0066] FIG. 5 shows an embodiment of an HEMT 70 according to the present invention that includes a gamma shaped first gate 76 instead of the T-shaped gate 66. The area below an overhanging section 76a can be left empty, can be filled by a portion of the first spacer layer 71, or can be filled by another material or layer. In the embodiment shown, the space is partially filled by the first spacer layer 71. Including a space below the overhanging section 76a can reduce capacitance between the first gate 76 and the source 42.

[0067] The overhanging sections 66a,76a can be made of the same or different materials than the remainder of the gates 66,76, and can be fabricated using many different methods. For example, overhanging sections can be fabricated using photo-resist techniques, and in one embodiment a photo-resist layer can be included on the first spacer layer and the overhanging section(s) formed on the photo-resist layer. Subsequent removal of the photo-resist layer can leave a space between the spacer layer and the overhanging section(s).

[0068] While the gates 66 and 76 are generally T-shaped and gamma shaped, respectively, it is understood that many different shapes are possible. One objective of including gates with these shapes is to include a section to improve conductivity to allow for higher frequency operation, with the section being enlarged to achieve this objective. Having a particular shape to the enlarged top portion may not be critical. The length of the overhangs 66a,76a can vary, with suitable lengths ranging from about 0.2μm to about 4μm, although other lengths can also be used. Further, while the embodiments of FIGs. 4 and 5 include T-shaped and gamma shaped first gates 66,76, other embodiments of the present invention include a T-shaped or gamma shaped second gate, or include a T-shaped or gamma shaped first gate and a T-shaped or gamma shaped second gate. If the second gate is T-shaped or gamma shaped, at least the bottom portion which would otherwise be directly on the barrier layer can be covered by a spacer layer 72 similar to or the same as the second spacer layer 52 from FIG. 2.

[0069] In addition to the T-shaped and gamma shaped gates 66,76 of FIGs. 4 and 5, many other gate shapes are possible. For example, gates with polygon cross-sections such as hexagonal, octagonal, and trapezoidal gates, for example, are possible. In one embodiment of an HEMT with one or more hexagon gates, the first spacer layer rises to the level of the midpoint of the hexagon. Another shaped gate has one or more overhangs like a T-shaped or gamma shaped gate, with a lower gate portion that tapers inward or outward as it rises to the upper portion of the gate.

[0070] Embodiments of HEMTs according to the present invention can also include one or more recessed gates. FIG. 6 shows an embodiment of a transistor according to the present invention similar to the HEMT 30 from FIGs. 2 and 3 (like reference numerals are used to indicate equivalent elements), but with recessed first and second gates 86,88. The gates 86,88 are recessed into the barrier layer 81. This recessed area can be formed at the same time as the apertures in the first spacer layer 50. In this embodiment, the second spacer layer 82 can cover at least the bottom of the second gate 88 and the side portions of the gate 88 within the recess in the barrier layer 81. The second spacer layer 82 can be the same or similar materials and thickness as the second spacer layer 52 from FIGs. 2 and 3. While the gates 86,88 are shown as only partially recessed into the barrier layer 81, each of the gates 86,88 could be fully recessed or different portions could be recessed to different depths in the barrier layer 81. Additionally, the gates 86,88 do not both need to be recessed, or can be recessed differently. Recessed T-shaped gates and gamma shaped gates are also possible, where part or all of the lower portion of the gate (e.g. the portion from the bottom of the overhang(s) and below) can be recessed into the barrier layer.

[0071] FIG. 7 shows another embodiment of a device according to the present invention. The HEMT 90 is similar to the HEMT 30 from FIGs. 2 and 3 in many respects. The HEMT 90 comprises a first gate 46 and a second gate 98. Similar to the first gate in the HEMT 30, the first gate 46 in the HEMT 90 is formed in an aperture in a first spacer layer 91, such that the first gate 46 is in contact with

the barrier layer 38. However, in the HEMT 90 the second gate is formed on a top surface of the first spacer layer 91 instead of in an aperture in the first spacer layer 91. The first spacer layer 91 can be made of any of the spacer layer materials previously discussed. The HEMT 90 may produce a higher parasitic capacitance C_{gd} than the HEMT 30 of FIGs. 2 and 3, such as for example at low drain voltages, but can have reduced cost and difficulty of manufacture.

[0072] FIG. 8 shows another embodiment of a device according to the present invention. The HEMT 100 is similar in many respects to the HEMT 30 shown in FIGs. 2 and 3 and described above. The HEMT 100 comprises a first gate 46 and a second gate 48. However, an insulating layer such as the second spacer layer 52 from FIG. 2 can be excluded from the HEMT 30. The second gate 48 can instead be separated from the barrier layer 38 by a thin section 110a of the first spacer layer 110. The first spacer layer 110 can be made of the same materials as the first spacer layer 50 from FIG. 2, and excluding the thin section 110a can have the same or similar thickness as the first spacer layer 50. The thin section 110a can have the same or similar thickness as the second spacer layer 52 from FIG. 2. One possible manufacturing method of the HEMT 100 includes placing a first gate 46 on or in the barrier layer 38, depositing the first spacer layer 110, and then etching a portion of the first spacer layer 110 to form the thin section 110a before depositing the second gate 48 on the thin section 110a. Alternatively, the first spacer layer 110 can be deposited before the first gate 46, and an aperture can be etched all the way to the barrier layer 38 to allow for placement of

the first gate 46. The first spacer layer 110 can also be partially etched to form a second aperture, with the thin section 110a remaining, for placement of the second gate 48. The remainder of the structure can be fabricated as described above.

[0073] FIG. 9 shows another embodiment of a device according to the present invention. The HEMT 120 is similar in many respects to the HEMT 100 shown in FIG. 8 and described above. In this embodiment, a first spacer layer 122 can be deposited in the region where the second gate 48 is to be placed (instead of, for example, depositing the first spacer layer 122 across the entire cross-section from the source 42 to the drain 44). The second gate 48 can then be placed on the first spacer layer 122 and the first gate 46 can be placed on the barrier layer 38. A second spacer layer 124 can then be deposited over both the first and second gates 46,48 with the remainder of the device being fabricated as described above.

[0074] While the above embodiments show dual-gate transistor structures, elements of the above embodiments can be applied to other structures. For example, one example of a cascode structure according to the present invention includes a cascode amplifier structure as described in the commonly assigned U.S. Pub. No. 2005/0051800 including two separate single-gate transistors, with a spacer layer similar to the second spacer layer 52 incorporated into the downstream of the two transistors.

[0075] The above embodiments and variations thereof can also be utilized in many different ways. For example, the

cascode structures can function as amplifiers, similar to those described in U.S. Pat. App. No. 2005/0051800. The above embodiments can also function as part of a larger system. For example, the above embodiments can function within integrated circuits such as monolithic microwave integrated circuits (MMICs).

[0076] FIG. 10 shows another embodiment of a device according to the present invention. The HEMT 130 can be similar to the HEMT 10 from FIG. 1A, and contain similar elements (marked with equivalent reference numerals). The HEMT 130 can include a gate 136 which can be surrounded by a first spacer layer 131. The gate 136 can have a gate length L_g that can vary, with suitable gate lengths ranging from 10nm to 1000nm or approximately 400nm, although other gate lengths can be used. In the HEMT 130, at least a portion of the spacer layer 131 can cover the gate 136, although in other embodiments the first spacer layer does not cover the gate.

[0077] An aperture 137 can be formed within the first spacer layer 131. The aperture 137 can have a length L_a similar in length to L_g, with one preferred embodiment having a length of approximately 500nm. In one embodiment, L_g is shorter than L_a. In one such embodiment L_g is approximately 400nm and/or L_a is approximately 500nm. In another embodiment, L_g and L_a are equal. In yet another embodiment, L_g can be larger than L_a. While FIG. 10 shows an embodiment having a single aperture 137, multiple apertures are possible.

[0078] The aperture 137 can expose a portion of the barrier layer 18. A second spacer layer 132 can at least partially,

and in some embodiments fully, cover the portion of the barrier layer 18 exposed by the aperture 137. The second spacer layer 132 can have many of the same attributes as the second spacer layer 52 from FIG. 2, including having similar or the same thicknesses and materials. In some embodiments, the non-zero thickness of the second spacer layer 132 is equal to or less than about 1500Å or ranges from 50Å to 1500Å. In other embodiments, the non-zero thickness is equal to or less than 800Å and/or ranges from 100Å to 800Å. In another embodiment, the thickness is approximately 300Å to 600Å and/or about 400Å. One embodiment of a second spacer layer 132 according to embodiments of the present invention is a 100Å to 800Å and/or approximately 400Å layer of SiN, SiO_2, or a combination thereof, although other materials are possible. Another embodiment of a second spacer layer 132 according to embodiments of the present invention is an 800-1500Å layer of TiO_x, which has a higher dielectric constant. If a second aperture is present, a thicker spacer layer can be present in the aperture nearer the gate, with one exemplary thickness of a spacer layer being 1000Å.

[0079] The second spacer layer 132 can be deposited selectively, such that the second spacer layer 132 only covers the exposed portion of the barrier layer 18, or such that the second spacer layer 132 only covers the exposed portion of the barrier layer 18 and the sidewalls of the aperture 137. Alternatively and in the embodiment shown in FIG. 10, the second spacer layer can be deposited across the entire distance between the source 22 and the drain 24 for ease of manufacture. The combination of the first spacer layer 131 and the second spacer layer can provide a

larger separation distance between the field plate 138 and the gate 136 than exists between the field 138 and the active semiconductor layers, such as the barrier layer 18. In other embodiments, something other than a spacer layer can provide one or both of these separations.

[0080] The HEMT 130 can also include a field plate 138. In the embodiment shown the field plate 138 is at least partially, and sometimes fully, between the gate 136 and the drain 24, although other embodiments are contemplated. The field plate 138 can at least partially cover the bottom portion of the aperture 137, and thus the portion of the second spacer layer 132 on the barrier layer 18 can at least partially be sandwiched between barrier layer 18 and the field plate 138. In other embodiments, the portion of the second spacer layer 132 is at least partially sandwiched between another active semiconductor layer and the field plate 138. In one embodiment the field plate 138 can cover at least the entire bottom of the aperture 137, as shown in FIG. 10, although other embodiments are contemplated. The field plate 138 can extend past the bottom and up the side of the aperture 137 and further toward the drain 24, as shown in the FIG. 10 embodiment, and in one such embodiment extends toward the drain 24 on the first spacer layer 131 outside of the aperture 137. In some transistors, an electric field can peak at the edge of a field plate. Embodiments where the field plate, such as the field plate 138, extends past the floor of the aperture 137 and up the drain-side of the aperture 137 can have decreased trapping and a lesser chance of breakdown. One explanation for this is that the edge of the field plate 138 is separated from the barrier layer 18 by a larger

distance. In one such embodiment the field plate 138 can extend outside the aperture 137 and toward the drain 24 over the first spacer layer 131. Embodiments with a field plate extending past the edge of the aperture can be more easily manufactured.

[0081] In the conventional prior art HEMT 10 from FIG. 1A, the field plate 28 is on the first spacer layer 21, which can limit how close the field plate 28 can be deposited to the active semiconductor layers. In the HEMT 130, due at least in part to the presence of the aperture 137 in the first spacer layer 131, at least a portion of the field plate 138 is separated from the active semiconductor layers by only the second spacer layer 132. As discussed above, the second spacer layer 132 can have a thickness less than that of the first spacer layer 131 or the first spacer layer 21 from FIG. 1A. By reducing the insulator thickness separating the field plate 138 from the active semiconductor layers, the drain bias dependence of the parasitic capacitance C_{gd} can be reduced. This can result in higher device linearity.

[0082] The field plate 138 can also extend toward the gate 136. In the embodiment shown, the field plate 138 extends past the nearest edge 136a of the gate 136. This arrangement can provide ease of manufacturing over other embodiments where a gap can be left between a gate and a field plate. Many other gate/field plate arrangements are possible, including the arrangements disclosed in the commonly assigned U.S. Pat. No. 7,550,783 to Wu et al. and entitled "Wide Bandgap HEMTs with Source Connected Field Plates," U.S. Pat. Pub. No. 2005/0253167 to Wu et al. and

entitled "Wide Bandgap Field Effect Transistors with Source Connected Field Plates," and U.S. Pat. Pub. No. 2006/0202272 to Wu et al. and entitled "Wide Bandgap Transistors with Gate-Source Field Plates", all three of which are fully incorporated by reference herein in their entirety. In some embodiments, the edge of the field plate 136 can be even with the edge 136a of the source, or the field plate 136 can stop short of extending to the edge 136a. Some alternative field plate arrangements will be discussed in detail below.

[0083] Some embodiments of transistors according to the present invention can include a relatively thin insulating layer (e.g., the second spacer layer 132) separating a field plate (e.g., the field plate 138) from a barrier layer, while still maintaining a relatively thick insulating layer or layers between the field plate and the gate. Such embodiments can generate the advantages of having a field plate near the active semiconductor layers, such as reducing the drain bias dependence which can increase linearity, while avoiding or reducing the complications of the field plate being too near the gate (e.g., avoiding a reduction in the breakdown voltage of the device). In the FIG. 10 embodiment, the field plate 138 is separated from the gate 136 by a portion of the first spacer layer 131 having a thickness L_s in addition to a portion of the second spacer layer 132. The thickness L_s can have many different values, with exemplary thicknesses being between 100Å to 2000Å, although other thicknesses are possible. In one embodiment, the thickness L_s can be between 400Å and 1200Å, with one exemplary thickness being approximately 800Å. If the thickness L_s is chosen properly,

some or all of the benefits of a second field plate can be realized without actually depositing the second field plate, leading to a reduction in manufacturing difficulty and cost.

[0084] In a preferred embodiment, the field plate 138 is connected to the source 22, although other connections are possible. The connection to the source 22 can be achieved in a number of manners, including but not limited to those described above with regard to connecting the second gate 48 of FIG. 3 to the source. For example, the field plate 138 can be connected to the source 22 can be connected to the source using a via/bus system. If the field plate 138 is on the top surface of the transistor, then one embodiment uses only buses. Conductive buses connecting the field plate 138 to the source 22 can be on the topmost surface of the HEMT 130. One or more buses can be used, with one embodiment including two buses. The greater the area covered by the buses, the greater the unwanted capacitance that can be introduced by the buses. The buses can have a sufficient number and width so that current effectively spreads between the source 22 and the field plate 138 while not covering too much of the HEMT active region. In one embodiment, the buses cover less than all of the HEMT active region. In one embodiment, the buses cover less than all of the topmost surface of the HEMT 130.

[0085] In one embodiment, the field plate 138 can be connected to the source 22 by a conductive path running outside the active region of the HEMT, similar to or the same as the conductive path 49b shown in FIG. 3. Conductive paths running outside the active region can be used in many

different embodiments, but can be particularly useful in embodiments where a spacer layer does not cover the active region between the field plate 138 and the source 22 and/or in embodiments using a gamma or T-shaped gate. Any combination of connection means can be used.

[0086] Devices according to the present invention can be manufactured using many different methods. After the formation of the source 22, gate 136, and drain 24, the first spacer layer 131 can be deposited using one of many deposition and/or growth techniques, such as PECVD (Plasma Enhanced Chemical Vapor Deposition). If necessary, the first spacer layer 131 can be patterned such that it remains principally on the active region of the HEMT 130, such that the source 22, gate 136, and drain 24 are available for contact. The first spacer layer 131 can then be etched to form the aperture 137; this step can be performed using, for example, a photo resist and/or any dry or wet etch process, although other processes are possible. The field plate 138 can then be deposited, such as by metal evaporation or many other methods. If necessary, additional spacer layers and/or field plates can be produced over the device shown in FIG. 10. This represents only one method of manufacturing the HEMT 130, as many other methods are possible. Some exemplary methods are described in U.S. Pat. No. 7,812,369 to Chini et al. and entitled "Fabrication of Single or Multiple Gate Field Plates," which is fully incorporated by reference herein in its entirety.

[0087] The device shown in FIG. 10, as well as the devices shown in FIGs. 11-17, can exhibit characteristics similar to two transistor structures such as cascode structures,

and/or can exhibit characteristics similar to the transistor structures shown above in FIGs. 2-9. The drain bias applied across the entire transistor can be distributed between a common source first stage and a common second gate stage. The common gate stage which can be formed through the inclusion of the field plate can absorb drain feedback capacitance C_{gd} or shield the first stage from this capacitance across a wide range of drain biases, and can also increase linearity. As the distance between the field plate and the semiconductor layers is lowered, the threshold voltage of the second stage can be lowered, which can allow the common gate stage to shield C_{gd} at lower values of drain bias.

[0088] FIG. 11 shows another embodiment of a device according to the present invention. The HEMT 140 is similar in many respects to the HEMT 130 shown in FIG. 10 and described above. An insulating layer such as the second spacer layer 132 from FIG. 2 can be excluded from the HEMT 140. The field plate 148 can instead be separated from the barrier layer 18 by a thin section 141a of the first spacer layer 141. The first spacer layer 141 can be made of the same materials as the first spacer layer 50 from FIG. 2. The thin section 141a can have the same or similar thickness as the second spacer layer 132 from FIG. 10. One possible manufacturing method of the HEMT 140 is very similar to the manufacturing method described above for the HEMT 100 from FIG. 8, but includes depositing the field plate 138 in the aperture 137 instead of the second gate of FIG. 8.

[0089] FIG. 11 also shows a gate/field plate arrangement that differs from the FIG. 10 embodiment. In the FIG. 11 embodiment, the field plate 148 does not extend over the gate, but instead is separated from the edge of the gate by a distance L_{gf}. The distance L_{gf} between the edge of the field plate 148 and the edge of the gate 146 can be wide enough to isolate the field plate 148, while being small enough to maximize the field effect provided. If L_{gf} is too wide the field effect can be reduced. In one embodiment, L_{gf} can be approximately 0.4 microns or less, although larger and smaller values are possible. While the FIG. 11 embodiment includes a distance L_{gf}, the arrangement discussed above with regard to a thin section 141a of the first spacer layer 141 can be used with any gate/field plate arrangement, including an arrangement where the field plate overlaps the gate. Further, while the aperture 137 in FIGs. 11-14, 16, and 17 are shown with vertical sidewalls, this is purely schematic, as sidewalls in any of these embodiments can be vertical, sloped, or a combination thereof. Sloped sidewalls can improve field plate deposition.

[0090] FIG. 12 shows another embodiment of a device according to the present invention. The HEMT 150 can include a T-shaped gate 156. While the FIG. 12 embodiment shows a T-shaped gate 156, many other shaped gates are possible, including but not limited to other gate shapes including overhangs such as a gamma shaped gate. A first section 151a of a first spacer layer 151 fills the areas below the overhangs of the gate 156. The first spacer layer 151 can have many of the same characteristics as the first spacer layer 131 from FIG. 10, including having the same or

similar thicknesses and/or materials. A second section 151b of the first spacer layer 151 can be deposited selectively over the T-shaped gate 156, or can be deposited over the entire length between the source 22 and the drain 24. The second section 151b can be made of the same or different materials than the first section 151a. One method of manufacture includes depositing the first section 151a of the first spacer layer 151, etching an aperture to allow for the deposition of the T-shaped gate 156, and then depositing the second section 151b of the first spacer layer 151 over the T-shaped gate 156. A second aperture 157 can be formed in the first spacer layer 151a to allow for placement of the field plate 158.

[0091] The second section 151b (and, if present over the gate 156 and as shown in FIG. 12, the second spacer layer 152) can serve to separate the gate 156 from the field plate 158, which can achieve the benefits previously discussed. The second section 151b can have a thickness the same as or similar to the thickness L_s, discussed above with regard to FIG. 10. Thus, the field plate 158 can be separated from the gate 156 by a greater distance than the barrier layer 18, allowing for isolation between the field plate 158 and gate 156 while realizing the benefits of having the field plate 158 near the barrier layer 18.

[0092] Many variants on the FIG. 12 embodiment are possible. For instance, in the embodiment shown, since the second section 151b is only deposited selectively over the T-shaped gate 156, only the first section 151a needs to be etched to allow for deposition of the second spacer layer 152 and the field plate 158 on the barrier layer 18.

Alternatively, as shown in FIG. 11, the first section 151a could be etched such that only a thin section remained, and the thin section could serve the same functional purpose as the second spacer layer 152. Alternatively, the second section 151b could be deposited over the entire area between the source 22 and drain 24. In one such embodiment, the second section 151b could be etched to leave only a thinned portion, which could serve the same functional purpose as the second spacer layer 152. In another variant on the FIG. 12 embodiment, a space is left beneath the overhang(s) of a shaped gate, as discussed above with regard to FIG. 5.

[0093] FIG. 13 shows another embodiment of a device according to the present invention. The HEMT 160 includes first and second spacer layers 161,162. The second spacer layer 162 can be similar to or the same as the second spacer layer 132 from FIG. 10 in many respects, including but not limited to material and thickness. In the embodiment shown, the first spacer layer 161 may not cover the gate 166. In such embodiments, the first field plate 168 may only be isolated from the gate 166 by the second spacer layer 162. This arrangement can provide a reduction in manufacturing difficulty and cost, as the first spacer layer does not necessarily need to be arranged on top of the gate 166.

[0094] In addition to first and second spacer layers 161,162 and a first field plate 168, the transistor 160 can include a second field plate 169, which can be on a third spacer layer 163. The third spacer layer 163 can cover the entire first field plate 168, as shown in FIG. 13.

Alternatively, the third spacer layer 163 should cover enough of the first field plate 168 to provide isolation between the first and second field plates 168,169. The first and second field plates 168,169 can overlap as shown in FIG. 13, or there can be a gap between the edges of the first and second field plates 168,169. The first and second field plates 168,169 can both be connected to the source using any of the connection means previously described, although other arrangements including gate connections are contemplated. This multiple field plate arrangement can further reduce the peak electric field in the device, resulting in increased breakdown voltage and reduced trapping. Multiple field plate arrangements are discussed in detail in the commonly assigned U.S. Pub. No. 2005/0253168 to Wu et al. and entitled "Wide Bandgap Transistors with Multiple Field Plates," and U.S. Pub. No. 2006/0202272 to Wu et al. and entitled "Wide Bandgap Transistors with Gate-Source Field Plates," each of which is fully incorporated by reference herein in its entirety. These field plate arrangements can be utilized in any of the embodiments discussed herein, and may be particularly useful when a first spacer layer (e.g., the first spacer layer 161 from FIG. 13) does not cover the gate such that only a second spacer layer (e.g., the second spacer layer 162) separates the gate and field plate.

[0095] Embodiments of the present invention can also include a gate and/or a field plate which are recessed into the barrier layer. The gate 166 from FIG. 13 can be recessed into the barrier layer 164 in an arrangement similar to or the same as the gate 86 and the barrier layer 81 from FIG. 6. The HEMT 160 also includes a field plate

which is recessed into the barrier layer 164. In the embodiment shown, an aperture 167 in the first spacer layer 161 in which parts of the second spacer layer 162 and the first field plate 168 can be placed is partially recessed into the barrier layer 164. The second spacer layer 162 and first field plate 168 can therefore be recessed into the barrier layer 164, with the second spacer layer 162 sandwiched between the first field plate 168 and the barrier layer 164. The second spacer layer 162 can cover at least the bottom of the aperture 167 and the sides of the section of the aperture 167 recessed into the barrier layer 164.

[0096] Embodiments of the present invention can also include buried field plates, or field plates which are at least partially, and sometimes fully, located under a gate overhang. FIG. 14 shows another embodiment of a device according to the present invention. The device 170 includes a T-shaped gate 176 with one overhang 176a longer than the other overhang 176b, although other gate shapes including at least one overhang can also be used. An aperture 177 can be formed in a first spacer layer, where a second spacer layer 172 and a field plate 178 can be at least partially deposited. The second spacer layer 172 can be similar to or the same as the second spacer layer 132 from FIG. 10 in many ways, including but not limited to material and thickness. The second spacer layer 172 can separate the field plate 178 from the barrier layer 18. As shown in FIG. 14, the field plate 178 can be deposited at least partially under the overhang 176a, and can be connected to the source using any of the connection means previously described. One particularly applicable connection means includes a

connection running outside the active region of the transistor 170.

[0097] In some embodiments of the present invention, an aperture 177 in a first spacer layer 171 and/or a field plate 178 can be located completely under a gate overhang. In one embodiment, a space remains between the field plate 178 and the gate overhang 176a. In another embodiment, a third spacer layer 173 (shown in phantom) can be deposited such that it occupies the space between the bottom of the gate overhang 176a and the field plate 178. The third spacer layer 173 can also cover the entire structure between source and drain, as shown in FIG. 14.

[0098] While in the FIG. 14 embodiment a portion of the first spacer layer 171 remains under the overhang 176a, in other embodiments no section of the spacer layer 171 remains under the overhang 176a. In such embodiments, the field plate 176 can still be isolated from the gate 176, such as by leaving one or more gaps between the field plate 178 and the gate 176, for example.

[0099] Buried field plate arrangements such as those described above can result in a reduced peak electric field, gate-to-source capacitance, and gate-to-drain capacitance, while also increasing gate conductance. Some buried field plate arrangements which can be incorporated into embodiments of the present invention are discussed generally in commonly assigned U.S. Pat. Pub. No. 2008/0128752 to Wu and entitled "GaN Based HEMTs with Buried Field Plates," which is fully incorporated by reference herein in its entirety.

[00100] In some embodiments, the first spacer layer and second spacer layer can be combined into a single spacer layer which has uneven thickness. FIG. 15 shows another embodiment of a transistor 180 according to the present invention. The transistor 180 can include an uneven spacer layer 182, which can include a thin portion 182a and a thick portion 182b. The thin portion 182a can have a thickness similar to or the same as the second spacer layer 132 from FIG. 10, while the thick portion 182b can have a thickness similar to or the same as the first spacer layer 131 from FIG. 10. The thin portion 182a can separate a field plate 188 from a barrier layer 18, while the thick portion 182b can separate the field plate 188 from a gate 186. Such embodiments can generate the advantages of having a field plate near the active semiconductor layers, such as reducing the drain bias dependence which can increase linearity, while avoiding or reducing the complications of the field plate being too near the gate (e.g., a reduction in the breakdown voltage of the device). The section of the thin portion 182 not covered by the field plate 188 can then optionally be covered by a second spacer layer 183, which can prevent trapping. In the embodiment shown, the second spacer layer 183 can be deposited over the entire length between the source and drain for ease of manufacturing.

[00101] In an alternative embodiment to FIG. 15, the spacer layer 182 is deposited with thicker portions adjacent the drain and the gate, with a thinner portion forming a "valley" between the two thicker portions. This can reduce the need for an additional spacer layer. In one such

embodiment, a field plate can cover the entire thinner portion or valley between the two thicker portions.

[00102] Some embodiments can include a spacer layer that is shaped to define more than one aperture. FIG. 16 shows another embodiment of a transistor 190 according to the present invention. The transistor 190 includes a first spacer layer 191 which is shaped to define two apertures 197a,197b. Both apertures 197a,197b can be at least partially filled by another spacer layer. In the embodiment shown, both apertures 197a,197b are filled by a second spacer layer 192, which can be similar to or the same as the second spacer layer 132 from FIG. 10 in many characteristics including material and thickness. In another embodiment, separate spacer layers partially fill each aperture. In one embodiment, the portion of the spacer layer 192b in the aperture 197b nearer the gate 196 can be thicker than the portion of the spacer layer 192a in the aperture 197a further from the gate 196. In one such embodiment, the thickness 192a can be approximately 100Å to 800Å or approximately 400Å, while the thickness 192b can be approximately 500Å to 1500Å or approximately 1000Å. In the embodiment shown, a field plate 198 can at least partially fills both apertures 197a,197b. In other embodiments, separate field plates can fill separate apertures.

[00103] FIG. 17 shows an embodiment of a transistor 200 according to the present invention that is similar in many respects to the transistor 150 in FIG. 12. In the FIG. 17 embodiment, both a first section 201a and second section 201b are deposited over the transistor from source 22 to drain 24. In this embodiment, both the first and second

sections 201a,201b can be etched to form an aperture 207 in which a spacer layer 202 and field plate 208 can be deposited. Because the field plate 208 can extend onto the top of the section 201b, it can be separated from the barrier layer 18 by a larger distance, which can reduce the field effect on the semiconductor layers and reduce trapping. As with all of the FIGs. 10-16 embodiments, the transistor 200 can include an additional spacer layer over the field plate 208 and/or include an additional field plate, such as in a configuration similar to that of FIG. 13.

[00104] The transistor 200 can be manufactured using many different methods. In one method, the first section 201a of the first spacer layer 201 is grown or deposited on the barrier layer 18. The first section 201a can be etched and the gate 156 can be deposited on the barrier layer 18. The metal forming the gate 156 can be patterned to extend across the first section 201a so as to form a T-shaped or gamma-shaped gate. The second section 201b can then be deposited or grown over the length of the transistor 200 between the source 22 and drain 24, and can cover the gate 156. Alternatively, the second section 201b can be deposited selectively, such as over the gate 156, instead of over the entire length of the transistor 200. This alternate method can produce a transistor similar to the transistor 150 from FIG. 12. In the FIG. 17 embodiment, the first and second sections 201a,201b of the first spacer layer 201 can be etched to form an aperture 207, which can expose the barrier layer 18. The second spacer layer can then be deposited, for example over the entire length of the transistor 200 between the source 22 and the drain 24,

such that the second spacer layer can cover at least the bottom of the aperture 207. A field plate 208 can then be deposited at least partially within the aperture 207. This is only one manufacturing method, and many other methods are possible. Some manufacturing methods which can be used to form devices according to the present invention are described in U.S. Pat. No. 7,812,369.

[00105] Any of the gate/field plate arrangements discussed in the present application, including those shown in FIGs. 10-17, can be interchanged with one another. For example, the field plate 148 in FIG. 11 could be substituted for the field plate 138 in FIG. 10, and such a device could have the benefits derived from maintaining a gap between the gate and field plate edge without sacrificing the benefits of the other aspects of the FIG. 10 embodiment (e.g., the benefit of the field plate being near the barrier layer). Single field plate embodiments described above could also include multiple field plates, including but not limited to arrangements discussed with regard to FIG. 13 and in the commonly assigned U.S. Pub. Nos. 2005/0253168 and 2006/0202272. Any of the FIGs. 10-17 embodiments could contain two or more and/or multiple apertures, as shown in FIG. 16. Mutually exclusive elements in any two of the above embodiments can be substituted for one another (e.g., a T-shaped gate substituted for a rectangular gate), and non-mutually exclusive elements can be added to an embodiment (e.g., a second aperture added to any of FIGs. 10-17). These represent only a few variations, and in embodiments of the present invention, as many different variations are possible.

[00106] Many variations of the features of the above embodiments are possible. Transistor structures with features that may be used in embodiments of the present invention are disclosed in the following commonly assigned publications, the contents of each of which are fully incorporated by reference herein in their entirety: U.S. Pat. No. 6,849,882 to Chavarkar et al. and entitled "Group-III Nitride Based High Electron Mobility Transistor (HEMT) With Barrier/Spacer Layer"; U.S. Pat. No. 7,230,284 to Parikh et al. and entitled "Insulating Gate AlGaN/GaN HEMT"; U.S. Pat. No. 7,501,669 to Parikh et al. and entitled "Wide Bandgap Transistor Devices With Field Plates"; U.S. Pat. No. 7,126,426 to Mishra et al. and entitled "Cascode Amplifier Structures Including Wide Bandgap Field Effect Transistor With Field Plates"; U.S. Pat. No. 7,550,783 to Wu et al. and entitled "Wide Bandgap HEMTs With Source Connected Field Plates"; U.S. Pat. No. 7,573,078 to Wu et al. and entitled "Wide Bandgap Transistors With Multiple Field Plates"; U.S. Pat. Pub. No. 2005/0253167 to Wu et al. and entitled "Wide Bandgap Field Effect Transistors With Source Connected Field Plates"; U.S. Pat. Pub. No. 2006/0202272 to Wu et al. and entitled "Wide Bandgap Transistors With Gate-Source Field Plates"; U.S. Pat. Pub. No. 2008/0128752 to Wu and entitled "GaN Based HEMTs With Buried Field Plates"; U.S. Pat. Pub. No. 2010/0276698 to Moore et al. and entitled "Gate Electrodes For Millimeter-Wave Operation and Methods of Fabrication; U.S. Pat. Pub. No. 2012/0049973 to Smith, Jr. et al. and entitled "High Power Gallium Nitride Field Effect Transistor Switches"; and U.S. Pat. Pub. No. 2012/0194276 to Fisher and entitled "Low Noise Amplifiers Including

Group III Nitride Based High Electron Mobility Transistors."

[00107] It is understood that the above arrangements can be applied to other transistors beyond HEMTs, including MESFETs and Metal Oxide Semiconductor Heterostructure Field Effect Transistor (MOSHFET), whether these transistors are single-gate transistors with one or more field plates, discrete dual-gate transistors, or part of a larger structure. The arrangements can also be applied to microwave and millimeter-wave power amplifiers for communication, instrumentation, military applications and so forth, including but not limited to monolithic microwave integrated circuits (MMICs).

[00108] Although the present invention has been described in considerable detail with reference to certain preferred configurations thereof, other versions are possible. The buried field plate and gate arrangement can be used in many different devices. The field plates and gates can also have many different shapes and can be connected to the source contact in many different ways. Accordingly, the spirit and scope of the invention should not be limited to the preferred versions of the invention described above.

We Claim:

1. A transistor, comprising:
a plurality of semiconductor layers on a substrate;
a source and a drain on at least one of said semiconductor layers;
a gate between said source and drain; and
a field plate;
wherein a separation between said field plate and said semiconductor layers is smaller than a separation between said field plate and said gate.

2. The transistor of claim 1, further comprising one or more spacer layers;
wherein said field plate is on at least one of said spacer layers;
wherein a first portion of said one or more spacer layers separates said field plate from said gate;
wherein a second portion of said one or more spacer layers separates said field plate from said semiconductor layers.

3. The transistor of claim 2, wherein said second portion is less than or equal to about 1500Å.

4. The transistor of claim 2, wherein said second portion is approximately 100Å to 800Å.

5. The transistor of claim 1, wherein at least one of said spacer layers is shaped to define an aperture; and
wherein said field plate is at least partially within said aperture.

6. The transistor of claim 5, wherein at least part of said second portion defines the bottom of said aperture.

7. The transistor of claim 5, wherein said field plate covers the bottom of said aperture.

8. The transistor of claim 1, wherein said field plate is at least partially over said gate.

9. The transistor of claim 1, wherein said field plate is separated from said gate by a first spacer layer and from said semiconductor layers by a second spacer layer.

10. The transistor of claim 1, wherein said field plate is connected to said source.

11. The transistor of claim 1, wherein said gate comprises one or more overhangs.

12. The transistor of claim 11, wherein a first spacer layer separates at least one of said overhangs from said semiconductor layers;

wherein a second spacer layer separates said field plate from said semiconductor layers; and

wherein a third spacer layer separates said field plate from said gate.

13. The transistor of claim 12, wherein the thickness of said second spacer layer is less than or equal to about 1500Å.

14. The transistor of claim 1, wherein said field plate is separated from a nearest edge of said gate by a gap with a length L_{gf}.

15. The transistor of claim 1, wherein at least part of said field plate is recessed below a top surface of said semiconductor layers.

16. The transistor of claim 1, where the placement of said field plate improves the linearity of said transistor.

17. A transistor, comprising:

a plurality of semiconductor layers on a substrate;

a source and a drain on at least one of said semiconductor layers;

a gate between said source and drain;

a spacer layer on said semiconductor layers, wherein said spacer layer is shaped to define an aperture;

a field plate at least partially within said aperture.

18. The transistor of claim 17, wherein a section of said semiconductor layers is exposed by said aperture;

further comprising a second spacer layer on said exposed section.

19. The transistor of claim 18, wherein said second spacer layer is at least partially sandwiched between said field plate and said exposed section.

20. The transistor of claim 17, wherein said field plate is separated from said semiconductor layers by a non-zero distance of about 1500Å or less.

21. The transistor of claim 17, wherein a section of said semiconductor layers is exposed by said aperture;

wherein said field plate is over said exposed section.

22. The transistor of claim 17, wherein the length of said aperture is larger than the length of said gate.

23. The transistor of claim 17, wherein a section of said spacer layer forms the bottom of said aperture.

24. The transistor of claim 17, wherein said gate comprises one or more overhangs;

wherein said field plate is at least partially below one of said overhangs.

25. The transistor of claim 17, wherein said spacer layer is shaped to define two or more apertures.

26. A transistor, comprising:

a plurality of semiconductor layers formed on a substrate;

a source and a drain on at least one of said semiconductor layers;

a gate between said source and drain;

a first field plate separated from said plurality of semiconductor layers by a non-zero distance of about 1500Å or less.

27. The transistor of claim 26, wherein said first field plate is separated from said plurality of semiconductor layers by between about 100Å and about 800Å.

28. The transistor of claim 26, wherein said first field plate is separated from said plurality of semiconductor layers by between about 300Å and about 600Å.

29. The transistor of claim 26, wherein said first field plate is separated from said plurality of semiconductor layers by a spacer layer.

30. The transistor of claim 26, further comprising a second field plate over said first field plate.

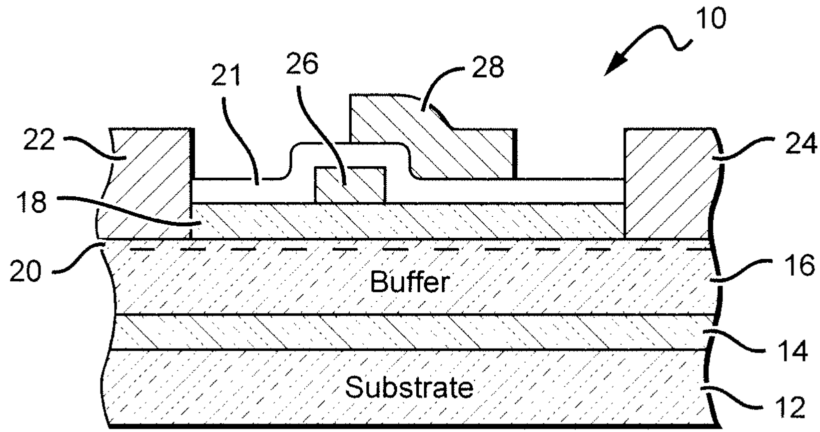
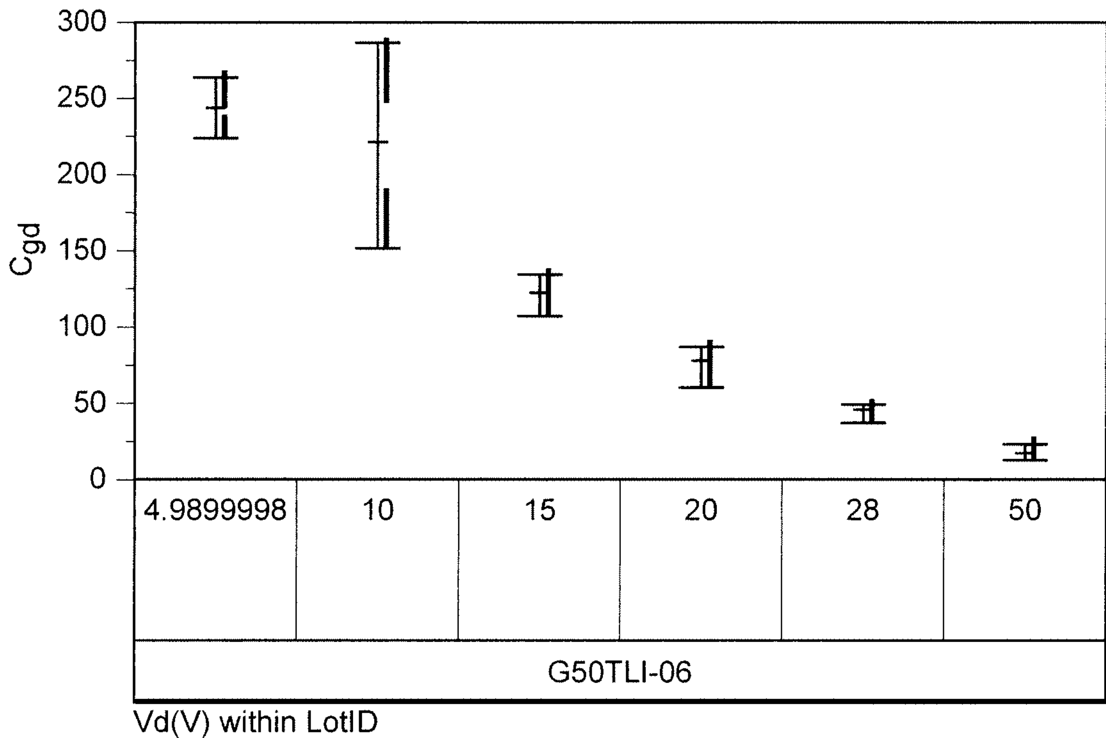


FIG. 1A
PRIOR ART

FIG. 1B
PRIOR ART



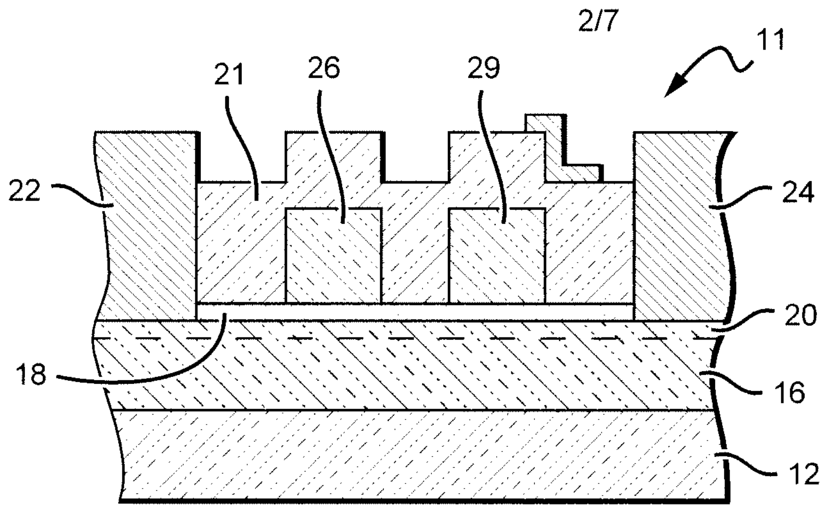


FIG. 1C
PRIOR ART

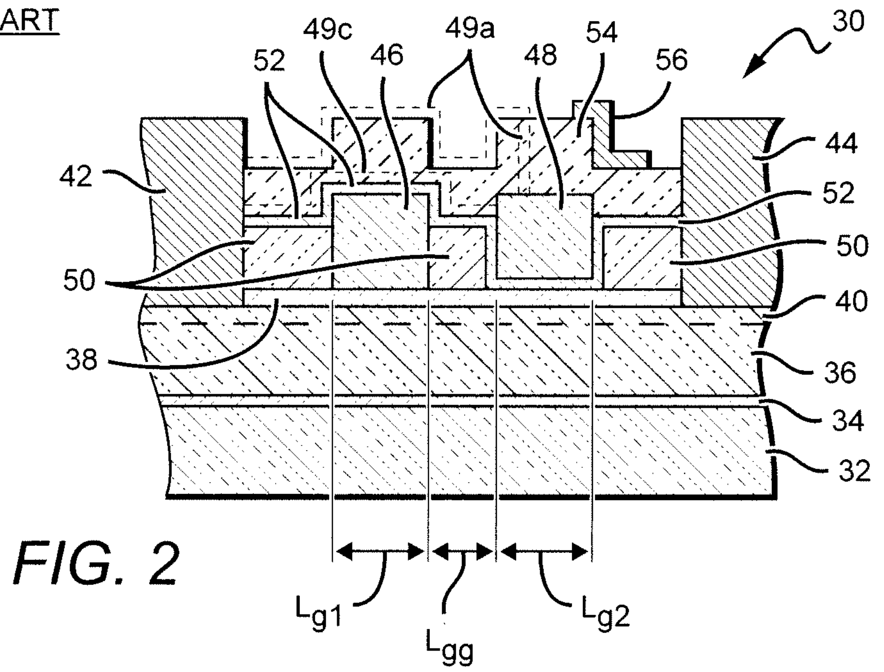
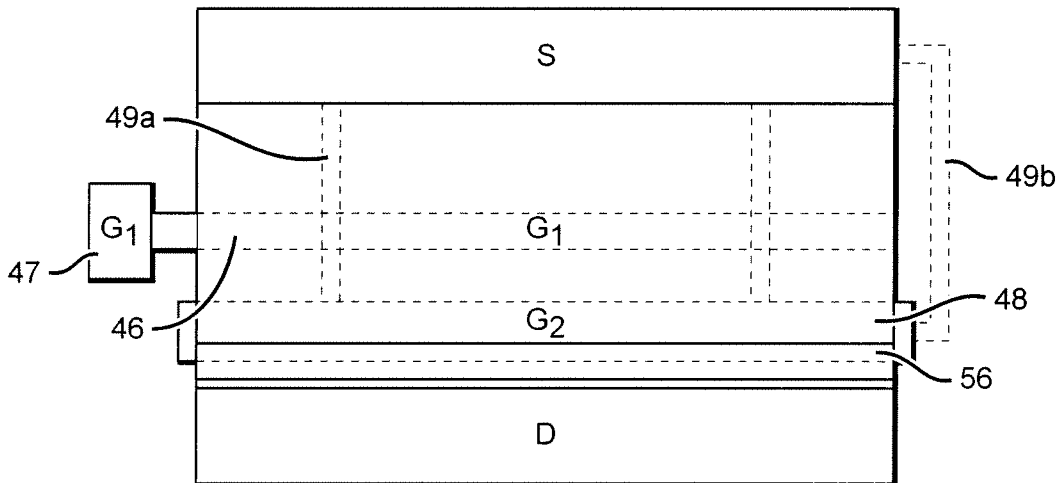


FIG. 2

FIG. 3



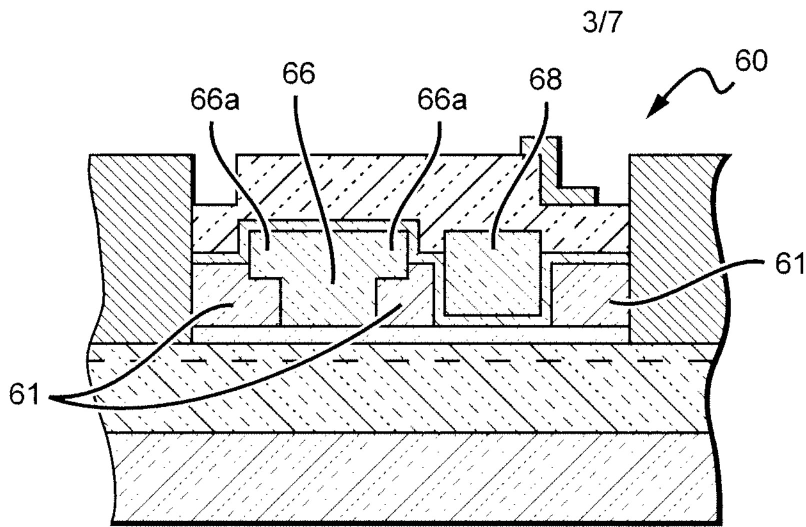


FIG. 4

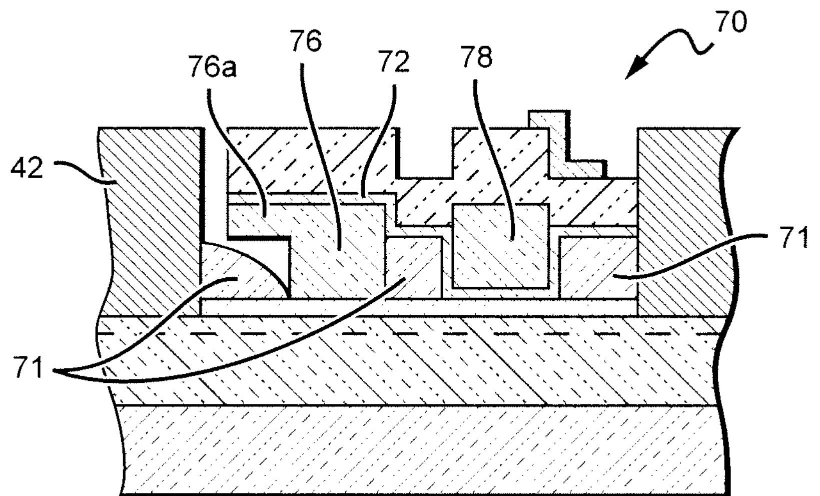


FIG. 5

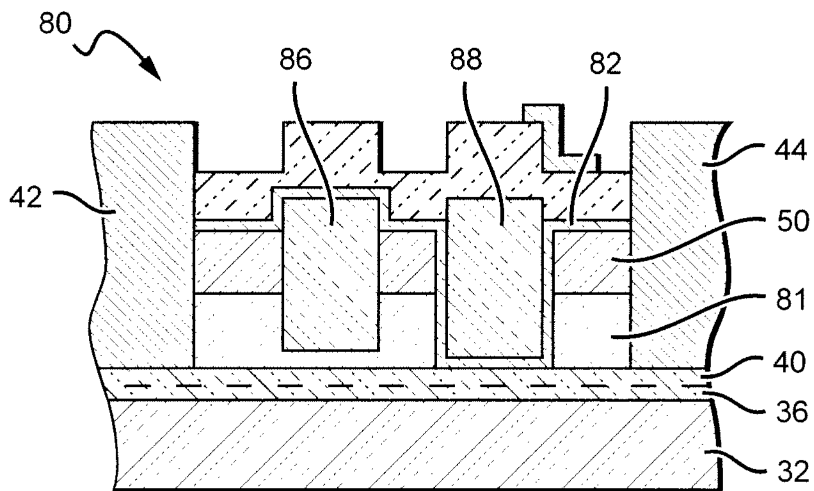


FIG. 6

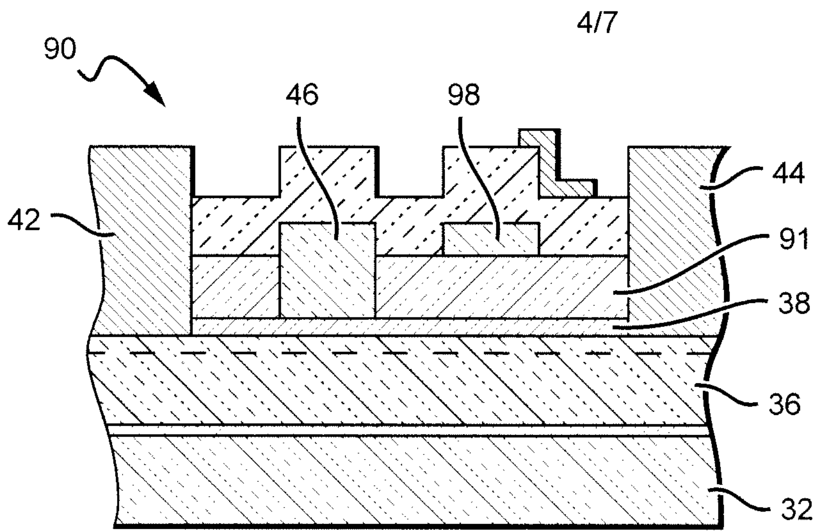


FIG. 7

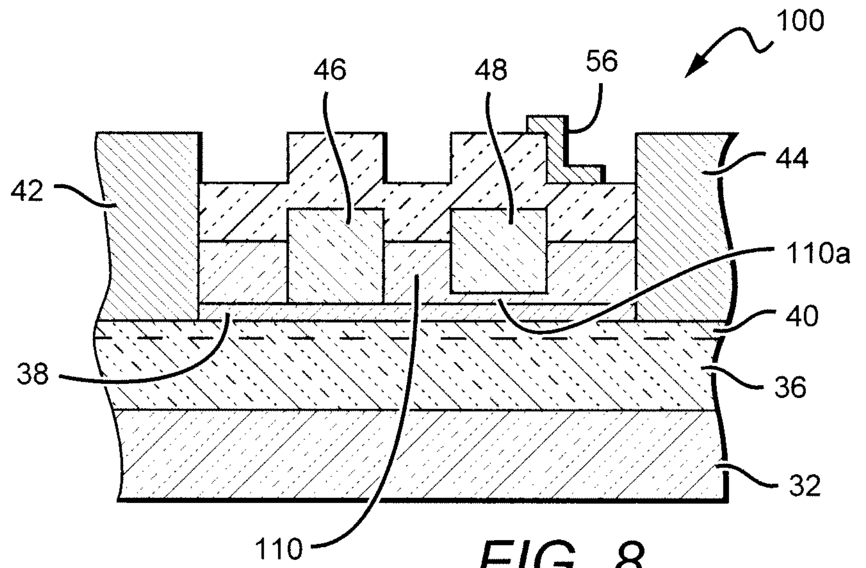


FIG. 8

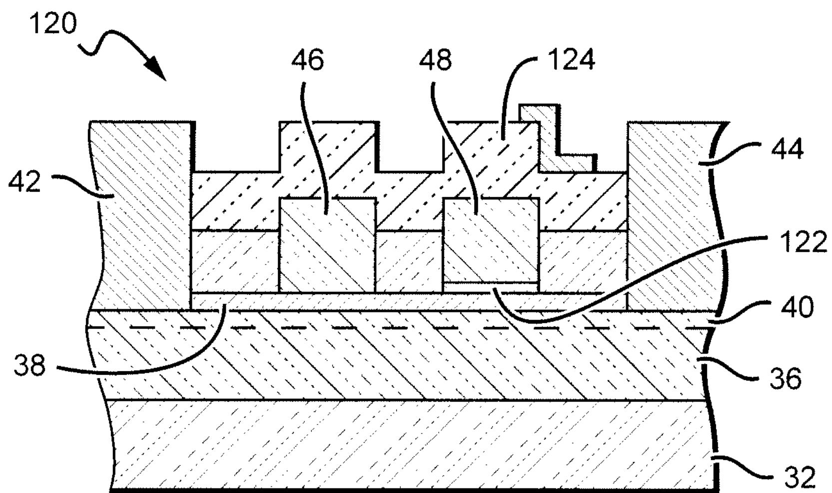


FIG. 9

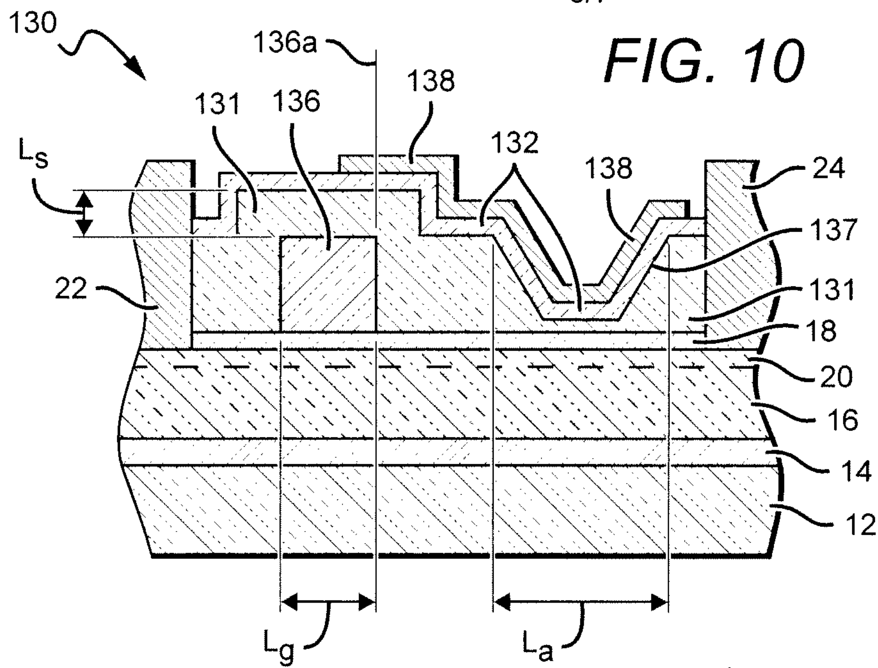


FIG. 10

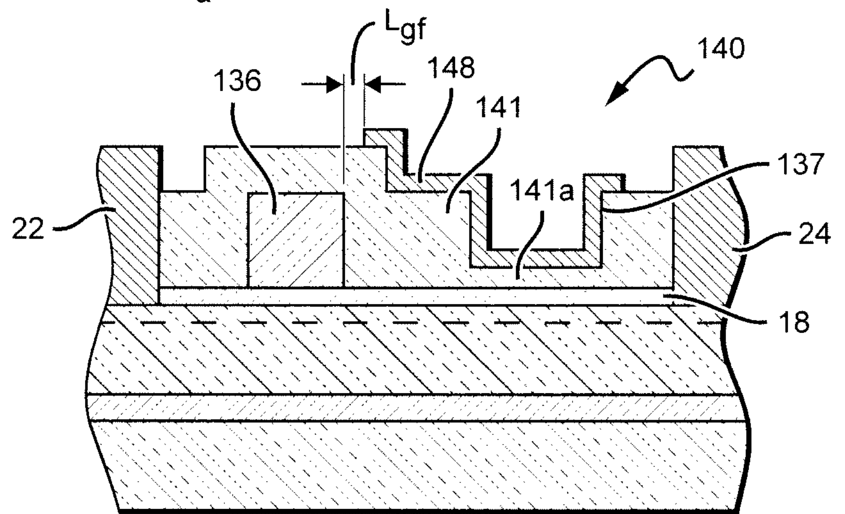
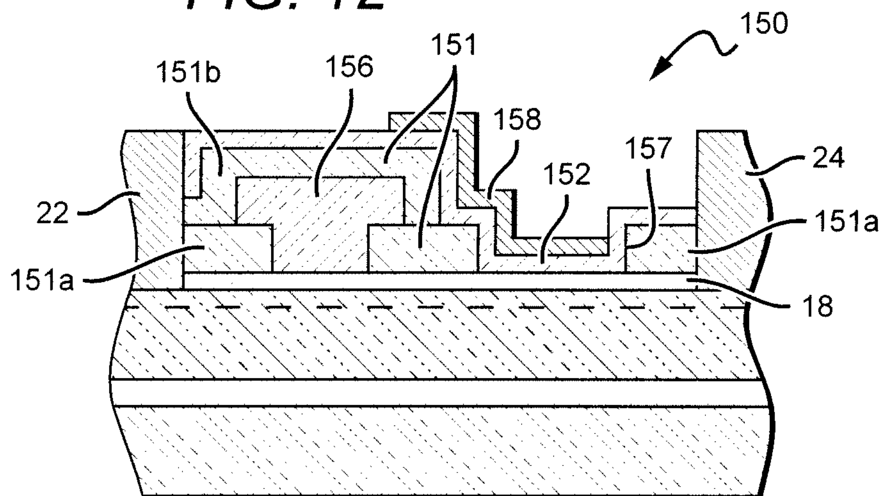


FIG. 11

FIG. 12



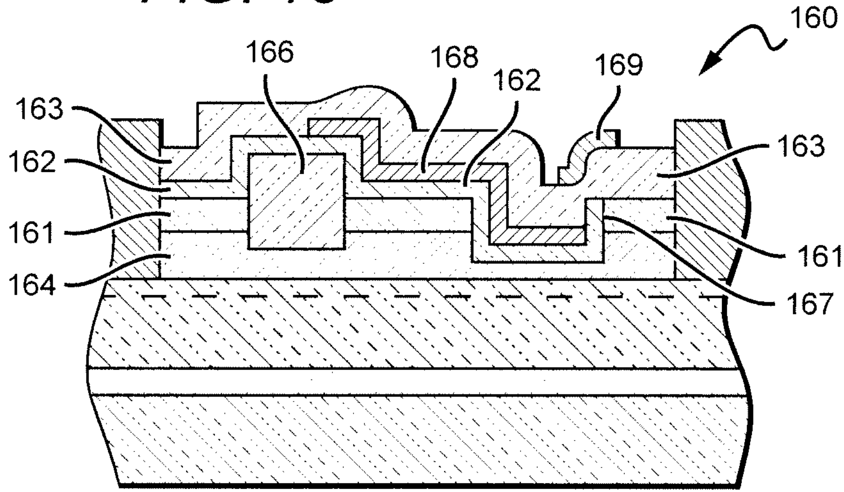


FIG. 13

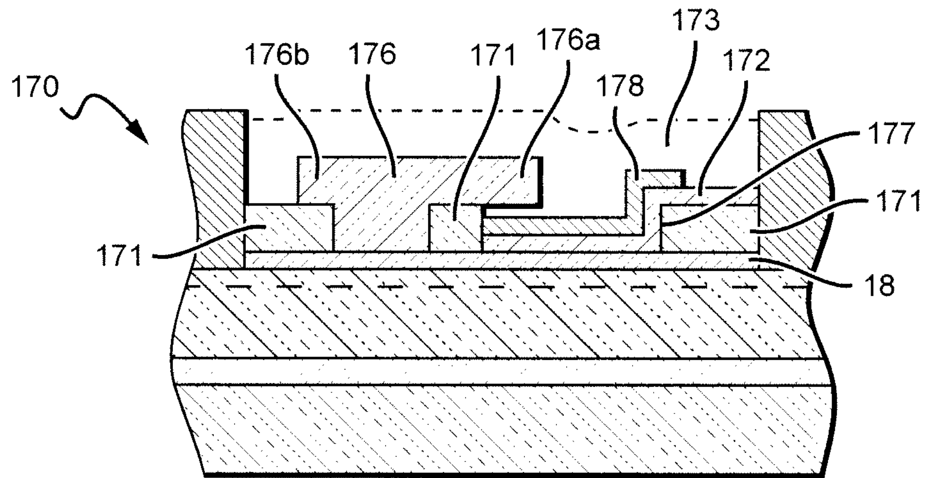


FIG. 14

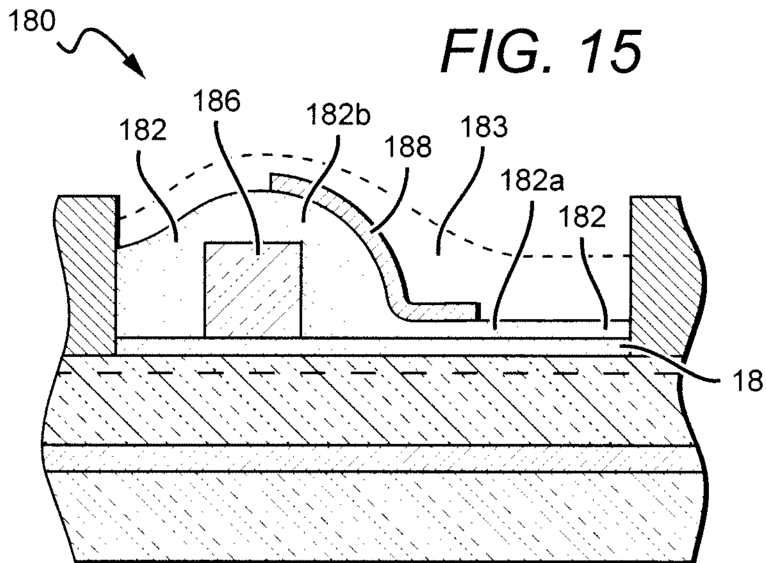
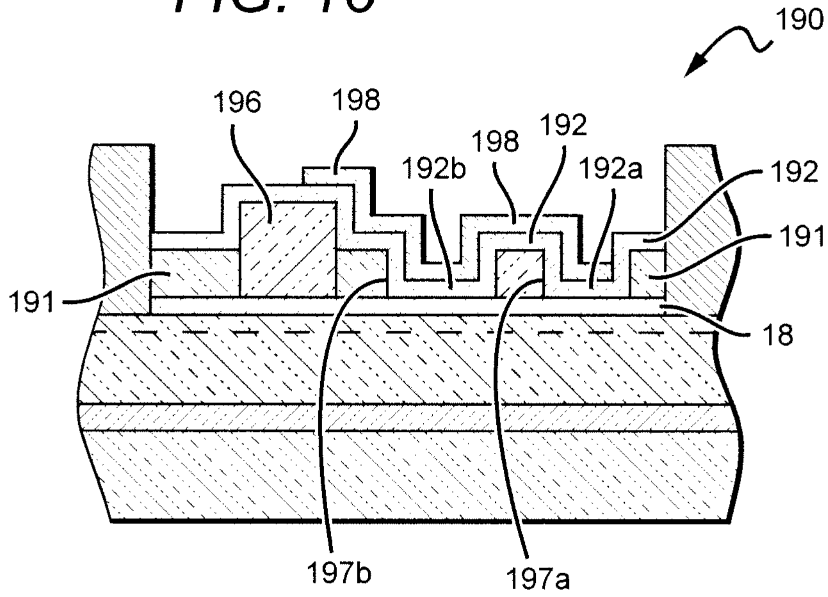


FIG. 15

FIG. 16



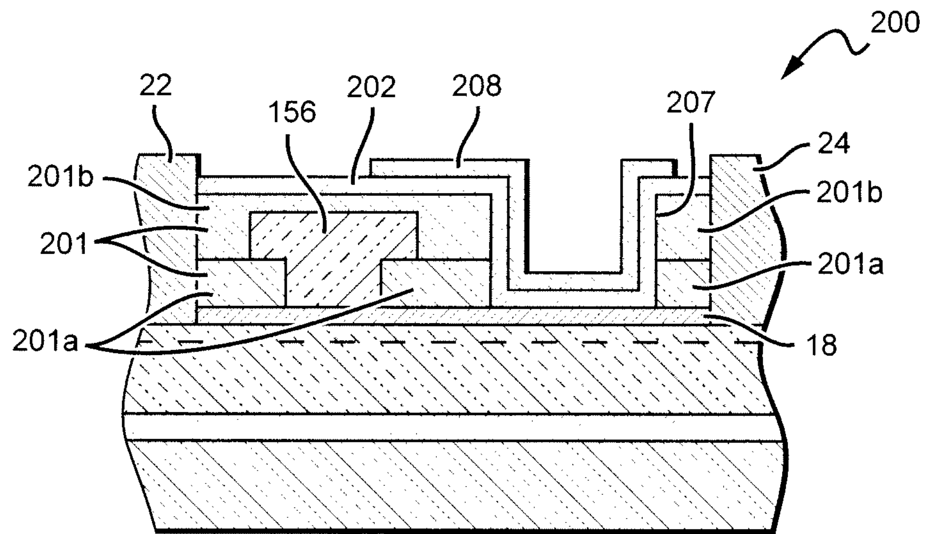


FIG. 17