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Lee et al.

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(54) **PIXEL ARRAY SUBSTRATE AND DRIVING METHOD THEREOF**

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(73) Assignee: **Au Optronics Corporation**, Hsinchu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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Related U.S. Application Data

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**
G02F 1/1362 (2006.01)

(52) **U.S. Cl.**
CPC .. ***G02F 1/136286*** (2013.01); ***G02F 1/136227*** (2013.01); *G02F 2001/136218* (2013.01); *G02F 2201/121* (2013.01); *G02F 2201/123* (2013.01)

(58) **Field of Classification Search**
None
See application file for complete search history.

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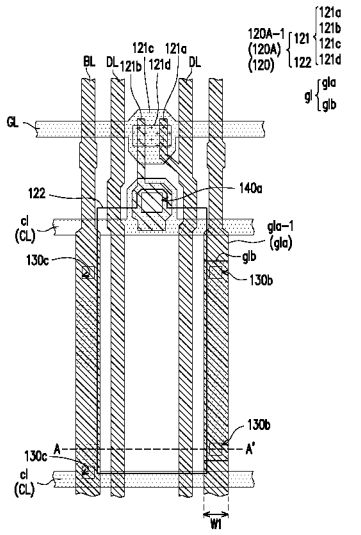
(74) *Attorney, Agent, or Firm* — JCIPRNET

(57) **ABSTRACT**

A pixel array substrate including a substrate, data lines, gate lines, pixels, and transfer lines is provided. The data lines are disposed on the substrate and arranged in a first direction. The gate lines are disposed on the substrate and arranged in a second direction interlaced with the first direction. The pixels are disposed on the substrate, each of which includes an active device electrically connected to one of the data lines and one of the gate lines and a pixel electrode electrically connected to the active device. The transfer lines are arranged in the first direction and electrically connected to the gate lines, respectively. The pixels include first pixels. In a top view of the pixel array substrate, at least one of the pixel electrodes of the first pixels is partially overlapped with one of the transfer lines. A driving method of a pixel array substrate is also provided.

16 Claims, 20 Drawing Sheets



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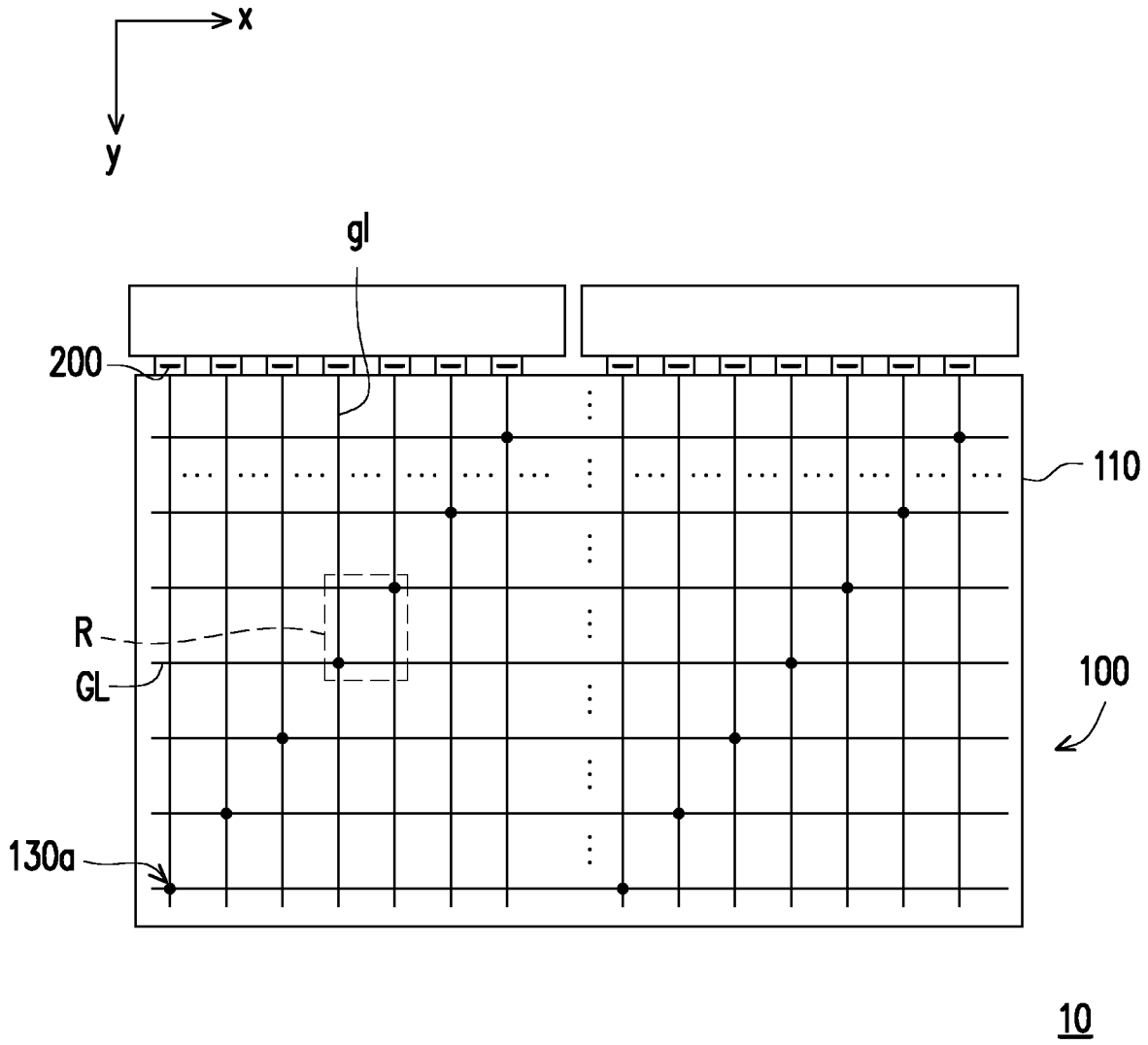

FIG. 1

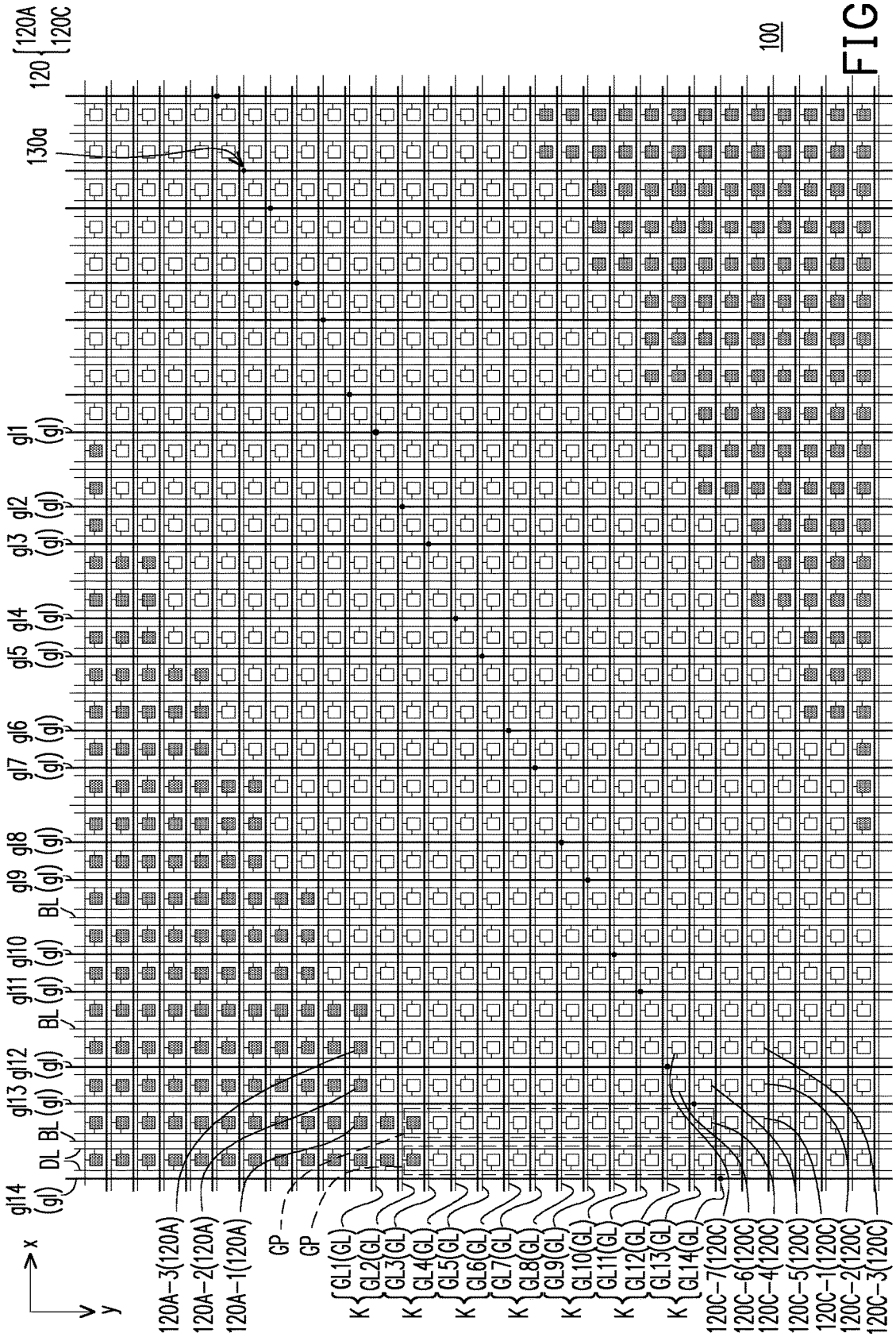
120
120A
120C
130a
100
gl1 (gl)
gl2 (gl)
gl3 (gl)
gl4 (gl)
gl5 (gl)
gl6 (gl)
gl7 (gl)
gl8 (gl)
gl9 (gl)
gl10 (gl)
gl11 (gl)
gl12 (gl)
gl13 (gl)
gl14 (gl)
BL
DL
x
y
120A-3(120A)
120A-2(120A)
120A-1(120A)
GP
GP
K
GL1(GL)
GL2(GL)
GL3(GL)
GL4(GL)
GL5(GL)
GL6(GL)
GL7(GL)
GL8(GL)
GL9(GL)
GL10(GL)
GL11(GL)
GL12(GL)
GL13(GL)
GL14(GL)
120C-7(120C)
120C-6(120C)
120C-4(120C)
120C-5(120C)
120C-1(120C)
120C-2(120C)
120C-3(120C)

FIG. 2

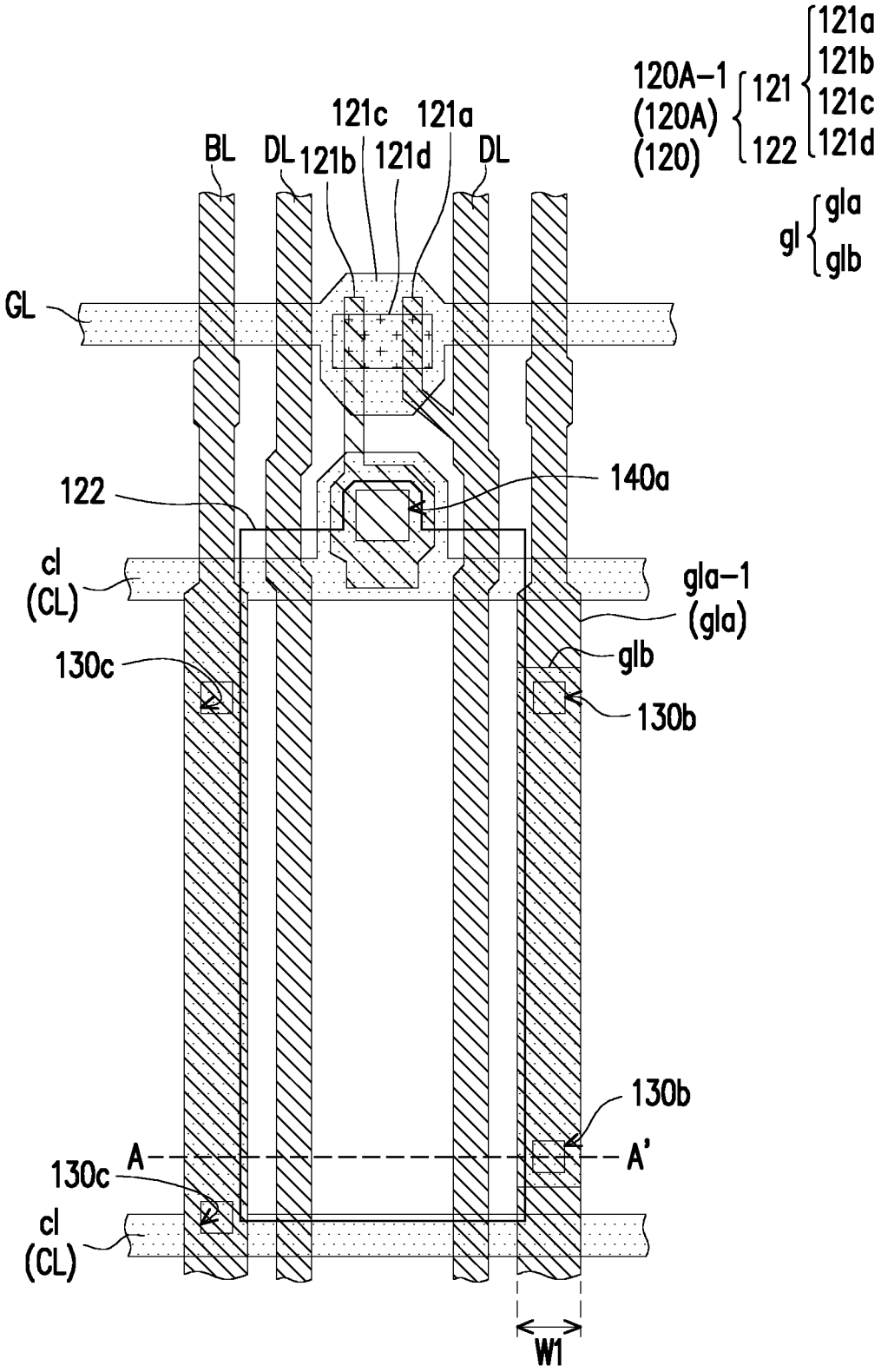
120A-1
(120A)
(120)
121
122
121a
121b
121c
121d
gl
gla
glb
BL
DL
DL
121c
121a
121b
121d
GL
122
140a
cl
(CL)
gla-1
(gla)
glb
130c
130b
130b
A
A'
130c
cl
(CL)
W1

FIG. 3

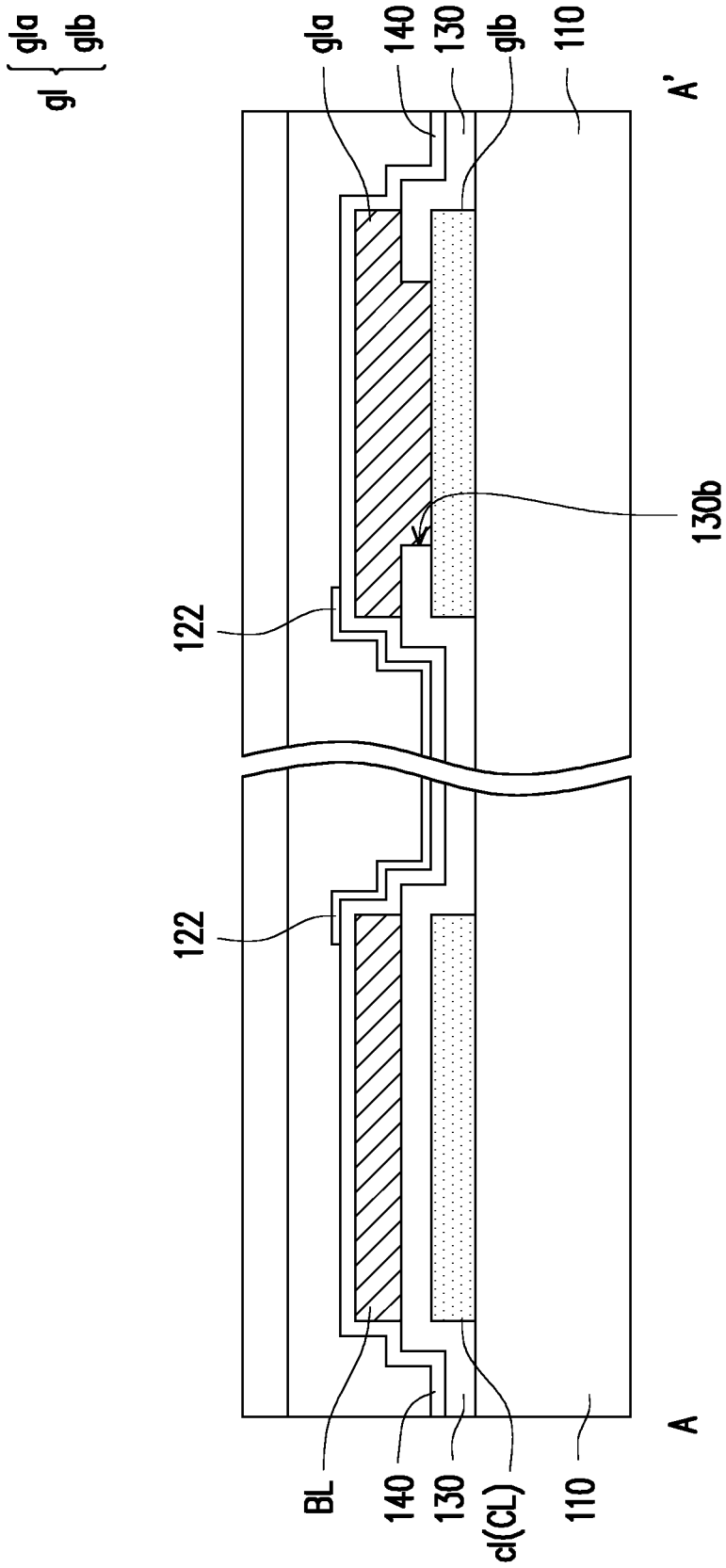
gl
gla
glb
gla
140
130
glb
110
A'
130b
122
122
BL
140
130
cl(CL)
110
A

FIG. 4

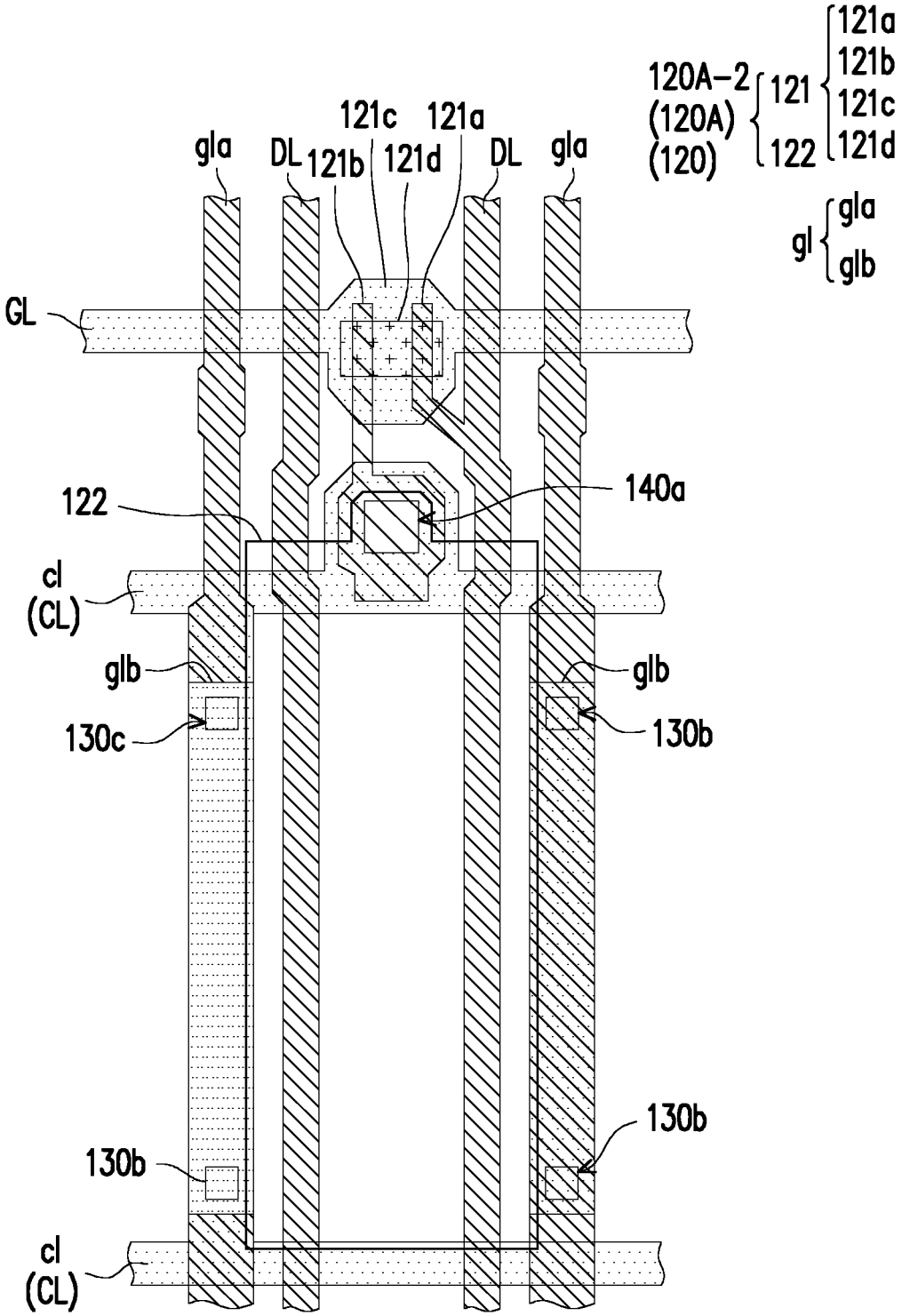
120A-2
(120A)
(120)
121
122
121a
121b
121c
121d
gl
gla
glb
121c
121a
gla
DL
121b
121d
DL
gla
GL
122
140a
cl
(CL)
glb
glb
130c
130b
130b
130b
cl
(CL)

FIG. 5

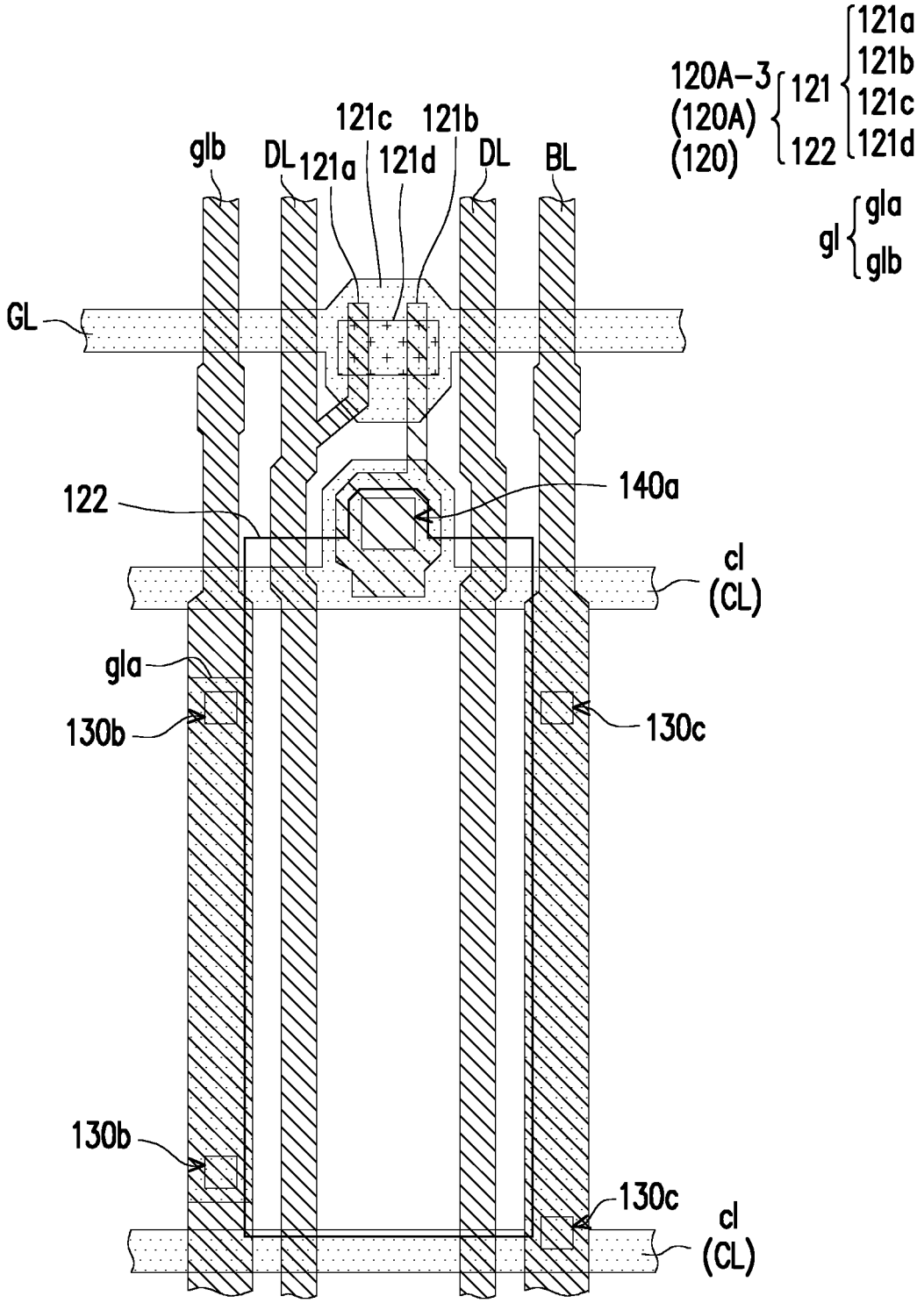
120A-3
(120A)
(120)
121
122
121a
121b
121c
121d
gl
gla
glb
glb
DL
121a
121d
121c
121b
DL
BL
GL
122
140a
cl
(CL)
gla
130b
130c
130b
130c
cl
(CL)

FIG. 6

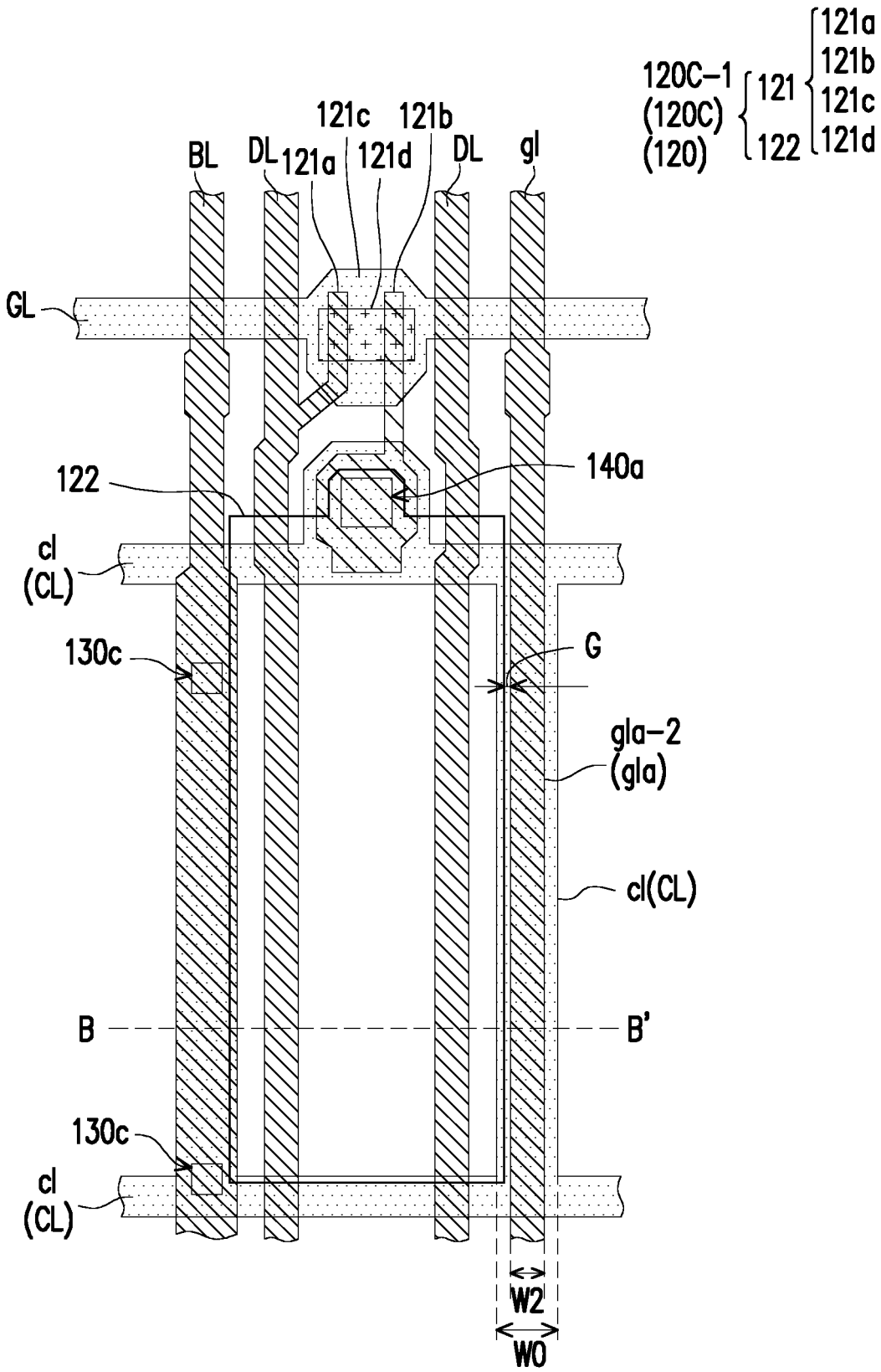
120C-1
(120C)
(120)
121
122
121a
121b
121c
121d
BL
DL
121a
121c
121b
121d
DL
gl
GL
122
140a
cl
(CL)
130c
G
gla-2
(gla)
cl(CL)
B
B'
130c
cl
(CL)
W2
W0

FIG. 7

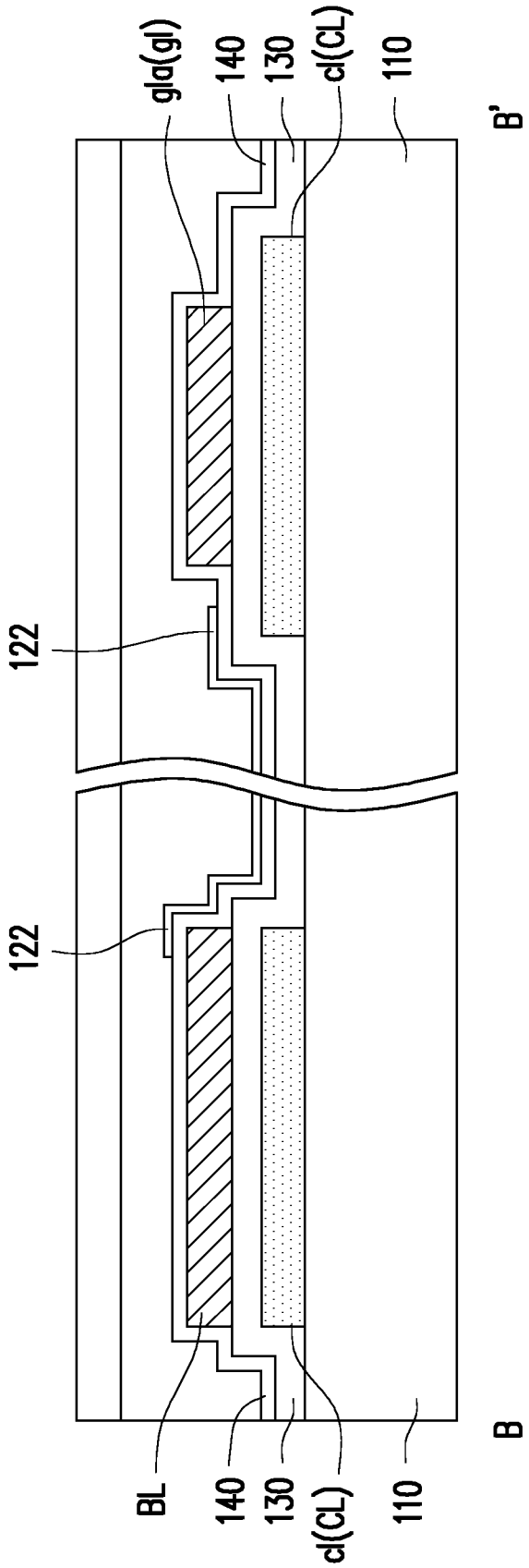

FIG. 8

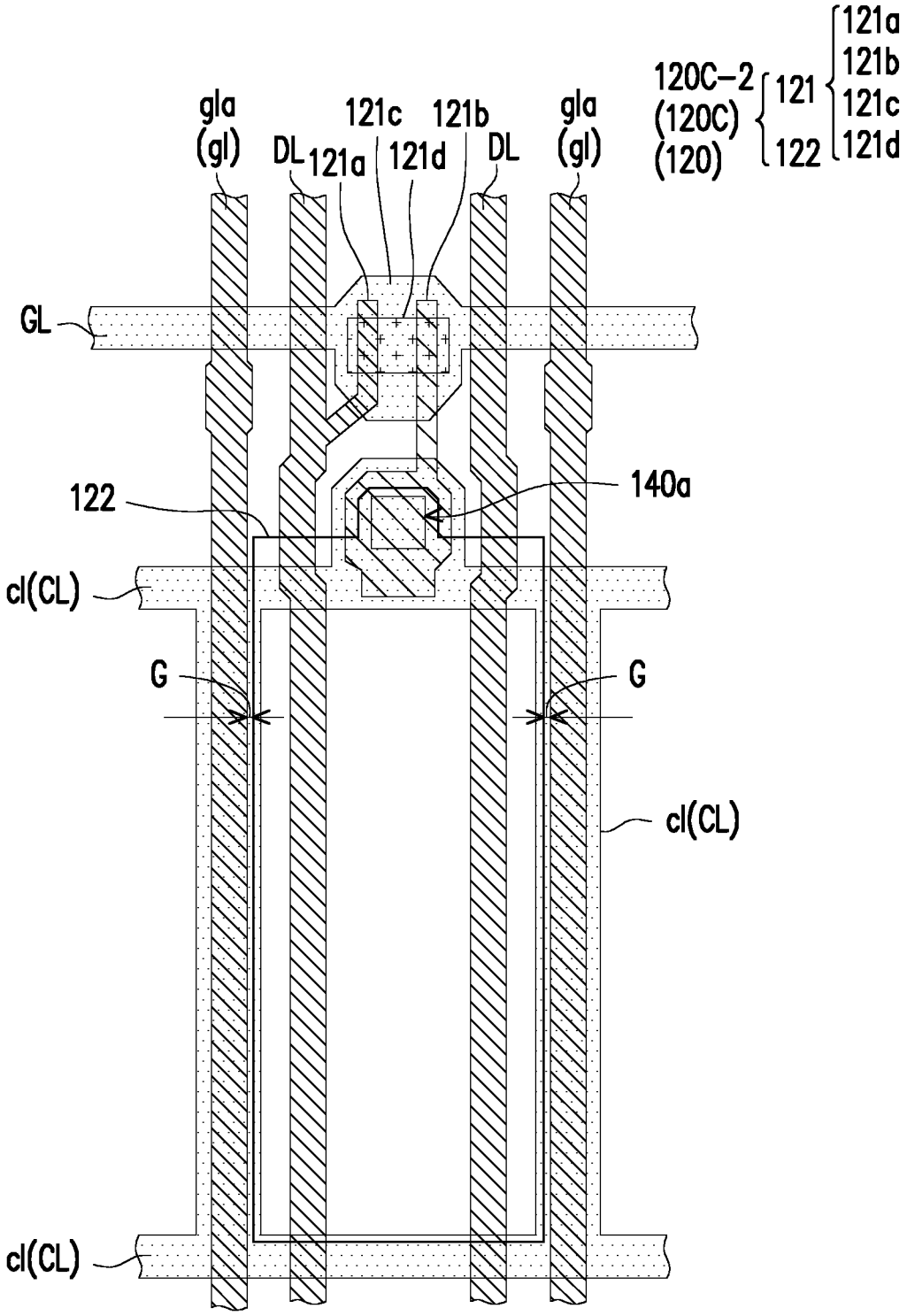
120C-2
(120C)
(120)
121
122
121a
121b
121c
121d
gla
(gl)
DL
121a
121c
121b
121d
DL
gla
(gl)
GL
122
140a
cl(CL)
G
G
cl(CL)
cl(CL)

FIG. 9

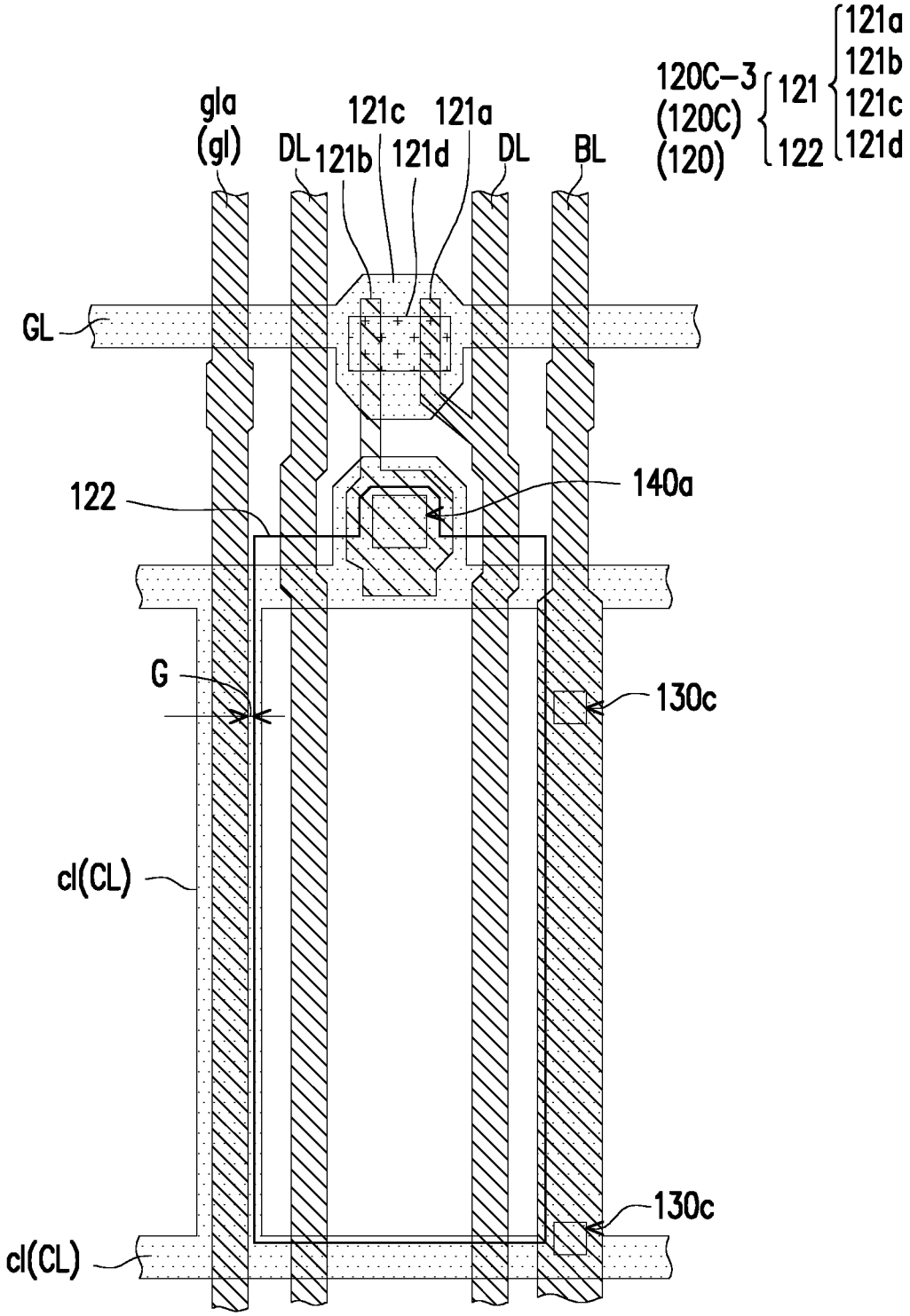
120C-3
(120C)
(120)
121
122
121a
121b
121c
121d
gla
(gl)
DL
121b
121c
121a
121d
DL
BL
GL
122
140a
G
130c
cl(CL)
130c
cl(CL)

FIG. 10

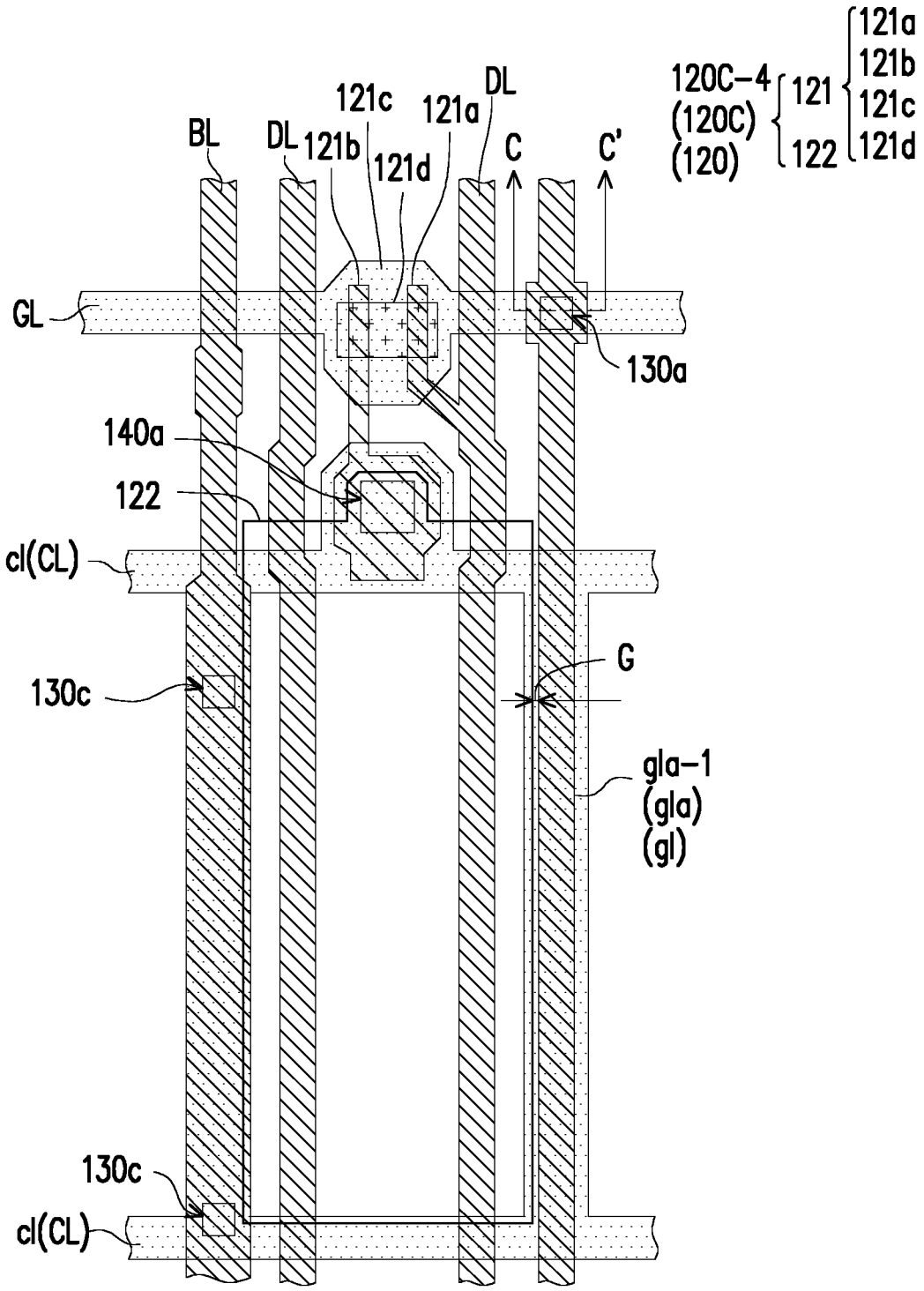
120C-4
(120C)
(120)
121
122
121a
121b
121c
121d
BL
DL
121b
121c
121a
121d
DL
C
C'
GL
130a
140a
122
cl(CL)
130c
G
gla-1
(gla)
(gl)
130c
cl(CL)

FIG. 11

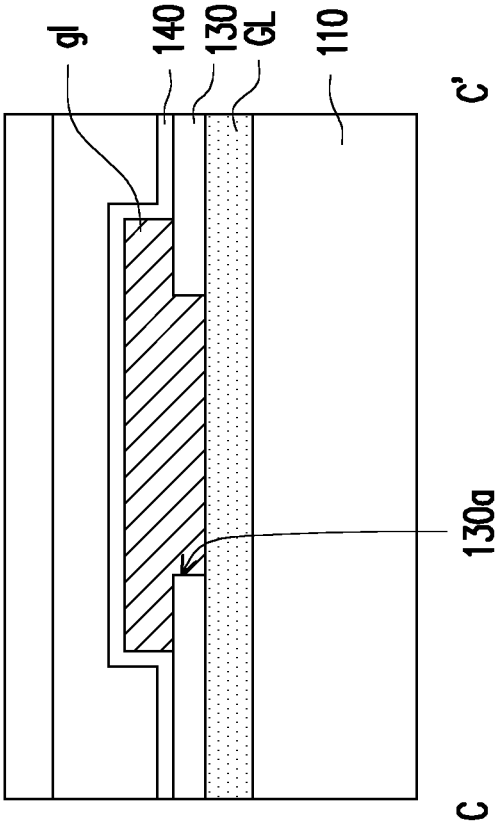

FIG. 12

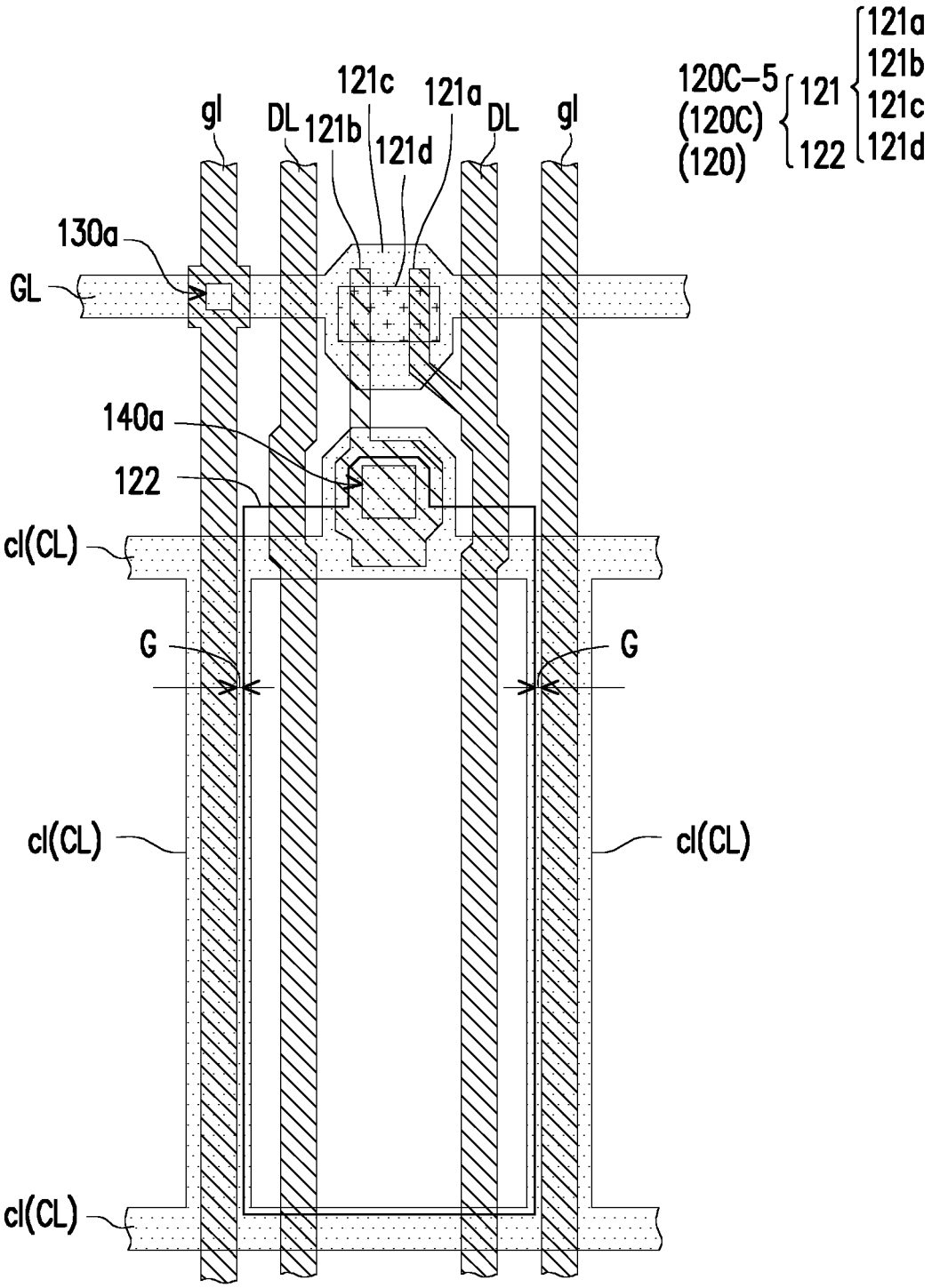
120C-5
(120C)
(120)
121
122
121a
121b
121c
121d
gl
DL
121b
121c
121a
121d
DL
gl
130a
GL
140a
122
cl(CL)
G
G
cl(CL)
cl(CL)
cl(CL)

FIG. 13

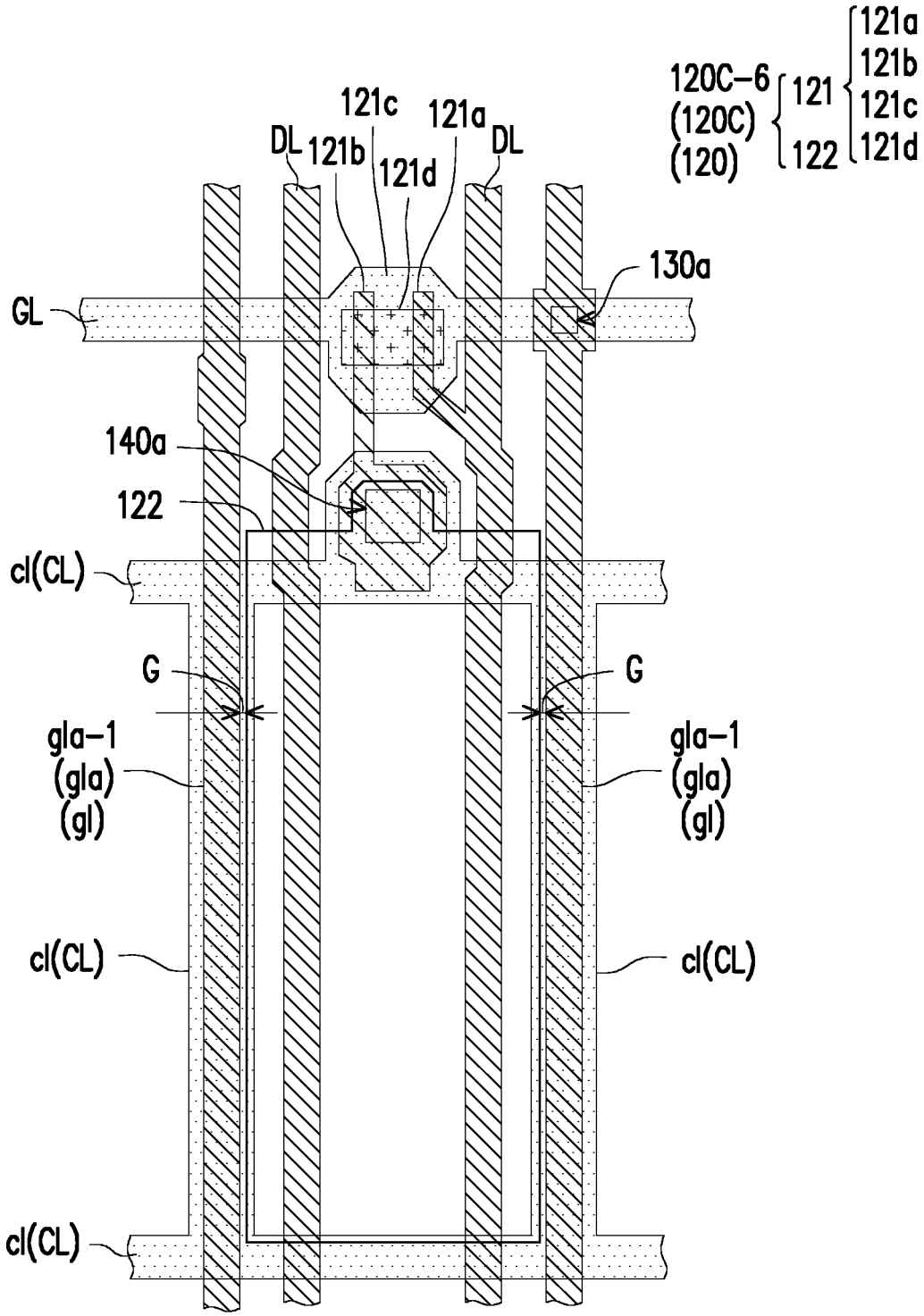
120C-6
(120C)
(120)
121
122
121a
121b
121c
121d
121c
121a
DL
121b
121d
DL
130a
GL
140a
122
cl(CL)
G
G
gla-1
(gla)
(gl)
gla-1
(gla)
(gl)
cl(CL)
cl(CL)
cl(CL)

FIG. 14

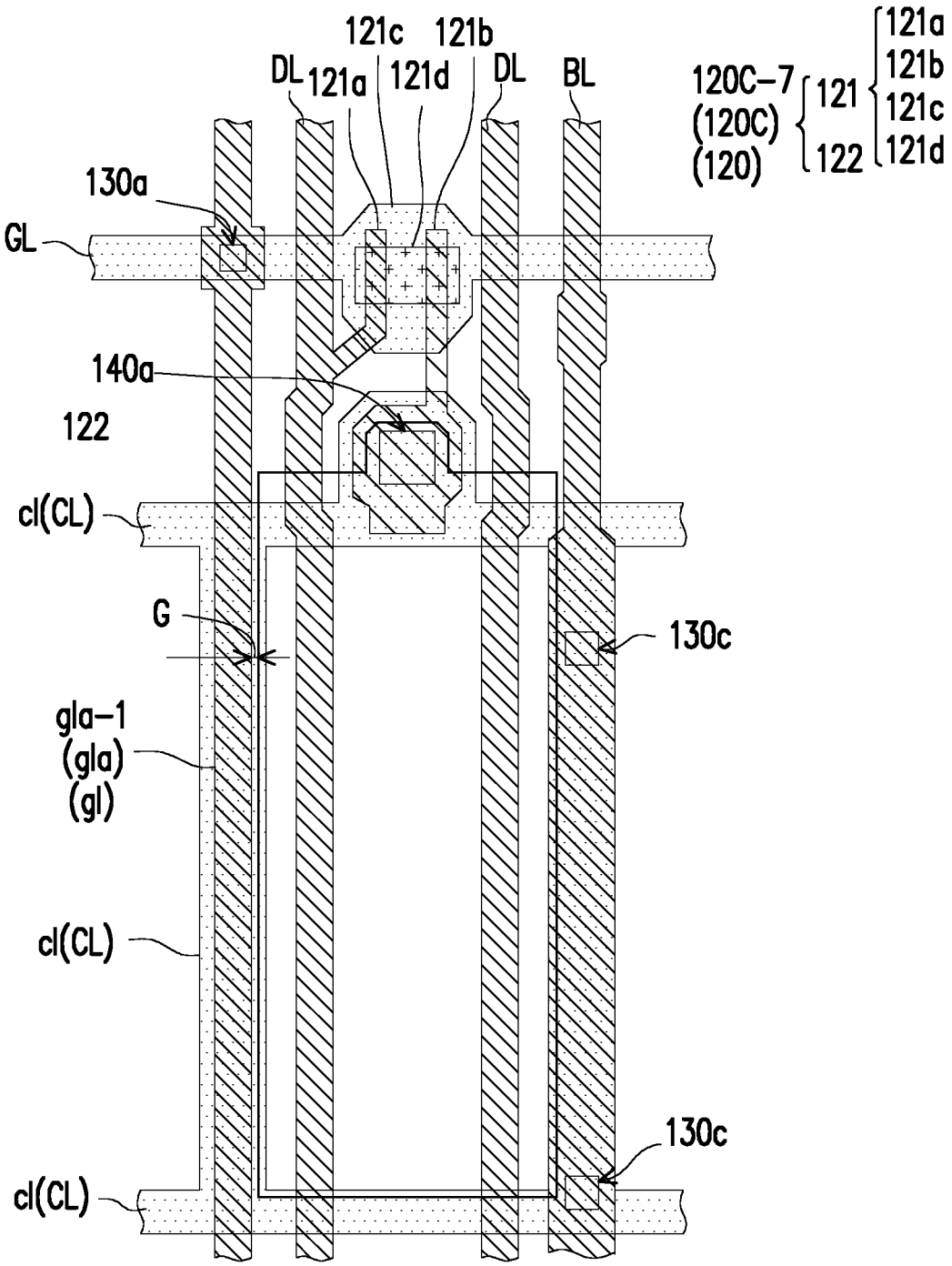
121c
121b
DL
121a
121d
DL
BL
120C-7
(120C)
(120)
121
122
121a
121b
121c
121d
130a
GL
140a
122
cl(CL)
G
130c
gla-1
(gla)
(gl)
cl(CL)
130c
cl(CL)

FIG. 15

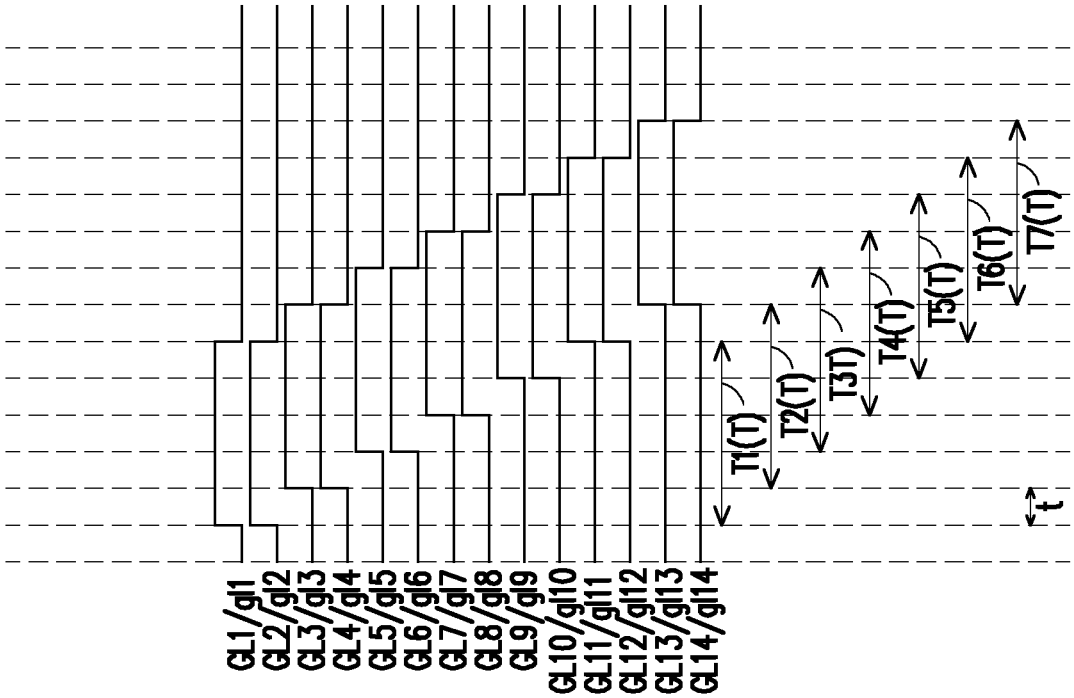
GL1/gl1
GL2/gl2
GL3/gl3
GL4/gl4
GL5/gl5
GL6/gl6
GL7/gl7
GL8/gl8
GL9/gl9
GL10/gl10
GL11/gl11
GL12/gl12
GL13/gl13
GL14/gl14
T1(T)
T2(T)
T3T)
T4(T)
T5(T)
T6(T)
T7(T)
t

FIG. 17

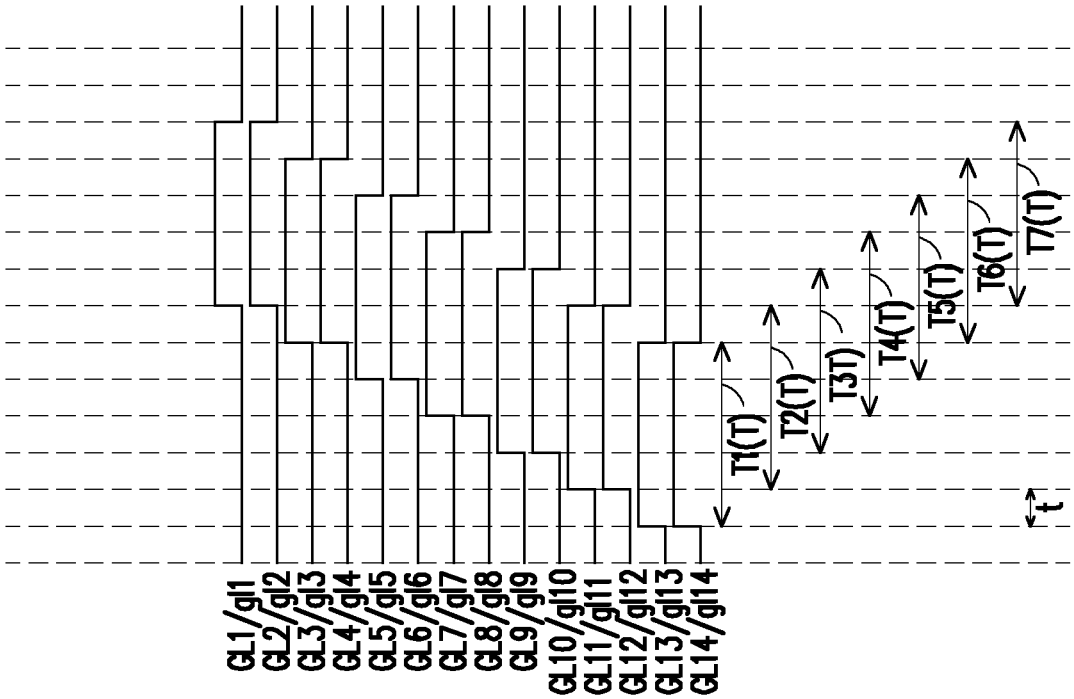
GL1/gl1
GL2/gl2
GL3/gl3
GL4/gl4
GL5/gl5
GL6/gl6
GL7/gl7
GL8/gl8
GL9/gl9
GL10/gl10
GL11/gl11
GL12/gl12
GL13/gl13
GL14/gl14
T1(T)
T2(T)
T3T)
T4(T)
T5(T)
T6(T)
T7(T)
t

FIG. 16

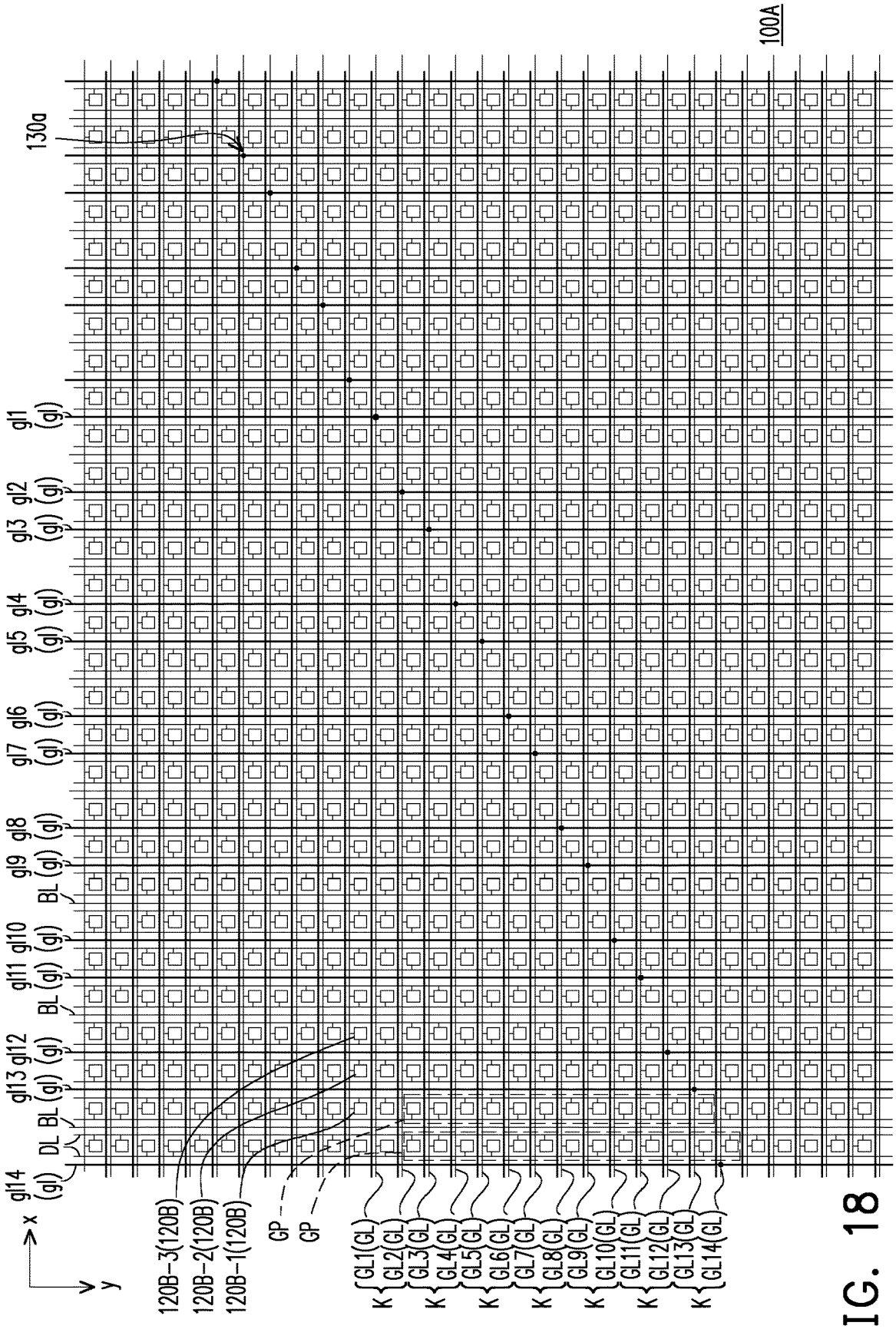
100A
130a
gl1 (gl)
gl2 (gl)
gl3 (gl)
gl4 (gl)
gl5 (gl)
gl6 (gl)
gl7 (gl)
gl8 (gl)
gl9 (gl)
gl10 (gl)
gl11 (gl)
gl12 (gl)
gl13 (gl)
gl14 (gl)
DL
BL
BL
BL
x
y
120B-3(120B)
120B-2(120B)
120B-1(120B)
GP
GP
K GL1(GL)
K GL2(GL)
K GL3(GL)
K GL4(GL)
K GL5(GL)
K GL6(GL)
K GL7(GL)
K GL8(GL)
K GL9(GL)
K GL10(GL)
K GL11(GL)
K GL12(GL)
K GL13(GL)
K GL14(GL)

FIG. 18

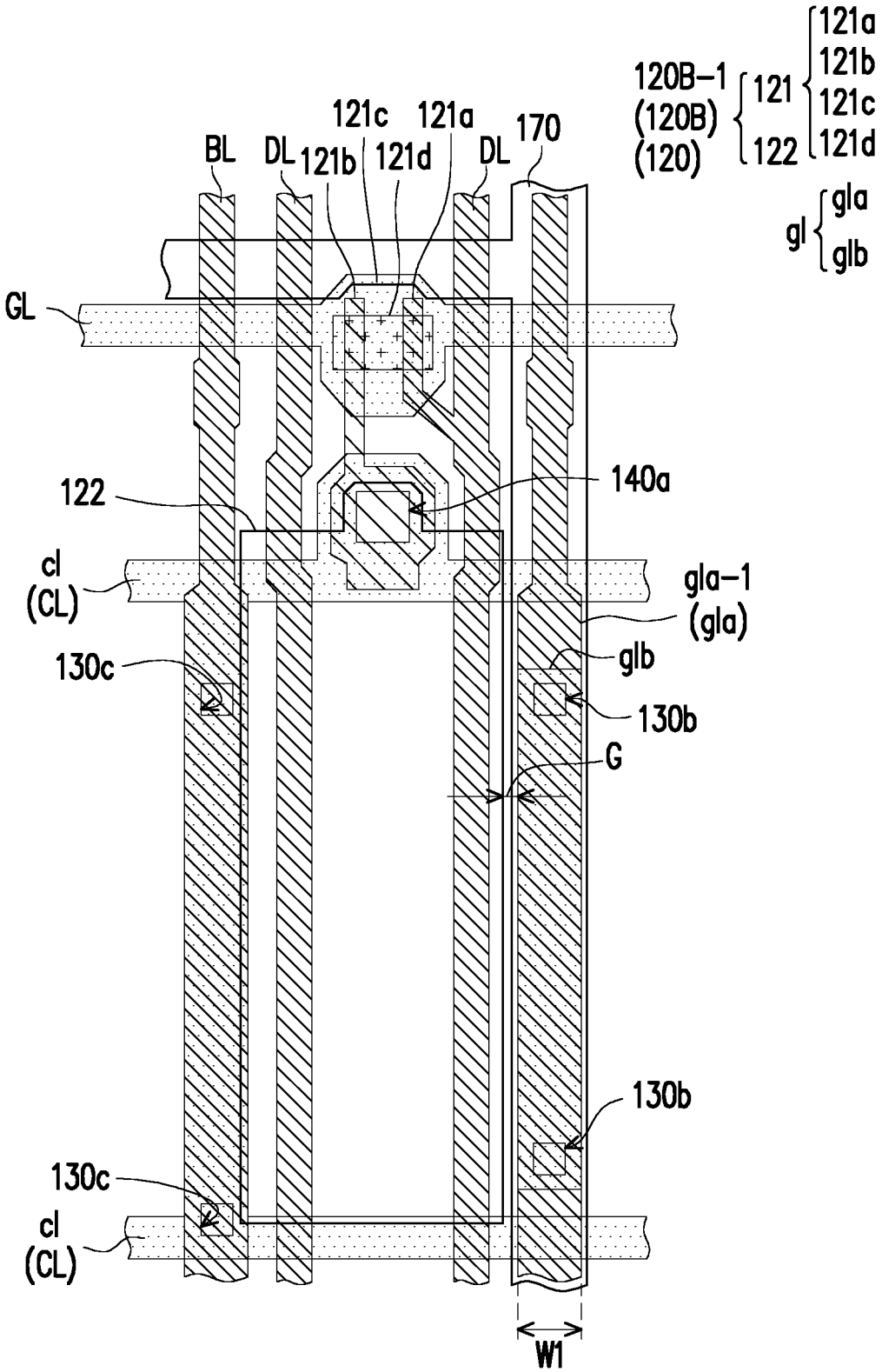
120B-1
(120B)
(120)
121
122
121a
121b
121c
121d
gl
gla
glb
BL
DL
121b
121c
121a
121d
DL
170
GL
122
140a
cl
(CL)
gla-1
(gla)
glb
130c
130b
G
130b
130c
cl
(CL)
W1

FIG. 19

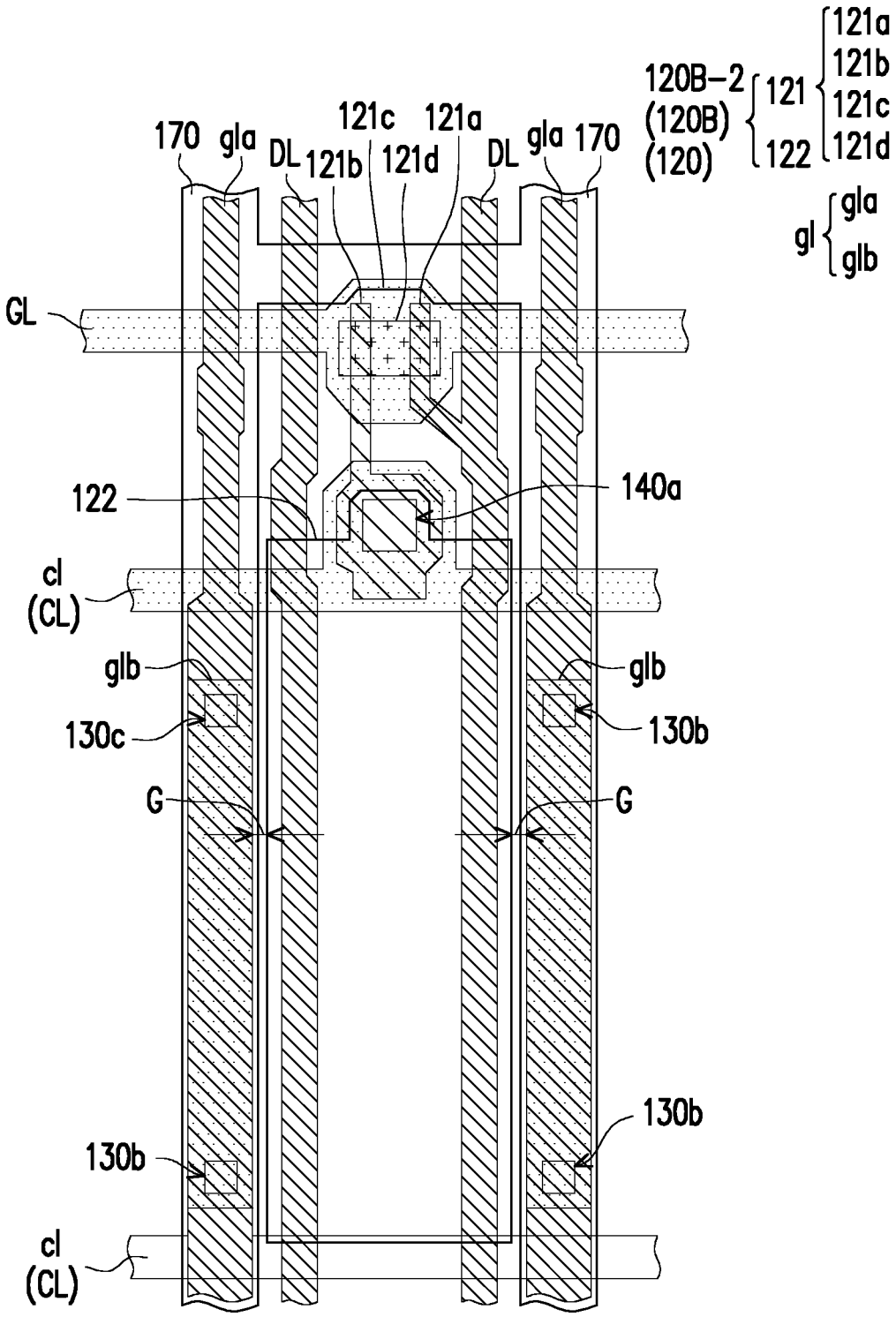
120B-2
(120B)
(120)
121
122
121a
121b
121c
121d
gl
gla
glb
170
gla
DL
121b
121c
121a
121d
DL
gla
170
GL
122
140a
cl
(CL)
glb
glb
130c
130b
G
G
130b
130b
cl
(CL)

FIG. 20

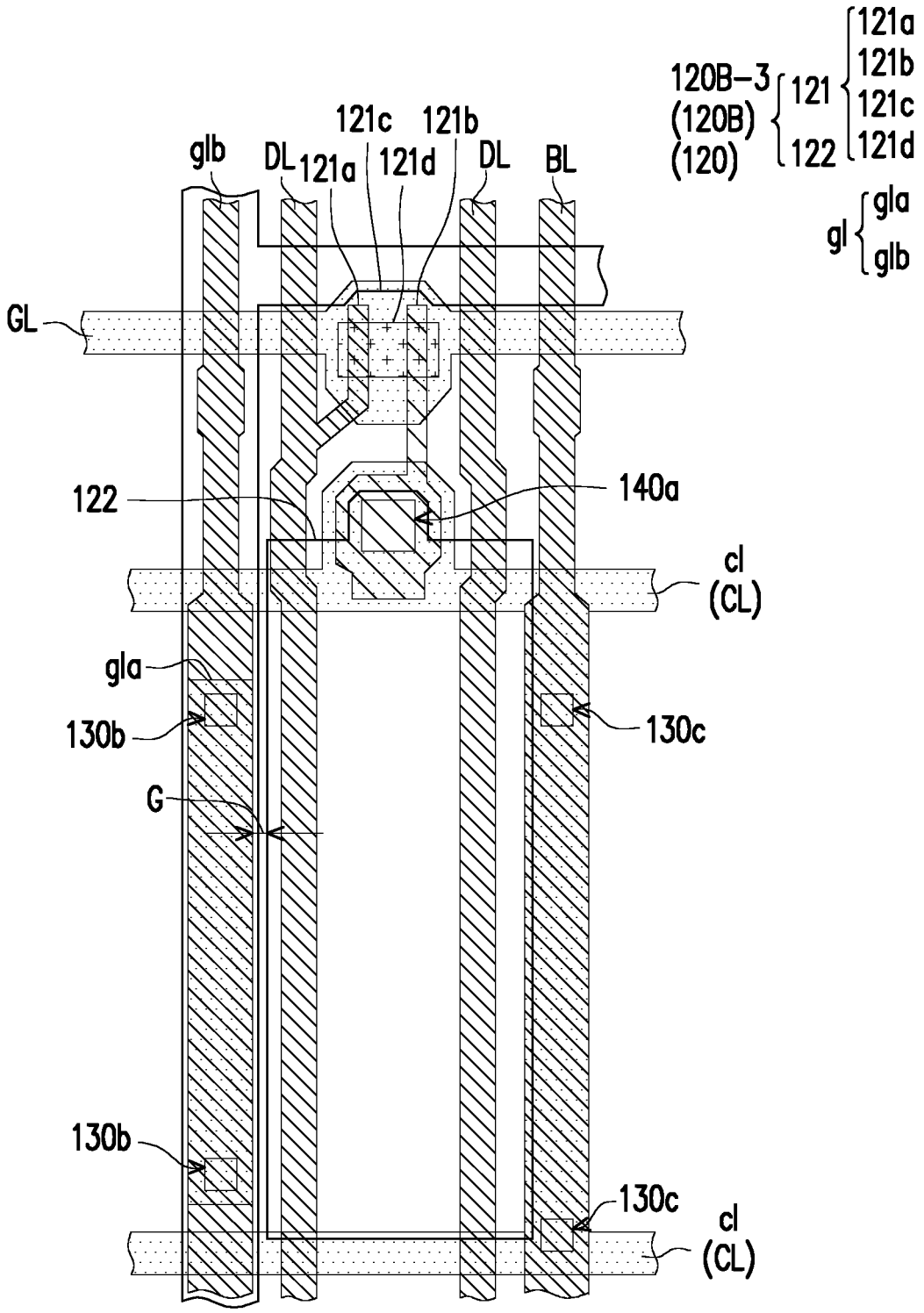
120B-3
(120B)
(120)
121
122
121a
121b
121c
121d
gl
gla
glb
glb
DL
121a
121d
DL
BL
121c
121b
GL
122
140a
cl
(CL)
gla
130b
130c
G
130b
130c
cl
(CL)

FIG. 21

PIXEL ARRAY SUBSTRATE AND DRIVING METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the domestic benefit of U.S. provisional application Ser. No. 62/811,012, filed on Feb. 27, 2019 and the priority benefit of Taiwan patent application serial no. 108138907, filed on Oct. 28, 2019. The entirety of each of the above-mentioned patent applications is hereby incorporated by reference herein and made a part of this specification.

BACKGROUND

Technical Field

The disclosure relates to a pixel array substrate and a driving method thereof.

Description of Related Art

With the development of display technologies, the demand for display devices is no longer limited to favorable optical characteristics, such as high resolution, high contrast, and wide viewing angles. People also expect the display devices to have elegant appearance. For instance, people expect the display devices to have narrow frames or even to be frameless.

Generally speaking, the display device includes a pixel array disposed in a display region, a data driving circuit disposed below the display region, and a gate driving circuit disposed on the left side, the right side, or both the left and the right sides of the display region. In order to reduce the width of the left and right sides of the frame of the display device, both the gate driving circuit and the data driving circuit may be disposed on the lower side of the display region. When the gate driving circuit is disposed on the lower side of the display region, a gate line extending in a horizontal direction can merely be electrically connected to the gate driving circuit through a transfer line extending in a vertical direction. The transfer line, however, occupies the layout area of the display region, and the number of circuits in the display region also increases, thus affecting an aperture ratio of a pixel array substrate of the display device and the manufacturing yield.

SUMMARY

The disclosure provides a pixel array substrate with favorable characteristics.

The disclosure provides another pixel array substrate with favorable characteristics.

According to an embodiment of the disclosure, a pixel array substrate a substrate, a plurality of data lines, a plurality of gate lines, a plurality of pixels, and a plurality of transfer lines. The data lines are disposed on the substrate and arranged in a first direction. The gate lines are disposed on the substrate and arranged in a second direction. The first direction is interlaced with the second direction. The pixels are disposed on the substrate. Each of the pixels includes an active device and a pixel electrode, the active device is electrically connected to one of the data lines and one of the gate lines, and the pixel electrode is electrically connected to the active device. The transfer lines are arranged in the first direction and electrically connected to the gate lines, respectively. The pixels include a plurality of first pixels. In a top view of the pixel array substrate, at least one of the pixel electrodes of the first pixels is partially overlapped with one of the transfer lines.

In an embodiment of the disclosure, the pixels further include a plurality of second pixels, and at least one of the second pixels further includes a common electrode. In the top view of the pixel array substrate, the pixel electrode and the common electrode of the at least one of the second pixels are partially overlapped, the common electrode of the at least one of the second pixels and the one of the transfer lines are overlapped, and a gap exists between the pixel electrode of the at least one of the second pixels and the one of the transfer lines.

In an embodiment of the disclosure, each of the transfer lines has a first portion and a second portion connected to each other. In the top view of the pixel array substrate, the first portion of each of the transfer lines and the at least one of the pixel electrodes of the first pixels are partially overlapped, a gap exists between the second portion of each of the transfer lines and the pixel electrode of the at least one of the second pixels, and a line width of the first portion of each of the transfer lines is greater than a line width of the second portion of each of the transfer lines.

In an embodiment of the disclosure, each of the transfer lines has a second portion. In the top view of the pixel array substrate, the gap exists between the second portion of each of the transfer lines and the pixel electrode of the at least one of the second pixels, and a line width of the second portion of each of the transfer lines is smaller than a line width of the common electrode of the at least one of the second pixels.

In an embodiment of the disclosure, the pixels further include a plurality of second pixels. Each of the second pixels includes a common electrode. In the top view of the pixel array substrate, the pixel electrode and the common electrode of each of the second pixels are partially overlapped, the common electrode of each of the second pixels is overlapped with a corresponding transfer line of the transfer lines, and a gap exists between the pixel electrode of each of the second pixels and the corresponding transfer line. The pixels include a plurality of pixel groups. At least one of the pixel groups includes n second pixels and one of the first pixels sequentially arranged along the corresponding transfer line. The pixel array substrate further includes an insulation layer sandwiched between the gate lines and the transfer lines. The insulation layer has a plurality of first through holes. The n second pixels of the at least one of the pixel groups include a first second pixel to an nth second pixel arranged in sequence, the active device of the first second pixel is electrically connected to one of the gate lines, and each of the transfer lines is electrically connected to the one of the gate lines through one of the first through holes of the insulation layer, wherein n is a positive integer greater than or equal to 2.

In an embodiment of the disclosure, each of the pixel groups includes n second pixels and one of the first pixels sequentially arranged along the corresponding transfer line, the n second pixels of each of the pixel groups include the first second pixel to the nth second pixel sequentially arranged; the active device of the first second pixel is electrically connected to one of the gate lines, each of the transfer lines is electrically connected to the one of the gate lines through one of the first through holes of the insulation layer, the one of the first pixels of each of the pixel groups is a pixel in the each of the pixel groups closest to the second

pixels of the each of the pixel groups, and the first pixels of the pixel groups are arranged substantially in a staircase shape.

In an embodiment of the disclosure, the pixel array substrate further includes an insulation layer. The insulation layer has a plurality of second through holes. Each of the transfer lines includes a main portion and at least one auxiliary portion, the insulation layer is sandwiched between the main portion and the at least one auxiliary portion, the main portion crosses over the gate lines, the at least one auxiliary portion is disposed between two adjacent gate lines of the gate lines and partially overlapped with the at least one of the pixel electrodes of the first pixels, and two different regions of the main portion are electrically connected to two ends of the at least one auxiliary portion through the second through holes of the insulation layer.

According to an embodiment of the disclosure, a driving method of a pixel array substrate is adapted for driving the above-mentioned pixel array substrate and includes following steps. In a first time interval, one of the gate lines electrically connected to the first second pixel of the at least one of the pixel groups is enabled to have a gate-on potential; in a second time interval, another one of the gate lines electrically connected to the first pixel of the at least one of the pixel groups is enabled to have the gate-on potential, wherein the first time interval and the second time interval are not overlapped in time sequence.

According to an embodiment of the disclosure, another driving method of a pixel array substrate disclosure is adapted for driving the above-mentioned pixel array substrate. The gate lines of the pixel array substrate are categorized into a plurality of gate line groups, and each of the gate line groups includes m gate lines, wherein m is a positive integer greater than or equal to 1, and the driving method includes following steps. The m gate lines of the same gate line groups are simultaneously turned on, wherein when each of the gate line groups is turned on, each of the m gate lines of the each of the gate line groups has a gate-on pulse. The gate line groups are sequentially turned on with a time delay, wherein a time length of the time delay is t, the time length of the gate-on pulse is T, and $n \geq \{[(T-t)/t]*m\}+m$.

According to an embodiment of the disclosure, another pixel array substrate includes a substrate, a plurality of data lines, a plurality of gate lines, a plurality of pixels, a plurality of transfer lines, and a shielding electrode. The data lines are disposed on the substrate and arranged in a first direction. The gate lines are disposed on the substrate and arranged in a second direction, wherein the first direction and the second direction are interlaced with each other. The pixels are disposed on the substrate. Each of the pixels includes an active device and a pixel electrode, wherein the active device is electrically connected to a corresponding data line of the data lines and a corresponding gate line of the gate lines, and the pixel electrode is electrically connected to the active device. The transfer lines are arranged in the first direction and electrically connected to the gate lines, respectively. In a top view of the pixel array substrate, a gap exists between the pixel electrode of at least one of the pixels and one of the transfer lines, the shielding electrode is separated from the pixel electrode of the at least one of the pixels, and the shielding electrode is overlapped with the one of the transfer lines.

According to an embodiment of the disclosure, a pixel array substrate includes a substrate, a plurality of data lines, a plurality of gate lines, and a plurality of pixels. The data lines are disposed on the substrate and arranged in a first direction. The gate lines are disposed on the substrate and arranged in a second direction, wherein the first direction is interlaced with the second direction. The pixels are disposed on the substrate, and each of the pixels includes an active device, a pixel electrode, and a portion of a transfer line. The active device is electrically connected to a corresponding data line of the data lines and a corresponding gate line of the gate lines, the pixel electrode is electrically connected to the active device, and the portion of the transfer line is arranged corresponding to the pixel electrode. The pixels include a first pixel, a second pixel, and a third pixel arranged in the second direction. The first pixel, the second pixel, and the third pixel include a plurality of portions of the transfer line and are structurally different from one another.

In an embodiment of the disclosure, in the top view of the pixel array substrate, the pixel electrode of the first pixel and the portion of the transfer line of the first pixel are partially overlapped.

In an embodiment of the disclosure, the second pixel further includes a common electrode. In the above-mentioned top view of the pixel array substrate, in the top view of the pixel array substrate, the pixel electrode and the common electrode of the second pixel are partially overlapped, the common electrode and the portion of the transfer line of the second pixel are overlapped, a gap exists between the pixel electrode and the transfer line of the second pixel, and the transfer line of the second pixel crosses over one of the gate lines electrically connected to the active device of the second pixel.

In an embodiment of the disclosure, the second pixel further includes a common electrode. In the top view of the pixel array substrate, the pixel electrode and the common electrode of the second pixel are partially overlapped, the common electrode and the portion of the transfer line of the second pixel are overlapped, a gap exists between the pixel electrode and the transfer line of the second pixel, and the portion of the transfer line of the second pixel is electrically connected one of the gate lines electrically connected to the active device of the second pixel.

In an embodiment of the disclosure, in the top view of the pixel array substrate, a line width of the portion of the transfer line of the first pixel is greater than a line width of the portion of the transfer line of the second pixel.

In an embodiment of the disclosure, in the top view of the pixel array substrate, the line width of the portion of the transfer line of the second pixel is smaller than a line width of the common electrode of the second pixel.

In order to make the aforementioned features and advantages of the disclosure comprehensible, embodiments accompanied with figures are described in detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the disclosure, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the disclosure and, together with the description, serve to explain the principles described herein.

FIG. **1** is a schematic top view of a display device **10** according to an embodiment of the disclosure.

FIG. **2** is a schematic top view of a pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **3** is a schematic enlarged view of a pixel **120A-1** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **4** is a schematic cross-sectional view of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **5** is a schematic enlarged view of a pixel **120**A-**2** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **6** is a schematic enlarged view of a pixel **120**A-**3** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **7** is a schematic enlarged view of a pixel **120**C-**1** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **8** is a schematic cross-sectional view of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **9** is a schematic enlarged view of a pixel **120**C-**2** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **10** is a schematic enlarged view of a pixel **120**C-**3** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **11** is a schematic enlarged view of a pixel **120**C-**4** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **12** is a schematic cross-sectional view of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **13** is a schematic enlarged view of a pixel **120**C-**5** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **14** is a schematic enlarged view of a pixel **120**C-**6** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **15** is a schematic enlarged view of a pixel **120**C-**7** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **16** shows signals of a plurality of transfer lines gl**1**-gl**14** (or a plurality of gate lines GL**1**-GL**14**) during a reverse scan of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **17** shows signals of the transfer lines gl**1**-gl**14** (or the gate lines GL**1**-GL**14**) during a forward scan of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **18** is a schematic top view of a pixel array substrate **100**A according to another embodiment of the disclosure.

FIG. **19** is a schematic enlarged view of a pixel **120**B-**1** of the pixel array substrate **100**A according to another embodiment of the disclosure.

FIG. **20** is a schematic enlarged view of a pixel **120**B-**2** of the pixel array substrate **100**A according to another embodiment of the disclosure.

FIG. **21** is a schematic enlarged view of a pixel **120**B-**3** of the pixel array substrate **100**A according to another embodiment of the disclosure.

DESCRIPTION OF THE EMBODIMENTS

Reference will now be made in detail to the present embodiments of the disclosure, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

In the accompanying drawings, the thicknesses of layers, films, panels, regions, and the like are enlarged for clarity. Throughout the specification, same reference numerals indicate same components. It should be understood that when a component such as a layer, film, region or substrate is referred to as being "on" or "connected" to another component, it may be directly on or connected to the another component, or intervening components may also be present. In contrast, when a component is referred to as being "directly on" or "directly connected to" another component, there are no intervening assemblies present. As used herein, "connection" may refer to a physical and/or electrical connection. In addition, an "electrical connection" or "coupling" may be the another component between two components.

As used herein, "about", "approximately", or "substantially" is inclusive of the stated value and means within an acceptable range of deviation for the particular value as determined by one of ordinary skill in the art, considering the measurement in question and the error associated with measurement of the particular quantity (i.e., the limitations of the measurement system). For instance, "about" can mean within one or more standard deviations, or within ±30%, ±20%, ±10%, ±5% of the stated value. Further, as used herein, "about", "approximately", or "substantially" may depend on optical properties, etch properties, or other properties to select a more acceptable range of deviations or standard deviations without one standard deviation for all properties.

Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which the disclosure belongs. It will be further understood that terms such as those defined in commonly used dictionaries should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and the disclosure and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

FIG. **1** is a schematic top view of a display device **10** according to an embodiment of the disclosure. In FIG. **1**, a pixel array substrate **100** and a driver device **200** are illustrated, while the other components of the display device **10** are omitted.

FIG. **2** is a schematic top view of the pixel array substrate **100** according to an embodiment of the disclosure and corresponds to a partial region R shown in FIG. **1**. A plurality of pixels **120**, a plurality of data lines DL, and a plurality of bridge devices BL shown in FIG. **2** are omitted in FIG. **1**.

Note that FIG. **2** schematically illustrates the pixel array substrate **100** and does not depict the actual layout of the pixel array substrate **100**; the actual layout of various pixels **120** of the pixel array substrate **100** is respectively shown in FIG. **3**, FIG. **5**-FIG. **7**, and FIG. **9**-FIG. **15**.

FIG. **3** is a schematic enlarged view of a pixel **120**A-**1** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **4** is a schematic cross-sectional view of the pixel array substrate **100** according to an embodiment of the disclosure and corresponds to a sectional line A-A' shown in FIG. **3**.

FIG. **5** is a schematic enlarged view of a pixel **120**A-**2** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **6** is a schematic enlarged view of a pixel **120**A-**3** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **7** is a schematic enlarged view of a pixel **120**C-**1** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **8** is a schematic cross-sectional view of the pixel array substrate **100** according to an embodiment of the disclosure and corresponds to a sectional line B-B' shown in FIG. **7**.

FIG. **9** is a schematic enlarged view of a pixel **120C-2** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **10** is a schematic enlarged view of a pixel **120C-3** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **11** is a schematic enlarged view of a pixel **120C-4** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **12** is a schematic cross-sectional view of the pixel array substrate **100** according to an embodiment of the disclosure and corresponds to a sectional line C-C' shown in FIG. **11**.

FIG. **13** is a schematic enlarged view of a pixel **120C-5** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **14** is a schematic enlarged view of a pixel **120C-6** of the pixel array substrate **100** according to an embodiment of the disclosure.

FIG. **15** is a schematic enlarged view of a pixel **120C-7** of the pixel array substrate **100** according to an embodiment of the disclosure.

The structure of the pixel array substrate **100** of this embodiment is described below with reference to FIG. **1**-FIG. **15**.

As shown in FIG. **1** and FIG. **2**, the display device **10** includes a pixel array substrate **100**, an opposite substrate (not shown) opposite to the pixel array substrate **100**, a display medium (not shown) disposed between the pixel array substrate **100** and the opposite substrate, and a driver device **200** for driving the pixel array substrate **100**. For instance, in this embodiment, the driver device **200** may include a chip, and the chip may be bonded to the pixel array substrate **100** through a chip on film (COF) process. However, the disclosure is not limited thereto. According to other embodiments, the chip may also be bonded to the pixel array substrate **100** through a chip on glass (COG) process, tape automated bonding (TAB), or another method.

The pixel array substrate **100** includes a substrate **110**. The substrate **110** is mainly configured to hold a plurality of components of the pixel array substrate **100**. For instance, in this embodiment, a material of the pixel array substrate **110** may be glass. However, the disclosure is not limited thereto. According to other embodiments, the material of the substrate **110** may also be quartz, organic polymer, an opaque/reflective material (such as wafer, ceramic, etc.), or any other appropriate material.

The pixel array substrate **100** includes a plurality of data lines DL and a plurality of gate lines GL. The data lines DL and the gate lines GL are disposed on the substrate **110**. The data lines DL are arranged in a first direction x, and the gate lines GL are arranged in a second direction y, wherein the first direction x and the second direction y are interlaced with each other. For instance, in this embodiment, the first direction x and the second direction y may be perpendicular to each other, which should however not be construed as a limitation in the disclosure.

In addition, the data lines DL and the gate lines GL belong to different film layers. For instance, in this embodiment, the gate lines GL may selectively belong to a first metal layer, and the data lines DL may selectively belong to a second metal layer, which should however not be construed as a limitation in the disclosure.

In consideration of conductivity, in this embodiment, the data lines DL and the gate lines GL are made of a metal material. However, the disclosure is not limited thereto. According to other embodiments, the data lines DL and the gate lines GL may also be made of other conductive materials, such as alloy, metal nitrides, metal oxides, metal oxynitrides, or a stacked layer of metal and other conductive materials.

With reference to FIG. **2**, FIG. **3**, and FIG. **4**, the pixel array substrate **100** includes a plurality of pixels **120**. The pixels **120** are disposed on the substrate **110**. Each of the pixels **120** includes an active device **121** and a pixel electrode **122**, the active device **121** is electrically connected to a corresponding data line DL and a corresponding gate line GL, and the pixel electrode **122** is electrically connected to the active device **121**.

For instance, in this embodiment, the active device **121** includes a thin film transistor having a source **121***a*, a drain **121***b*, a gate **121***c*, and a semiconductor pattern **121***d*. The insulation layer **130** is sandwiched between the gate electrode **121***c* and the semiconductor pattern **121***d*, the source **121***a* and the drain **121***b* are respectively electrically connected to two different regions of the semiconductor pattern **121***d*, the source **121***a* is electrically connected to a corresponding data line DL, the gate **121***c* is electrically connected to a corresponding gate line GL, and the drain **121***b* is electrically connected to the pixel electrode **122**. In this embodiment, each of the pixels **120** further includes a common electrode cl, and the common electrode cl and the pixel electrode **122** are partially overlapped to form a storage capacitor.

For instance, in this embodiment, the gate electrode **121***c* and the common electrode cl may selectively belong to the first metal layer, and the source electrode **121***a* and the drain electrode **121***b* may selectively belong to the second metal layer. The pixel array substrate **100** may further include an insulation layer **140** disposed on the second metal layer. The pixel electrode **122** may be disposed on the insulation layer **140** and electrically connected to the drain electrode **121***b* of the thin film transistor through a through hole **140***a* of the insulation layer **140**; however, the disclosure is not limited thereto.

In this embodiment, the pixel electrode **122** may belong to a transparent conductive layer, which includes metal oxides, such as indium tin oxide, indium zinc oxide, aluminum tin oxide, aluminum zinc oxide, indium germanium zinc oxide, other suitable oxides, or a stacked layer of at least two of the above, which should however not be construed as a limitation in the disclosure.

With reference to FIG. **2** and FIG. **3**, in this embodiment, the pixels **120** may be arranged in a plurality of pixel rows, and the pixels **120** in each pixel row are arranged in the first direction x; the common electrodes cl of the pixels **120** in the same pixel row may be directly connected to form a common electrode pattern CL; the common electrode patterns CL in the pixel rows are arranged in the second direction y; the pixel array substrate **100** further includes a plurality of bridge devices BL arranged in the first direction x; the common electrode patterns CL in the pixel rows may be electrically connected to each other through the bridge devices BL.

In other words, as shown in the top view of the pixel array substrate **100**, the bridge devices BL and the common electrode patterns CL having the same reference potential may be interlaced into a mesh-like conductive pattern. However, the disclosure is not limited thereto. According to other embodiments, the common electrodes cl of the pixels

120 may also be electrically connected to each other by the bridge devices arranged in another manner.

For instance, in this embodiment, the common electrode patterns CL may selectively belong to the first metal layer, the bridge devices BL may selectively belong to the second metal layer, and the bridge devices BL may be electrically connected to the common electrodes CL through the through holes **130***c* of the insulation layer **130**. The pattern CL, However, the disclosure is not limited thereto.

With reference to FIG. **1**, FIG. **2**, and FIG. **3**, the pixel array substrate **100** also includes a plurality of transfer lines gl. The transfer lines gl are disposed on the substrate **110** and arranged in the first direction x. The transfer lines gl arranged in the first direction x are electrically connected to the gate lines GL arranged in the second direction y, respectively.

With reference to FIG. **2**, FIG. **3**, and FIG. **4**, for instance, in this embodiment, the gate lines GL may selectively belong to the first metal layer, and main portions gla of the transfer lines gl may selectively belong to the second metal layer. The insulation layer **130** is disposed between the first metal layer and the second metal layer, and the insulation layer **130** has a plurality of first through-holes **130***a*. The main portions gla of the transfer lines gl may be electrically connected to the gate lines GL through the first through-holes **130***a* of the insulation layer **130**, respectively, which should however not be construed as a limitation in the disclosure.

With reference to FIG. **1** and FIG. **2**, in this embodiment, a source driving circuit connected to the data lines DL is disposed on the first side (e.g., an upper side) of the substrate **110**, the gate lines GL are electrically connected to a gate driving circuit provided on the first side (e.g., the upper side) of the substrate **110** through the transfer lines gl. That is, in this embodiment, the source driving circuit and the gate driving circuit are disposed on the same side of the substrate **110**. In addition, in this embodiment, the source driving circuit and the gate driving circuit may be selectively integrated into the same driver device **200** (e.g., a chip), which should however not be construed as a limitation in the disclosure.

With reference to FIG. **2**, FIG. **3** and FIG. **4**, the pixels **120** include a plurality of first pixels **120**A. For clear illustration, the first pixels **120**A in FIG. **2** are illustrated in form of a plurality of rectangular patterns with spots. In the top view of the pixel array substrate **100**, the pixel electrode **122** of each of the first pixels **120**A is partially overlapped with at least one of the transfer lines gl. Since the pixel electrode **122** of each first pixel **120**A is partially overlapped with at least one transfer line gl, an area occupied by the pixel electrode **122** of the first pixel **120**A is large, which is conducive to the improvement of an aperture ratio of the pixel array substrate **100**.

With reference to FIG. **2**, FIG. **3**, FIG. **5**, and FIG. **6**, in this embodiment, the first pixels **120**A may include various first pixels **120**A-**1**, **120**A-**2**, and **120**A-**3**. As shown in FIG. **2**, the first pixel **120**A-**1**, the first pixel **120**A-**2**, and the first pixel **120**A-**3** may be arranged in the first direction x.

With reference to FIG. **2**, FIG. **3**, and FIG. **4**, a first edge (e.g., a right edge) of the pixel electrode **122** of the first pixel **120**A-**1** is located on one of the transfer lines gl, and a second edge (e.g., a left edge) of the pixel electrode **122** of the first pixel **120**A-**1** is disposed on the common electrode cl and the bridge device BL. In this embodiment, the bridge devices BL shield gaps between two adjacent pixel electrodes **122**. The bridge devices BL may also be referred to as shielding metal, which should however not be construed as a limitation in the disclosure.

With reference to FIG. **2** and FIG. **5**, the first edge (e.g., the right edge) and the second edge (e.g., the left edge) of the pixel electrode **122** of the first pixel **120**A-**2** may be located on two of the transfer lines gl, respectively.

With reference to FIG. **2** and FIG. **6**, the first edge (e.g., the right edge) of the pixel electrode **122** of the first pixel **120**A-**3** is located on the common electrode cl and the bridge device BL, and the second edge (e.g., the left edge) of the pixel electrode **122** of the first pixel **120**A-**3** may be located on one of the transfer lines gl.

With reference to FIG. **2**, in this embodiment, the pixels **120** of the pixel array substrate **100** further include a plurality of second pixels **120**C. For clear illustration, the second pixels **120**C in FIG. **2** are depicted by a plurality of blank rectangular patterns.

With reference to FIG. **2** and FIG. **7**, in the top view of the pixel array substrate **100**, the pixel electrodes **122** of the second pixels **120**C and the common electrodes cl of the second pixels **120**C are partially overlapped, and the common electrodes cl of the second pixels **120**C overlap the transfer lines gl. Gaps G exists between the pixel electrodes **122** of the second pixels **120**C and the transfer lines gl. That is, the pixel electrodes **122** of the second pixels **120**C and the common electrodes cl of the second pixels **120**C are partially overlapped, but the pixel electrodes **122** of the second pixels **120**C and the transfer lines gl do not overlap.

Since the pixel electrodes **122** of the second pixels **120**C and the transfer lines gl do not overlap, the parasitic capacitance between the pixel electrodes **122** of the second pixels **120**C and the transfer lines gl is small, which is conducive to the reduction of a feedthrough voltage caused by the parasitic capacitance, thereby improving the performance of the display device **10**.

With reference to FIG. **2**, FIG. **3**, and FIG. **7**, in this embodiment, the main portion gla of the same transfer line gl has a first portion gla-**1** and a second portion gla-**2** connected to each other; in the top view of the pixel array substrate **100**, the first portion gla-**1** of the transfer line gl and the pixel electrode **122** of the first pixel **120**A are partially overlapped, and a gap exists between the second portion gla-**2** of the transfer line gl and the pixel electrode **122** of the second pixel **120**C. In particular, a line width W**1** of the first portion gla-**1** of the transfer line gl is larger than a line width W**2** of the second portion gla-**2** of the transfer line gl. That is, a thickness of the transfer line gl next to the pixel electrode **122** of the second pixel **120**C is reduced, so that the transfer line gl is not overlapped with the pixel electrode **122** of the second pixel **120**C. With reference to FIG. **7**, in addition, according to this embodiment, the line width W**2** of the second portion gla-**2** of the main portion gla of the transfer line gl is smaller than a line width W**0** of the common electrode cl of the second pixel **120**C.

With reference to FIG. **2**, FIG. **7**, FIG. **9**, FIG. **10**, FIG. **11**, FIG. **13**, FIG. **14**, and FIG. **15**, in this embodiment, the second pixels **120**C include various second pixels **120**C-**1**, **120**C-**2**, **120**C-**3**, **120**C-**4**, **120**C-**5**, **120**C-**6**, and **120**C-**7**.

With reference to FIG. **2**, the second pixels **120**C-**1**, **120**C-**2**, and **120**C-**3** are sequentially arranged in the first direction x.

With reference to FIG. **2**, FIG. **7**, and FIG. **8**, the transfer line gl is disposed next to the first edge (e.g., the right edge) of the pixel electrode **122** of the second pixel **120**C-**1**, and the first edge of the pixel electrode **122** of the second pixel **120**C-**1** is overlapped with the common electrode cl but is not overlapped with the transfer line gl. The transfer line gl

is not electrically connected to the gate **121***c* of the active device **121** of the second pixel **120C-1**. The second edge (e.g., the left edge) of the pixel electrode **122** of the second pixel **120C-1** is disposed on the common electrode cl and the bridge device BL.

With reference to FIG. **2** and FIG. **9**, a plurality of transfer lines gl are disposed next to the first edge and the second edge (e.g., the right edge and the left edge) of the pixel electrode **122** of the second pixel **120C-2**, the first edge and the second edge of the pixel electrode **122** of the second pixel **120C-2** is overlapped with the common electrode cl but is not overlapped with the transfer lines gl, and the transfer lines gl are not electrically connected to the gate **121***c* of the active device **121** of the second pixel **120C-2**.

With reference to FIG. **2** and FIG. **10**, the first edge of the pixel electrode **122** of the second pixel **120C-3** is disposed on the common electrode cl and the bridge device BL; the transfer line gl is disposed next to the second edge (e.g., the left edge) of the pixel electrode **122** of the second pixel **120C-3**, and the transfer line gl is not electrically connected to the gate **121***c* of the active device **121** of the second pixel **120C-3**.

With reference to FIG. **2**, FIG. **11**, FIG. **12**, FIG. **13**, FIG. **14**, and FIG. **15**, the common electrode cl of each second pixel **120C-4**, **120C-5**, **120C-6**, and **120C-7** and at least one transfer line gl are overlapped, and the at least one transfer line gl is electrically connected to the gate **121***c* of the active device **121** of each of the second pixels **120C-4**, **120C-5**, **120C-6**, and **120C-7** through at least one first through hole **130***a* of the insulation layer **130** disposed next to the second pixels **120C-4**, **120C-5**, **120C-6**, and **120C-7**.

With reference to FIG. **2**, the second pixels **120C-4** and **120C-5** are sequentially arranged in the first direction x, the second pixels **120C-6** and **120C-5** are sequentially arranged in the second direction y, and the second pixels **120C-6** and **120C-7** are arranged sequentially in the first direction x.

With reference to FIG. **2**, FIG. **11**, and FIG. **12**, one transfer line gl is disposed next to the first edge (e.g., the right edge) of the pixel electrode **122** of the second pixel **120C-4**, and the transfer line gl is electrically connected to the gate **121***c* of the active device **121** of the second pixel **120C-4**; the second edge (e.g., the left edge) of the pixel electrode **122** of the second pixel **120C-4** is disposed on the common electrode cl and the bridge device BL.

With reference to FIG. **2** and FIG. **13**, one transfer line gl is disposed next to the first edge (e.g., the right edge) of the pixel electrode **122** of the second pixel **120C-5**, and the transfer line gl is not electrically connected to the gate **121***c* of the active device **121** of the pixel **120C-5**; another transfer line gl is disposed next to the second edge (e.g., the left edge) of the pixel electrode **122** of the second pixel **120C-5** and electrically connected to the gate **121***c* of the active device **121** of the second pixel **120C-5**.

With reference to FIG. **2** and FIG. **14**, one transfer line gl is disposed next to the first edge (e.g., the right edge) of the pixel electrode **122** of the second pixel **120C-6**, and the transfer line gl is electrically connected to the second pixel **120C-6** of the gate **121***c* of the active device **121**; another transfer line gl is disposed next to the second edge (e.g., the left edge) of the pixel electrode **122** of the second pixel **120C-6** and is not electrically connected to the active device **121** of the second pixel **120C-6**.

With reference to FIG. **2** and FIG. **15**, the first edge (e.g., the right edge) of the pixel electrode **122** of the second pixel **120C-7** is disposed on the common electrode cl and the bridge device BL, one transfer line gl is disposed next to the second edge (e.g., the left edge) of the pixel electrode **122** of the second pixel **120C-7**, and the transfer line gl is electrically connected to the gate **121***c* of the active device **121** of the second pixel **120C-7**.

With reference to FIG. **2**, FIG. **3**, and FIG. **7**, in this embodiment, each of the transfer lines gl may include a main portion gla and at least one auxiliary portion glb. The main portion gla crosses over a plurality of gate lines GL, and each of the at least one auxiliary portion glb is disposed between two adjacent gate lines GL and partially overlapped with the pixel electrode **122** of one of the first pixels **120A**. Two ends of each of the at least one auxiliary portion glb are electrically connected to two different regions of the main portion gla. That is, in this embodiment, each of the transfer lines gl may be formed by connecting the main portion gla belonging to different conductive layers and a plurality of auxiliary portions glb in parallel, so as to reduce the resistance value.

For instance, in this embodiment, the main portion gla of each transfer line gl may be selectively formed in the second metal layer, and the at least one auxiliary portion glb of each transfer line gl may be selectively formed in the first metal layer, the two ends of each of the at least one auxiliary portion glb may be electrically connected to the two different regions of the main portion gla through the second through hole **130***b* of the insulation layer **130**, which should however not be construed as a limitation in the disclosure.

FIG. **16** shows signals of a plurality of transfer lines gl**1**-gl**14** (or a plurality of gate lines GL**1**-GL**14**) during a reverse scan of the pixel array substrate **100** according to an embodiment of the disclosure.

With reference to FIG. **2** and FIG. **16**, the pixels **120** include a plurality of pixel groups GP. Each pixel group GP includes one first pixel **120A** and n second pixels **120C** sequentially arranged along one transfer line gl (e.g., gl**14**). The n second pixels **120C** and one first pixel **120A** are sequentially arranged in a reverse scan direction (e.g., the opposite direction of the second direction y), and the gate line GL (e.g., GL**14**) electrically connected to the first pixel **120A** is electrically connected to the transfer line gl (e.g., gl**14**) through the first through hole **130***a* of the insulation layer **130**, wherein n is a positive integer greater than or equal to 2. In other words, in the same pixel group GP, another second pixel **120C** is disposed between the first pixel **120A** and one second pixel **120C** disposed corresponding to the first through hole **130***a*.

In this embodiment, the first pixel **120A** of each pixel group GP is the pixel **120** closest to the second pixel **120C** of the pixel group GP, and the first pixels **120A** of the pixel groups GP are arranged substantially in a staircase shape.

In this embodiment, the number n of the second pixels **120C** of each pixel group GP may be determined according to a driving method of the gate lines GL (or a driving method of the transfer lines gl).

Specifically, in this embodiment, the gate lines GL are divided into a plurality of gate line groups K, each of the gate line groups K includes m gate lines, and m gate lines GL of the same gate line group K are simultaneously turned on, wherein m is a positive integer greater than or equal to 1; when each of the gate line groups K is turned on, each of the m gate lines GL of the gate line group K has a gate-on pulse, and a time length of the gate pulse is T; the gate line groups K are sequentially turned on with a time delay, a time length of the time delay is t, $n \geq \{[(Tt)/t]*m\}+m$, $T=kt$, and k is a positive integer greater than or equal to 1.

For instance, in this embodiment, the gate lines GL are divided into a plurality of gate line groups K, and each of the gate line groups K includes 2 gate lines GL (i.e., m=2), two

gate lines GL of the same gate line group K are turned on at the same time. When each of the gate line groups K is turned on, each of the two gate lines GL of the gate line group K has the gate-on pulse, k=5, and the time length of the gate pulse T=5t, $n \geq \{[(5t-t)/t]*2\}+2$, i.e., $n \geq 10$. That is, in this embodiment, the number of the second pixel **120**Cs of one pixel group GP is greater than or equal to 10, e.g., 11 or 12; however, the disclosure is not limited thereto. According to this embodiment, note that k being 5 is merely exemplary, which should however not be construed as a limitation in the disclosure. In other embodiments, k may be a positive integer other than 5 and greater than or equal to 1.

In the same pixel group GP, one gate line GL (e.g., GL**14**) electrically connected to the first second pixel **120**C has a gate-on potential in a time interval T**1**, and another gate line GL (e.g., GL**2**) electrically connected to the first pixel **120**A has the gate-on potential in a time interval T**7**. The time interval T**1** and the time interval T**7** are not overlapped in time sequence.

That is, when the gate line GL**2** has the gate-on potential and the first pixel **120**A of the pixel group GP is charged, the signal of the transfer line gl**14** adjacent to the first pixel **120**A has been switched to a gate-off potential; therefore, even though the pixel electrode **122** of the first pixel **120**A and the transfer line gl**14** are partially overlapped, the signal of the transfer line gl**14** does not easily affect the potential of the pixel electrode **122** of the first pixel **120**A.

On the other hand, in the same pixel group GP**1**, the gate lines GL**13**-GL**5** that are electrically connected to other second pixels **120**C (e.g., the second to ten second pixels **120**C) respectively have the gate-on potential in the time intervals T**1**, T**2**, T**3**, T**3**, and T**5**. When the gate lines GL**13**-GL**5** have the gate-on potential and other second pixels **120**C (e.g., the second to ten second pixels **120**C) are charged, the signal of the transfer line gl**14** adjacent to other second pixels **120**C (e.g., the second to ten second pixels **120**C) is switched from the gate-on potential to the gate-off potential. However, the pixel electrodes **122** of other second pixels **120**C (e.g., the second to ten second pixels **120**C) do not overlap the transfer line gl**14**, and the parasitic capacitance between the transfer line gl**14** and the pixel electrodes **122** of other second pixels **120**C (e.g., the second to ten second pixels **120**C) is small; therefore, the change of the signal of the transfer line gl**14** does not easily affect the potentials of the pixel electrodes **122** of other second pixels **120**C (e.g., the second to ten second pixels **120**C).

According to this embodiment, note that the pixel electrode **122** of the first pixel **120**A and the transfer line gl are overlapped, and the area occupied by the pixel electrode **122** of the first pixel **120**A is large, which is conducive to the improvement of the aperture ratio of the pixel array substrate **100**. In addition, in this embodiment, the transfer line gl may include the main portion gla and the at least one auxiliary portion glb which belong to two different electrical metal layers and are electrically connected to each other through the second through hole **130***b*, i.e., the transfer line gl may have a double-layer metal wiring design, which is conducive to the reduction of the overall resistance value of the transfer line gl, so that the pixel array substrate **100** may be easily driven. The pixel electrode **122** of the second pixel **120**C and the transfer line gl are not overlapped, and the potential of the pixel electrode **122** of the second pixel **120**C is not easily affected by the parasitic capacitance between the transfer line gl and the pixel electrode **122** of the second pixel **120**C. In this embodiment, the positions of the first pixels **120**A and the positions of the second pixels **120**C appropriately arranged according to the driving method of the gate lines GL, so as to form the pixel array substrate **100** which has the high aperture ratio and may be easily driven.

In the embodiment shown in FIG. **16**, the pixel array substrate **100** is driven in a reverse scan manner. However, the pixel array substrate **100** is not limited to being driven in a forward scan manner or the reverse scan manner. FIG. **17** shows signals of the transfer lines gl**1**-gl**14** (or the gate lines GL**1**-GL**14**) during a forward scan of the pixel array substrate **100** according to an embodiment of the disclosure. The pixel array substrate **100** shown in FIG. **2** may also be driven in the forward scan manner shown in FIG. **17**. People having ordinary knowledge in the art are able to implement the invention according to one or more embodiments, and therefore no repetitive descriptions will be given hereinafter.

With reference to FIG. **2**, FIG. **3**, FIG. **7**, and FIG. **11**, from another perspective, each of some of the pixels **120** of the pixel substrate **100** may include an active device **121**, a pixel electrode **122**, and a portion of a transfer line gl, the active device **121** is electrically connected to a corresponding data line DL and a corresponding gate line GL, the pixel electrode **122** is electrically connected to the active device **121**, and a portion of the transfer line gl is disposed corresponding to the pixel electrode **122**.

The pixels **120** include a first pixel **120**A-**1**, a second pixel **120**C-**1**, and a second pixel **120**C-**4** (also referred to as a third pixel) arranged in the second direction y. The first pixel **120**A-**1**, the second pixel **120**C-**1**, and the second pixel **120**C-**4** include plural portions of the same transfer line gl; that is, one portion of the transfer line gl of the first pixel **120**A-**1**, one portion of the transfer line gl of the second pixel **120**C-**1**, and one portion of the transfer line gl of the second pixel **120**C-**4** are directly connected. In particular, the structure of the first pixel **120**A-**1**, the structure of the second pixel **120**C-**1**, and the structure of the second pixel **120**C-**4** are different from one another.

With reference to FIG. **2** and FIG. **3**, specifically, in this embodiment, the transfer line gl of the first pixel **120**A-**1** and the pixel electrode **122** of the first pixel **120**A-**1** are partially overlapped.

With reference to FIG. **2** and FIG. **7**, the pixel electrode **122** of the second pixel **120**C-**1** and the common electrode cl of the second pixel **120**C-**1** are partially overlapped, and the common electrode cl of the second pixel **120**C-**1** and one portion of the transfer line gl of the second pixel **120**C-**1** are overlapped. A gap G exists between the pixel electrode **122** of the second pixel **120**C-**1** and the transfer line gl of the second pixel **120**C-**1**, and one portion of the transfer line gl of the second pixel **120**C-**1** crosses over one gate line GL electrically connected to the active device **121** of the second pixel **120**C (i.e., one portion of the transfer line gl of the second pixel **120**C-**1** is electrically independent from the active device **121** of the second pixel **120**C), which is different from that in the first pixel **120**A-**1**.

With reference to FIG. **2** and FIG. **11**, the pixel electrode **122** of the second pixel **120**C-**4** and the common electrode cl of the second pixel **120**C-**4** are partially overlapped, and the common electrode cl of the second pixel **120**C-**4** and one portion of the transfer line gl of the second pixel **120**C-**4** are overlapped. A gap G exists between the pixel electrode **122** of the second pixel **120**C-**4** and the transfer line gl of the second pixel **120**C-**4**. One portion of the transfer line gl of the second pixel **120**C-**4** is a gate line GL electrically connected to the active device **121** electrically connected to the second pixel **120**C-**4**, which is different from that in the second pixel **120**C-**1**.

In the following embodiments, the same reference numbers are applied to denote the same or similar devices, and

the description of the same technical content is omitted. The omitted parts may be referred to as those provided in the previous embodiments and will not repeated in the following embodiments.

FIG. **18** is a schematic top view of a pixel array substrate **100**A according to another embodiment of the disclosure. In FIG. **18**, the substrate of the pixel array substrate **100**A is omitted.

Note that FIG. **18** schematically illustrates the pixel array substrate **100**A and does not show the actual layout of the pixel array substrate **100**A. The actual layout of various pixels **120**B of the pixel array substrate **100**A is depicted in FIG. **19**. FIG. **20**, and FIG. **21**. In addition, a shielding electrode **170** shown FIG. **19**, FIG. **20**, and FIG. **21** is omitted in FIG. **18**.

FIG. **19** is a schematic enlarged view of a pixel **120**B-**1** of the pixel array substrate **100**A according to another embodiment of the disclosure.

FIG. **20** is a schematic enlarged view of a pixel **120**B-**2** of the pixel array substrate **100**A according to another embodiment of the disclosure.

FIG. **21** is a schematic enlarged view of a pixel **120**B-**3** of the pixel array substrate **100**A according to another embodiment of the disclosure.

With reference to FIG. **18**, FIG. **19**, FIG. **20**, and FIG. **21**, the pixel array substrate **100**A includes a plurality of data lines DL, a plurality of gate lines GL, a plurality of pixels **120**B, and a plurality of transfer lines gl. The data lines DL are arranged in a first direction x, and the gate lines GL are arranged in a second direction y, wherein the first direction x and the second direction y are interlaced with each other. Each of the pixels **120**B includes an active device **121** and a pixel electrode **122**. The active device **121** is electrically connected to one corresponding data line DL and one corresponding gate line GL. The pixel electrode **122** is electrically connected to the active device **121**. The transfer lines gl are arranged in the first direction x and electrically connected to the gate lines GL arranged in the second direction y, respectively.

Different from the aforementioned pixel array substrate **100**, the pixel array substrate **100**A provided in this embodiment further includes a shielding electrode **170**. In the top view of the pixel array substrate **100**A, a gap G exists between the transfer line gl and the pixel electrode **122** of at least one pixel **120**B, the shielding electrode **170** is separated from the pixel electrode **122** of the pixel **120**B, and the shielding electrode **170** and the transfer line gl are overlapped. The shielding electrode **170** may block an electric field generated by the transfer line gl, so as to reduce the adverse effect of the transfer line gl on the potential of the pixel electrode **122**. For instance, in this embodiment, the shielding electrode **170** and the pixel electrode **122** may belong to the same transparent conductive layer, which should however not be construed as a limitation in the disclosure.

In this embodiment, the pixels **120**B may include various pixels **120**B-**1**, **120**B-**2**, and **120**B-**3**. One pixel **120**B-**1**, one pixel **120**B-**2**, and one pixel **120**B-**3** are arranged in the first direction x.

The pixel **120**B-**1**, the pixel **120**B-**2**, and the pixel **120**B-**3** are similar to the aforementioned first pixel **120**A-**1**, first pixel **120**A-**2**, and first pixel **120**A-**3**, respectively, and the difference lies in that at least one gap G exists between each of the pixel electrodes **122** of the pixels **120**B-**1**, **120**B-**2**, and **120**B-**3** and at least one adjacent transfer line gl, and the shielding electrode **170** is overlapped with the transfer lines gl of the pixel electrodes **122** adjacent to the pixels **120**B-**1**, **120**B-**2**, and **120**B-**3**.

It will be apparent to those skilled in the art that various modifications and variations can be made to the disclosed embodiments without departing from the scope or spirit of the disclosure. In view of the foregoing, it is intended that the disclosure covers modifications and variations provided that they fall within the scope of the following claims and their equivalents.

What is claimed is:

1. A pixel array substrate, comprising:

a substrate;

a plurality of data lines, disposed on the substrate and arranged in a first direction;

a plurality of gate lines, disposed on the substrate and arranged in a second direction, wherein the first direction and the second direction are interlaced with each other;

a plurality of pixels, disposed on the substrate, each of the pixels comprising an active device and a pixel electrode, wherein the active device is electrically connected to a corresponding data line of the data lines and a corresponding gate line of the gate lines, and the pixel electrode is electrically connected to the active device; and

a plurality of transfer lines, arranged in the first direction and electrically connected to the gate lines, respectively,

wherein the pixels comprise a plurality of first pixels, and in a top view of the pixel array substrate, at least one of the pixel electrodes of the first pixels is partially overlapped with one of the transfer lines.

2. The pixel array substrate according to claim **1**, wherein the pixels further comprise a plurality of second pixels, at least one of the second pixels further comprises a common electrode,

in the top view of the pixel array substrate, the pixel electrode and the common electrode of the at least one of the second pixels are partially overlapped, the common electrode of the at least one of the second pixels and the one of the transfer lines are overlapped, and a gap exists between the pixel electrode of the at least one of the second pixels and the one of the transfer lines.

3. The pixel array substrate according to claim **2**, wherein the one of the transfer lines has a first portion and a second portion connected to each other,

in the top view of the pixel array substrate, the first portion of the one of the transfer lines and the at least one of the pixel electrodes of the first pixels partially overlap, a gap exists between the second portion of the one of the transfer lines and the pixel electrode of the at least one of the second pixels, and a line width of the first portion of the one of the transfer lines is greater than a line width of the second portion of the one of the transfer lines.

4. The pixel array substrate according to claim **2**, wherein the one of the transfer lines has a second portion,

in the top view of the pixel array substrate, the gap exists between the second portion of the one of the transfer lines and the pixel electrode of the at least one of the second pixels, and a line width of the second portion of the one of the transfer lines is smaller than a line width of the common electrode of the at least one of the second pixels.

5. The pixel array substrate according to claim 1, wherein the pixels further comprise a plurality of second pixels, each of the second pixels comprises a common electrode,

in the top view of the pixel array substrate, the pixel electrode and the common electrode of each of the second pixels are partially overlapped, the common electrode of each of the second pixels is overlapped with a corresponding transfer line of the transfer lines, and a gap exists between the pixel electrode of each of the second pixels and the corresponding transfer line,

the pixels comprise a plurality of pixel groups, and at least one of the pixel groups comprises n second pixels and one of the first pixels sequentially arranged along the corresponding transfer line;

the pixel array substrate further comprising:

an insulation layer, sandwiched between the gate lines and the transfer lines and having a plurality of first through holes, the n second pixels of the at least one of the pixel groups comprising a first second pixel to an nth second pixel arranged in sequence, the active device of the first second pixel being electrically connected to one of the gate lines, each of the transfer lines being electrically connected to the one of the gate lines through one of the first through holes of the insulation layer, wherein n is a positive integer greater than or equal to 2.

6. The pixel array substrate according to claim 5, wherein each of the pixel groups comprises n second pixels and one of the first pixels sequentially arranged along the corresponding transfer line, the n second pixels of each of the pixel groups comprise the first second pixel to the nth second pixel arranged in sequence; the active device of the first second pixel is electrically connected to one of the gate lines, each of the transfer lines is electrically connected to the one of the gate lines through one of the first through holes of the insulation layer, the one of the first pixels of each of the pixel groups is a pixel in the each of the pixel groups closest to the second pixels of the each of the pixel groups, and the first pixels of the pixel groups are arranged substantially in a staircase shape.

7. The pixel array substrate according to claim 1, further comprising:

an insulation layer having a plurality of second through holes, wherein each of the transfer lines comprises a main portion and at least one auxiliary portion, the insulation layer is sandwiched between the main portion and the at least one auxiliary portion, the main portion crosses over the gate lines, the at least one auxiliary portion is disposed between two adjacent gate lines of the gate lines and partially overlapped with the at least one of the pixel electrodes of the first pixels, and two different regions of the main portion are electrically connected to two ends of the at least one auxiliary portion through the second through holes of the insulation layer.

8. A driving method for driving the pixel array substrate according to claim 5, wherein the driving method comprises:

in a first time interval, enabling one of the gate lines electrically connected to the first second pixel of the at least one of the pixel groups to have a gate-on potential; and

in a second time interval, enabling another one of the gate lines electrically connected to the first pixel of the at least one of the pixel groups to have the gate-on potential, wherein the first time interval and the second time interval are not overlapped in time sequence.

9. A driving method for driving the pixel array substrate according to claim 5, wherein the gate lines are categorized into a plurality of gate line groups, and each of the gate line groups comprises m gate lines, wherein m is a positive integer greater than or equal to 1, and the driving method comprises:

simultaneously turning on the m gate lines of the same gate line groups, wherein when each of the gate line groups is turned on, each of the m gate lines of the each of the gate line groups has a gate-on pulse; and

sequentially turning on the gate line groups with a time delay, wherein a time length of the time delay is t, the time length of the gate-on pulse is T, and $n \geq \{[(T-t)/t]*m\}+m$.

10. A pixel array substrate, comprising:

a substrate;

a plurality of data lines, disposed on the substrate and arranged in a first direction;

a plurality of gate lines, disposed on the substrate and arranged in a second direction, wherein the first direction and the second direction are interlaced with each other;

a plurality of pixels, disposed on the substrate, each of the pixels comprising an active device and a pixel electrode, wherein the active device is electrically connected to a corresponding data line of the data lines and a corresponding gate line of the gate lines, and the pixel electrode is electrically connected to the active device;

a plurality of transfer lines, arranged in the first direction and electrically connected to the gate lines, respectively; and

a shielding electrode, wherein in a top view of the pixel array substrate, a gap exists between the pixel electrode of at least one of the pixels and one of the transfer lines, the shielding electrode is separated from the pixel electrode of the at least one of the pixels, and the shielding electrode is overlapped with the one of the transfer lines.

11. A pixel array substrate, comprising:

a substrate;

a plurality of data lines, disposed on the substrate and arranged in a first direction;

a plurality of gate lines, disposed on the substrate and arranged in a second direction, wherein the first direction and the second direction are interlaced with each other; and

a plurality of pixels, disposed on the substrate, each of the pixels comprising an active device, a pixel electrode, and a portion of a transfer line, wherein the active device is electrically connected to a corresponding data line of the data lines and a corresponding gate line of the gate lines, the pixel electrode is electrically connected to the active device, and the portion of the transfer line is arranged corresponding to the pixel electrode,

wherein the pixels comprise a first pixel, a second pixel, and a third pixel arranged in the second direction, and the first pixel, the second pixel, and the third pixel comprise a plurality of portions of the transfer line and are structurally different from one another.

12. The pixel array substrate according to claim 11, wherein in the top view of the pixel array substrate, the pixel electrode of the first pixel and the portion of the transfer line of the first pixel are partially overlapped.

13. The pixel array substrate according to claim 12, wherein the second pixel further comprises a common electrode; in the top view of the pixel array substrate, the

pixel electrode and the common electrode of the second pixel are partially overlapped, the common electrode and the portion of the transfer line of the second pixel are overlapped, a gap exists between the pixel electrode and the transfer line of the second pixel, and the transfer line of the second pixel crosses over one of the gate lines electrically connected to the active device of the second pixel.

14. The pixel array substrate according to claim **13**, wherein the second pixel further comprises a common electrode; in the top view of the pixel array substrate, the pixel electrode and the common electrode of the second pixel are partially overlapped, the common electrode and the portion of the transfer line of the second pixel are overlapped, a gap exists between the pixel electrode and the transfer line of the second pixel, and the portion of the transfer line of the second pixel is electrically connected one of the gate lines electrically connected to the active device of the second pixel.

15. The pixel array substrate according to claim **13**, wherein in the top view of the pixel array substrate, a line width of the portion of the transfer line of the first pixel is greater than a line width of the portion of the transfer line of the second pixel.

16. The pixel array substrate according to claim **15**, wherein in the top view of the pixel array substrate, the line width of the portion of the transfer line of the second pixel is smaller than a line width of the common electrode of the second pixel.

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