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(71) Applicant (for all designated States except US):
FAIRCHILD SEMICONDUCTOR CORPORATION
[US/US]; 3030 Orchard Parkway, San Jose, CA 95134 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **DOMELJ, Martin**
[SE/SE]; c/o Fairchild Semiconductor Corporation, 3030 Orchard Parkway, San Jose, CA 95134 (US). **KONSTANTINOV, Andrei** [SE/SE]; c/o Fairchild Semicon-

ductor Corporation, 3030 Orchard Parkway, San Jose, CA 95134 (US). **ZARING, Carina** [SE/SE]; c/o Fairchild Semiconductor Corporation, 3030 Orchard Parkway, San Jose, CA 95134 (US). **GUMAELIUS, Krister** [SE/SE]; c/o Fairchild Semiconductor Corporation, 3030 Orchard Parkway, San Jose, CA 95134 (US). **REIMARK, Mats** [SE/SE]; c/o Fairchild Semiconductor Corporation, 3030 Orchard Parkway, San Jose, CA 95134 (US).

(74) Agent: **BADEL, Xavier, Claude, Yves**; P.O. Box 45086, S-104 30 Stockholm (SE).

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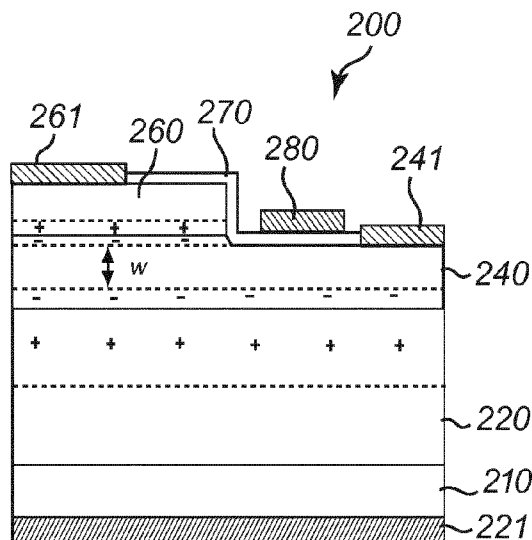


Fig. 2b

(57) Abstract: New designs for silicon carbide (Si C) bipolar junction transistors (BJTs) and new methods of manufacturing such Si C BJTs are provided. The Si C BJT comprises a collector region (220), a base region (240) and an emitter region (260). Further, a surface passivation layer is deposited between an emitter contact for contacting the emitter region and a base contact for contacting the base region. The deposited surface passivation layer induces the formation of a depletion region under said surface passivation layer in the extrinsic part of said base region. Further, the Si C BJT comprises a surface gate arranged at the deposited surface passivation layer. The surface gate is configured to apply a negative electric potential to the deposited surface passivation layer with respect to the electric potential in the base region. The present invention is advantageous in that it provides Si C BJTs with improved blocking capabilities.



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BIPOLAR JUNCTION TRANSISTOR IN SILICON CARBIDE WITH IMPROVED BREAKDOWN VOLTAGE

FIELD OF THE INVENTION

The present invention relates to the field of power semiconductor device technology and, in particular, to silicon carbide bipolar junction
5 transistors for high power applications. The present invention relates also to methods of manufacturing such silicon carbide bipolar junction transistors.

BACKGROUND OF THE INVENTION

Power transistors may be used as switches in power electronic
10 systems. The switches alternate between conducting a high current in the on-state and blocking a high voltage in the off-state. Two important figures of merit for power switches are low power losses during forward conduction and low power losses during switching between on and off. Low power losses are beneficial because they enable energy savings and because more compact
15 systems can be constructed as the heat dissipation caused by the power losses is reduced.

Silicon carbide (SiC) bipolar junction transistors (BJTs) are power transistors that have the advantage of providing substantially lower power losses during conduction and switching as compared to standard silicon (Si)
20 power transistors thanks to the high breakdown electric field of SiC. In addition, SiC has a high thermal conductivity and is a wide bandgap semiconductor and may therefore advantageously be used for manufacturing devices for high power, high temperature and high frequency applications.

With reference to Figure 1, a standard SiC BJT 100 is described. The
25 SiC BJT 100 comprises a substrate 110 on which a collector layer 120, a base layer 140 and an emitter layer 160 have been grown by epitaxy. In the case of a NPN SiC BJT, the epitaxial structure may normally comprise a low-doped n-type collector layer 120 grown on top of a highly doped n-type substrate 110, a p-type base layer 140 and a highly doped n-type emitter
30 layer 160. After epitaxial growth, the emitter region 160 and the base region

140 are defined using dry etch techniques, thereby providing an elevated emitter region or mesa (i.e. elevated structure) 160. Ohmic contacts 161 and 141 are formed to the emitter region 160 and the base region 140, respectively, and a collector Ohmic contact 121 may be formed at the backside of the substrate 110 to connect the collector region 120.

The Ohmic contact 141 to the base region 140 may be improved by providing a region 142 having an increased acceptor doping using e.g. selective ion implantation followed by a subsequent high-temperature anneal before forming the contact 141. The portion of the base layer 140 located under the emitter mesa 160, i.e. within the outline of the emitter edges, is conventionally referred to as the intrinsic base region 145 whereas the portion of the base layer 140 not capped with the emitter region 160 is conventionally referred to as the extrinsic base region (or extrinsic part of the base region).

Further, a dielectric layer 170 may be used for surface passivation on top of the SiC BJT 100, between the base and emitter metal contacts 161 and 141, in order to terminate the dangling bonds of the atoms on the SiC surface, and thereby reduce the density of defects which cause surface recombination and surface leakage currents.

Two of the most relevant figures of merits of a BJT are usually the common emitter current gain and the breakdown voltage. In an article entitled "Surface-passivation effects on the performance of 4H-SiC BJTs" published on 1 January 2011 in IEEE Transactions on electronic devices vol. 58 pages 259-265, a study was performed for a number of surface-passivation layers grown or deposited under different process conditions. The study shows that providing surface passivation by plasma-enhanced chemical vapor deposition (PECVD) of silicon dioxide subsequently annealed in N₂O ambient at 1100°C for three hours results in the highest current gain. With such a PECVD silicon dioxide layer as a surface passivation layer, the maximum current gain is increased by 60% as compared to that obtained with a conventional thermally-grown oxide layer. However, such surface passivation results also in the BJT having the lowest breakdown voltage. Further, large variations in breakdown voltage for the devices manufactured with different surface passivation layers in the study have been observed.

Thus, there is a need for providing new designs of SiC BJTs and new methods of manufacturing such BJTs that would alleviate at least some of the above-mentioned drawbacks.

5 SUMMARY OF THE INVENTION

An object of the present invention is to alleviate at least some of the above disadvantages and drawbacks of the prior art and to provide an improved alternative to prior art SiC BJTs.

Generally, it is an object of the present invention to provide a SiC BJT
10 with improved blocking capabilities, i.e. with an improved breakdown voltage. Further, it is an object of the present invention to provide methods of manufacturing such a SiC BJT.

These and other objects of the present invention are achieved by means of the SiC BJT and the method of manufacturing such a SiC BJT as
15 defined in the independent claims. Preferred embodiments are defined in the dependent claims.

According to a first aspect of the present invention, there is provided a silicon carbide (SiC) bipolar junction transistor (BJT). The SiC BJT comprises a collector region, a base region and an emitter region. Further, a surface
20 passivation layer is deposited between an emitter contact for contacting the emitter region and a base contact for contacting the base region. The deposited surface passivation layer induces the formation of a depletion region under the surface passivation layer in the extrinsic part of the base region. Further, the SiC BJT comprises a surface gate (or surface electrode)
25 arranged at the deposited surface passivation layer. The surface gate is configured to apply a negative electric potential to the deposited surface passivation layer with respect to the electric potential in the base region.

According to a second aspect of the present invention, there is provided a method of manufacturing a SiC BJT including a collector region, a
30 base region and an emitter region. The method comprises the steps of depositing a surface passivation layer on top of the BJT, the deposited surface passivation layer inducing the formation of a depletion region under the surface passivation layer in the extrinsic part of the base region, and

providing (or forming) a surface gate at the surface passivation layer. The surface passivation layer is arranged between an emitter contact for contacting the emitter region and a base contact for contacting the base region. The surface gate is arranged to apply a negative electric potential with respect to the electric potential in the base region.

The present invention is based on the understanding that a surface passivation layer deposited between the emitter contact and the base contact (which surface passivation layer may have been subsequently annealed after deposition) may induce the formation of a depletion region under the surface passivation layer in the extrinsic part of the base region and that the presence of such a depletion region reduces the effective thickness of the base region and thereby limits (or decreases) the breakdown voltage of the BJT due to punch-through. The formation of a depletion region, which extends below the surface of the base region, reduces the separation distance between the depletion regions at the base-collector and the base-emitter junctions and this causes a reduction of the collector-emitter punch-through breakdown voltage. In the present invention, a surface gate (or surface electrode) is provided at the deposited surface passivation layer and the surface gate is configured such that a negative electric potential with respect to the electric potential in the base region can be applied to the deposited surface passivation layer. With the present invention, the depletion region induced by the deposited surface passivation layer can be reduced in size (and preferably suppressed) and a BJT with an improved punch-through breakdown voltage is achieved. The present invention is therefore advantageous in that it provides a BJT with an improved breakdown voltage.

Further, the BJT of the present invention is also advantageous in that it provides the benefit of a deposited (and possibly subsequently annealed) surface passivation layer in terms of improved current gain (as compared to BJTs comprising surface passivation layers e.g. grown by conventional thermal oxidation). In the present invention, a surface passivation layer providing a high or even the highest common emitter current gain, for example a passivation layer obtained by deposition (such as PECVD) and subsequent annealing, may be selected for the SiC BJT although it induces

the formation of a depletion region in the extrinsic part of the base region. The inventors have recognized that such a deposited (and possibly annealed) surface passivation layer may result in the formation of a depletion region in the SiC region located under the surface passivation layer and that a surface gate may be provided for enabling appliance of a negative potential to the deposited surface passivation layer with respect to the potential of the SiC region in order to reduce, and possibly suppress, such a depletion region.

In other words, the invention is advantageous in that it provides the benefits of a deposited surface passivation layer, although it induces a depletion region in the extrinsic part of the base region, like e.g. in terms of common emitter current gain, while still providing improved blocking capabilities.

It will be appreciated that the base region (or base layer) of a SiC BJT is normally defined by two parts (or regions), the intrinsic part interfacing (or capped by) the emitter region and the extrinsic part not capped by the emitter region. The outer sidewalls of the emitter region define the boundary limits between these two parts. The presence of the deposited surface passivation layer on top of the BJT results in the formation of a depletion region in the extrinsic part of the base region.

The depletion region is present in the extrinsic part of the base region of the BJT after deposition of the surface passivation layer (under steady state conditions and before appliance of any negative electric potential to the surface gate of the BJT). In the case of a thermally grown oxide such as used in conventional BJTs, no (or at least negligible) depletion region is formed.

Advantageously, the surface gate may be configured to apply an electric potential having a value (magnitude) for reducing, and preferably eliminating, the depletion region formed under the surface passivation layer in the extrinsic part of the base region. In the present embodiment, the surface gate may be configured to apply an electric potential to the deposited surface passivation layer independently of any other applied potentials such as those applied to e.g. the emitter contact and the base contact of the BJT. The surface gate may be configured to apply any potential value to the deposited surface passivation layer, and in particular a negative potential suppressing

the depletion region formed below the base surface because of the presence of the deposited surface passivation layer.

The depletion region resulting from deposition of the surface passivation layer may probably be due to pinning of the surface potential and formation of a surface inversion channel of electrons. In this case, a depletion region with negatively charged acceptor ions reaching down below the top surface is formed. The formation of such a depletion region at the surface may depend on several factors such as the doping concentration of the base layer or base region, the thickness of the surface passivation layer, the charge in the surface passivation layer and/or the charge at the interface between SiC and the surface passivation layer. The occurrence of such a depletion region may therefore depend on the detailed process technology conditions and in particular on the method used to fabricate the surface passivation layer. The negative potential to be applied to the deposited surface passivation layer may then be selected accordingly. For example, a negative potential of about 2 Volts has shown to perform well for a SiC BJT comprising a 650 nm thick base region having a doping level of about $3 \times 10^{17} \text{ cm}^{-3}$ and a 100 nm thick surface passivation layer deposited by PECVD followed by a post-anneal at a temperature of about 1100-1300 °C for a duration of about 0.5 to 4 hours in N_2O . As will be further explained below, a negative potential of about 2 V may also be obtained by connecting the surface gate to the emitter contact.

According to an embodiment, the base dose, Q_B , of the base region may be determined as a function of a desired punch-through breakdown voltage, V_{CE-PT} , for the BJT according to the following expression:

$$V_{CE-PT} \approx \frac{q \times Q_B^2}{2 \times \epsilon_s \times N_C} \quad \text{Equation 1}$$

wherein N_C is the doping concentration for the collector region, q is the electron charge ($1.6 \times 10^{-19} \text{ C}$) and ϵ_s is the dielectric constant of SiC.

It will be appreciated that the base dose Q_B may be determined by the doping level N_B in the base region and the thickness W_B of the base region. The base dose may be calculated by multiplying the base thickness W_B with

the doping level (or doping concentration) N_B in case of a constant doping level through the thickness of the base region or may be calculated as the integral of the doping level (doping concentration) over the thickness of the base region.

- 5 Further, it will be appreciated that Equation 1 provides an approximation of the punch-through breakdown voltage (or the base dose) and that it is applicable for normal base and collector doping concentrations in a SiC BJT designed for a high voltage of 600 V or higher. This means that the doping concentration in the base region is in general more than ten times
- 10 higher than the doping concentration in the collector region and that the doping concentration in the collector region is designed for state-of-the-art performance in terms of forward voltage drop for a given voltage rating. For example, design conditions for a 1200 V SiC BJT can be a doping concentration of the base region in the range of $1.5 \times 10^{17} \text{ cm}^{-3}$ to $5 \times 10^{17} \text{ cm}^{-3}$,
- 15 a doping concentration for the collector region in the range of $5 \times 10^{15} \text{ cm}^{-3}$ to $1.5 \times 10^{16} \text{ cm}^{-3}$ and a collector thickness in the range of 15 μm to 8 μm (micrometers). It will be appreciated that an adequate collector thickness may be selected depending on the selected doping concentration of the collector region.
- 20 With the present embodiment, the parameters of the base region, and in particular the base dose, may be defined in accordance with a desired or targeted punch-through breakdown voltage. The present embodiment is advantageous in that, with the surface gate configured to apply a negative potential to the deposited surface passivation layer with respect to the electric
- 25 potential in the base region, the punch-through breakdown voltage increases to values which are close to the value calculated using equation 1. In contrast, prior art BJTs present large discrepancies from expected punch-through breakdown voltages. The base dose in prior art BJTs has so far been determined in an empirical manner. The present invention is therefore
- 30 advantageous in that it facilitates and improves the design of SiC BJTs, in accordance with equation 1. As will be further illustrated in the detailed description, the present invention provides a good correlation between the

desired (or targeted) breakdown voltage of a SiC BJT and its true (measured) breakdown voltage.

It will be appreciated that the breakdown voltage of the SiC BJT is determined by either the punch-through breakdown voltage or the avalanche breakdown voltage depending on which of them has the lowest value. The
5 desired punch-through breakdown voltage may therefore preferably be determined using equation 1 and such that it is larger than the avalanche breakdown voltage.

According to an embodiment, the base dose of the base region may be
10 comprised in the range of $1\text{--}1.9\times 10^{13}\text{ cm}^{-2}$, such as $1.1\text{--}1.5\times 10^{13}\text{ cm}^{-2}$, and is preferably equal to about $1.3\times 10^{13}\text{ cm}^{-2}$. With the parameters defined in the present embodiment, a punch-through breakdown voltage of about 1500 V can be achieved for a standard doping concentration of the collector region in the range of about $5\text{--}9\times 10^{15}\text{ cm}^{-3}$. Even more specifically, for a doping
15 concentration of $6\times 10^{15}\text{ cm}^{-3}$ in the collector region, the base dose may preferably be equal to $1.4\times 10^{13}\text{ cm}^{-2}$. The present embodiment is advantageous in that it provides a 1200 V rating of a power transistor made in SiC. In contrast, the base dose for conventional SiC BJTs of equivalent rating is $2\times 10^{13}\text{ cm}^{-2}$, i.e. of a higher value, which has the disadvantage of reducing
20 the current gain.

According to an embodiment, the surface passivation layer may be located on a sidewall of the base-emitter junction, or a sidewall of the emitter region, and extend on the surface of the BJT towards the base contact. The highest effect provided by the surface passivation layer with respect to
25 increase of the current gain is obtained by the portion covering the extrinsic part of the base region and the corner defined by the intersection of this portion with the elevated structure (or mesa) defining the emitter region. Thus, the surface passivation layer may be located at least in the portion covering the extrinsic part of the base region and the corner defined by the intersection
30 between the etched surface of the base region and the emitter mesa.

According to an embodiment, the surface passivation layer may be made of a dielectric material and the surface gate may be made of a conductive material. For example, the surface passivation layer may be made

of silicon dioxide deposited by e.g. PECVD and the surface gate may be made of highly doped poly-silicon or metal such as aluminum, titanium or titanium tungsten.

According to an embodiment, the surface gate may be electrically
5 connected to the emitter contact. As a result, the electric potential applied to the surface gate is the same as the electric potential applied to the emitter contact. In the present embodiment, the electric potential applied to the surface passivation layer is therefore determined by the electric potential applied to the emitter contact. The present embodiment is particularly
10 advantageous in that it facilitates the design and the manufacturing of the SiC BJT since a single electrode needs to be formed for both the emitter region and the surface gate.

Still referring to the embodiment wherein the surface gate may be electrically connected to the emitter contact, the value of the electric potential
15 applied to the surface passivation layer corresponds to the value of the electric potential applied to the emitter region. In case the applied potential is not sufficient to compensate for the depletion region formed under the surface passivation layer, i.e. to sufficiently reduce or suppress the depletion region, the thickness of the surface passivation layer may be adjusted such that the
20 value of the targeted punch-through breakdown voltage can be reached. A decrease of the thickness of the surface passivation layer (i.e. a thinner surface passivation layer) enhances the effect of the electric potential applied via the surface gate and decreases the depletion region more effectively, thereby increasing the punch-through breakdown voltage. However, a
25 decrease of the thickness of the surface passivation layer may also increase the risk for dielectric breakdown in the surface passivation layer, i.e. in the dielectric material itself. The thickness of the surface passivation layer may therefore be adjusted accordingly. For a silicon dioxide layer deposited by
30 about 100 nanometers. For such surface passivation layers, when the surface gate is connected to the emitter contact, the electric potential applied to the surface passivation layer may be in the range of about 2-3 Volts for typical bias conditions.

Referring to the method of manufacturing a SiC BJT in accordance with the second aspect of the present invention, the step of deposition may include plasma enhanced chemical vapor deposition (PECVD) of a silicon dioxide layer. Further, the PECVD or more generally the deposition of the surface passivation layer may be followed by post-deposition-anneal in e.g. N₂O or NO ambient. Post-annealing in NO ambient is advantageous in that it further increases the current gain of the transistor.

The annealing subsequent to the deposition of the surface passivation layer may be performed at a temperature of about 1000-1400°C, such as 1100-1300°C for a duration in the range of about 0.5 to 4 hours.

It will be appreciated that the embodiments described above in connection to the first aspect of the present invention are also combinable with any of the embodiments described in connection to the manufacturing method of the second aspect of the present invention, and vice versa.

Further objectives of, features of, and advantages with, the present invention will become apparent when studying the following detailed disclosure, the drawings and the appended claims. Those skilled in the art will realize that different features of the present invention can be combined to create embodiments other than those described in the following.

BRIEF DESCRIPTION OF THE DRAWINGS

The above, as well as additional objects, features and advantages of the present invention, will be better understood through the following illustrative and non-limiting detailed description of preferred embodiments of the present invention, with reference to the appended drawings, in which:

Fig. 1 shows a schematic cross-sectional view of a standard SiC BJT;

Fig. 2a illustrates the limitation in breakdown voltage due to a deposited surface passivation layer;

Fig. 2b shows a schematic cross-sectional view of a SiC BJT in accordance with an exemplifying embodiment of the present invention;

Figs. 3 and 4 show schematic cross-sectional views of SiC BJTs in accordance with other exemplifying embodiments of the present invention;

Fig. 5 shows the calculated base dose as a function of punch-through breakdown voltage for a base doping of $3 \times 10^{17} \text{ cm}^{-3}$ and a collector doping of $6 \times 10^{15} \text{ cm}^{-3}$; and

Fig. 6 shows the open-base blocking characteristics of four BJTs located close to each other on the same wafer, wherein two of the BJTs are manufactured without any surface gate and two of the BJTs include a surface gate in accordance with an embodiment of the present invention.

All the figures are schematic, not necessarily to scale, and generally only show parts which are necessary in order to elucidate the invention, wherein other parts may be omitted or merely suggested.

DETAILED DESCRIPTION

With reference to Figure 2a, the limitation in breakdown voltage in a SiC BJT due to a deposited surface passivation layer is illustrated.

Figure 2a shows a SiC BJT 100 comprising a substrate 110 on which a collector layer 120, a base layer 140 and an emitter layer 160 have been grown. The structure of the SiC BJT 100 shown in Figure 2a is equivalent to the structure of the SiC BJT described above with reference to Figure 1. The surface passivation layer 170 may be made of a dielectric material such as e.g. silicon dioxide deposited on top of the SiC BJT 100. The purpose of the surface passivation layer 170 is to stabilize the surface recombination of minority carriers. The surface passivation layer 170 may cover an edge of the elevated emitter region 160 (or emitter mesa) and part of the extrinsic part of the base region 140.

More specifically, Figure 2a shows the SiC BJT 100 in the blocking mode with a representation of the depletion regions formed in the device under such conditions, in particular the depletion region formed under the surface passivation layer 170 in the extrinsic part of the base region 140 (i.e. at the etched surface of the base region 140). The depletion region formed under the surface passivation layer 170 may be formed due to pinning of the surface potential and formation of a surface inversion channel of electrons. As a result, the effective thickness of the base region is reduced, thereby reducing the punch-through electrical breakdown of the BJT. The separation

between the space charge region formed at the collector-base boundary and the space charge region formed at the base-emitter boundary is denoted W in the figures. In Figure 2a, the formation of the depletion region under the deposited surface passivation layer 170 in the extrinsic part of the base region 140 (i.e. which extends below the surface of the base region 140) reduces the separation W .

With reference to Figure 2b, there is shown a schematic view of a SiC BJT in accordance with an exemplifying embodiment of the present invention.

Figure 2b shows a SiC BJT 200 comprising a substrate 210 on which a collector layer 220, a base layer 240 and an emitter layer 260 have been grown. The SiC BJT 200 shown in Figure 2b is equivalent to the SiC BJT 100 described with reference to Figure 2a except that it further comprises a surface gate 280 (or surface electrode) arranged at the deposited surface passivation layer 270. The surface gate 280 may be a metal electrode which is located on top of the surface passivation layer 270 which is present on the etched side-wall of the base-emitter junction and along the exposed base and emitter surfaces. The surface gate 280 is configured to apply a negative potential to the deposited surface passivation layer 270 with respect to the electric potential in the base region 240. As illustrated in Figure 2b, appliance of a negative potential to the deposited surface passivation layer 270 with respect to the electric potential of the base region 240 reduces and, possibly totally suppresses, the depletion region formed in the extrinsic part of the base region 240 as a result of the deposition of the surface passivation layer 270. Consequently, the separation or distance W between the space charge region formed at the collector-base boundary and the space charge region formed at the base-emitter boundary is increased as compared to that obtained without appliance of a negative potential to the deposited surface passivation layer (i.e. the effective thickness of the base region is increased as compared to that shown in Figure 2a). The transistor 200 described with reference to Figure 2b is advantageous in that the punch-through breakdown voltage is increased and, thus, that it provides improved blocking capabilities.

In addition, the effective thickness of the base region corresponds to the separation or distance W between the space charge region formed at the

collector-base boundary and the space charge region formed at the base-emitter boundary, without being affected by any space charge region (or depletion region) formed or induced in the extrinsic part of the base region. Accordingly, the resulting punch-through breakdown voltage of the device is more easily predictable, thereby facilitating the design of the device.

The SiC BJT 200 comprises also contact areas 261 and 241 for electrical connection to the emitter region 260 and the base region 240, respectively, and another contact area 221 formed at the backside of the substrate 210 for electrical connection the collector region 220.

The SiC BJT 200 may be a NPN vertical BJT comprising a n-type collector region 220 disposed on a highly-doped n-type substrate 210, a p-type base region 240 and an n-type emitter region 260. The vertical direction corresponds to the growth direction of the layers forming the collector region 220, the base region 240 and the emitter region 260 on top of the substrate 210.

With reference to Figures 3 and 4, there are shown schematic views of SiC BJTs in accordance with other exemplifying embodiments of the present invention.

Figures 3 and 4 show SiC BJTs 300 and 400, respectively, whose structures are equivalent to the structure of the SiC BJT 200 described with reference to Figure 2b but with another design of the surface gate.

As compared to the SiC BJT 200 shown in Figure 2b, Figure 3 shows an embodiment wherein the surface gate 380 of the SiC BJT 300 covers at least part of the surface located above the extrinsic part of the base region 340 but also extends towards the emitter contact 361 by covering an edge of the mesa or elevated structure of the emitter region 360. In the embodiments described with reference to Figures 2b and 3, the surface gates or electrodes 280 and 380, respectively, are electrically isolated from the emitter and base contacts (denoted 261 and 264, respectively, in Figure 2b and denoted 361 and 364, respectively, in Figure 3) and enable application of an arbitrary bias between the surface gate and the emitter and base contacts. In Figure 3, the surface passivation layer is denoted 370, the collector region is denoted 320, the substrate is denoted 310 and the collector contact is denoted 321.

In Figure 4, an embodiment wherein the surface gate 480 of the SiC BJT 400 may be electrically connected to the emitter contact 461 of the emitter region 460 is shown. In the present embodiment, the emitter contact 461 extends towards the base contact 441 of the base region 440 (without electrically connecting the base contact 441) and covers at least part of the deposited surface passivation layer 470. In this configuration, the emitter contact 461 is herein referred to as an emitter extended gate. As the emitter extended gate 461 is connected to the emitter region 460, it supplies a negative electric potential, with respect to that of the base region 440, for operating the transistor 400 in blocking mode and thereby applies a negative electric potential on top of the deposited surface passivation layer 470 with respect to that of the base region 440. As a result, the depletion region formed under the surface passivation layer in the extrinsic part of the base region is reduced and a BJT with improved blocking capabilities is provided.

In Figure 4, the collector region is denoted 420, the substrate is denoted 410 and the collector contact is denoted 421.

Figure 5 shows the calculated base dose as a function of punch-through breakdown voltage (V_{CE}) for a base doping of $3 \times 10^{17} \text{ cm}^{-3}$ and a collector doping of $6 \times 10^{15} \text{ cm}^{-3}$, in accordance with Equation 1. The graph in Figure 5 indicates that a base dose of about $1.3 \times 10^{13} \text{ cm}^{-2}$ provides a punch-through breakdown voltage of 1500 V, which is suitable for a 1200 V rating of a power transistor, i.e. for a 1200 V rated SiC BJT.

In prior art devices, the punch-through breakdown voltage is difficult to predict, in particular because of the positive surface potential resulting from the presence of a deposited surface passivation layer and creating a depletion region extending below the base surface (and possibly also creating an electron inversion layer at the surface of the BJT). In addition, there may be a certain amount of over-etch at the base-emitter junction of an epitaxial BJT and in particular there may be a higher over-etch, so-called trenching, locally at the edge of the emitter mesa. Punch-through breakdown can occur as the depletion region from the base-collector junction reaches the etched surface. Further, redistribution of material during ion implantation annealing (for the implanted ions under the base contact, see region 142 in Figure 1)

may also increase the risk of punch-through (i.e. reducing the punch-through breakdown voltage) by producing nitrogen doping (i.e. n-type doping) in the etched trench. The punch-through breakdown voltage obtained in prior art devices is dependent on the above mentioned issues and the reliability of prior art methods for designing and fabricating SiC BJTs in terms of achievable punch-through breakdown voltage is therefore limited. In prior art BJTs, the parameters of the base region are determined in an empirical manner and the base dose for a 1200 V rated BJT is generally $2 \times 10^{13} \text{ cm}^{-2}$, i.e. higher than for the SiC BJT of the present invention. Thus, the present invention is also advantageous in that it enables design of SiC BJTs with a low base dose Q_B , which provides a higher current gain.

With the surface gate configured to apply a negative potential to the deposited surface passivation layer with respect to the electric potential of the base region, the punch-through breakdown voltage reaches, or at least is close to, the values as determined by equation 1. The present invention is therefore advantageous in that it provides a more reliable method for designing and fabricating SiC BJTs in terms of achievable punch-through breakdown voltage. A likely explanation for the improved breakdown voltage using a surface gate according to the present invention is that the negative potential at the surface gate repels electrons and suppresses the formation of an electron inversion layer and the formation of a depletion region below the base top surface. It will be appreciated that after deposition and anneal of the surface passivation layer, a depletion region may be formed and, in some cases, wherein the surface potential induced by the surface passivation layer is even more enhanced, an electron inversion layer may also be formed. In the latter cases, the surface gate is configured to apply a negative potential sufficient for suppressing both the depletion region and the electron inversion layer.

Figure 6 shows measured open-base blocking characteristics for four BJTs located close to each other on the same wafer. Two of the BJTs, for which the characteristics are denoted *B*, comprise a surface gate connected to the emitter contact (i.e. an emitter extended surface gate). These two BJTs have an open-base breakdown voltage of about 1500 V. The two other BJTs,

for which the characteristics are denoted A, have no surface gate and have open-base breakdown voltages of about 950 V.

According to secondary ion mass spectrometry (SIMS) measurements on test structures on the same wafer as the BJTs measured in Figure 6, the
5 base dose is about $1.4 \times 10^{13} \text{ cm}^{-2}$. According to equation 1 (or as shown in Figure 5), such a base dose would lead to a punch-through breakdown voltage of 1760 V, which is relatively close to the value of 1500 V measured for the BJTs comprising an emitter extended gate in accordance with the present invention. The results in Figure 6 together with the SIMS
10 measurement of the base dose clearly illustrates the efficiency of the present invention in improving the collector-emitter punch-through breakdown voltage for SiC BJTs.

Even though the invention has been described with reference to specific exemplifying embodiments thereof, many different alterations,
15 modifications and the like will become apparent for those skilled in the art. The described embodiments are therefore not intended to limit the scope of the invention, as defined by the appended claims.

CLAIMS

1. A silicon carbide, SiC, bipolar junction transistor, BJT, (200) comprising a collector region (220), a base region (240) and an emitter region (260), wherein a surface passivation layer (270) is deposited between an emitter
 5 contact (261) for contacting said emitter region and a base contact (241) for contacting said base region, said surface passivation layer inducing formation of a depletion region under said surface passivation layer in an extrinsic part of said base region, said SiC BJT further comprising a surface gate (280) arranged at the deposited surface passivation layer and configured
 10 to apply a negative electric potential to the deposited surface passivation layer with respect to an electric potential in said base region.

2. The SiC BJT as defined in claim 1, wherein said surface gate is configured to apply an electric potential having a value for reducing, and
 15 preferably eliminating the depletion region formed under said surface passivation layer in the extrinsic part of said base region.

3. The SiC BJT as defined in claim 1 or 2, wherein a base dose, Q_B , of said base region is determined as a function of a desired punch-through
 20 breakdown voltage, V_{CE-PT} , for said BJT according to following expression:

$$V_{CE-PT} \approx \frac{q \times Q_B^2}{2 \times \epsilon_S \times N_C}$$

wherein N_C is a doping concentration for said collector region, q is an
 25 electron charge and ϵ_S is dielectric constant of SiC.

4. The SiC BJT as defined in any one of the preceding claims, wherein a base dose of said base region is comprised in the range of $1-1.9 \times 10^{13} \text{ cm}^{-2}$, such as $1.1-1.5 \times 10^{13} \text{ cm}^{-2}$ and is preferably equal to about $1.3 \times 10^{13} \text{ cm}^{-2}$.
 30

5. The SiC BJT as defined in any one of the preceding claims, wherein said surface passivation layer is located on a sidewall of a base-emitter

junction, or a sidewall of said emitter region, and extends on the surface of said BJT towards said base contact.

6. The SiC BJT as defined in any one of the preceding claims, wherein
5 said surface passivation layer comprises a dielectric material and the surface gate comprises a conductive material.

7. The SiC BJT as defined in any one of the preceding claims, wherein
the deposited surface passivation layer is a layer of silicon dioxide deposited
10 by plasma enhanced chemical vapor deposition.

8. The SiC BJT as defined in any one of the preceding claims, wherein
said surface gate is electrically connected to said emitter contact.

15 9. Method of manufacturing a silicon carbide, SiC, bipolar junction transistor, BJT, comprising a collector region, a base region and an emitter region, said method comprising the steps of:

depositing a surface passivation layer on top of said BJT, said
passivation layer being arranged between an emitter contact for contacting
20 said emitter region and a base contact for contacting said base region, said surface passivation layer inducing formation of a depletion region under said surface passivation layer in an extrinsic part of said base region; and

forming a surface gate at said surface passivation layer, said surface
gate being arranged to apply a negative electric potential with respect to an
25 electric potential in said base region.

10. The method of claim 9, wherein said surface gate is arranged to
provide an electric potential reducing, and preferably eliminating, the
depletion region formed under said surface passivation layer.

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11. The method of claim 9 or 10, wherein the base dose, Q_B , of said base region is determined as a function of a desired breakdown voltage, V_{CE-PT} , for said BJT according to following:

$$V_{CE-PT} \approx \frac{q \times Q_B^2}{2 \times \epsilon_s \times N_C}$$

wherein N_C is a doping concentration for said collector region, q is an
5 electron charge and ϵ_s is dielectric constant of SiC.

12. The method of any one of claims 9-11, wherein the base dose of said
base region is comprised in the range of $1-1.9 \times 10^{13} \text{ cm}^{-2}$, and is preferably
equal to about $1.3 \times 10^{13} \text{ cm}^{-2}$.

10

13. The method of any one of claims 9-12, wherein the step of deposition
comprises plasma enhanced chemical vapor deposition, PECVD, of a silicon
dioxide layer.

15 14. The method of any one of claims 9-13, further comprising annealing
the deposited surface passivation layer.

15. The method of claim 14, wherein the annealing is performed in N_2O or
NO ambient.

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1/3

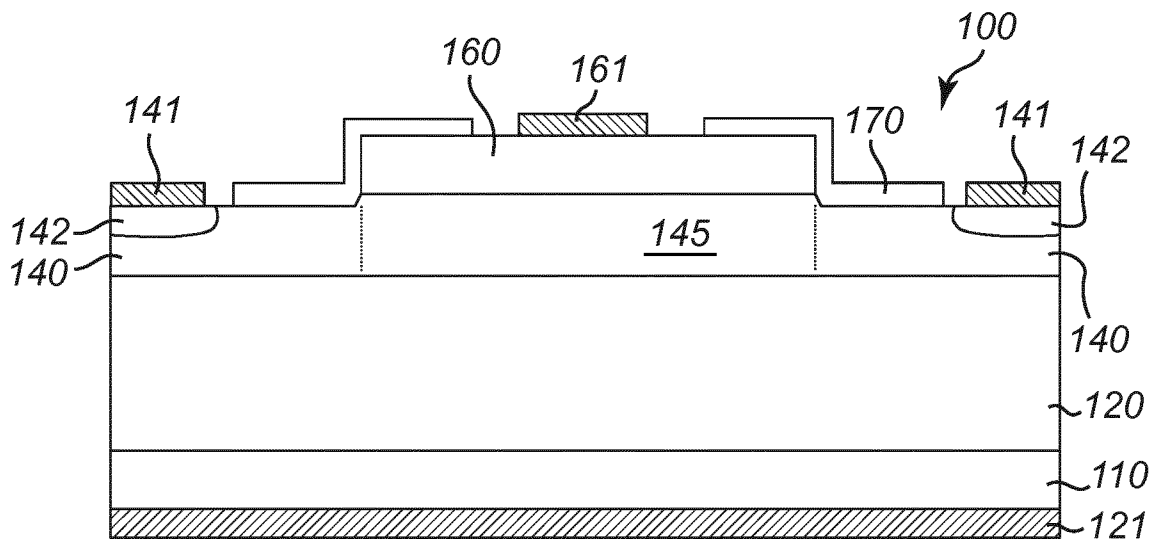


Fig. 1

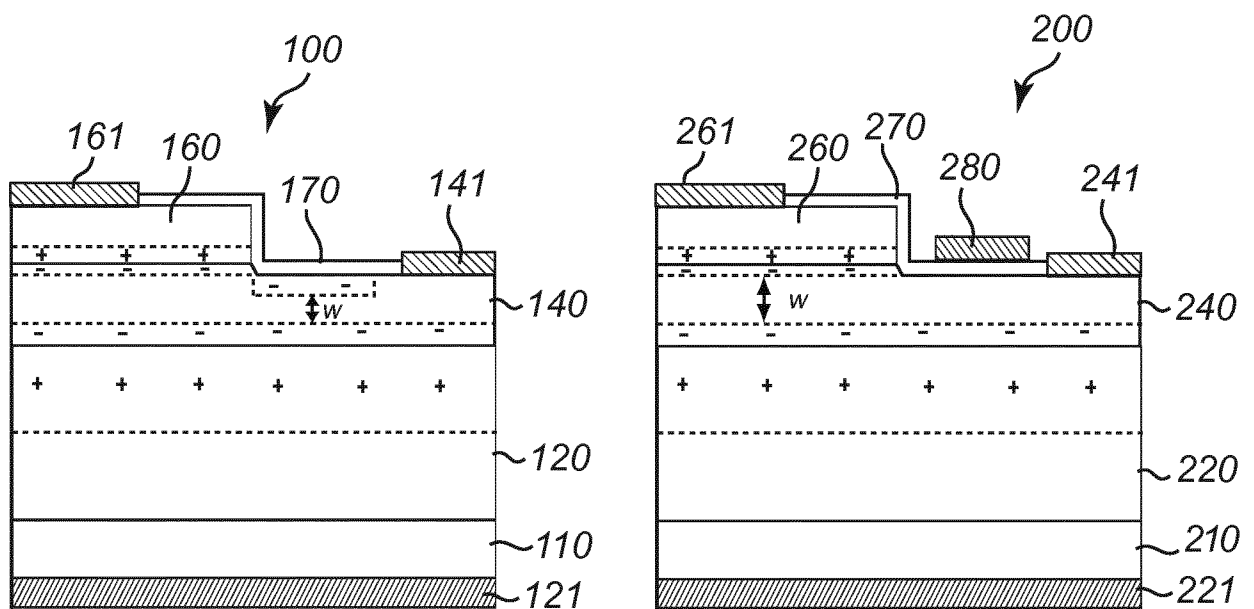


Fig. 2a

Fig. 2b

2/3

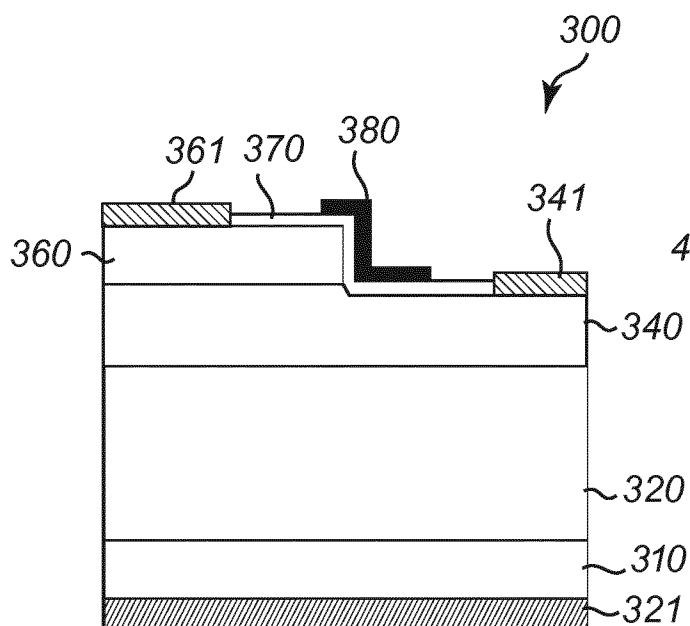


Fig. 3

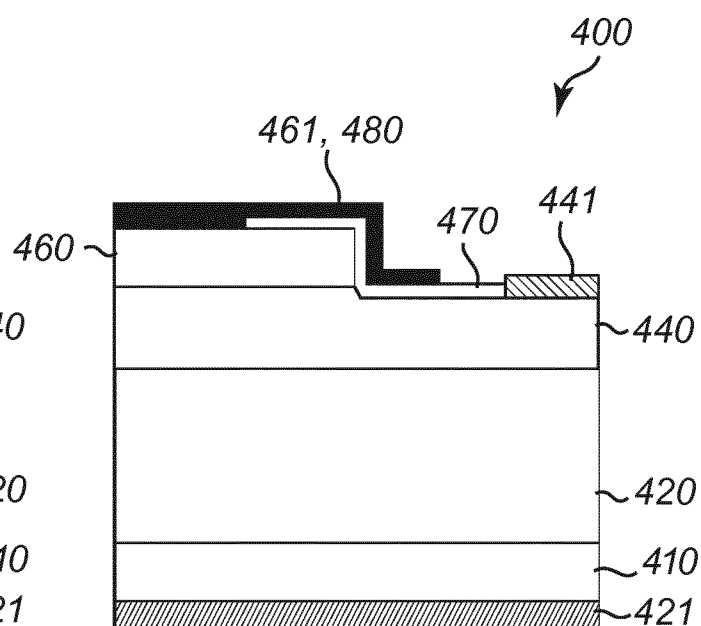


Fig. 4

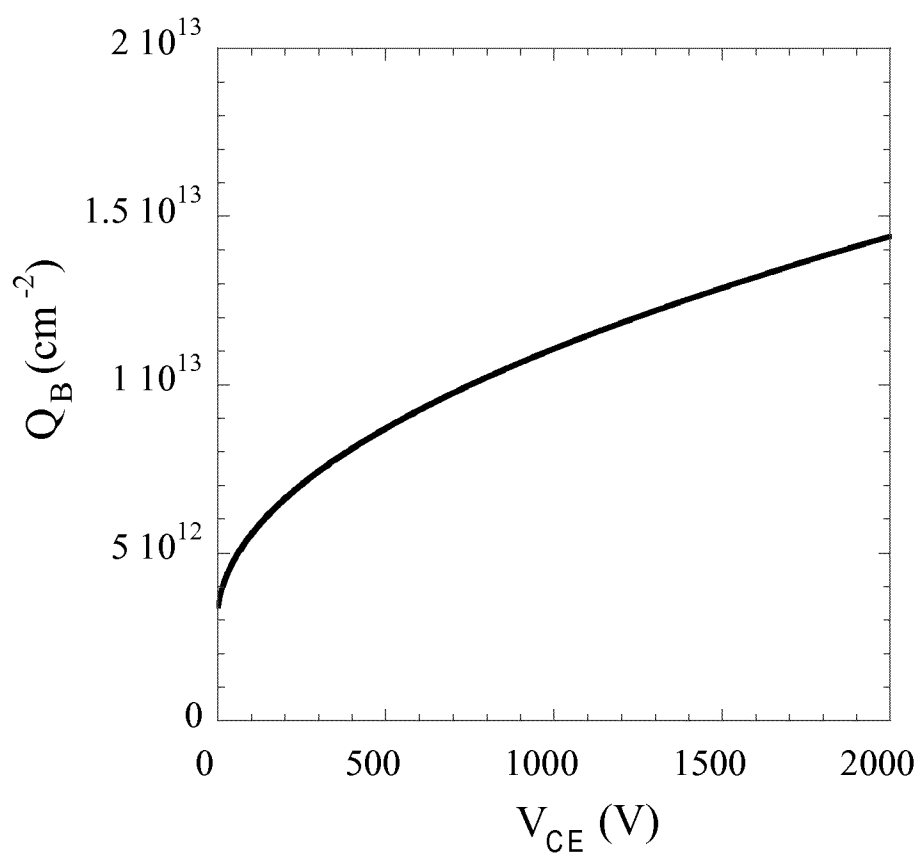
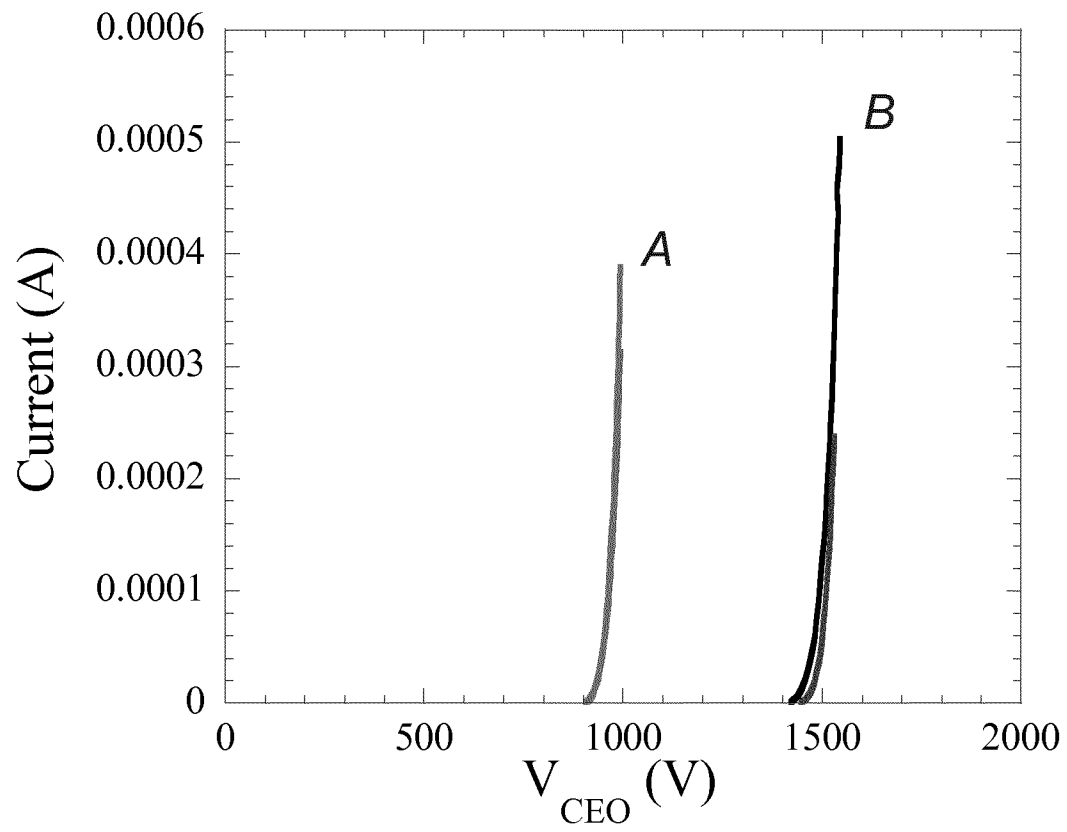


Fig. 5

3/3

*Fig. 6*

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2012/057565

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L29/73 H01L29/732 H01L29/40 H01L29/16
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2010/110725 A1 (TRANSIC AB [SE]; DOMEIJ MARTIN [SE]) 30 September 2010 (2010-09-30)	1-6, 8-12, 14
Y	the whole document	7, 13, 15
Y	----- "Surface-passivation effects on the performance of 4H-SiC BJTs", IEEE TRANSACTIONS ON ELECTRONIC DEVICES, vol. 58, 1 January 2011 (2011-01-01), pages 259-265, XP002679486, cited in the application the whole document -----	7, 13, 15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

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Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Baillet, Bernard

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2012/057565

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2010110725 A1	30-09-2010	CN 102362353 A	22-02-2012
		KR 20110134486 A	14-12-2011
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		WO 2010110725 A1	30-09-2010
