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(54) **STRUCTURE COMPRISING A RUTHENIUM METAL MATERIAL**

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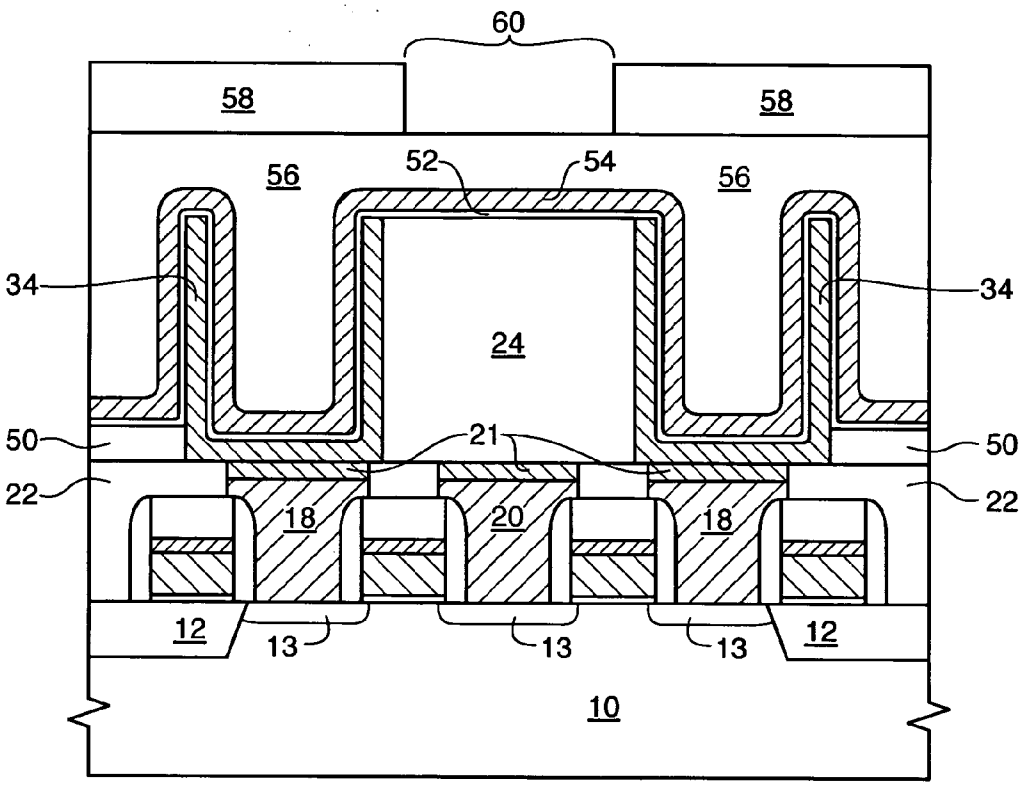
USPC **257/296**; 257/412

(57) **ABSTRACT**

A method for forming a ruthenium metal layer comprises combining a ruthenium precursor with a measured amount of oxygen to form a ruthenium oxide layer. The ruthenium oxide is annealed in the presence of a hydrogen-rich gas to react the oxygen in the ruthenium oxide with hydrogen, which results in a ruthenium metal layer. By varying the oxygen flow rate during the formation of ruthenium oxide, a ruthenium metal layer having various degrees of smooth and rough textures can be formed.



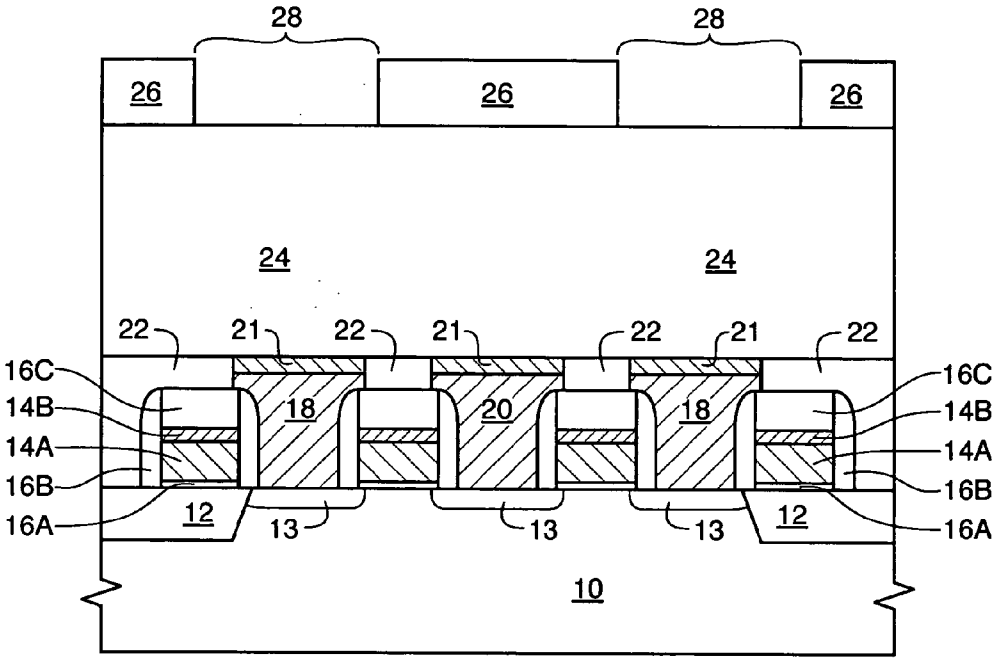

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FIG. 1

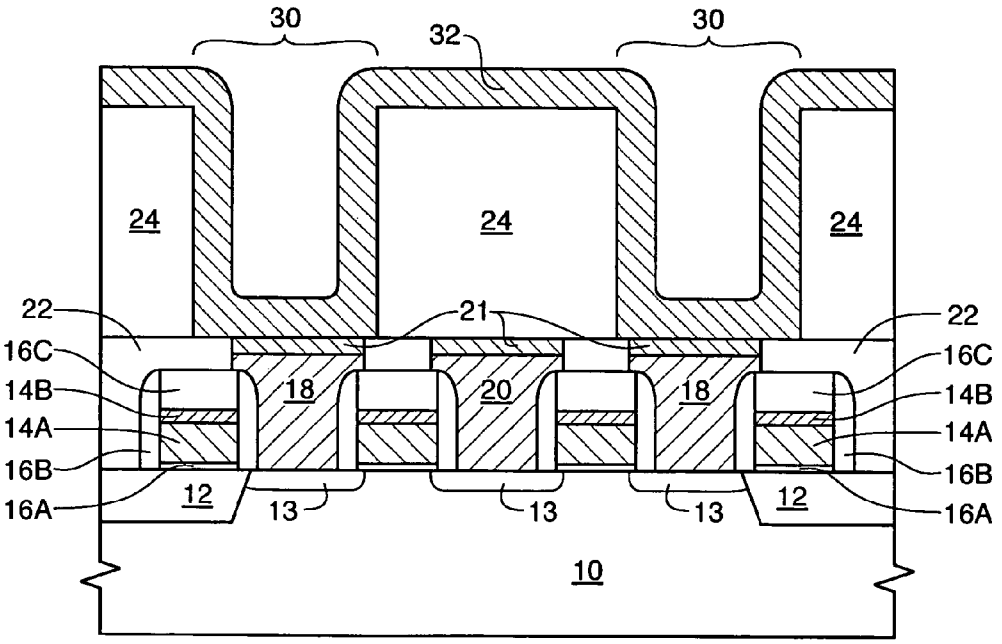
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FIG. 2

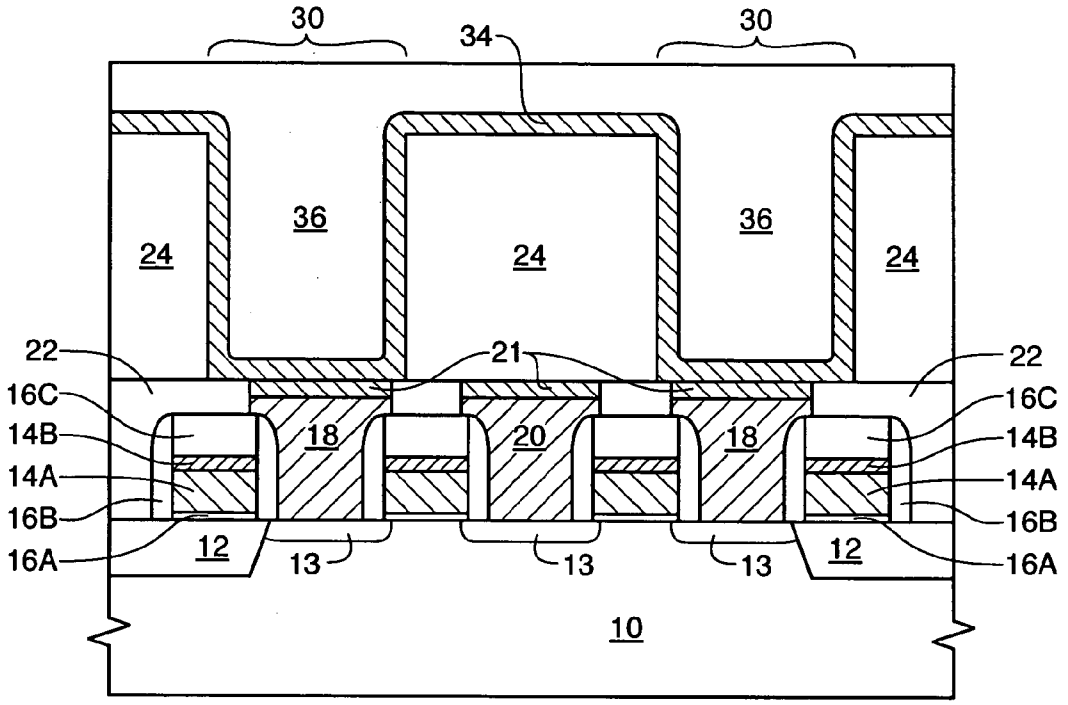
30
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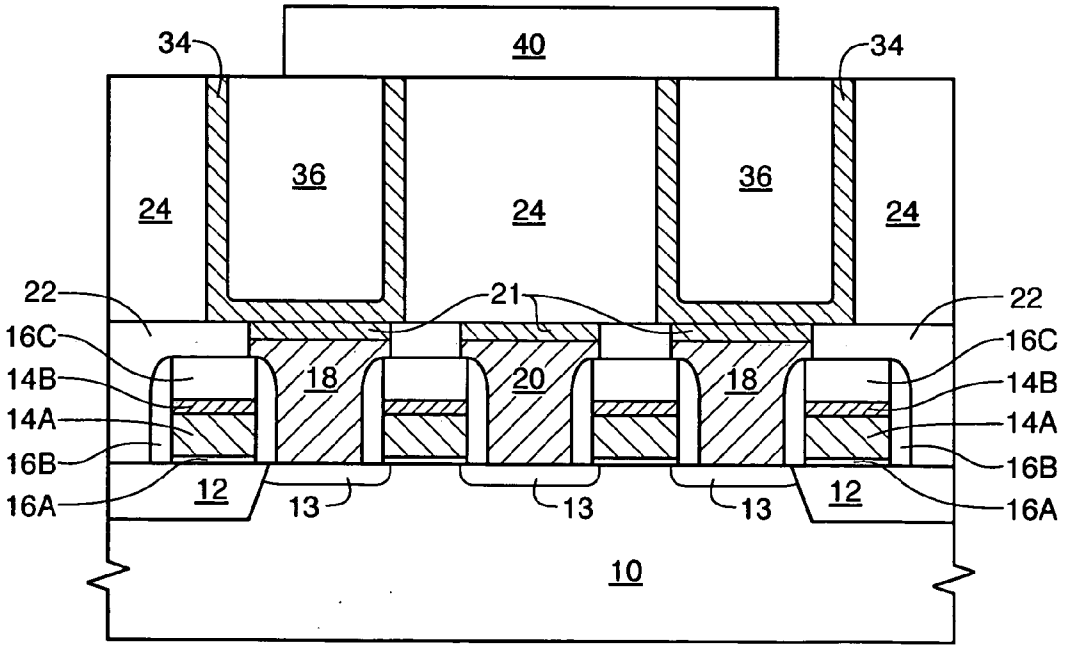
FIG. 3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14A
14A
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16B
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FIG. 4

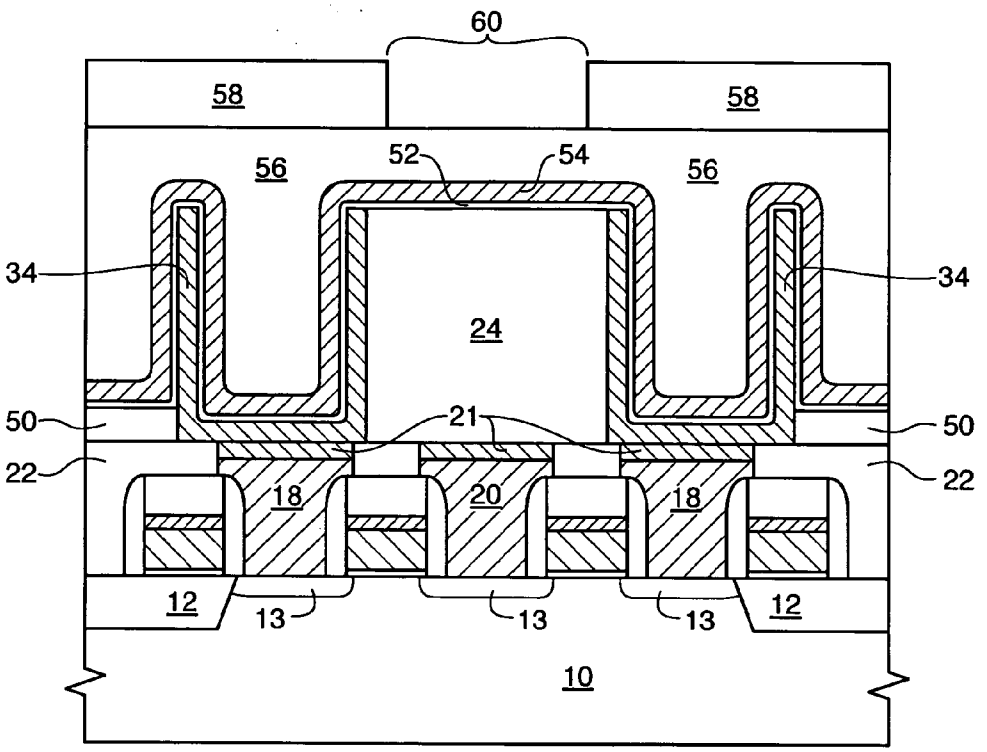

FIG. 5

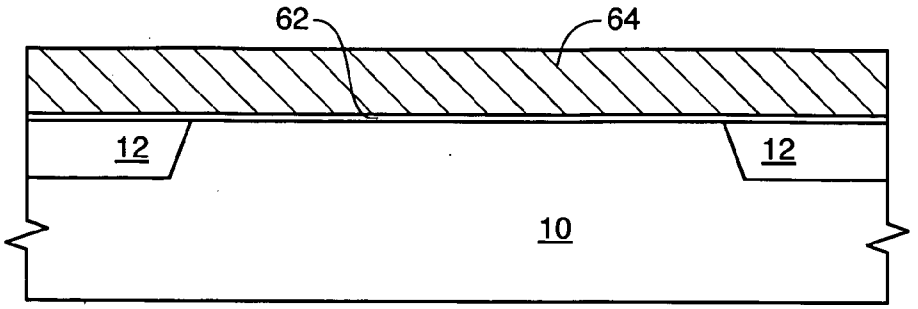

FIG. 6

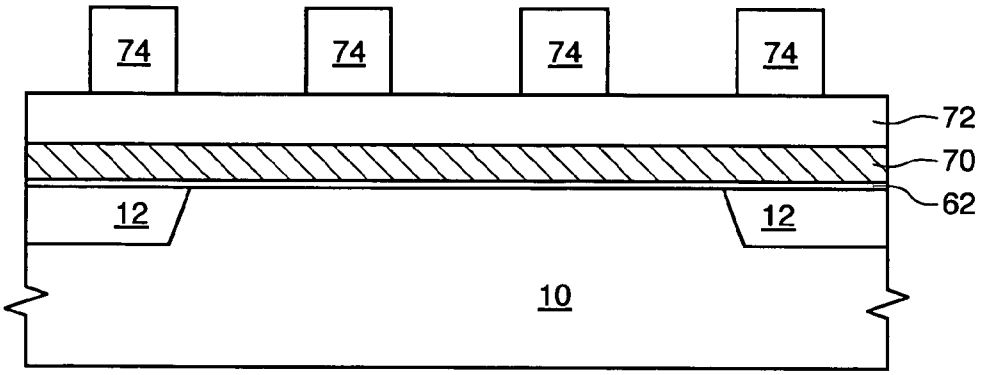

FIG. 7

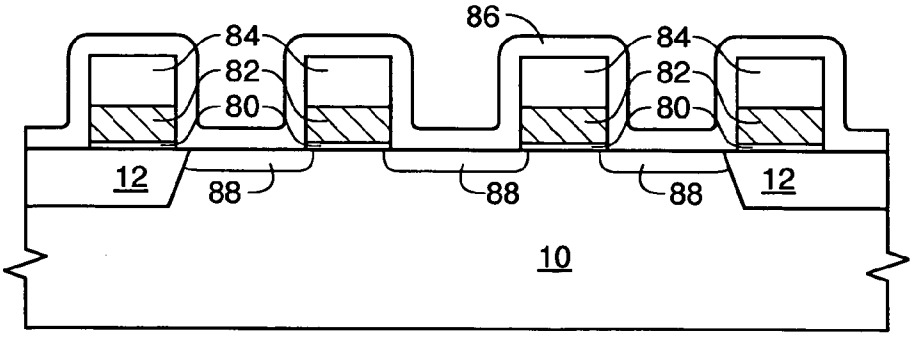

FIG. 8

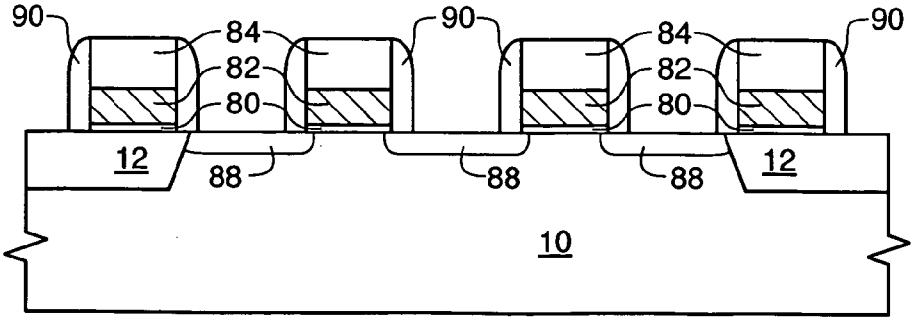

FIG. 9

STRUCTURE COMPRISING A RUTHENIUM METAL MATERIAL

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of U.S. patent application Ser. No. 11/389,707, filed Mar. 27, 2006, pending, which application is a continuation of U.S. patent application Ser. No. 10/658,868, filed Sep. 8, 2003, now U.S. Pat. No. 7,018,675, issued Mar. 28, 2006, which is a divisional of U.S. patent application Ser. No. 09/710,626, filed Nov. 10, 2000, now U.S. Pat. No. 6,617,248, issued Sep. 9, 2003, the disclosure of each of which is hereby incorporated herein in its entirety by this reference.

TECHNICAL FIELD

[0002] This invention relates to the field of semiconductor assembly and, more particularly, to a method for forming layer of ruthenium metal.

BACKGROUND

[0003] During the manufacture of semiconductor devices such as dynamic random access memories (DRAMs), microprocessors, and logic devices, several conductive structures are commonly formed. For example, transistor gates and capacitor bottom (storage) and top plates, typically manufactured from doped polysilicon, and interconnects and runners, typically formed from aluminum and/or copper, are formed on various types of devices.

[0004] A conductive material that has been used for various semiconductor device structures such as capacitor plates in ferroelectric devices is ruthenium oxide (RuO_2). Ruthenium oxide exhibits good step coverage and a uniform thickness across various topographies. However, RuO_2 is not stable and is a strong oxidizer. It will, over time, oxidize various metal layers that are in close proximity. For example, if RuO_2 is used as a capacitor bottom plate, it will oxidize a titanium nitride or tungsten nitride top plate through a tantalum pentoxide (Ta_2O_5) capacitor dielectric. Further, a barrier layer must be formed to protect a polysilicon contact pad from the RuO_2, as the RuO_2 will oxidize the polysilicon and result in a bottom plate being electrically isolated from the contact pad by a silicon dioxide layer.

[0005] Attempts have also been made to use ruthenium metal as capacitor plates or as various other structures, as ruthenium metal is stable and is easily planarized during chemical mechanical polishing (CMP). However, methods for forming a ruthenium metal layer, for example, using chemical vapor deposition (CVD), result in a layer that has poor step coverage and has a rough surface. Ruthenium metal is formed excessively thin over features with excessive slope changes, and it does not adequately form in narrow areas such as deep digit line contact openings in a manner adequate to maintain its conductive integrity.

[0006] A method for forming a uniform ruthenium metal layer across severe topographies and that forms within deep, narrow openings would be desirable.

SUMMARY

[0007] The present invention provides a new method that reduces problems associated with the manufacture of semiconductor devices, particularly problems in forming a ruthenium metal layer. In accordance with one embodiment of the invention a ruthenium precursor and oxygen are introduced into a chamber to form a ruthenium oxide layer. Next, the ruthenium oxide layer is heated in the presence of a hydrogen-rich gas to convert the ruthenium oxide layer to a ruthenium metal layer.

[0008] As will be discussed, the uniformity of the completed ruthenium metal layer is significantly dependent on the flow rate of oxygen introduced with the ruthenium precursor. As the flow rate of oxygen is increased from a minimum to form the ruthenium oxide layer, the uniformity of the completed ruthenium metal layer increases. As the oxygen flow rate increases past a critical point, however, the uniformity of the completed ruthenium metal layer begins to deteriorate.

[0009] While it is believed that a uniform ruthenium metal layer formed in accordance with various described embodiments is most desirable, a less than uniform ruthenium metal layer formed in accordance with the descriptions herein may also have utility.

[0010] Objects and advantages will become apparent to those skilled in the art from the following detailed description read in conjunction with the appended claims and the drawings attached hereto.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIG. **1** is a cross section depicting a wafer substrate assembly in one exemplary use of the method described herein;

[0012] FIG. **2** depicts the FIG. **1** structure subsequent to a dielectric etch and the formation of a ruthenium oxide layer;

[0013] FIG. **3** depicts the FIG. **2** structure subsequent to annealing the ruthenium oxide layer to form a ruthenium metal layer, and after forming a protective layer over the ruthenium metal layer;

[0014] FIG. **4** depicts the FIG. **3** structure subsequent to performing an etch of the ruthenium metal layer and after forming a mask layer over the wafer substrate assembly surface;

[0015] FIG. **5** depicts the FIG. **4** structure subsequent to forming a cell dielectric layer, a capacitor top plate layer, a planar dielectric layer, and a mask layer to define an opening to a digit line contact pad;

[0016] FIG. **6** is a cross section depicting another exemplary embodiment of the invention to form a transistor control gate;

[0017] FIG. **7** depicts the FIG. **6** structure after converting ruthenium oxide to ruthenium metal, and after the formation of a gate capping layer and a patterned photoresist layer;

[0018] FIG. **8** depicts the FIG. **7** structure after etching the capping layer, the ruthenium metal layer, and the gate oxide layer, and after forming a spacer layer; and

[0019] FIG. **9** depicts the FIG. **8** structure after a spacer etch.

[0020] It should be emphasized that the drawings herein may not be to exact scale and are schematic representations. The drawings are not intended to portray the specific parameters, materials, particular uses, or the structural details of the invention, which can be determined by one of skill in the art by examination of the information herein.

DETAILED DESCRIPTION

[0021] Various embodiments of the inventive method comprise forming a ruthenium oxide layer, then converting the ruthenium oxide layer to ruthenium metal. To form the ruthe-

nium oxide layer, a ruthenium precursor and an oxygen source are introduced into a chamber such as an Applied Materials 5000 chemical vapor deposition (CVD) tool. It should be noted that the values specified herein are calibrated for an Applied Materials 5000, but they may be modified for other chambers if necessary.

[0022] The oxygen source, such as O_2 gas, is preferably pumped into the chamber at a flow rate of between about 10 standard cm^3 (sccm) and about 1000 sccm, more preferably at a flow rate of between about 150 sccm and about 250 sccm, and most preferably at about 200 sccm.

[0023] The ruthenium precursor may include a number of materials, including tricarbonyl-1,3-cyclohexadiene ruthenium (referred to herein as "CHDR"), bisethylcyclopentadienylruthenium ($Ru(C_2H_5C_5H_4)_2$, referred to herein as "Ru $(EtCp)_2$"), and ruthenium octanedionate (referred to herein as "$Ru(OD)_3$"). The ruthenium precursor is preferably pumped into the chamber at a flow rate of between about 10 sccm to about 2000 sccm, more preferably at a flow rate of between about 100 and about 1000 sccm, and most preferably at a flow rate of about 500 sccm.

[0024] The chamber further comprises an environment having a pressure preferably between about 0.1 Torr to about 90 Torr, and more preferably at a pressure of between about 1.0 Torr and about 9.0 Torr. A chamber temperature of between about 100° C. and about 600° C., more preferably between about 150° C. and about 450° C., and most preferably about 210° C. would be sufficient. At the preferred parameters the ruthenium oxide forms at a rate of about 200 Å/minute.

[0025] The oxygen source gas flow rate was found during testing to significantly affect the quality of the completed ruthenium metal layer. When the flow rate of O_2 was around 200 sccm during the above-described formation of RuO_2, for example between about 150 sccm and 250 sccm, the completed ruthenium metal layer was relatively uniform and had minimal pinholing. At an O_2 flow rate above or below about 200 sccm, especially at flow rates less than about 200 sccm, the completed ruthenium metal layer was subject to an increasing number of pinholes and an increasingly rough surface the further the flow rate varied from about 200 sccm. While a smooth ruthenium metal layer will be desirable in most uses, a rough layer may also be useful, for example to form a layer having an increased surface area.

[0026] Using the gas and precursor flow rates, temperature, and pressure indicated, the ruthenium oxide forms at a rate of about 200 Å/minute. The material that forms is believed to be a mixture of Ru and RuO_2, however it is expected that RuO_x where "x" is other than 2 will also form in various ratios. RuO_2 content in the film increases as the O_2 flow rate increases.

[0027] Next, the ruthenium oxide layer is heated or annealed in the presence of a hydrogen-rich gas to form the ruthenium metal layer. The hydrogen-rich gas reacts with the oxygen from the ruthenium oxide layer, leaving a layer of ruthenium metal. Sufficient hydrogen-rich gasses include ammonia (NH_3) and hydrogen gas (H_2), preferably at a flow rate of between about 100 sccm and about 10,000 sccm, more preferably between about 500 sccm and about 8,000 sccm, and most preferably between about 3,000 sccm and about 6,000 sccm. The chamber further comprises an environment having a pressure preferably between about 1 Torr to about 760 Torr, and more preferably at a pressure of between about 100 Torr and about 660 Torr. A chamber temperature of between about 400° C. and about 800° C., more preferably between about 450° C. and about 750° C., and most preferably between about 475° C. and about 650° C. would be sufficient. For generally any thickness of RuO_2, an annealing duration of between about 10 seconds and about 5 minutes will be sufficient, and a duration of between about 30 seconds and about 3 minutes, for example 60 seconds, will be sufficient for most thicknesses.

[0028] Upon completion of the anneal step, the resulting ruthenium metal layer will have a thickness of from about 50% to about 80% of the thickness of the ruthenium oxide layer before annealing.

[0029] FIGS. **1-5** depict an exemplary use of a ruthenium metal layer as a capacitor bottom plate formed in one inventive embodiment of the invention. FIG. **1** depicts a semiconductor wafer substrate assembly comprising a semiconductor wafer **10**, field oxide **12**, doped wafer areas **13**, transistor control gates typically comprising a polysilicon gate **14**A and silicide **14**B, and surrounding dielectric typically comprising gate oxide **16**A, nitride spacers **16**B, and capping layer **16**C, for example tetraethyl orthosilicate (TEOS). The device further comprises polysilicon contact pads including pads **18**, to which the ruthenium metal container capacitor bottom plate will be electrically coupled, and pads **20** (only one depicted), which will form a portion of a digit line contact to the wafer **10**. FIGS. **1-5** further depict a conductive barrier layer **21** such as tungsten nitride (WN_x), TiN, TaN, TaSiN, TiSiN, and tungsten, or a stack of more than one of these layers. A dielectric layer **22**, for example borophosphosilicate glass (BPSG), separates the pads.

[0030] The polysilicon layer that forms pads **18**, **20** is recessed within layer **22** before formation of barrier layer **21**, layer **21** is formed, then layer **21** can be removed from over oxide layer **22** using chemical mechanical polishing (CMP). A barrier layer between about 50 Å and about 1,000 Å thick would be sufficient. Also depicted is a second layer of dielectric **24**, which can be one or more layers of TEOS and/or BPSG. With current technology, layer **24** can be about 14,000 Å thick. A layer of photoresist **26** defines openings **28**, which overlie pads **18** to which the container capacitors will be electrically coupled. The structure of FIG. **1** is exposed to a vertical anisotropic etch, which removes the dielectric layer **24** selective to the polysilicon contact pads **18**.

[0031] FIG. **2** depicts openings **30** in dielectric **24**, which result from the etch of the FIG. **1** structure. The etch exposes barrier layer **21**, which is electrically coupled with pads **18**, **20**, and the pads **18**, **20** contact the doped regions **13**. Pads **18** decrease the amount of oxide that the etch of the FIG. **1** structure must remove. Without pads **18**, the etch would be required to remove the additional thickness of oxide layer **22** to expose doped regions **13**.

[0032] After forming the openings, a blanket layer of ruthenium oxide (RuO_2) **32**, is formed over exposed surfaces including barrier layer **21**. The barrier layer prevents oxidation of the polysilicon pads **18** by the RuO_2 layer. A RuO_2 layer between about 300 angstroms (Å) thick and about 400 Å thick would be sufficient for this exemplary embodiment. Such as layer can be formed by providing a CHDR precursor at a flow rate of about 500 sccm and an O_2 flow rate of about 200 sccm in a chamber having a temperature of about 210° C. and a pressure of from about 1 Torr to about 9 Torr for about 2 minutes.

[0033] Next, the RuO_2 **32** is converted to ruthenium metal **34** as depicted in FIG. **3**. This can be completed in situ in the

chamber or in a different chamber by providing a hydrogen gas (H_2) or ammonia (NH_3) flow rate of between about 500 sccm and 5,000 sccm, at a temperature of between about 475° C. and about 750° C. at a pressure of between about 5 Torr to about 660 Torr for a duration of between about one minute and about three minutes. This results in a ruthenium metal layer bottom plate layer **34** between about 150 Å and about 250 Å thick.

[0034] Subsequently, the openings **30** are filled with a sacrificial protective material **36** such as photoresist and the ruthenium metal and a portion of dielectric **24** are etched, for example using CMP. This removes the ruthenium metal from the horizontal surface of dielectric **24** to result in the ruthenium metal capacitor bottom plate structures **34** of FIG. **4**. A photoresist mask **40** is formed over the structure to protect the oxide layer between the two container capacitors depicted, then an oxide etch is completed to remove a portion of the exposed oxide depicted as **50** in FIG. **5**. Next, the photoresist layers **36**, **40** of FIG. **4** are removed and a blanket cell dielectric layer such as silicon nitride **52** (cell nitride), Ta_2O_5, Al_2O_3, HfO_2,ZrO_2, barium strontium titanate (BST), hafnium silicate (HfO_2.SiO_2) or zirconium silicate (ZrO_2.SiO_2) is formed. Next, a capacitor top plate **54** is formed, for example from TiN, tungsten nitride (or a WN_x layer), Pt, Ru, W, Pt—Rh, Ta, TaN, RuO_2, etc. A planar layer of BPSG **56**, which with current technology has a thickness of about 4,000 Å, is formed and a patterned photoresist layer **58** is formed that defines an opening **60**, which will expose digit line contact pad **20**. Wafer processing continues according to means know in the art to form a semiconductor memory device.

[0035] The exemplary embodiment described above will provide a smooth capacitor ruthenium metal bottom plate layer. It may be desirable to provide a rough bottom plate layer to increase the surface area and therefore the capacitance between the bottom and top plates. Such a layer can be formed according to the description above, except that an O_2 flow rate of between about 10 sccm and about 100 sccm is provided. This process will result in a rough ruthenium metal surface subsequent to annealing the RuO_2 layer. However, a conductive bottom layer such as WN_x or TaN may be necessary under the ruthenium metal layer to ensure complete electrical conduction across the layer with minimal resistance. This may be required because at the lower O_2 flow rates required to form the textured ruthenium metal layer after annealing, RuO_2 step coverage and coverage across vertical or near vertical surfaces may not be adequate to form a blanket layer, which is free from pinholing and may even form regions of isolated ruthenium metal.

[0036] FIGS. **6-9** depict an embodiment of the invention for use as a control gate layer. FIG. **6** depicts a semiconductor wafer **10** having regions of field oxide **12** formed therein. FIG. **6** further depicts blanket gate oxide layer **62**, for example about 60 Å thick, formed thereover. The gate oxide may comprise any number of materials, including SiO_2, SiO_xN_y (oxynitride), HfO_2, ZrO_2, TiO_2, Ta_2O_5, hafnium silicate (HfO_2.SiO_2), or zirconium silicate (ZrO_2.SiO_2) formed according to means known in the art. After forming the gate oxide layer, a blanket layer of RuO_2 **64**, for example between about 200 Å and about 1,000 Å thick, is formed thereover. Such a layer can be formed by providing a CHDR precursor at a flow rate of about 500 sccm and an O_2 flow rate of about 200 sccm in a chamber having a temperature of about 210° C. and a pressure of from about 1 Torr to about 9 Torr for between about one minute and about five minutes based on a formation rate of about 200 Å/min.

[0037] Next, the RuO_2 **64** is converted to ruthenium metal **70** as depicted in FIG. **7**. This can be completed in a chamber by providing a hydrogen gas (H_2) or ammonia gas (NH_3) flow rate of between about 500 sccm and about 5,000 sccm, at a temperature of between about 475° C. and about 750° C. at a pressure of about 5 Torr to about 660 Torr for a duration of between about one minute and about three minutes. These process parameters result in a ruthenium metal layer **70** between about 150 Å to about 800 Å thick.

[0038] Subsequently, a planar gate capping layer **72** about 2,500 Å thick is formed over the ruthenium layer. This capping layer can be a planar layer of silicon nitride between about 100 Å and about 500 Å thick, and can also comprise a thin TEOS layer interposed between the ruthenium metal control gate and the nitride capping layer. After completing the nitride capping layer, a patterned photoresist layer **74** is formed. The structure of FIG. **7** is etched using an anisotropic etch that defines the transistor gate stack including gate oxide **80**, ruthenium metal control gate **82**, and nitride capping layer **84** as depicted in FIG. **8**. The ruthenium metal layer can be etched using O_2 or O_3 with a biased plasma in a dry etch chamber.

[0039] After etching the FIG. **7** structure to result in the gate stack of FIG. **8**, any necessary wafer implantation, for example, using arsenic, phosphorous, or boron, is performed to alter the electrical characteristics of the wafer and to form doped regions **88** according to means known in the art. Next, a conformal blanket spacer layer **86**, such as a silicon nitride layer, is formed over exposed surfaces. A Si_3N_4 layer between about 400 Å and about 1,000 Å thick, formed according to means known in the art, would be sufficient.

[0040] Finally, the spacer layer is etched to form spacers **90** as depicted in FIG. **9**. Wafer processing continues according to means known in the art to form a functional semiconductor device.

[0041] While this invention has been described with reference to illustrative embodiments, this description is not meant to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as additional embodiments of the invention, will be apparent to persons skilled in the art upon reference to this description. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.

1. A semiconductor device comprising:

first and second dielectric sidewalls; and

a smooth-surfaced ruthenium metal material adjacent the first and second dielectric sidewalls.

2. The semiconductor device of claim **1**, wherein the smooth-surfaced ruthenium metal material defines at least one capacitor bottom plate.

3. The semiconductor device of claim **1**, wherein the smooth-surfaced ruthenium metal material defines at least one gate of a transistor.

4. The semiconductor device of claim **3**, wherein the at least one gate comprises at least one control gate.

5. The semiconductor device of claim **1**, further comprising first and second spacers on the first and second dielectric sidewalls.

6. The semiconductor device of claim **1**, wherein the smooth-surfaced ruthenium metal material is on an oxide.

7. The semiconductor device of claim **6**, wherein the oxide is a gate oxide.

8. The semiconductor device of claim **1**, wherein the first and second dielectric sidewalls define an opening in a dielectric material, wherein the smooth-surfaced ruthenium metal material is formed at least partially within the opening.

9. A semiconductor device, comprising:

a dielectric material having an opening therein, the opening defined by sidewalls; and

a smooth-surfaced ruthenium metal material in contact with the sidewalls of the dielectric material.

10. The semiconductor device of claim **9**, wherein the smooth-surfaced ruthenium metal material is in contact with the sidewalls of the dielectric material and with a conductive material below the opening.

11. The semiconductor device of claim **9**, wherein an upper surface of the dielectric material is co-planar with an upper surface of the smooth-surfaced ruthenium metal material.

12. The semiconductor device of claim **9**, further comprising a cell dielectric material on the smooth-surfaced ruthenium metal material.

13. The semiconductor device of claim **12**, further comprising a capacitor top plate on the cell dielectric material.

14. The semiconductor device of claim **13**, further comprising another dielectric material on the capacitor top plate and filling a remainder of the opening.

15. The semiconductor device of claim **9**, wherein the smooth-surfaced ruthenium metal material comprises a capacitor bottom plate.

16. A semiconductor device, comprising:

a transistor gate stack on a semiconductor wafer, the transistor gate stack comprising a gate oxide, a ruthenium control gate on the gate oxide, and a capping material on the ruthenium control gate.

17. The semiconductor device of claim **16**, wherein the ruthenium control gate comprises smooth-surfaced ruthenium.

18. The semiconductor device of claim **16**, further comprising spacers on sidewalls of the transistor gate stack.

19. The semiconductor device of claim **16**, wherein the smooth-surfaced ruthenium control gate comprises a thickness of between about 150 Å and about 800 Å.

20. The semiconductor device of claim **16**, wherein the capping material comprises a thickness of between about 100 Å and about 500 Å.

* * * * *