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(54) Title: THIN-FILM DEVICE

(57) Abstract: Embodiments of methods, apparatuses, devices and systems associated with a thin-film device 200 are disclosed.



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THIN-FILM DEVICE

BACKGROUND

Electronic devices, such as integrated circuits, solar cells, or electronic
10 displays, for example, may be comprised of one or more electrical devices, such
as one or more thin-film transistors (TFTs). Methods or materials utilized to form
electrical devices such as these may vary, and one or more of these methods or
materials may have particular disadvantages. For example, use of such methods
15 or materials may be time-consuming or expensive, may involve the use of high
temperature processing, or may not produce devices having the desired
characteristics.

BRIEF DESCRIPTION OF THE DRAWINGS

20 Subject matter is particularly pointed out and distinctly claimed in the
concluding portion of the specification. The claimed subject matter, however, both
as to organization and method of operation, together with objects, features, and
advantages thereof, may best be understood by reference of the following detailed
description when read with the accompanying drawings in which:

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FIG. 1 is a depiction of an embodiment of a thin-film transistor structure
having laser annealed active regions;

FIG. 2 is a depiction of an embodiment such as a thin-film transistor;

30

FIG. 3 is a depiction of a simplified top view of the embodiment of FIG. 2;
and

FIG. 4 is a depiction of an embodiment having adjacent thin-film transistor structures.

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DETAILED DESCRIPTION

In the following detailed description, numerous specific details are set forth to provide a thorough understanding of claimed subject matter. However, it will be understood by those skilled in the art that claimed subject matter may be practiced without these specific details. In other instances, methods, procedures, components and circuits that would be understood by one of ordinary skill have not been described in detail so as not to obscure claimed subject matter.

Electronic devices, such as semiconductor devices, display devices, nanotechnology devices, conductive devices, and dielectric devices, for example, may comprise one or more electronic components. The one or more electronic components may comprise one or more thin-film components, which may be comprised of one or more thin films. In the context of this application the term or means a sentential connective that forms a complex sentence which is true when at least one of its constituent sentences is true. In this context, the term thin film refers to a layer of one or more materials formed to a thickness, such that surface properties of the one or more materials may be observed, and these properties may vary from bulk material properties. Thin films may additionally be referred to as component layers, and one or more component layers may comprise one or more layers of material, which may be referred to as material layers, for example. The one or more material or component layers may have electrical or chemical properties, such as conductivity, chemical interface properties, charge flow, or processability. The one or more material or component layers may additionally be patterned, for example. The one or more material or component layers, in combination with one or more other material or component layers may form one or more electrical components, such as thin-film transistors (TFTs), capacitors, diodes, resistors, photovoltaic cells, insulators, conductors, optically active

components, or the like. Components such as TFTs, in particular, may, for example, be utilized in components including smart packages and display components including, for example, radio frequency identification (RFID) tags and electroluminescent and a liquid crystal displays (LCD), such as active matrix liquid
5 crystal display (AMLCD) devices, for example.

At least as part of the fabrication process of electronic components, such as thin-film transistors, one or more layers of material may be formed at least as part of one or more of the component layers, such as by forming at least a portion
10 of an electrode, including: source, drain, or gate electrodes; a channel layer; or a dielectric layer. These one or more layers of material may be formed on or over a substrate, for example.

In at least one embodiment, one or more processes utilized may comprise
15 one or more low temperature processes. In this context, low temperature processes or processing refers to one or more processes that may be performed at relatively low temperatures as compared to one or more other processes. For example, processes that may be utilized to form material layers of a TFT, may be performed at particular temperatures, such as temperatures equal to or less than
20 approximately 300 degrees Celsius, including processes performed at temperatures equal to or less than approximately 100 degrees Celsius. It should be noted that particular temperature ranges may depend in part on the type of materials or processes utilized, and claimed subject matter is not limited in this respect. In at least one embodiment, utilization of low temperature processes
25 may provide the capability to utilize materials that would not be suitable for use in non-low temperature processes, for example. Additionally, use of low temperature materials or processes may result in the formation of a component, such as a TFT, having improved mechanical flexibility or resistance to mechanical failure such as by delamination or cracking, as compared to components formed
30 by use of non-low temperature processes, and may additionally result in the formation of a device having other properties, as will be explained in more detail

later. However, it is worthwhile to note that claimed subject matter is not limited in this respect.

One or more processes or materials, such as low temperature processes or materials may be utilized to form one or more material or component layers of a component. For example, one or more temperature sensitive materials, such as temperature sensitive substrate materials, channel layer materials or dielectric layer materials may be utilized, and this may include materials that may have characteristics such as flexibility, for example, or may include materials not suitable for use in non-low temperature processes, for example. Additionally, one or more low temperature processes, such as selective annealing; vacuum deposition processes including RF (radio frequency) sputtering, DC sputtering, DC-pulsed sputtering, or reactive sputtering, wherein the substrate may be unheated or maintained at a suitably low temperature; atomic layer deposition (ALD); or evaporation processes, including thermal or electron-beam evaporation, for example, may be utilized in at least one embodiment.

Furthermore, electrical components, such as TFTs, for example, may be at least partially formed by laser annealing or processing. In this context laser annealing refers to locally exposing a selected portion of a suitable material to one or more laser beams to alter at least one or more properties of the suitable material. Laser annealing in this context, as opposed to thermal annealing of the entire substrate, may obviate the need for subtractive processing or selective removal, such as by photolithography and the like, of portions of the suitable material that may otherwise hinder device to device electrical isolation for adjacent thin-film transistors. In addition, laser annealing may, under some circumstances, be performed at lower temperatures than thermal annealing, which may allow use of heat sensitive substrates that may otherwise be damaged by thermal annealing. Furthermore, laser annealing may allow thermal treatment to higher temperatures than may be appropriate for use with heat sensitive substrates under other circumstances due to the controlled thermal transient from the laser, the localized nature of the laser spot, or the thermal conduction pathways from the

localized laser spot, for example. It should of course be noted that claimed subject matter is not limited in this regard.

Fig. 1 is a depiction of an embodiment 100 of a thin-film transistor structure having laser annealed active regions. With regard to Fig. 1, embodiment 100 may include a substrate 110. Substrate 110 may comprise an organic or an inorganic material, for example. In addition, embodiment 100 may include laser annealed regions 120, 121, 122, 123, 124, and 125. It should be noted that claimed subject matter is not limited to any particular number of laser annealed regions. In this context, laser annealed regions 120, 121, 122, 123, 124, and 125, may be formed by selectively exposing a region of a material, such as an oxide material, to one or more laser beams or laser pulses. The oxide material may comprise any of a number of suitable materials such as zinc oxide, tin oxide, indium oxide, cadmium oxide, gallium oxide, or combinations thereof, including zinc tin oxide, zinc indium oxide, or combinations thereof, to name but a few examples. Furthermore, embodiment 100 may include active regions 130, 131, 132, 133, 134, and 135. Active regions 130, 131, 132, 133, 134, and 135 may be formed through a combination of laser annealed regions 120, 121, 122, 123, 124 and 125, and optionally including other semiconductor layers, which when combined with other thin-film structures or layers may form a transistor or a portion of a transistor, such as a channel region, for example. It should be noted that claimed subject matter is not limited in this regard.

With regard to Fig. 1, substrate 110 may comprise one or more types of plastic or one or more organic substrate materials, such as polyimides (PI), including Kapton[®]; polyethylene terephthalates (PET); polyethersulfones (PES); polyetherimides (PEI); polycarbonates (PC); polyethylenenaphthalates (PEN); acrylics, including acrylates and methacrylates, such as polymethylmethacrylates (PMMA); or combinations thereof, but claimed subject matter is not so limited. Additionally, substrate 110 may also comprise one or more inorganic materials, including silicon, silicon dioxide, one or more types of glass, quartz, sapphire, stainless steel and metal foils, including foils of aluminum or copper, or a variety of

other suitable materials, for example, but claimed subject matter is not so limited. Additionally, in at least one embodiment, wherein a substrate material is substantially comprised of one or more metals, an insulator layer may be utilized in addition to the one or more metals to form the substrate. A choice of substrate materials may determine certain characteristics or tolerances that may influence the available semiconductor fabrication processes that are suitable for use with a particular substrate material. For example, organic substrate materials may be more sensitive to heat and as such may be more suitable for use with lower temperature processes than those that may be suitable for use with inorganic substrates under certain circumstances. Choice of substrate material may depend on a variety of factors including, but not limited to, heat sensitivity, cost, flexibility, durability, resistance to failure, surface morphology, chemical stability, optical transparency, barrier properties, etc. and of course it should be noted that claimed subject matter is not limited in this regard.

In addition, the oxide material may further comprise various combinations of the above listed oxides with other oxides such as lead oxide, copper oxide, silver oxide, or antimony oxide, to name but a few examples. Of course it should be noted that claimed subject matter is not limited in this regard. The laser beams or laser pulses may be generated by a UV excimer laser generating laser beams or laser pulses having an approximate range of 193-337 nanometers in wavelength, such as approximately 248 nanometers in wavelength, for example, though other lasers having different wavelength ranges may be employed, and claimed subject matter is not limited in this regard. Laser treatment parameters, such as fluence, shot count, scan speed, duty cycle, etc. may be varied to achieve desired electrical, physical, or chemical properties in the laser annealed regions, and again claimed subject matter is not limited in this regard. For example, the UV excimer laser may be employed with a fluence of approximately 5 to 600 millijoules per square centimeter, and a shot count of approximately 10 to 5000, to name but a few possible laser treatment parameters. Again, however, it should be noted that the above laser treatment parameters are provided as merely examples and that claimed subject matter is not so limited.

Fig. 2 is a diagram of an embodiment 200, such as thin film transistor, for example, that may include portions that may correspond to one of the active regions of Fig. 1. With regard to Fig. 2, embodiment 200 may comprise a first layer 210, such as a substrate, for example. Embodiment 200 may further comprise a second layer 220. Second layer 220 may comprise a gate electrode layer, for example. Embodiment 200 may also include third layer 230, such as a gate dielectric layer which may comprise silicon dioxide or other materials. Embodiment 200 may further include an un-patterned oxide layer 240. Un-patterned oxide layer 240 may comprise a blanket coated oxide layer deposited using a vacuum deposition process. In this context, blanket coated may refer to any un-patterned deposition such as one that may cover a relatively small portion of a substrate up to and including a deposition that may cover a relatively large portion of a substrate, which may under some circumstances include an entire substrate, depending on various factors, for example. In the context of embodiment 200, a blanket coated oxide layer may correspond to an actual surface area on the order of centimeters, for example, though again it should be noted that claimed subject matter is not so limited. In addition, blanket coated or un-patterned oxide layer may comprise a layer such that, as deposited and without further treatment, the area of the blanket coated or un-patterned oxide layer may be substantially larger than that of a single thin-film transistor or other semiconductor component, for example. With regard to un-patterned oxide layer 240, vacuum deposition processes may include, but are in no way limited to, RF (radio frequency) sputtering, DC sputtering, DC-pulsed sputtering, or reactive sputtering, for example, though again claimed subject matter is not so limited. Un-patterned oxide layer 240 may comprise an oxide material such as zinc oxide, tin oxide, indium oxide, cadmium oxide, gallium oxide, or combinations thereof, including zinc tin oxide, zinc indium oxide, or combinations thereof, to name but a few examples.

In embodiment 200 un-patterned oxide layer 240 may have a selectively annealed active region 250, which may, within the structure of embodiment 200

and along with other layers or structures depicted or not shown, function as a channel region for a transistor, such as a thin-film transistor for example.

Selectively annealed active region 250 may be formed by laser annealing a selected portion of un-patterned oxide layer 240. In this context laser annealing
5 may comprise selectively exposing the selected portion of un-patterned oxide later 240 to at least one or more laser pulses or laser beams. The one or more laser pulses or laser beams may, as discussed above, be generated by a UV excimer laser generating laser beams or laser pulses at approximately 193-337
10 nanometers in wavelength, though other types of lasers which may or may not have different wavelength ranges may be employed, such as solid-state visible or near-IR lasers with wavelengths of 355-1064 nanometers, far-IR lasers with wavelengths of 9.6-10.6um, or fiber lasers with wavelengths of 775-2100nm, to name but a few examples, and it should be noted that claimed subject matter is not limited in this regard. Laser treatment parameters, such as fluence, shot
15 count, pulse length, firing frequency, scan speed, duty cycle, etc. may be varied to achieve desired electrical, physical, or chemical properties in the laser annealed regions, and again claimed subject matter is not limited in this regard.

Embodiment 200 may further include a source electrode 260 and a drain electrode 270. Although other materials and deposition processes may be used,
20 source electrode 260 may be formed by RF sputtering indium-tin oxide (ITO) above or onto un-patterned oxide layer 240, or gate insulator layer 230, for example, although claimed subject matter is not so limited. Likewise, drain electrode 270 may be formed by RF sputtering indium-tin oxide above or onto un-patterned oxide layer 240, or insulator layer 230, for example. Source electrodes
25 260 and drain electrode 270 may have a thickness that under some circumstances may be in a range of approximately 50 to 500 nm, although it should be noted that claimed subject matter is not limited in this regard.

First layer 210 may comprise one or more types of plastic or one or more
30 organic substrate materials, such as polyimides (PI), including Kapton; polyethylene terephthalates (PET); polyethersulfones (PES); polyetherimides (PEI); polycarbonates (PC); polyethylenenaphthalates (PEN); acrylics, including

acrylates, and methacrylates, such as polymethylmethacrylates (PMMA); or combinations thereof, but it should be noted that claimed subject matter is not so limited. Additionally, first layer 210 may additionally comprise one or more inorganic materials, including silicon, silicon dioxide, one or more types of glass, stainless steel and metal foils, including foils of aluminum and copper, for example, but again claimed subject matter is not so limited. Additionally, in at least one embodiment, wherein a first layer 210 may comprise a substrate material that substantially comprises one or more metals, an insulator layer (not shown) may be utilized in addition to the one or more metals to form a first layer 210, for example. Second layer 220 may comprise a metal such as Al, Ag, In, Sn, Zn, Ti, Cr, Mo, Au, Pd, Pt, Cu, W, Ni or combinations thereof. It should be noted that claimed subject matter is not limited in this regard. First layer 220 may under some circumstances have a thickness that may be in a range of approximately 50 to 500 nm, although it should be noted that claimed subject matter is not limited in this regard. In addition, second layer 220 may comprise other conductive materials, such as other metals or doped oxide semiconductors, such as n-type doped zinc oxide, indium oxide, or tin oxide, including indium tin oxide (ITO), to name but a few examples, though other materials may be used to form a gate layer and will be understood by one of ordinary skill.

Additionally third layer 230 may comprise other materials such as inorganic dielectrics such as zirconium oxide, tantalum oxide, yttrium oxide, lanthanum oxide, silicon oxide, aluminum oxide, hafnium oxide, barium zirconate titanate, barium strontium titanate, silicon nitride, or silicon oxynitride, to name but a few examples. In addition, third layer 230 may comprise organic dielectrics such as curable monomers, including UV curable acrylic monomers, UV curable monomers, thermal curable monomers; acrylic polymers; polymer solutions such as melted polymers or oligomer solutions; poly methyl methacrylate, poly vinylphenol; benzocyclobutene; or one or more polyimides, to name but a few examples. In addition, third layer 230 may have a thickness that may under some circumstance be in a range of approximately 20 to 1000 nm, although it should be noted that claimed subject matter is not limited in this regard. In addition, third

layer 230 may under some circumstance comprise multiple sub-layers, including one or more inorganic dielectric or organic dielectric layers, though other materials may be used to form a gate insulator layer and will be understood by one of ordinary skill and claimed subject matter is not limited in this regard. Un-patterned oxide layer 240 may have a thickness which under some circumstances may be in a range of approximately 10 to 500 nm, although it should be noted that claimed subject matter is not limited in this regard. For example, un-patterned oxide layer 240 may comprise zinc tin oxide with a zinc:tin atomic ratio in the range of approximately 1:1 to approximately 4:1, RF sputtered above or onto gate insulator layer 230, to a thickness of approximately 50 nm, though this is just an example and claimed subject matter is not so limited. By way of example, RF sputtering may be carried out with an unheated substrate, examples of which are discussed above, at 100W RF (for an approximately 3-inch diameter target), in an approximately 90% argon and 10% oxygen environment at 5 mTorr. It should be noted that the above details of an RF sputtering process are provided merely for illustration and claimed subject matter is not limited in this regard. Furthermore, the oxide material of un-patterned oxide layer 240 may further comprise combinations of the above listed oxides with other oxides such as lead oxide, copper oxide, silver oxide, or antimony oxide for example, though other materials may be suitable as well and claimed subject matter is not limited in this regard. In addition, source electrode 260 and drain electrode 270 may also comprise other materials such as other doped oxide semiconductors, such as n-type doped zinc oxide, indium oxide, or tin oxide, or metals, such as Al, Ag, In, Sn, Zn, Ti, Cr, Mo, Au, Pd, Pt, Cu, W, Ni, or combinations thereof, to name but a few examples and again claimed subject matter is not so limited.

Fig. 3 is a depiction of a simplified top view of embodiment 200. With regard to Fig. 3, un-patterned oxide layer 240, as discussed above with regard to Fig. 2, may have been formed over gate insulator layer 230 (shown in Fig. 2), by a vacuum deposition process, for example. Active region 250 may be formed by selectively annealing a selected portion of un-patterned oxide layer 240. Again, selectively annealing a selected portion of un-patterned oxide layer may comprise

laser annealing a selected portion of un-patterned oxide layer 240, such as by exposing the selected portion to one or more laser beams or laser pulses, for example. As discussed above, the one or more laser beams or pulses may be generated by a UV excimer laser or other lasers, for example. Again, it should be noted that claimed subject matter is not so limited. As discussed above, laser treatment parameters can be varied in a number of ways to produce desired physical, electrical, or chemical properties in the selected portion of un-patterned oxide layer 240, for example. Desired properties for active region 250 may comprise a range for transistor turn-on voltage, a range of channel carrier concentration, a range of transistor channel mobility, and a maximum acceptable defect density, for example, although claimed subject matter is not so limited. As discussed above, embodiment 200 may additionally have a source, such as source electrode 260, along with a drain, such as drain electrode 270. As shown in Fig. 3 there may be a gap between source electrode 260 and drain electrode 270. Active region 250 may be positioned at least partially within the gap between source electrode 260 and drain electrode 270. In this context, active region 250 may, in combination with source electrode 260, drain electrode 270 or other layers or structures, function as a channel region such that the combination may function as a transistor, such as a thin-film transistor, for example.

Though embodiment 200 has been described above with regard to a particular structure it should be noted that the thin-film transistors may be of any type or structure, including but not limited to, horizontal, vertical, coplanar electrode, staggered electrode, top-gate, bottom-gate, single-gate, and double-gate, to name but a few. In this context, a coplanar electrode configuration may mean a transistor structure where the source and drain electrodes are positioned on the same side of the channel layer as the gate electrode. In this context, a staggered electrode configuration may mean a transistor structure where the source and drain electrodes are positioned on the opposite side of the channel layer as the gate electrode.

Fig. 4 is a depiction of an embodiment 400. With regard to Fig. 4, embodiment 400 may include a first layer 410, such as a substrate layer. In this context a substrate layer may, for example, comprise one or more types of plastic or one or more organic substrate materials. Embodiment 400 may further
5 comprise a first gate electrode 420 and a second gate electrode 425. Embodiment 400 may further include a third layer 430, such as a gate insulator layer, which may comprise silicon dioxide or other materials such as inorganic dielectrics such as zirconium oxide, tantalum oxide, yttrium oxide, lanthanum oxide, silicon oxide, aluminum oxide, hafnium oxide, barium zirconate titanate,
10 barium strontium titanate, silicon nitride, or silicon oxynitride, as just a few examples.

Embodiment 400 may further include an un-patterned or blanket coated oxide layer 440. In this context, blanket coated may refer to any un-patterned
15 deposition of a material or materials such as a deposition that may cover a relatively small portion of a substrate and up to and including a deposition that may cover a relatively large portion of a substrate, depending on various factors, for example. In the context of embodiment 400, a blanket coated oxide layer may correspond to an actual surface area on the order of centimeters, for example,
20 though again it should be noted that claimed subject matter is not so limited. In addition, un-patterned or blanket coated may mean that the as deposited layer is such that without further treatment or processing the area of the as deposited layer may be substantially larger than that of a single thin-film transistor or other semiconductor component, for example. Un-patterned oxide layer 440 may
25 comprise an oxide layer deposited using a vacuum deposition process. Un-patterned oxide layer 440 may comprise an oxide material such as zinc oxide, tin oxide, indium oxide, cadmium oxide, gallium oxide, or combinations thereof, including zinc tin oxide, zinc indium oxide, to name but a few examples. For example, un-patterned oxide layer 440 may comprise zinc tin oxide with zinc:tin
30 atomic ratio in the range of approximately 1:1 to approximately 4:1, RF sputtered above or onto gate insulator layer 430, though it should be noted that this is just an example and claimed subject matter is not so limited. In addition, the RF

sputtering may be carried out with a heated or unheated substrate, examples of which are discussed above, at 100W RF (for an approximately 3-inch diameter target), in an approximately 90% argon and 10% oxygen environment or at approximately 5 mTorr, for example. Again, the details of the sputtering process
5 described above are provided merely for illustration and are in no way intended to limit claimed subject matter.

In embodiment 400, un-patterned oxide layer 440 may further comprise a first selectively annealed active region 450 and a second selectively annealed
10 active region 460. As discussed further below first selectively annealed active region 450 and second selectively annealed active region 460 may, within the overall structure and in connection with other layers or structures of embodiment 400, function as a first channel region and a second channel region for a first transistor and a second transistor, respectively, such as a first and a second thin-
15 film transistor, for example. First selectively annealed active region 450 and second selectively annealed active region 460 may be formed by laser annealing a respective first selected portion and a second selected portion of un-patterned oxide layer 440. In this context laser annealing may comprise selectively exposing the first and second selected portions of un-patterned oxide layer 440 to
20 at least one or more laser pulses. The at least one or more laser pulses may, as discussed above, be generated by a UV excimer laser. The UV excimer laser may, for example, be operable to generate laser beams or laser pulses having an approximate wavelength range of 193-337 nanometers, such as having a wavelength of approximately 248 nanometers. As discussed above, it should be
25 noted that other types of lasers which may or may not have different wavelength ranges or power ranges may be employed, and claimed subject matter is not limited in this regard. Laser treatment parameters, such as fluence, shot count, pulse length, firing frequency, scan speed, duty cycle, etc. may be varied to achieve desired electrical, physical, or chemical properties in the laser annealed
30 regions, and again claimed subject matter is not limited in this regard.

Embodiment 400 may further include a first source electrode 470 and a first drain electrode 475. Although other materials and deposition processes may be used, first source electrode 470 may be formed by RF sputtering indium-tin oxide above or onto un-patterned oxide layer 440 or gate insulator layer 430, for

5 example. Likewise, first drain electrode 475 may be formed by RF sputtering indium-tin oxide above or onto un-patterned oxide layer 440 or gate insulator layer 430, for example. Again, different materials or deposition processes, such as other sputtering processes, thermal evaporation processes, e-beam evaporation processes or chemical vapor deposition processes, for example, may be used to
10 form first source electrode 470 and first drain electrode 475, and claimed subject matter is not limited to the particular processes and materials described above.

Embodiment 400 may further include a second source electrode 480 and a second drain electrode 485. Although other materials and deposition processes may be used, second source electrode 480 may be formed by RF sputtering
15 indium-tin oxide above or onto un-patterned oxide layer 440 or gate insulator layer 430, for example. Second source electrode 480 and second drain electrode 485 may be formed by RF sputtering indium-tin oxide above or onto un-patterned oxide layer 440 or gate insulator layer 430, for example. Again different materials or deposition processes may be used to form second source electrode 480 and
20 second drain electrode 485, and claimed subject matter is not limited in this regard.

In embodiment 400 first gate electrode 420, first source electrode 470, first drain electrode 475, gate insulator layer 430, and first active region 450 may function as a first transistor 490, such that first active region 450 may function as a
25 first channel region. Likewise, second gate electrode 425, second source electrode 480, second drain electrode 485, gate insulator layer 430, and second active region 460 may function as a second transistor 495, such that second active region 460 may function as a second channel region. Embodiment 400 may achieve effective electrical isolation between first transistor 490 and second
30 transistor 495 without requiring a subtractive processing of non-annealed portions of un-patterned oxide layer 440, such as by employing a photolithography process or the like, for example. For certain materials, such as zinc oxide, indium oxide,

tin oxide, cadmium oxide, gallium oxide, or combinations thereof, including zinc tin oxide, zinc indium oxide, or other combinations thereof, to name but a few examples, and for appropriately selected deposition technique and conditions, the non-annealed portions of the un-patterned oxide layer 440 may exhibit certain

5 properties, such as a relatively large and positive (in the case of n-channel transistor) turn-on voltage, relatively low mobility, relatively low carrier concentration, or relatively high trap density, such that the non-annealed portion of the un-patterned oxide layer may exhibit relatively low conductivity resulting in relatively minimal leakage between adjacent transistor structures 490 and 495.

10 When materials such as those mentioned above or below are used to form un-patterned oxide layer 440, the properties of the non-annealed material may hinder device to device current leakage between adjacent transistors, such as first transistor 490 and second transistor 495. However, as discussed above, any selectively annealed portion, such as first active region 450 and second active

15 region 460, of un-patterned oxide layer 440, may, due having been selectively annealed, have properties such that the selectively annealed portion may function as a part, such as a channel region, of a thin-film transistor, for example.

For example, an un-patterned oxide layer, such as un-patterned oxide layer

20 440, when comprising zinc oxide, tin oxide, indium oxide, cadmium oxide, gallium oxide, or combinations thereof, including zinc tin oxide, zinc indium oxide, or other combinations thereof, which may have been RF sputtered onto a gate insulating layer, such as gate insulating layer 430, may have properties such as relatively low mobility, relatively high trap density and relatively large, and in the case of an

25 n-channel transistor, positive turn-on voltage such that un-patterned oxide layer 440 may not effectively pass current laterally between adjacent contacts, such as adjacent transistor sources and drains, for example. However, active regions 450 and 460, having been selectively annealed by exposure to one or more laser beams or pulses generated by an UV excimer laser, or other lasers, for example,

30 in a laser treatment process such as, but not limited to, those described above or below may exhibit much different properties such as a relatively smaller turn-on voltage, a relatively lower trap density, and a relatively higher mobility such that

active regions 450 and 460 may have suitable properties for functioning as channel regions in first transistor 490 and second transistor 495 respectively.

In addition to the materials described above, first layer 410 may comprise materials, such as polyimides (PI), including Kapton; polyethylene terephthalates (PET); polyethersulfones (PES); polyetherimides (PEI); polycarbonates (PC); polyethylenenaphthalates (PEN); acrylics, including acrylates, and methacrylates, such as polymethylmethacrylates (PMMA); or combinations thereof, but it should be noted that claimed subject matter is not so limited. Additionally, first layer 410 may comprise one or more inorganic materials, including silicon, silicon dioxide, one or more types of glass, stainless steel and metal foils, including foils of aluminum and copper, for example, but claimed subject matter is not so limited. Additionally, in at least one embodiment, wherein a first layer 410 may comprise a substrate material that substantially comprises one or more metals, an insulator layer (not shown) may be utilized in addition to the one or more metals to form a first layer 410, for example. In addition to the materials listed above, first gate electrode 420 and second gate electrode 425 may comprise materials such as metals or doped oxide semiconductors, such as n-type doped zinc oxide, indium oxide, or tin oxide, including indium-tin oxide (ITO), to name but a few examples, though other materials may be used to form a gate layer and will be understood by one of ordinary skill. Additionally, first gate electrode 420 and second gate electrode 425 may comprise a metal such as Al, Ag, In, Sn, Zn, Ti, Cr, Mo, Au, Pd, Pt, Cu, W, Ni or combinations thereof, or other conductive material. However, it should be noted that claimed subject matter is not limited in this regard. In addition third layer 430 may comprise organic dielectrics such as curable monomers, including UV curable acrylic monomers, UV curable monomers, or thermal curable monomers; acrylic polymers; polymer solutions such as melted polymers or oligomer solutions; poly methyl methacrylate; poly vinylphenol; benzocyclobutene; or one or more polyimides, to name but a few examples. Furthermore, third layer 430 may comprise multiple sub-layers, including one or more inorganic dielectric or organic dielectric layers, though other materials may

be used to form a gate insulator layer and will be understood by one of ordinary skill.

With regard to un-patterned oxide layer 440, vacuum deposition processes
5 may include, but are in no way limited to, RF (radio frequency) sputtering, DC sputtering, DC-pulsed sputtering, reactive sputtering, thermal evaporation, electron-beam evaporation, chemical vapor deposition (CVD), or atomic layer deposition (ALD), for example. With further regard to un-patterned oxide layer 440, the oxide material may under some circumstances further comprise
10 combinations of the above listed oxides with other oxides such as lead oxide, copper oxide, silver oxide, and antimony oxide, for example, though other materials may be suitable as well, and of course claimed subject matter is not limited in this regard.

With regard to first source electrode 470 and first drain electrode 475, other
15 materials may be used, such as other doped oxide semiconductors, such as n-type doped zinc oxide, indium oxide, and tin oxide, or metals, such as Al, Ag, In, Sn, Zn, Ti, Cr, Mo, Au, Pd, Pt, Cu, W, Ni, or combinations thereof, to name but a few examples, although again, it should be noted that claimed subject matter is
20 not limited in this regard. With regard to second source electrode 480 and second drain electrode 485, other doped oxide semiconductors, such as n-type doped zinc oxide, indium oxide, and tin oxide, or metals, such as Al, Ag, In, Sn, Zn, Ti, Cr, Mo, Au, Pd, Pt, Cu, W, Ni, or combinations thereof, may be used, to name but a few examples, and again claimed subject matter is not so limited.

25 Though embodiment 400 has been described above with regard to a particular structure it should be noted that the thin-film transistors may be of any type or structure, including but not limited to, horizontal, vertical, coplanar electrode, staggered electrode, top-gate, bottom-gate, single-gate, and double-
30 gate, to name but a few. In this context, a coplanar electrode configuration may mean a transistor structure where the source and drain electrodes are positioned on the same side of the channel layer as the gate electrode. In this context, a

staggered electrode configuration may mean a transistor structure where the source and drain electrodes are positioned on the opposite side of the channel layer as the gate electrode.

5 The above embodiments are provided merely as examples and claimed subject matter is not so limited. Though above embodiments are described in terms of one or two transistors the claimed subject matter is not so limited. One skilled in the art, in light of this disclosure, could make embodiments having as many transistors as necessary to form a wide variety of semiconductor devices or
10 circuits. It will, of course, also be understood that, although particular embodiments have just been described, the claimed subject matter is not limited in scope to a particular embodiment or implementation.

 In the preceding description, various aspects of the claimed subject matter
15 have been described. For purposes of explanation, specific numbers, systems or configurations were set forth to provide a thorough understanding of claimed subject matter. However, it should be apparent to one of ordinary skill having the benefit of this disclosure that claimed subject matter may be practiced without the specific details. In other instances, features or methods that would be understood
20 by one of ordinary skill were omitted or simplified so as not to obscure claimed subject matter. While certain features have been illustrated or described herein, many modifications, substitutions, changes or equivalents will now occur to one of ordinary skill. It is, therefore, to be understood that the appended claims are intended to cover all such modifications or changes as fall within the true spirit of
25 claimed subject matter.

What is claimed is:

Claims:

1. An apparatus comprising:
a substrate having a blanket coated semiconductor oxide material disposed thereover;
an annealed active region of a thin-film device disposed over said substrate, wherein said annealed active region includes a selected portion of said blanket coated semiconductor oxide material.
2. The apparatus of claim 1, wherein said oxide material comprises at least one of zinc oxide, tin oxide, indium oxide, cadmium oxide, gallium oxide, zinc tin oxide, zinc indium oxide, tin indium oxide, and combinations thereof.
3. The apparatus of claim 1, wherein said oxide material comprises zinc tin oxide, with a zinc:tin atomic ratio between approximately 1:4 and approximately 4:1.
4. The apparatus of any of the above claims, wherein said thin-film device further comprises a thin-film transistor channel region formed by selectively annealing a selected portion of said blanket coated oxide material.
5. The apparatus of any of the above claims, wherein the annealed selected portion further comprises a laser annealed selected portion of said blanket coated semiconductor oxide material.
6. The apparatus of any of the above claims, further comprising a source electrode and a drain electrode and wherein said source electrode, said drain electrode, and said channel region are configured such that said source electrode, said drain electrode, and said channel region are operable to function as a transistor.

7. The apparatus of claim 1, further comprising:
 - a first transistor comprising a first active region comprising a first selectively annealed portion of said blanket coated semiconductor oxide material; and
 - a second transistor comprising a second active region comprising a second selectively annealed portion of said blanket coated semiconductor oxide material.
8. The apparatus of claim 7, wherein said first active region and said second active region comprise thin-film transistor channels.
9. The apparatus of claim 7, wherein said blanket coated semiconductor oxide material further comprises a non-laser annealed portion and wherein said non-annealed portion substantially hinders current leakage between said first transistor and said second transistor.
10. A method comprising:
 - forming an un-patterned material layer; and
 - selectively annealing a first portion of said un-patterned material layer to form a semiconductive active region
11. The method of claim 10, wherein said un-patterned material layer comprises an un-patterned oxide layer.
12. The method of claim 11, and further comprising:
 - forming a source electrode and a drain electrode, wherein said source electrode and said drain electrode are positioned such that the selectively annealed portion of said un-patterned oxide layer is operable to function as a channel region.
13. The method of claim 12, wherein selectively annealing a first portion of said un-patterned oxide layer comprises applying a first laser pulse to a selected portion of said un-patterned oxide layer.

14. The method of claim 13, wherein selectively annealing a first portion of said un-patterned oxide layer further comprises generating said first laser pulse with a first laser.

15. The method of claim 14, wherein the oxide material comprises at least one of zinc oxide, indium oxide, tin oxide, zinc tin oxide, zinc indium oxide, and combinations thereof.

Fig. 1

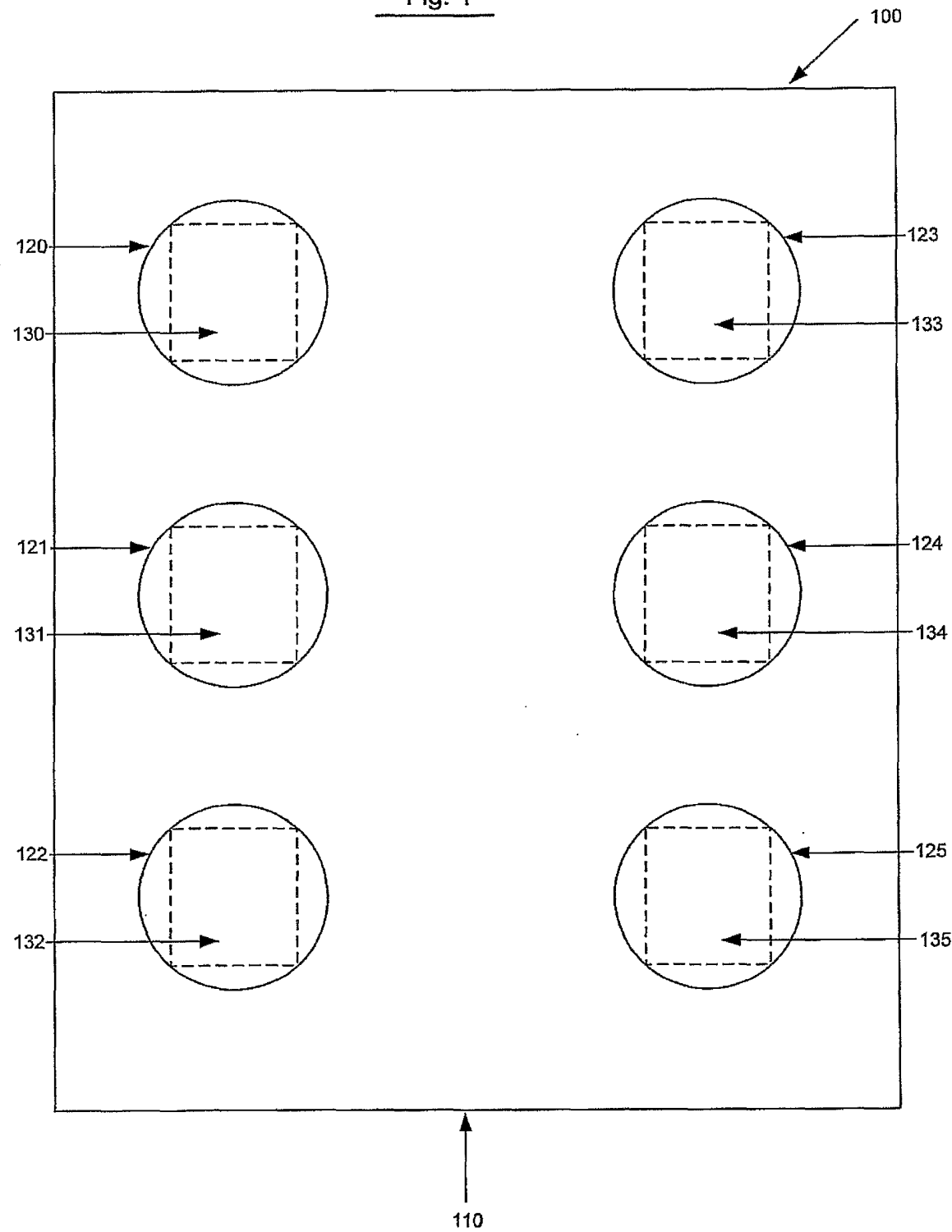


Fig. 2

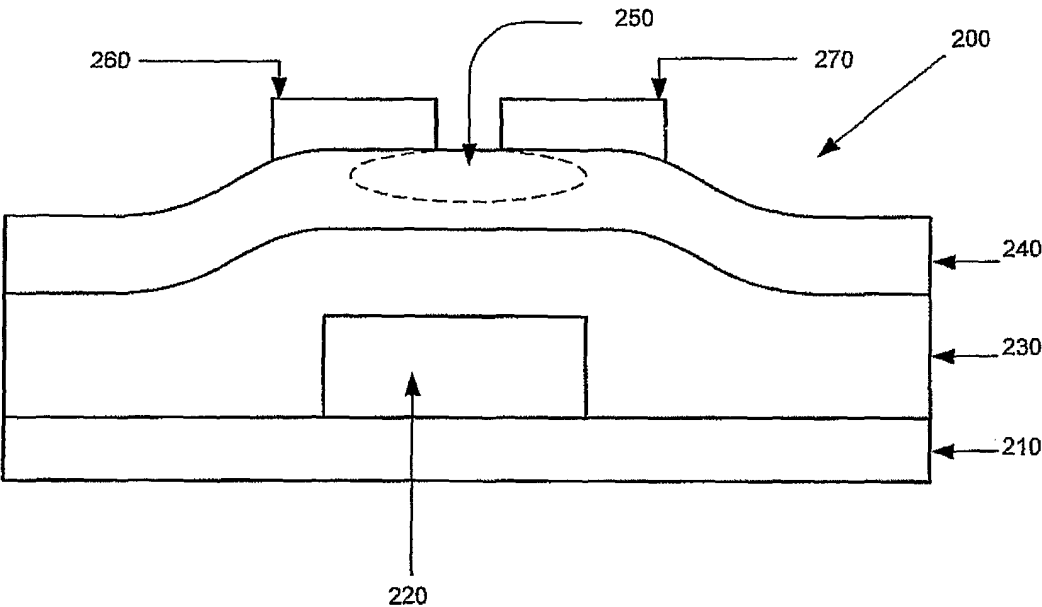


Fig. 3

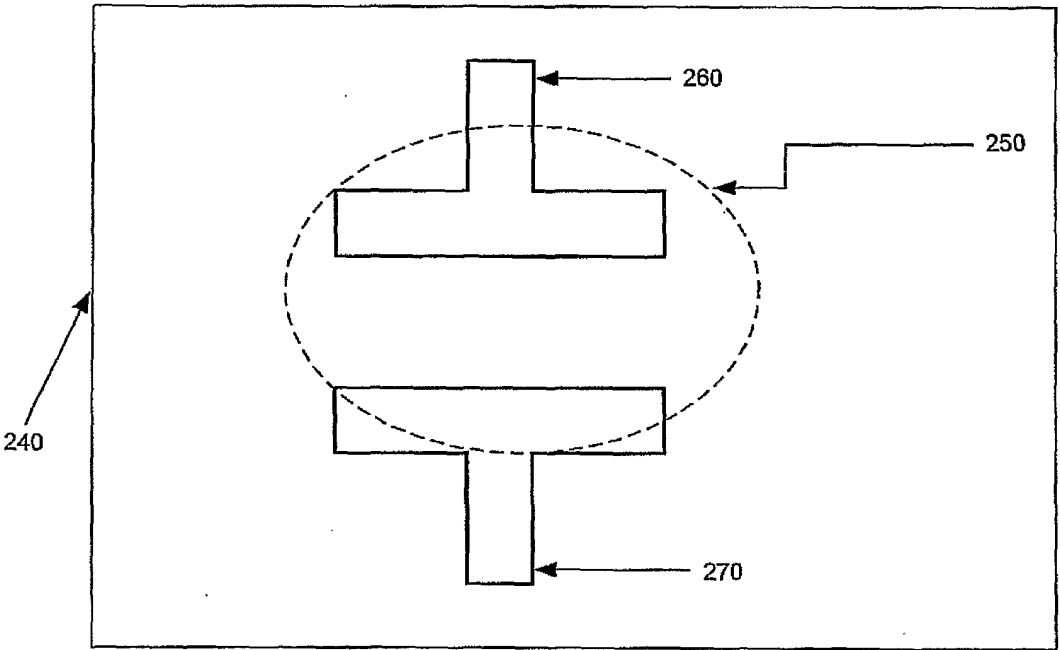


Fig. 4

