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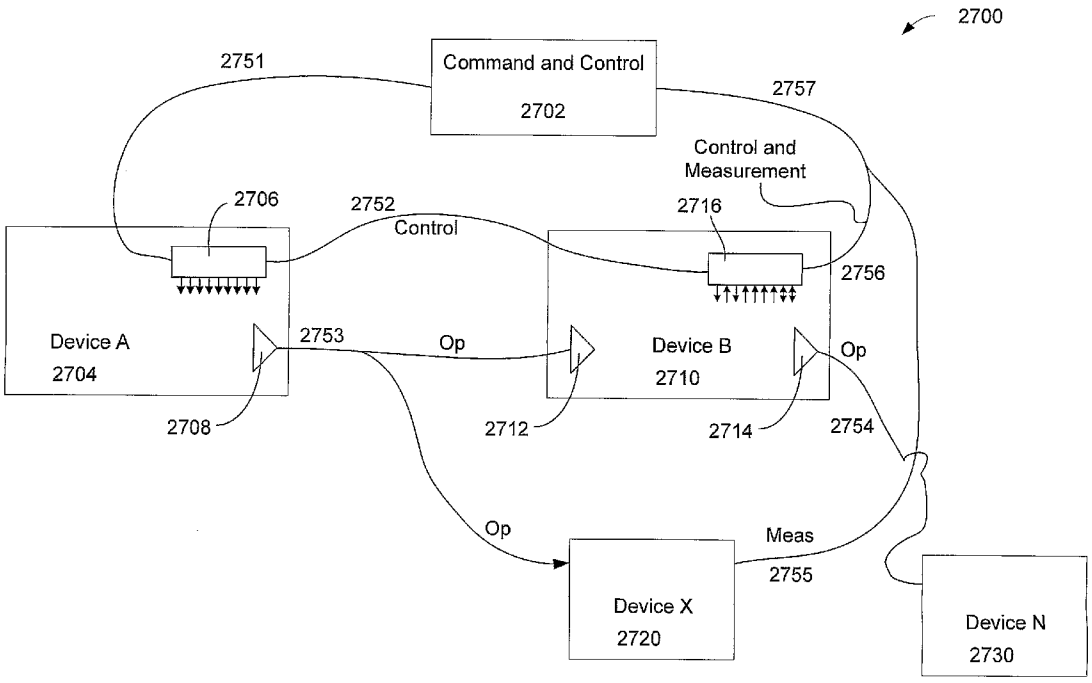
(54) **Title:** METHOD AND APPARATUS FOR PARAMETER ADJUSTMENT, TESTING, AND CONFIGURATION



(57) **Abstract:** A method and apparatus for parameter monitoring, adjustment, testing, and/or configuration of devices have been disclosed.

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Method and Apparatus for Parameter Adjustment, Testing, and Configuration

RELATED APPLICATIONS

[0000] This patent application claims priority of U.S. Provisional Application Serial No. 60/698320 filed 12 July 2005 titled " Method and Apparatus for Parameter Adjustment, Testing, and Configuration ", which is hereby incorporated herein by reference. This application is related to Application Serial No. 11/064038 filed 2/22/2005 titled "In-Situ Monitor Of Process And Device Parameters In Integrated Circuits", which is hereby incorporated herein by reference. This application is related to Application Serial No. 11/142758 filed 5/31/2005 titled "Test Circuits For In Situ Monitor Of Process And Device Parameters In Integrated Circuits", which is hereby incorporated herein by reference.

FIELD OF THE INVENTION

[0001] The present invention pertains to devices. More particularly, the present invention relates to a method and apparatus for parameter adjustment, testing, and configuration of devices.

BACKGROUND OF THE INVENTION

[0002] Devices, particularly electronic devices, are becoming smaller, faster, and generally more difficult to design and debug at the system level.

[0003] Board interconnection testing is possible using JTAG (Joint Test Action Group) if devices have such a capability. Not all devices have such a capability, so this may present a problem.

[0004] Device configuration, such as register reads/writes and in-system memory programming, is possible using JTAG, I2C (Inter-Integrated Circuit), and other serial interfaces. Device configuration, especially through serial interfaces has been troublesome and limited to EPROM or direct processor links for data download.

[0005] Emulation and debug interfaces for processors are possible using JTAG. This may assist in emulation and debugging but has been limited to simple data sourcing and gathering.

[0006] System setup configuration, such as board power on/off, and monitoring (power supply voltage and board/component temperature), is possible via, for example the SMBus (System Management Bus) and/or ACPI (Advanced Configuration and Power Interface). However, these interfaces may not assist in debugging. This may present a problem.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The invention is illustrated by way of example and not limitation in the figures of the accompanying drawings in which:

[0008] Figure 1 illustrates a network environment in which the method and apparatus of the invention may be implemented;

[0009] Figure 2 is a block diagram of a computer system in which some embodiments of the invention may be used;

[0010] Figure 3 describes various embodiments of the invention and a generalized way of describing interconnects;

[0011] Figure 4 illustrates one embodiment of the invention showing a block diagram of an example system;

[0012] Figure 5 illustrates one embodiment of the invention where not all devices have a serial data chain capability;

[0013] Figure 6 illustrates one embodiment of the invention showing an external system that has serial data devices;

[0014] Figure 7 illustrates one embodiment of the invention showing use at a system level for a processor and memory;

[0015] Figure 8 illustrates one example of the processor and memory clock timing for the embodiment shown in Figure 7;

[0016] Figure 9 illustrates one embodiment of the invention showing a SERDES example;

[0017] Figure 10 illustrates one embodiment of the invention for static offset in a PLL;

[0018] Figure 11 shows an example of edge aligned clocks in a single data rate application according to Figure 10;

[0019] Figure 12 illustrates one embodiment of the invention showing a cross point;

[0020] Figure 13 illustrates one embodiment of the invention showing a shifting of a cross point which needs to be corrected to that shown in figure 12;

[0021] Figure 14 illustrates a differential amplifier which in an embodiment of the invention is monitored for cross point information;

[0022] Figure 15, Figure 16, and Figure 17 illustrate waveforms for an embodiment of the invention as shown in Figure 14;

[0023] Figure 18, and Figure 19 illustrate embodiments of the invention relating to on die termination;

[0024] Figure 20 is an embodiment of the invention showing a way to determine if and when ground bounce occurs;

[0025] Figure 21, and Figure 22 illustrate embodiments of the invention showing an example of signal level testing using a serial data chain;

[0026] Figure 23 is a waveform according to Figure 21 and/or Figure 22;

[0027] Figure 24 illustrates one embodiment of the invention for determining VOH maximum;

[0028] Figure 25, and Figure 26 illustrate embodiments of the invention showing variable on die termination examples; and

[0029] Figure 27 illustrates one embodiment of the invention showing operational, control, and measurement communications.

DETAILED DESCRIPTION

[0030] The invention, as exemplified in various embodiments, illustrates device and/or system parameter adjustment, testing, configuration, measurement, monitoring, etc.

[0031] For ease of discussion, the interface used in describing various embodiments of the invention will be described as a serial bus of some type and/or a serial chain. The invention is not so limited and other interfaces, such as a parallel bus, parallel chains, etc. may be used.

[0032] In one embodiment of the invention, serial interfaces are "extended" or "expanded" to allow for:

a) tuning the interaction of components in a system for best performance;

b) modifying the operation of components in a system which may not, by setting fixed values at design time, be guaranteed to interoperate; and

c) monitoring of any change in parameters set in a) or b) above over time, as a way to predict degradation and/or failure.

[0033] In one embodiment of the invention, serial chains may be used to configure and monitor many parameters within devices and systems. The invention in various embodiments addresses many new areas where JTAG and other serial data chain configurations can be used to address specific needs for both configuration and monitoring of parameters within systems and/or devices.

[0034] Since various embodiments of the invention cover a wide range of applications, the discussion has been addressed in four major parts. These are:

1) The device level,

2) Interface level,

3) The system level, and

4) Performance monitoring and trend tracking.

These four categories are for discussion only and are not intended to limit the scope of the invention or applicability in more than one area. Indeed the present invention, in various embodiments, may be used in all the above areas, and at the same time.

[0035] Briefly, the device level is the location where physical interaction takes place. In a device, for example, parameters may be adjusted or monitored, based upon the instructions received in the serial data chain.

[0036] Briefly, the interface level allows interaction outside of a device. While serial data is handled within a device, the device as instructed by the serial data chain may have the capability of interacting with the "interface" to affect and/or monitor device conditions.

[0037] Briefly, the system level allows adjusting and/or monitoring the devices and interfaces within a system and allows system manipulation and monitoring. Through the serial data chains, systems may be made to perform under specially selected operating conditions to allow configuration, testing, measuring, or monitoring in ways that were previously not possible or were difficult.

[0038] Briefly, performance monitoring and trend tracking allows looking at the accumulation of data over time and allows another level of system performance monitoring, trend tracking, failure prediction and analysis, and parameter adjustment as conditions change.

[0039] To assist in the description of the invention, interconnect terminology is used. For simplicity of explanation, devices will be illustrated that are interconnected for main "operation," and interconnected for "control." These operation and control interconnects may be separate physical interconnects or may be a shared resource. For example, assume that two devices, an output buffer and an input receiver are interconnected so that during main operation the input receiver receives the output buffer's signals. This is the main operational interconnect. In addition, the output buffer and input receiver may have a separate control interface which is connected between the output buffer and the input receiver. This control interface may be used to affect the operation of one or more devices. For example, a control signal emanating from the output buffer may indicate when the buffer has entered a high-Z state and based on this the input receiver may disable input stages so that erroneous signals are not received, input devices do not enter linear mode drawing large amounts of power, etc. What is to be appreciated is that the control interconnect can affect the main interconnect operation.

[0040] Figure 3 describes various embodiments of the invention and a generalized way of describing interconnects, for both control and operating signals (for example: data, clock, status indication), between components. Referring to Figure 1, note that the interconnects may be on a board, between boards, via a backplane, via external cable, on-chip interconnects, etc. In one embodiment of the invention as shown in Figure 3, types ii, iii, and iv require devices to be individually selected or addressed by either knowing the interconnect sequence in advance (most applicable to type iv) or by the device having a preset address (for example, by hardwiring pins on a device).

[0041] Referring to Figure 3, the control interconnect may be a serial connection, for example, (ii), (iii) or (iv). In various embodiments of the invention, type (ii) may be an SPI (serial peripheral interface), type (ii) or (iii) may be I2C, SM-BUS, IPMI (PICMG management interface), and type (iv) may be JTAG. What is to be appreciated is that the control interconnect may be implemented in a variety of forms and is not limited to those shown as combinations are also possible.

[0042] Referring to Figure 3, to simplify the operating signal interconnect description, devices connected as (i) or (iv) are considered together as pairs, devices connected as (ii) or (iii) are considered together as master/slave with the leftmost device being the master and all others being slaves. The possible combinations of operating signal and control interconnects are then:

Possible combinations for type (i)/(iv) are:

1) Neither device supports the control interface.
2) Either or both devices support the control interface but do not support the programmability or measurement techniques described below.
3) At least one of the devices supports at least a subset of the programmability or

measurement techniques described below.

4) Both devices support at least a subset of the programmability or measurement techniques described below.

Possible combinations for type (ii)/(iii) are:

1) No device supports the control interface.
2) Only the master device supports the control interface but does not support the programmability or measurement techniques described below.
3) Only some or all of the slave devices support the control interface but do not support the programmability or measurement techniques described below.
4) Only the master device supports at least a subset of the programmability or measurement techniques described below.
5) Only some or all of the slave devices support at least a subset of the programmability or measurement techniques described below.
6) All the devices support at least a subset of the programmability or measurement techniques described below.

[0043] Note that the other types can be made equivalent to these by adding buffer devices whose function provides a serial control interface to some or all of the interconnect signals.

[0044] Some products will fit naturally into some of these types and combinations. For example, clock type products (that distribute a clock signal to multiple "dumb" chips) fit into type (ii) (point to multipoint) with subtype 4 (only the clock chip is "intelligent").

[0045] In one embodiment of the invention, system configuration is possible. The system will contain serial data chains that interconnect devices within the system and allow programming of those devices, monitoring of conditions within those devices, etc.

[0046] Figure 4 illustrates one embodiment of the invention 400 showing a block diagram of an example system where there is a system input 402, system output 404, and several internal devices that are controlled by the serial data chain. For clarification, the serial data chain (representing a control path also called control communication) is shown with dashed lines in the figure, whereas "operational data" also called operational communication is denoted with solid lines.

[0047] In one embodiment of the invention, in a system there will be a serial data controller that generates the serial data chain and receives the serial data back from the system. The controller may be one or more devices, and the serial data returning from the system may be returned to the originating device and/or one or more of the other controllers. In one embodiment of the invention the serial chain configurations may be JTAG, SM Bus, I^2C (I2C), etc. In one embodiment of the invention, the serial chain may be high-speed serial links, operating with or without a serial protocol.

[0048] Figure 5 illustrates one embodiment of the invention 500 where not all devices have a serial data chain capability. For clarification, the serial data chain (representing a control path) is shown with dashed lines in the figure, whereas "operational data" is denoted with solid lines. This is an example of a system with "incompatible" devices. In the figure, one of the devices 506 shown has no serial data chain capability, and therefore there is no connection in the serial data chain. In this configuration, the device with no capability 506 would not be able to receive or send on the serial chain, however, the serial chain can communicate with other devices that have connections to the incompatible device. Through the nearby devices that do have a serial link, information can be communicated to and from the incompatible device. This situation is discussed later.

[0049] Figure 6 illustrates one embodiment of the invention 600 showing how an external system 608 that has serial data devices, but no intelligent controller may communicate with a system that has a controller. For clarification, the serial data chain (representing a control path) is shown with dashed lines in the figure, whereas "operational data" is denoted with solid lines. This illustrates a connection across system boundaries. In one embodiment of the invention, the external system receives and passes serial data to and from an adjoining system, avoiding the need to have any control capability within itself. It would also be possible to perform some type of translation of the serial data before crossing between systems. As an example of this, if the External System were very remote, the serial data could be grouped into a packet of instructions, sent over a data link of any type, the instructions then put into the serial data chain and the remote system would respond to the instructions. The data returned would be gathered and sent back to the originating system over any type of communications link. The originating and destination devices are not necessarily the same. For example, the originating source for the control may come from a first system block, proceed to be communicated to a second system block, which then communicates it to a destination in a third system block.

[0050] Figure 7 illustrates one embodiment of the invention 700 showing use at a system level for a processor and memory. This is an example of type (ii) subtype 4. Referring to the figure, clock generator 709 supplies clocks 711 and 707 (via ports 710, and 708 respectively) to a processor 701 (port 712) and a memory 705 (port 706) which communicate via memory bus 703 (in communication with port 702 on the processor 701 and port 704 on the memory 705). Control processor 714 may be on the same board or not. The control bus 713 is in communication (via port 715) of the controller 714 with the memory 705 (via 717), the processor 701 (via 716), and the clock generator 709 (via 718).

[0051] In one embodiment of the invention, as illustrated in Figure 7, on power-up the processor 701 may or may not (for example, due to timing) be able to communicate with the memory 705, in either case, the timing between the processor 701 and the memory 705 may be adjusted for operation and/or optimization.

[0052] Figure 8 illustrates one example of the processor and memory clock timing for the embodiment shown in Figure 7. The relative phase of clocks 707 and 711 (Figure 7) determines how close to the center of the data the clock is (see Figure 8) at the memory during writing and at the

processor during reading, and hence both whether the memory can be read/written at all, and if so how much margin is left to allow for error free operation in the presence of noise. Note that for some memory types the clock is aligned differently with respect to data for best performance (although within the memory, the relationship of Figure 8 is often desirable). For example, some systems may prefer to be edge aligned.

[0053] In one embodiment of the invention, with reference to Figure 7 and Figure 8, the clock generator (709) is capable of changing the phase relationship between the clocks. Looking at Figure 8, the relative clock phase of clock 707 to clock 711 (Figure 7) is varied from +180 degrees to –180 degrees. This may be by a continuous variation or in discrete steps. Note that if certain characteristics of the system design are known, a lesser range may be chosen, the range mentioned covers any arbitrary design, where no consideration is given to correct data/clock phase at the memory. From power up:

1. The processor (701) is set to execute, using internal code, a write, then read loop using varying data and report the status on interface (716) to control bus (713).
2. The control processor (714) reprograms the clock generator (709), using control bus interface (713) and monitors the status of the read/write operations.
3. When the clock phase has been varied over the chosen range, the control processor determines the window of correct operation and programs the clock generator for the phase, which puts operation in the middle of the window.

Optionally, the operation may be repeated from time to time during normal operation to account for temperature related changes, or other changes. Optionally, the control processor could be in a piece of test equipment, the sequence above taking place one time during factory test and the resulting setup could be stored in non-volatile storage in, or related to, the clock generator 709. For example, on a system board, such parameters as the setup may be stored in a flash memory device.

[0054] Figure 9 illustrates one embodiment of the invention 900 showing a SERDES (serializer/deserializer) example. This SERDES example is a clocking type(ii) subtype 4.

[0055] Referring to Figure 9, clock generator 909 is supplying clock 911 (via interface 910) to SERDES 901 (via 912). Control processor 914 may be on the same board or not. The control bus 913 is in communication with SERDES 901 (via 916), clock generator 909 (via 918), via 915 from the control processor 914. The control bus 913 (from port 915 to port 917) and another clock 907 (from port 908 to port 906) may optionally go to the second SERDES 905. SERDES devices have loopback and error checking capability. SERDES 905 may be on the same board as SERDES 901 or on another board within a piece of equipment.

[0056] In one embodiment of the invention, with reference to Figure 9, on power-up the SERDES devices may or may not be able to communicate with each other via link 903 (ports 902 and 904

respectively on SERDES devices 901 and 905). The technique for optimization is the same for both cases. The clock generator 909 is capable of changing the frequency of clocks 911 and 907. The frequency can be varied over a range wider than the operating range of the SERDES devices. From power up:

1. The SERDES 901 is set to transmit a test pattern and monitor receive data for this pattern, and report the status (correct or incorrect data) on interface 916 to control bus 913. SERDES 905 is set to loopback received data as transmit data. These settings can be achieved by control bus 913, or SERDES 901 can set SERDES 905 using inband control.
2. The control processor 914 reprograms the frequency of clock generator 909 using control bus interface 913 and monitors the status of the read/write operations.
3. When the clock frequency has been varied over the chosen range, the control processor 914 determines the window of correct operation and programs the clock generator 909 for the frequency which puts operation in the middle of the operating window.

Optionally, the optimization operation may be repeated from time to time during normal operation to account for temperature related changes, other changes, etc. Optionally, the control processor could be in a piece of test equipment, the sequence above taking place one time during factory test and the resulting setup could be stored in non-volatile storage in, or related to, the clock generator.

[0057] In another embodiment of the invention, the frequency may be relatively fixed and adjustments such as pre-emphasis, termination, etc. may be adjusted to provide the best general signal integrity. This approach may also be employed before a frequency change is made thus insuring that a "fall-back" frequency is working properly.

[0058] In one embodiment of the invention, parameters of devices may be configured, modified, etc. This is a device level control. For example, most operations accomplished by a serial data chain are originated at the device level. It is the device itself that contains the circuitry to monitor the serial data chain and react to content on the chain. As an example, to operate with a JTAG serial data chain, all devices that will react to the serial data chain need to have a JTAG port. In systems that have devices with serial data chain capabilities, those devices within the system can begin to act together at the interface level, and then at the system level to monitor, adjust, and control the system.

[0059] For example, parameters may be configured and/or monitored. At the device level, the serial scan chain within the device may have control over parameters that influence the system operation and performance. The following list includes many of those device parameters that may be adjusted, monitored, and/or controlled by a serial data chain thus having a system effect. The parameters may be one or more of the following, combinations, or derivatives:

1) Voltage

2) Current

3) Time

4) Temperature

5) Device State

[0060] In one embodiment of the invention, parameters related to voltage are signal levels. This includes the actual voltages of V_{IH}, V_{IL}, V_{OH}, V_{OL} (voltage input high (also VIH), voltage input low (also VIL), voltage output high (also VOH), voltage output low (also VOL) – respectively) when operating, for example, in a steady state condition.

[0061] In one embodiment of the invention, parameters related to voltage are overshoot and undershoot. This includes when an input or output signal moves beyond its final resting voltage. For example, the amount of overshoot/undershoot can be monitored.

[0062] In one embodiment of the invention, parameters related to voltage are Vix and Vox. As differential signal speeds increase, the cross point (or crosspoint) of signals becomes crucial. Vix is the input cross point which could be detected and reported on the serial scan chain. The Vox, which is the differential output signal cross point, could be sensed and adjusted through a serial scan chain. In other embodiments, the Vix and/or Vox may be monitored and/or adjusted.

[0063] In one embodiment of the invention, parameters related to voltage are switching noise. Switching noise is caused by (among other things) multiple bits switching at the same time. It is possible to detect the amount of noise present due to switching and report the information on the serial data chain. Some common names for switching noise are "ground bounce", "simultaneous switching interference", and "inter symbol interference" (denoted GB, SSI, and ISI respectively).

[0064] In one embodiment of the invention, parameters related to voltage are power regulation. Adding a serial data chain to a power regulator may be used to control system turn on, voltage level, power monitoring, etc. For example, if the regulator is of the type that uses an external power device to actually pass the power, contained within many variable regulators is a voltage sense circuit and some form of adjustment mechanism (like an external resistor). If a serial data chain is added to a device of this type, portions of the system power could be under the control of the serial data chain.

[0065] In one embodiment of the invention, parameters related to current may be similar to the ones associated with the parameters for voltage discussed above. Additionally, current limits may be monitored, set, and reported through the use of a serial chain.

[0066] One of skill in the art will appreciate that a combination of parameters is also possible. For example, a voltage current combination.

[0067] In one embodiment of the invention, parameters related to a voltage current combination may be output impedance. A device's output impedance may be modeled as consisting of an R_{OH}, and R_{OL}. Sometimes these are combined to simply be designated as Ro. If there are frequency dependent characteristics to the output, the impedance may be designated as Zo, etc. These parameters and others may be monitored and/or adjusted by, for example, a serial chain in an embodiment of the invention.

[0068] In one embodiment of the invention, parameters related to a voltage current combination may be input impedance. There are a variety of adjustable parameters that can be associated with input impedance. One of these could be some form of On Die Termination (ODT). ODT typically is represented by an R_T and V_T, which may be implemented as described later. These parameters may be monitored and/or adjusted by, for example, a serial chain in an embodiment of the invention.

[0069] In one embodiment of the invention, parameters related to time are clock skew. At low operating speeds a clock driver may need very little skew between the device outputs. As system speeds increase, skew is frequently needed between various parts of the system to compensate for timing differences. Monitoring and/or adjustment of the skew may be achieved in one embodiment of the invention.

[0070] In one embodiment of the invention, parameters related to time are data input deskewing. As bus frequencies increase, the skew between bits on a data bus has become a significant issue. At times, the skew can be so significant, that accurate data capture is not possible with a single clock. Deskewing the bits realigns the data for accurate capture.

[0071] In one embodiment of the invention, parameters related to time are data output deskewing. In some systems, the data becomes skewed as it travels over busses, around corners in traces, and through varying transmission line environments. If the environment is known, it is possible to adjust the skew of the outputs so that all outputs arrive at their destination substantially simultaneously. A corollary to this is to adjust the skew of data destined for different parts of the system so that system timings can be optimized. Additionally, if the environment is not known, for example, a plug-in board may plug into a different chassis, or into different slots in the same chassis, then embodiments of the invention may be used to optimize system timings.

[0072] In one embodiment of the invention, parameters related to time are training. As system speeds increase, training of badly skewed data busses may be necessary so that proper bit alignment can be identified and locked in. The serial data chain can be used to initiate, control, regulate, and stop training.

[0073] In one embodiment of the invention, parameters related to time are edge alignment, for example center aligned. At low speeds center aligned clocking of devices may be needed. As system speeds have increased, edge aligned clocking may be more beneficial. Edge aligned and center aligned devices have difficulty communicating with each other. Some devices such as the fastest DRAMs (dynamic random access memory) today have center aligned input data and edge aligned output data. Whether a device uses center aligned or edge aligned clocking of data is controllable through a serial data chain. Any clock phase between center and edge aligned is also selectable.

[0074] In one embodiment of the invention, parameters related to time are data capture. As system speed increases, there is increased use of phase splitters to accurately capture input data. These often require the use of a PLL (phase locked loop) or DLL (delay locked loop) to perform the capture. The phase splitters or other methods of capture may be under serial data chain control.

[0075] One of skill in the art will appreciate that a derivative of parameters is also possible. For example, a time derivative.

[0076] In one embodiment of the invention, a time derivative is slew rates. A device output slew rate may be monitored and/or adjusted in an embodiment of the invention.

[0077] In one embodiment of the invention, a time derivative is preemphasis. It is often necessary for some signals to achieve higher voltage levels initially, with reduced levels later (or with subsequent bits at the same logic level). Often the goal is to achieve an adequate slew rate to insure timing and switching, and then reduced power. The reduced voltage later also helps to ease the initiation of a subsequent transition to the opposite state. Some of the items that the serial data chain may adjust include the presence of preemphasis, the amount of preemphasis, and the strength of the "post-emphasis" signal. Pre-emphasis is an amplification of high frequency components and/or a reduction of lower frequency components to counteract the frequency dependent loss of a medium.

[0078] In one embodiment of the invention, a time derivative is phase offset. The phase offset of a PLL or DLL can be adjusted in one embodiment of the invention by using, for example, a serial data chain.

[0079] In one embodiment of the invention, a time derivative is frequency detection. An external clock signal may be compared against a known clock. The differences between the two may be compared, allowing a reporting of the actual frequency, or detecting a good or bad clock. Note that the frequencies need not be in the same range, for example, in one embodiment of the invention a 10MHz signal may be compared to a 1MHz signal by dividing by it by 10 before the comparison. In another embodiment the clock compared against may be the serial control clock. In yet another embodiment of the invention, the frequencies may be not related in any manner, yet detection that the clocks have not gone bad may be achieved by, for example, feeding one clock input into the set input and the other clock into the reset input on a flip-flop and observing if the flip-flop output changes state.

[0080] In one embodiment of the invention, parameters may be related to temperature. For example, it may be important to monitor temperatures on different chips or even sections of a chip. This may be an early indicator of a problem, such as a circuit malfunction, a system level issue, such as a fan problem, a reliability issue, etc. Temperature may be monitored by a variety of mechanisms, such as, but not limited to, shift in thresholds, changes in resistance, diode drops, oscillator frequency change, etc.

[0081] In one embodiment of the invention, a derivative of temperature is a rate of change in temperature. For example, a rapid increase in the temperature of a chip or system may be an early indication of impending failure. In one embodiment of the invention, this may be monitored and under control actions may be taken, for example, shutting down a system power supply if a device becomes too hot for reliable operation.

[0082] In one embodiment of the invention, parameters related to device state are internal state machine status. For state machine controlled devices monitoring the state for correct operation (not stalled or in an invalid state) is possible in one embodiment of the invention.

[0083] In one embodiment of the invention, parameters related to device state are status. A representation of a device's internal status can be made available. This would allow detection of fault states or states incompatible with connected devices.

[0084] One of skill in the art will appreciate that the examples above are but a sampling of parameters that may be monitored and/or controlled. The discussion that follows describes some of the approaches for embodiments of the invention that control and/or monitor parameters.

[0085] Clock skew as discussed above may involve input clock and phase splitter operations, output clock and shifting of the clock, edge alignment, center alignment, etc. Some systems are edge aligned, some are centered aligned. In one embodiment of the invention, one part can do both types of alignment, or any range of alignment (+/-180 degrees shift).

[0086] In one embodiment of the invention, a serial data chain is used to affect static phase offset. In PLL and DLL devices, there is a need to "lock" the output signal to the input signal. A block diagram of a PLL is shown in Figure 10. The "goal" of the PLL in an application is to "Lock" the output signal to the input signal so there is no phase difference between the two. Within the PLL block diagram is a "Phase Detector" that will compare the feedback signal it is receiving from the output of the PLL with the input signal to the PLL. If the two are identical or at "spec", it will make no changes to the output frequency of the PLL. If the two are different than a designated amount, the Phase detector will adjust the output frequency very slightly to start moving the phase towards the desired offset. In some applications, it is desirable that the output of the PLL be slightly ahead of, or behind, the Input. In other words, it is necessary to adjust the static phase offset of the PLL to something other than zero. Possible applications of this are high speed clocking situations where a designer wants to better align the clock with data.

[0087] An example of this is the use of edge aligned clocks to avoid skew between the clock and data in high speed applications. The receiver of the clock and data must then capture the data using a clock that is not properly positioned for a traditional clock/data relationship.

[0088] Figure 11 shows an example of edge aligned clocks in a single data rate application. The clock edge is very closely aligned with the data in the example. To accurately clock the data into a register, the clock must be shifted as shown in the bottom waveform in the figure. The "internal" clock is positioned to accurately capture the center of the data and accurately determine the high or low state of the data. One of skill in the art will appreciate that the internal clock, whose edges are being aligned to data, is not visible to any tester, and is different from the external clock.

[0089] In one embodiment of the invention, as shown in Figure 10, the shifting of the clock is accomplished through a serial data chain 1002. The chain 1002 is in communication with a control function 1004. There are two possible ways to accomplish this shifting. The first is to adjust the phase

detector of the PLL to perform a shift in the static phase offset of the signal via control signal 1006. The other way to accomplish this would be to lock the static phase offset at zero and shift the output signals (except for the one used for feedback) of the PLL by a programmed amount via control signal 1008. Both of these techniques may be accomplished by means of the serial data chain and may be used individually or combined.

[0090] In one embodiment of the invention, the cross point as illustrated in Figure 12 is monitored and/or adjusted. Figure 12 also indicates an ideal cross point for signaling.

[0091] As clocking speeds increase and signal integrity becomes of paramount importance in high speed signal lines, the crossing point of differential signals (Vox and Vix) becomes a significant factor as shown in Figure 12. Input receivers are designed to toggle within a designated range of voltage crossing. If the crossing point is not observed, several things can happen, among them:

1) The input structures of the receiver may not properly sense whether the signal is high or low (e.g. outside operational range of a differential amplifier).
2) The receiver may receive jitter on the input signal.
3) The receiver response time may be affected

[0092] If signals become distorted, it is possible the crossing point has shifted to a less desirable position as shown in Figure 13. In this figure, either the rising and/or falling edge have been shifted, causing uncertainty. There are many possible causes of this skew between the signals. In one embodiment of the invention, it is possible to measure the skew between the differential inputs and report the results on the serial data channel.

[0093] Figure 14 illustrates a differential amplifier, which in an embodiment of the invention is monitored for cross point information. There are several possible ways to measure the input cross point and report the result back on the serial data chain, for example, the input differential amplifier can be observed. The current source 1402 at the bottom of the amplifier attempts to keep a continuous current flowing through the differential amplifier, regardless of input levels. When Input is high and Input* (Input bar) is low, all of the current flows down the left side of the differential amplifier. When the two signals reverse direction entirely, all of the current flows down the right side of the differential amplifier.

[0094] During the transition where the two input signals (Input and Input*) are making the transition, if the current source 1402 maintains current, and the input FETs (field effect transistors) can actively make the exchange from one side to the other, there should be little disruption in the voltage level 1404 at the current source 1402 as the current switches from one side to the other as shown in Figure 15. This is an ideal cross point crossing and causes little voltage disruption which is sensed in one embodiment of the invention 1500.

[0095] If the crosspoint is not observed, and one side makes a transition before the other, measurable anomalies develop in the voltage at the current source, and if the crosspoints go to the extreme, the current from the current source 1402 will not be maintained. For example, if both sides of

the input go temporarily low, both sides of the differential amplifier will shut off, causing the current source 1402 to hit its lower voltage (at 1404) limit (sucking all of the available current) as shown in Figure 16. This is a cross point crossing low in the differential amplifier and this voltage disruption is sensed in one embodiment of the invention 1600.

[0096] If both sides of the differential amplifier turn on as shown in Figure 17, the current source 1402 will reach a higher voltage level (at 1404) than a normal transition with the cross point in the middle. This is a cross point crossing high in the differential amplifier and this voltage disruption is sensed in one embodiment of the invention 1700.

[0097] If the crosspoint is somewhere other than at the ideal, but not at the limits, the voltage effects will still be present, but reduced in size. These characteristics may be accumulated and reported on the serial data chain in an embodiment of the invention.

[0098] In one embodiment of the invention on die termination may be monitored and/or adjusted. In applications where On Die Termination (ODT) is used, it is possible to configure the ODT using the serial data stream. Figure 18 shows one embodiment of an ODT configuration. It consists of an input to a device that is high impedance. In addition, there is termination resistor (R_T) tied to a termination voltage (V_T). The termination resistance may be equal to the line impedance, or slightly different. Most interfaces use a V_T that is at the mid point between the power supply and GND (ground). There are variances on this configuration (e.g. GTL - Gunning Transceiver Logic), but the concept is the same.

[0099] Given that Figure 18 is the idealized situation, real applications usually have difficulty providing a true V_T at the mid voltage between the supply rails. The V_T requires the addition of an additional voltage supply to the component, or an internal voltage generation that consumes power and a significant amount of circuitry. One solution is the use of the Thevenin equivalent circuit shown in Figure 19. In the figure, V_T has been replaced by a resistive divider between V_{DDQ} and GND. If R_{IH} and R_{IL} are matched, and their parallel value is equivalent to R_T, Figure 18 and Figure 19 are electrically identical.

[00100] One embodiment of the invention, as shown in the circuit of Figure 19, allows the adjustment of R_{IH} and R_{IL} thus allowing the user to balance the input and tune the circuit to the received input signal. In many cases these adjustments can tune out overshoot and undershoot, or improve rise and fall times of the signal. Additionally, an off-center signal can be slightly pulled higher or lower by adjusting the values of R_{IH} and R_{IL}. This has the Thevenin effect of changing the values of V_T and R_T in Figure 18. The values of R_{IH} and R_{IL} can be set using the Serial Data Chain in an embodiment of the invention. This means the serial scan chain has the capability of setting the Thevenin values of R_T and V_T anywhere within operational limits of the circuit. This allows the serial data chain to have complete control over the receiver termination characteristics.

[00101] In one embodiment of the invention device output slew rates may be monitored and/or adjusted. Device output slew rates are one of the primary causes of transmission line troubles within a

system. If the slew rate is too slow, the signal speed also slows down and the actual positioning of the signal edge is less precise, causing poor system performance. If the slew rate is too fast, transmission line and switching noise develop, causing poor signal quality and other problems.

[00102] In one embodiment of the invention, the device slew rate may be adjusted and set to a single value through the use of a serial data chain. In another embodiment of the invention, the device slew rate may be adjusted by setting the number of, and timing sequence of, transistors used to drive the output stage. In another embodiment the slew rate may be adjusted through the serial data chain depending upon the status of the transition. Some possibilities are:

1) Driving hard at the start of the transition to initiate a fast slew rate, then reducing the drive as the transition progresses, to avoid overshooting and/or undershooting.

2) Reducing the initial drive, to avoid a fast slew rate, then adding drive strength as the signal progresses to insure sufficient drive to complete the transition and overdrive heavy termination.

In these and other applications, it is possible to set the drive characteristics through the serial data chain, to optimize the slew rate for the interface and make adjustments if the needed. One mechanism for doing this is to control the number of fingers or transistors driving the output. Another possibility is to time the sequence during which the output transistors will turn on (staging) to optimize the slew rate.

[00103] In one embodiment of the invention device switching noise may be monitored and/or adjusted. Switching noise may be caused by multiple bits switching in tandem, or by varying the number of bits switching, etc. The switching causes a surge of current through the ground or power structure of the device, creating a voltage difference between the internal and external supply or ground. In the circuit in Figure 20, an impedance (Z) is shown between the internal and external GND level. If a large surge of current passes through this impedance, the internal and external GND levels would be different. Some common names for switching noise are "ground bounce", "simultaneous switching interference", and "inter symbol interference" (denoted GB, and SSI respectively).

[00104] In one embodiment of the invention, it is possible to detect the amount of actual noise caused by the switching and to report this information on the serial data chain. The information can be used to identify switching conditions, which may cause device upset or poor output signal quality. Knowing the amount of switching noise may give insight into failure causes or conditions.

[00105] Figure 20 is an embodiment of the invention showing a way to check ground bounce (one form of switching noise). The circuit consists of a differential amplifier tied to V_{REF} externally. Most interfaces have some form of reference voltage that is externally supplied and kept as noise free as possible. If there is no V_{REF}, the V_{REF} could be any externally supplied, quiet voltage that is approximately ½ V_{DDQ}. Under noise free conditions, the internal capacitor shown will charge to the

V_{REF} voltage level and remain there. The signal shown as "Noise Detection" will remain at a constant level.

[00106] In the event that the internal and external GND levels should suddenly become different, most notably if a surge of current flows through the impedance in the ground, Z, due to switching noise, the capacitor shown will force the voltage across the differential amplifier to change and a signal will be generated on the "Noise Detection" output. This signal may be monitored by the serial data chain and report noise levels back to a controller.

[00107] While Figure 20 is only for Ground Bounce, one of skill in the art will appreciate that a similar circuit may be developed with the capacitance tied to V_{DDQ} to detect bounce in the upper voltage. In effect, the noise level on any internal voltage relative to an external voltage may be monitored by the serial data chain in various embodiments of the invention.

[00108] In one embodiment of the invention interface level considerations may be monitored and/or adjusted. At the interface level, things become more interesting. While the building blocks remain at the device level, these building blocks may be used to analyze the interface to monitor and/or adjust the interface for optimum performance.

[00109] In one embodiment of the invention, not all devices will have serial data capability. Most devices within a system will not have a serial data capability, especially before a large number of devices are available in the market. In the meantime there will be various levels to the amount of control that can be achieved through a serial data chain.

[00110] Any device that has a serial data chain (as shown by various embodiments of the present invention) has the capability of controlling or sensing any parameters within itself or in contact with its interfaces as provided those capabilities are built into the device. When two devices with full capability share an interface, it is possible for the two devices to both monitor the interface, adjust the interface, and to test the interface by interacting with the other device to verify the successful achievement of all tests.

[00111] In the event that only one device on an interface has a serial data chain, the situation becomes more difficult, but it is still possible to achieve a successful testing or configuration of the interface. As an example of one embodiment, if the non-compliant device (i.e. having no embodiments of the present invention) is a bus driver, and the compliant device (i.e. implementing one or more embodiments of the present invention) is a receiver, the receiver could sense the characteristics of the driver, report those to the controller, and the controller could make adjustments to the receiver to optimize receipt of the data.

[00112] As an example of the reverse, where the controlled device is the driver and the non-compliant device is the receiver, the controlled device could adjust to optimize the signal integrity, either by monitoring its own output, or by allowing the controller to dictate conditions, based upon the known bus environment.

[00113] In the event that there are two non-compatible devices sitting on an interface, but there are devices with serial data chains sitting around them, the serial data chains could be used to force certain conditions into the non-compatible device, and observations could be made concerning the emergence of correct or incorrect information from those devices.

[00114] When dealing with interfaces between devices that have serial data chains, and those that don't, some of the capability is lost, but the capabilities that remain are very usable. The following scenarios exist:

1) Ideal – All devices have serial data chains. All devices are configurable. All devices have appropriate monitoring capabilities. A complete analysis and configuration can be done on the interface.

2) Good – Some devices have serial data chains, but some do not or their data capability is limited. In this scenario, the complaint devices can adjust their parameters and monitor their interfaces in accordance with their capabilities, but some capabilities may be missed due to a lack of access.

3) Possibly Useful – Most devices do not have serial data capabilities. The configurable (compliant) devices that exist can monitor and adjust their parameters as needed, but their visibility into the system and their ability to control the system is limited. Interfaces that have no contact with a serial device must rely upon the flow of data to pass information. Problems that develop may be isolated to a region, but probably not to a specific device, bit, or interface.

[00115] In various embodiment of the invention, these are some of the parameters that can be configured and/or monitored at the Interface level:

1) Data alignment.

2) Transmission line

3) Overshoot

4) Termination scheme

[00116] With respect to transmission line configuration, in one embodiment of the invention with a serial data chain, it is possible to completely analyze the configuration of a transmission line, and report to the user/controller through the serial data chain. Some of these items are:

1) Output impedance of the driver

2) Termination impedance at the receiver

   a. Is the termination balanced

   b. The Thevenin VT

3) The VOH and VIH

4) The VOL and VIL

5) The amount of overshoot and undershoot for both high and low

a. Input overshoot

b. Output overshoot

[00117] Figure 21 illustrates on embodiment of the invention showing an example of signal level testing using a serial data chain. Figure 21 shows an example of how serial data can be routed to an input structure to allow testing of the signal lines associated with that input. In the example, a user could actively test the design as shown and verify connections and signal levels.

[00118] Generally, the values of Ro, R_T, VREF and V_{TT} will be set for optimum performance over signal line Zo. As a simplified example, the following signal levels could be set.

$Ro = 50\Omega$

$R_T = 50\Omega$

$V_{TT} = V_{DDQ}/2$

V_{REF} = Don't care (not used in the test)

[00119] In this example configuration, the output driver could be driven low (by either serial control or other means). The driver will pull the transmission line low and eventually settle into a voltage divider circuit between V_{TT} and GND. With the example values, the voltage between Ro and R_T should eventually settle at ½ of V_{TT} or $V_{DDQ}/4$. Different values for the parameters will produce different voltage levels on the input to the receiver (so calculations may need to be done).

[00120] Once in this configuration, the serial data chain could load data into the DAC, the input Vref bypassed with the mux and the voltage level varied under serial control. Using this technique, the exact trip point for the receiver input could be determined, allowing a determination of several transmission line characteristics. In one embodiment of the invention some form of current limiting may be utilized in the input structure as the two input signals approach each other.

[00121] Using the serial data chain several items of merit on the transmission line could be tested. Examples are:

1) As shown the V_{OL} could be tested
2) Reversing the output voltage of the driver from a low to a high could test the V_{OH}.
3) If the output driver is turned off entirely, the level of V_{TT} could be verified.
4) If either Ro or R_T is fixed and known, the value of the other could be verified.
5) If Ro is variable, it could be verified as functional and the accuracy tested.
6) If R_T is variable (e.g. On die), it could be verified as functional and the accuracy tested.
7) Differences between the signal high and signal low values of the all of the parameters could be tested.

[00122] Taking this idea a bit further, one of skill in the art will appreciate that various embodiments of the invention can come up with additional uses for circuits of this type. Figure 22 shows an example of how a trip point can be set by utilizing a serial device to load a DAC to establish a limit voltage. If the circuit in the figure operates normally with high speed data traveling down the transmission line, the voltage on the DAC could be set to a maximum signal level. If the signal should

exceed this value, it would cause the register to toggle. This could be picked up on the serial data line and the fact that a trip point was exceeded sent back to the controller. This technique may be used to check overshoot and undershoot within the operating range between Vddq and GND. Checking for overshoot and undershoot beyond Vddq and GND may also be accomplished by other means, including charge pumps, floating gates that would toggle if the voltage exceeds set points, etc. These conditions could be reported back immediately or may be stored on-chip and reported back later. The on-chip storage may be volatile or non-volatile.

[00123] For example, if a device senses that it is operating outside of established operation ranges, it could store this in a non-volatile memory that may be retrieved at a later time.

[00124] As an example of how the circuit of Figure 22 may be used to test an actual signal, Figure 23 shows an example logic transition from a low to a high. If the V_{OH} signal level is nominally set to reside at the point shown, a user may wish to know how much beyond V_{OH} the signal level is traveling as overshoot. Through the serial chain, a user could check the value of the overshoot and report back through the serial chain the value discovered. One method of doing that is as shown, where the user would set a trip point for the maximum value. If that value is exceeded the observation would be caught in a register and returned through the serial chain.

[00125] In one embodiment of the invention, another method of verifying overshoots would be to utilize an ADC (analog to digital converter) as shown in Figure 24. This technique captures the peak of the overshoot and returns it to the serial data chain. In the example, the input signal is buffered as it enters the device so that the signal will not affect the actual external signal, but the voltage is retained. The voltage flows through the diode and charges the capacitor. If the capacitor is small, and the diode has a low voltage drop across it, the voltage on the capacitor will indicate the maximum voltage on the signal. As the signal continues and drops in voltage the maximum value is retained by the capacitor and the reverse biased diode, and can be sampled by the ADC and sent back to the serial data controller.

[00126] While the example in Figure 24 was for a V_{OH} maximum measurement, the V_{OL} may also be checked by reversing the polarity of the diode. The capacitor in both circuits would need to be reset (voltage returned toward the Vref) to initiate a new test. Placing a high value resistor across the capacitor would allow the capacitor voltage to decay, allowing future measurements based upon only recent voltage excursions and aging past excursions. Errors caused by the drop across the diode can be calibrated out of the measurement. One method would be to simply adjust the reading of the ADC. The capacitor should be large enough to hold the voltage until the ADC can make a reading, yet as small as possible to reduce measurement impact and to allow fast data capture.

[00127] In one embodiment of the invention, monitoring and/or adjustment of the ODT at the interface level is possible. Using the serial data chain interface to control the ODT characteristics as discussed earlier, it is possible to adapt ODT to the interface environment and adjust for device location within the circuit.

[00128] One of skill in the art will appreciate, that expanding upon the programming concept, it may be beneficial to turn off the ODT termination. An example of when this would be necessary is if the device is in the center of a string of devices. It would be best for circuit operation if the device at the end of the string of devices had ODT active (on), but all other devices in the string had no ODT (ODT off) to prevent signal distortion and excessive loading of the line.

[00129] Figure 25 shows one embodiment of the invention with a device with ODT and a couple of switches that could be controlled by the Serial Data Chain to allow completely shutting off the ODT. The switches may be contained within the R_{IL} and R_{IH} of the input termination.

[00130] Figure 26 demonstrates how, in one embodiment of the invention, this concept may be used to control the ODT on a multidrop transmission line. On the left is the transmission line driver. Devices along the transmission line all have the ODT turned off, except the last device in the chain, which will provide the correct termination for the transmission line.

[00131] By adjusting or turning ODT on and off with the serial data chain, all devices within the chain could be identical products with ODT, and adjusted after they are in a system. An added advantage is that the system configuration can change easily and the termination scheme can self adapt to the new configuration, without needing to have a new system layout or design generated. For instance, in Figure 26, if the receiver on the far right were to become disconnected, the second to the last receiver would be required to adapt its termination scheme to reduce transmission line noise.

[00132] In one embodiment of the invention, the serial data chain may be used to adjust the ODT to reverse the bus. An additional item that may be configurable using a serial data chain would be the ability to reverse the direction flow of the bus and change the termination scheme. While the serial chain itself (depending upon the speed) may not be fast enough to reconfigure the bus every time a bi-directional bus changed directions, the rules for making the change could be loaded (via the serial data chain) into each device and each device would respond properly to the change in direction. For example, if the device at the far end of the bus suddenly becomes the driver, it would turn off its ODT and drive the bus. Intermediate devices on the bus would keep ODT off regardless of who is driving. If the driver in Figure 26 suddenly stopped acting as the driver, it could turn on ODT to terminate the transmission line in the other direction. Thus, serial data chains could be used to configure each device for its location on the bus.

[00133] In one embodiment of the invention, system level observations, monitoring, and/or adjustments may be made. For example, as system speeds increase, tuning and adjustment of the system to achieve optimum performance is becoming more beneficial. It is also becoming increasingly beneficial to predict the required adjustments to guarantee operation when the system is powered on. Temperature, voltages, and other environmental conditions may affect a system to the point that operation is not possible until real time adjustments are made.

[00134] In one embodiment of the invention, power-up configuration of a system is possible. Using a serial data chain approach, the serial data operates at a speed and under conditions that should

be operational, even when the system itself is not operational. By utilizing the serial data chains, the system can start diagnostics and proceed with the task of configuring all of the interfaces (internal and external) for maximum performance. Once fully configured, the system should be operational under any circumstances.

[00135] By doing a "power-up" configuration of this type, the devices in the system can have a level of adjustability that would not be permissible otherwise. If a device must be built and hardwired to work correctly every time it is inserted into a system, regardless of the configuration or conditions within that system, the device is restricted to a very narrow range of predictable performance characteristics that are adapted to the "average" application. If an application is not "average" or if conditions dynamically change within the application, the "average" device may not work, or may not work at peak performance.

[00136] If devices with serial data chains are built to allow adjustments throughout the "normal" range, and possibly into the "extreme", when an "extreme" or unusual application appears, the adjustments can be made at the system level, either at startup or continuously if conditions are changing.

[00137] In one embodiment of the invention, tuning and adjustment of a system is possible. It is rare that conditions will remain constant within systems during normal operation. Temperatures change, usage levels change, voltages change, and configurations change. Powering a system on causes the system to start from a "cold" situation and eventually change to "hot" as time progresses, system usage increases, and maybe external temperatures increase. The only way to maintain optimum performance under changing conditions is to allow adjustment of the system parameters as conditions change. Using a serial data chain to configure devices allows for automatic monitoring of the parameters and adjustments as the need arises.

[00138] In one embodiment of the invention, assistance with the design of a system is possible. When designing a new system, usually extensive simulations are done and the designs are tweaked based upon the simulations. The simulations must include all operational conditions, and must very accurately predict the device and system performance to guarantee operation. The design becomes very difficult when devices do not exactly match the application needs. Special problems arise when variable conditions are part of the design and only fixed device parameters are available.

[00139] Using a serial data chain to configure the devices, allows a far greater flexibility in the system design, so that the constraints the designer must place on system parameters are less restrictive. If the system after it is built, can provide a wide range of automatic adjustability, the design limitations become less restrictive, and possibly these can be converted to performance improvements and/or reduced costs.

[00140] System designs also struggle with unknowns. Until a system is built and operating in its intended final environment, it is difficult to realize and include all of the factors that may affect final operational characteristics. If a system has the capability of self-tuning and adjusting of the actual

interface parameters by using the serial data chains, unpredicted anomalies can be tuned out of the system. Components that have no serial data chain would be fixed, or require some other form of adjustment.

[00141] Ideally, within a system, the single available component for the application could be inserted, and then adjusted upon power up to correct for the operating environment. The ideal characteristics could be sensed, and then both the drivers and receivers could be adjusted to optimize for the existing conditions. As conditions change, so would the adjustments.

[00142] In one embodiment of the invention, monitoring the reliability of a system is possible. For example, a security system built using serial data chain devices (i.e. embodiments of the present invention) and intended to work in a heavily air-conditioned environment could be configured during power up for optimal performance. In the rare event the air-conditioning breaks down the importance of maintaining the security system increases, as workers must exit the area. The increasing heat could have a profound effect on the system performance, causing a shifting of parameters throughout the system.

[00143] The serial data chain could be configured to automatically monitor parameters within the system and make adjustments as parameters drift. By constantly adjusting to the changing environment, operation can be guaranteed or extended beyond what a fixed design would provide. If instead, the system was allowed to drift beyond parameter limits, system failure, or false reporting of data would be possible. In this situation, the serial data chain may report this to give an early indication that system failure was eminent. In either case, information from the serial data chain could be sent out to a remote monitoring site, to allow a tracking of conditions within the system.

[00144] In one embodiment of the invention, effective environmental testing of a system is possible. Most well designed systems need to go through some form of environmental testing during the product development phase. This usually includes operation under hot, cold, vibrating, or shock (drop) conditions. The environmental tests tend to point out marginal conditions or early failure points within systems that are otherwise working. In these harsh conditions, applying the test equipment necessary to monitor all of the conditions needed is almost impossible. Usually these tests rely upon some gross system failure to point out that there was a failure, and then examination may pinpoint the reason for the failure. Exacerbating the situation is the bulky test equipment with limited numbers of probes and limited data gathering potential. Sustaining a harsh environmental condition with bulky test equipment attached is troublesome at best. As always, attaching test equipment to a device affects the device performance. Frequently, the effects of the test equipment completely disguise the actual operating conditions.

[00145] Using the serial scan chain (as described in the present invention) gives complete access to all points in the system controlled by the scan chain. The scan chain is designed into the system, and therefore has no parasitic effect beyond the normal system configuration. Scope-probes, signal analyzers, and other bulky test equipment are not needed. Using a serial scan chain for environmental

testing requires only that some form of access to the scan chain be allowed. In some applications, it is possible that the entire scan chain control is within the system, meaning the entire system can be inserted into the environmental chamber without extra bulky attachments. It may be possible for the system to self-monitor, adjust, and either store the information for later retrieval (such as in a non-volatile memory), or report conditions through some external mechanism. Using the serial scan chain in this way will allow monitoring of conditions and viewing of drift or failures as they develop. The adjustment limits can be tested. True operation in a vibrating environment can be observed without concern about shaking bulky probes in the process.

[00146] In one embodiment of the invention, failure analysis of a system is possible. Failure analysis is troublesome, especially when being done in the field, or at a customer site. Using a serial scan chain, data can be gathered from all locations within the system and then the problems isolated. Having the actual data from the sensing locations would provide material for failure analysis that is not available by any external probing technique. The failure mechanism would not be affected by the testing method. If multiple systems are failing, a commonality of failures can be researched using the serial data. Failure analysis may be done in real time for one or more systems or may be done off-line in a statistical approach. Norms of operation and failure may be monitored and predicted based on aggregated information from the field, operating unit, as well as input from manufacturers. For example, life testing of devices may yield an early life failure indicator.

[00147] In one embodiment of the invention, inter-system failure analysis of a system is possible. Particularly troublesome is a failure that develops at a customer site between vendors. In this scenario both vendors had fully operational systems when tested alone, or in their own labs. When systems are interconnected, frequently in front of a customer, failures are common. A finger pointing exercise frequently follows. If there is a serial data chain present, the system with the serial data chain could both analyze the failure, and possibly make adjustments to adapt to the previously unseen conditions, eliminating the failure. Regardless, the serial data chain should be able to identify conditions on the interface and report those conditions, allowing the user insight into potential problems and which side of the interface is at fault.

[00148] In one embodiment of the invention, performance monitoring and trend tracking is possible. Using the serial data chains, it is possible to continuously monitor system performance and parameters within the system. By monitoring the internal conditions, it should be possible to identify patterns that develop under all operating conditions. In the event of a failure, the operating conditions should be accessible and provide insight into the problem, especially in the case of random occurrences that otherwise can not be monitored. In systems that have a finite lifetime, trend tracking will give insight into "time to failure" or "remaining life". This could be used as a predictive failure mechanism so that repairs or replacement can be done when convenient, rather than in an emergency situation. Some possible applications would allow customers to perform routine maintenance, and report analysis back to the factory. The factory link could be direct from system to factory in applications where

security is not an issue. The factory could monitor failure prone areas, and perform corrective action before any failure.

[00149] One of skill in the art will appreciate that the present invention may be practiced at the lowest circuit level, at chip level, at board level, system level, and at a network level. What is to be appreciated is the ability of the present invention to be used to configure and/or optimize the operation of components, circuits, chips, boards, systems, and networks depending upon where it is deployed.

[00150] For example, embodiments of the invention may be used to adjust circuit performance of individual devices (via parameter adjustment, testing, and configuration of the devices). At the chip level, embodiments of the invention may be used to adjust, for example, drive levels, skew, etc. between blocks of circuitry on an IC. At the board level, embodiments as described above may be used to adjust operation between devices on a circuit board. Also discussed above were embodiments of the invention being used at the system level. One of skill in the art will appreciate that networks of such embodiments may also be deployed.

[00151] For the sake of discussion numerous embodiments of the present invention have been illustrated and discussed using a serial interface and/or a dedicated interface or control bus. The invention is not so limited. For example, the present invention may be practiced without the use of a dedicated control bus whether it be serial, parallel, or a combination. For example an existing data bus may be used. For example, referring to Figure 7, block 701 may represent a microprocessor communicating via a data and address port 702 over communication lines 703 with a memory interface port 704 of a memory 705. Further to this scenario, the microprocessor 701 and the memory 705 in one embodiment of the invention may decide to adjust how the data and address lines are driven as well as the input circuitry used to receive such so as to optimize performance. In one embodiment, the microprocessor may communicate via 703 a command to enter an "adjustment" mode of operation. For example, for sake of discussion assume that within 703 the data bus is composed of 32 lines of communication. In one embodiment of the invention the microprocessor 701 may want to adjust the output drive level of the 32 data lines to the memory 705 for optimum performance. In one embodiment of the invention this may be done by having the microprocessor 701 adjust the output drive level of 16 lines while the memory 705 may be reporting back to the microprocessor the status of optimization on the 16 other lines. In similar fashion the remaining 16 lines may be adjusted.

[00152] One of skill in the art will appreciate that the output of the memory 705 going to the microprocessor 701 may also benefit from optimization and the technique discussed above may be used to achieve this.

[00153] Additionally, not only the outputs but inputs as well may be optimized using various embodiments of the invention.

[00154] One of skill in the art will appreciate that other device and interfaces other than the microprocessor to memory interface above may be used as well. For example, in other embodiments I/O buses such as high-speed serial interfaces (Firewire, USB, SATA, Ethernet, etc), as well as parallel

buses (backplanes, ATA, SCSI, etc.) may be used for parameter adjustment, testing, and configuration of devices

[00155] What is to be appreciated is that by using the techniques described in the present invention, for example, the concept of using a serial data control chain, a parallel data chain control chain, or an existing bus or lines as a control chain, or any combination of these as a control to monitor low level device parameters, adjust interfaces, predict failures, and perform the functions described, gives a new functional capability at device, system, and performance levels. As interface speeds increase, it becomes impossible for a single device with a set interface to adapt to all possible applications at all speeds. Allowing the device to monitor the interface and adapt, will allow a significant boost to interface speed, reliability, and testability.

[00156] Figure 27 illustrates one embodiment of the invention 2700 showing operational, control, and measurement communications. At 2702 is a command and control block which is capable of sending and receiving communications via links 2751 and 2757. Device A 2704 is in communication with command and control 2702 via link 2751. As shown here Device A 2704 has a local control 2706 which has outputs only (arrows emanating out of block 2706) which may control aspects of Device A 2704, for example an output driver 2708. That is, Device A 2704 is a device which can received control commands and is in control communication with 2702 via link 2751. Exiting Device A the control communication of Device A 2704 goes via link 2752 into Device B 2710 at block 2716. Device A 2704 is also in operational communication (Op) via buffer 2708 with Device B 2710 at input 2712 via operational communication link 2753. Also Device X 2720 is in operational communication with Device A 2704 via link 2753. For example, in one embodiment, the output buffer 2708 of Device A 2704 may be adjusted by control signals from 2702 which are received by 2706 which then adjusts 2708 and the output of 2708 may then be communicated to 2710 and 2720 via 2753. Device B 2710 as illustrated here at 716 has outputs, inputs, and bidirectional connections on Device B and thus can receive commands as well as, for example, measurements from Device B 2710. For example, input buffer 2712 may provide a measurement of threshold and communicate this to block 2716 as a measurement which may then be used locally and/or communicated as a measurement via link 2757. Link 2756 communicates control communications received via 2752 and also measurement communications from Device B 2710. Thus 2756 has both control and measurement communications. Device B 2170 is in operational communication with Device N 2730 via link 2754. Link 2754, as illustrated may be from an output buffer 2714. Buffer 2714 may be in communications with and either be controlled by and/or provide measurements to block 2716. For example, block 2716 may control how fast the buffer 2714 may slew a signal based on a control communication received from link 2752 which may have originated with Command and Control 2702. Command and Control 2702 may in turn have based the control communications to 2716 based upon a measurement 2716 communicated to it via links 2756 and 2757. Device X 2720 as noted is in operational communication with Device A 2704 via link 2753. Device X 2720 as illustrated has a measurement capability and measurements are

communicated via like 2755 to like 2757 which in turn is in communication with Command and Control 2702.

[00157] Figure 27 illustrates a variety of devices in communication. For example, Device A, Device B, Device X, and Device N are all in operational communication. Device A is in operational communication with Device B and Device X via link 2753. Device B is in operational communication with Device N 2730 via link 2754. Device A and Device B are in control communication via link 2752. Device X 2720 and Device B are in measurement communication via link 2755 and 2756. Device N 2730 as noted is in operational communication with Device B via link 2754. Note that Device N 2730, as illustrated is not in control or measurement communication with any other device.

[00158] What is to be appreciated is that for a group of devices, some of the devices may be in different communication subgroups, such as operational, control, and measurement and that these subgroups do not necessarily include the same devices. In Figure 7 the devices (exclusive of Command and Control 2702 which may also be considered a device) in operational communications are Device A, Device B, Device X, and Device N; the devices (again exclusive of Command and Control 2702) in control communication are Device A, and Device B; and the devices (again exclusive of Command and Control 2702) in measurement communication are Device B, and Device X.

[00159] Command and Control 2702 as illustrated in Figure 27 is shown as a separate entity from the other devices for the sake of illustration and clarity. As such, it may be considered an external command and control and thus is in control communication with Device A, and Device B. It is also in measurement communication with Device B, Device X. In other embodiments the command and control as illustrated in 2702 may be incorporated into one or more of the devices in any group. For example, the command and control of 2702 may be incorporated into Device A 2704. In another embodiment the command and control of 2702 may in both Device A 2704 and Device B 2170.

[00160] Figure 27 for the sake of illustration has shown individual devices in communication. One of skill in the art will appreciate that some or all of the devices may be located on a single device, such as an integrated circuit (IC) where the devices may be considered "blocks" or "components" on the IC (for example, Figure 14 illustrates a differential amplifier). For example, referring to Figure 27, Device A 2704, Device B, 2170, and Command and Control 2702 may be on a single IC and the output of this IC might then drive a another device, such as, Device X 2720 via link 2753 and receive a measurement via link 2755, and drive another device such as Device N 2730 without receiving any measurement. Other arrangements are possible in which devices may or may not be in operational, control, and measurement communication.

[00161] While the above description of Figure 27 details control, measurement, and operational communications, it is not to be implied that each communication must be via a separate link or channel. For example, in one embodiment of the invention, a bus or serial data chain may be used, for example, to communicate both control and measurement over the same communication channel at the same time. One of skill in the art will appreciate that a type of communication may be indicated by a

data header ("control", "measurement", etc.) and then the data follows. Thus multiple different types of messages may be sent/received over the same communications channel or link.

[00162] Thus a method and apparatus for parameter adjustment, testing, and configuration of devices have been described.

[00163] Figure 1 illustrates a network environment 100 in which the techniques described may be applied. The network environment 100 has a network 102 that connects S servers 104-1 through 104-S, and C clients 108-1 through 108-C. More details are described below.

[00164] Figure 2 is a block diagram of a computer system 200 in which some embodiments of the invention may be used and which may be representative of use in any of the clients and/or servers shown in Figure 1, as well as, devices, clients, and servers in other Figures. More details are described below.

[00165] Referring back to Figure 1, Figure 1 illustrates a network environment 100 in which the techniques described may be applied. The network environment 100 has a network 102 that connects S servers 104-1 through 104-S, and C clients 108-1 through 108-C. As shown, several computer systems in the form of S servers 104-1 through 104-S and C clients 108-1 through 108-C are connected to each other via a network 102, which may be, for example, a corporate based network. Note that alternatively the network 102 might be or include one or more of: the Internet, a Local Area Network (LAN), Wide Area Network (WAN), satellite link, fiber network, cable network, or a combination of these and/or others. The servers may represent, for example, disk storage systems alone or storage and computing resources. Likewise, the clients may have computing, storage, and viewing capabilities. The method and apparatus described herein may be applied to essentially any type of communicating means or device whether local or remote, such as a LAN, a WAN, a system bus, etc. Thus, the invention may find application at both the S servers 104-1 through 104-S, and C clients 108-1 through 108-C.

[00166] Referring back to Figure 2, Figure 2 illustrates a computer system 200 in block diagram form, which may be representative of any of the clients and/or servers shown in Figure 1. The block diagram is a high level conceptual representation and may be implemented in a variety of ways and by various architectures. Bus system 202 interconnects a Central Processing Unit (CPU) 204, Read Only Memory (ROM) 206, Random Access Memory (RAM) 208, storage 210, display 220, audio, 222, keyboard 224, pointer 226, miscellaneous input/output (I/O) devices 228, and communications 230. The bus system 202 may be for example, one or more of such buses as a system bus, Peripheral Component Interconnect (PCI), Advanced Graphics Port (AGP), Small Computer System Interface (SCSI), Institute of Electrical and Electronics Engineers (IEEE) standard number 1394 (FireWire), Universal Serial Bus (USB), etc. The CPU 204 may be a single, multiple, or even a distributed computing resource. Storage 210, may be Compact Disc (CD), Digital Versatile Disk (DVD), hard disks (HD), optical disks, tape, flash, memory sticks, video recorders, etc. Display 220 might be, for example, an embodiment of the present invention. Note that depending upon the actual

implementation of a computer system, the computer system may include some, all, more, or a rearrangement of components in the block diagram. For example, a thin client might consist of a wireless hand held device that lacks, for example, a traditional keyboard. Thus, many variations on the system of Figure 2 are possible.

[00167] For purposes of discussing and understanding the invention, it is to be understood that various terms are used by those of skill in the art to describe techniques and approaches. Furthermore, in the description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be evident, however, to one of skill in the art that the present invention may be practiced without these specific details. In some instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring the present invention. These embodiments are described in sufficient detail to enable those of skill in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical, electrical, and other changes may be made without departing from the scope of the present invention.

[00168] Some portions of the description may be presented in terms of algorithms and symbolic representations of operations on, for example, data bits within a computer memory, and/or logic circuitry. These algorithmic descriptions and representations are the means used by those of skill in the arts to most effectively convey the substance of their work to others of skill in the art. An algorithm is here, and generally, conceived to be a self-consistent sequence of acts leading to a desired result. The acts are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like.

[00169] It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the discussion, it is appreciated that throughout the description, discussions utilizing terms such as "processing" or "computing" or "calculating" or "determining" or "displaying" or the like, can refer to the action and processes of a computer system, or similar electronic computing device, that manipulates and transforms data represented as physical (electronic) quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission, or display devices.

[00170] Further, any of the methods according to the present invention can be implemented in hard-wired circuitry, by programmable logic, or by any combination of hardware and software.

[00171] An apparatus for performing the operations herein can implement the present invention. This apparatus may be specially constructed for the required purposes, or it may comprise a general-

purpose computer, selectively activated or reconfigured by a computer program stored in the computer. Such a computer program may be stored in a computer readable storage medium, such as, but not limited to, any type of disk including floppy disks, hard disks, optical disks, compact disk- read only memories (CD-ROMs), and magnetic-optical disks, read-only memories (ROMs), random access memories (RAMs), electrically programmable read-only memories (EPROM)s, electrically erasable programmable read-only memories (EEPROMs), FLASH memories, magnetic or optical cards, etc., or any type of media suitable for storing electronic instructions either local to the computer or remote to the computer.

[00172] The algorithms and displays presented herein are not inherently related to any particular computer or other apparatus. Various general-purpose systems may be used with programs in accordance with the teachings herein, or it may prove convenient to construct more specialized apparatus to perform the required method. For example, any of the methods according to the present invention can be implemented in hard-wired circuitry, by programming a general-purpose processor, or by any combination of hardware and software. One of ordinary skill in the art will immediately appreciate that the invention can be practiced with computer system configurations other than those described, including hand-held devices, multiprocessor systems, microprocessor-based or programmable consumer electronics, digital signal processing (DSP) devices, set top boxes, network PCs, minicomputers, mainframe computers, and the like. The invention can also be practiced in distributed computing environments where tasks are performed by remote processing devices that are linked through a communications network.

[00173] The methods of the invention may be implemented using computer software. If written in a programming language conforming to a recognized standard, sequences of instructions designed to implement the methods can be compiled for execution on a variety of hardware platforms and for interface to a variety of operating systems. In addition, the present invention is not described with reference to any particular programming language. It will be appreciated that a variety of programming languages may be used to implement the teachings of the invention as described herein. Furthermore, it is common in the art to speak of software, in one form or another (e.g., program, procedure, application, driver,...), as taking an action or causing a result. Such expressions are merely a shorthand way of saying that execution of the software by a computer causes the processor of the computer to perform an action or produce a result.

[00174] It is to be understood that various terms and techniques are used by those knowledgeable in the art to describe communications, protocols, applications, implementations, mechanisms, etc. One such technique is the description of an implementation of a technique in terms of an algorithm or mathematical expression. That is, while the technique may be, for example, implemented as executing code on a computer, the expression of that technique may be more aptly and succinctly conveyed and communicated as a formula, algorithm, or mathematical expression. Thus, one of skill in the art would recognize a block denoting A+B=C as an additive function whose implementation in hardware and/or

software would take two inputs (A and B) and produce a summation output (C). Thus, the use of formula, algorithm, or mathematical expression as descriptions is to be understood as having a physical embodiment in at least hardware and/or software (such as a computer system in which the techniques of the present invention may be practiced as well as implemented as an embodiment).

[00175] A machine-readable medium is understood to include any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine-readable medium includes read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.); etc.

[00176] As used in this description, "one embodiment" or "an embodiment" or similar phrases means that the feature(s) being described are included in at least one embodiment of the invention. References to "one embodiment" in this description do not necessarily refer to the same embodiment; however, neither are such embodiments mutually exclusive. Nor does "one embodiment" imply that there is but a single embodiment of the invention. For example, a feature, structure, act, etc. described in "one embodiment" may also be included in other embodiments. Thus, the invention may include a variety of combinations and/or integrations of the embodiments described herein.

[00177] Thus a method and apparatus for parameter adjustment, testing, and configuration of devices have been described.

CLAIMS

What is claimed is:

1. A method comprising:

connecting one or more devices so that they are in operational communication;

connecting a first subset of said one or more devices so that they are in control communication;

connecting a second subset of said one or more devices so that they are in measurement communication;

receiving one or more messages from one or more devices in said second subset of said one or more devices;

transmitting one or more messages to one or more devices in said first subset of said one or more devices; and

adjusting operation of said one or more devices in said first subset of said one or more devices based on said one or more transmitted messages.

2. The method of claim 1 wherein said connecting is via a topology selected from the group consisting of point to point, point to multi-point, bussed, daisy chained, and directed acyclic graph.

3. The method of claim 1 wherein said receiving is serially receiving and said transmitting is serially transmitting.

4. The method of claim 1 wherein said adjusting operation is adjusting a parameter selected from the group consisting of placement of a signal edge, phase of a signal, frequency of a signal, signal timing, delay of a signal, rise time of a signal, fall time of a signal, output drive of a signal, output slew rate of a signal, output drive level, voltage output high, voltage output low, input threshold, input threshold voltage high, input threshold voltage low, termination of a signal, output impedance, input impedance, ground bounce, overshoot, undershoot, current, temperature, polarity of signaling, bit rates, skew, jitter, input offset, output offset, device state, and mode of operation.

5. The method of claim 4 wherein said signal is a clock.

6. The method of claim 1 wherein said receiving one or more messages is receiving information about a parameter selected from the group consisting of signal edge placement, signal phase, signal frequency, signal timing, signal delay, signal rise time, signal fall time, signal output drive, signal slew rate, output drive level, voltage output high, voltage output low, input threshold, input threshold voltage high, input threshold voltage low, output impedance, input impedance, ground bounce,

overshoot, undershoot, current, temperature, power consumption, time, device state, mode of operation, pass, and fail.

7. The method of claim 6 wherein said receiving one or more messages is receiving one or more messages at a serial data chain controller.

8. The method of claim 4 wherein said transmitting one or more messages is transmitting one or more messages to a serial data chain device.

9. The method of claim 1 wherein said operational communication is data communication during normal operation of said connected one or more devices.

10. The method of claim 1 wherein said control communication is used for said adjusting operation.

11. The method of claim 1 wherein said measurement communication is used in said receiving one or more messages.

12. The method of claim 1 wherein said receiving, and said transmitting are communicated on a common link.

13. The method of claim 1 wherein said first subset and said second subset are in a relationship selected from the group consisting of a same subset, different subsets, and overlapping subsets.

14. An apparatus comprising:

a serial data chain controller having a chain output, and a chain input;

a first device having an output, a register having an input and an output, a chain input, and a chain output, said chain input coupled to receive said serial data chain controller chain output, said register input in communication with said chain input, said register output in communication with said first device output;

one or more next devices each having an output, a register having an input and an output, a chain input, and a chain output, each successive next device chain input coupled to receive the prior next device chain output, each next device register input in communication with said next device chain input, said next device register output in communication with said next device output;

a final device having a register having an input and an output, a chain input and a chain output, said chain input coupled to receive a last next device chain output, and said final device chain output coupled to said serial data chain controller input, said register output in communication with said final device output.

15. The apparatus of claim 14 wherein said serial data chain controller further comprises a communication input, and a communication output.

16. The apparatus of claim 15 further comprising an external interface having an input and an output, said input coupled to receive said communication output, and said output coupled to said communication input.

17. The apparatus of claim 16 wherein said serial data chain controller communicates commands to one or more of said devices' (said first device, said one or more next devices, said final device) register affecting said respective devices' output.

18. The apparatus of claim 16 wherein said serial data chain controller receives measurements from one or more of said devices (said first device, said one or more next devices, said final device) indicating information about said respective devices' output.

19. An apparatus comprising:

means for connecting one or more devices so that they are in operational communication;

means for connecting a first subset of said one or more devices so that they are in control communication;

means for transmitting one or more messages to one or more devices in said first subset of said one or more devices; and

means for adjusting operation of said one or more devices in said first subset of said one or more devices based on said one or more transmitted messages.

20. The apparatus of claim 19 further comprising:

means for connecting a second subset of said one or more devices so that they are in measurement communication;

means for receiving one or more measurement communication messages from one or more devices in said second subset of said one or more devices; and

means for adjusting operation of said one or more devices in said first subset of said one or more devices based on said one or more received measurement communication messages.

21. The apparatus of claim 20 wherein said adjusting operation of said one or more devices is a device parameter selected from the group consisting of signal edge placement, signal phase, signal frequency, signal timing, signal delay, signal rise time, signal fall time, signal output drive, signal slew rate, output

drive level, voltage output high, voltage output low, input threshold, input threshold voltage high, input threshold voltage low, output impedance, input impedance, ground bounce, overshoot, undershoot, current, temperature, power consumption, time, device state, and mode of operation.

22. An apparatus comprising:

means for connecting one or more components on an integrated circuit (IC) so that they are in operational communication;

means for connecting a first subset of said one or more components so that they are in control communication;

means for transmitting one or more messages to one or more devices in said first subset of said one or more devices; and

means for adjusting operation of said one or more devices in said first subset of said one or more devices based on said one or more transmitted messages.

23. The apparatus of claim 22 wherein said means for adjusting operation is means for adjusting a parameter selected from the group consisting of placement of a signal edge, phase of a signal, frequency of a signal, signal timing, delay of a signal, rise time of a signal, fall time of a signal, output drive of a signal, output slew rate of a signal, output drive level, voltage output high, voltage output low, input threshold, input threshold voltage high, input threshold voltage low, termination of a signal, output impedance, input impedance, ground bounce, overshoot, undershoot, current, temperature, polarity of signaling, bit rates, skew, jitter, input offset, output offset, device state, and mode of operation.

24. The apparatus of claim 22 wherein said means for receiving one or more messages is means for receiving information about a parameter selected from the group consisting of signal edge placement, signal phase, signal frequency, signal timing, signal delay, signal rise time, signal fall time, signal output drive, signal slew rate, output drive level, voltage output high, voltage output low, input threshold, input threshold voltage high, input threshold voltage low, output impedance, input impedance, ground bounce, overshoot, undershoot, current, temperature, power consumption, time, device state, mode of operation, pass, and fail.

25. The apparatus of claim 22 wherein said first subset and said second subset are in a relationship selected from the group consisting of a same subset, different subsets, and overlapping subsets.

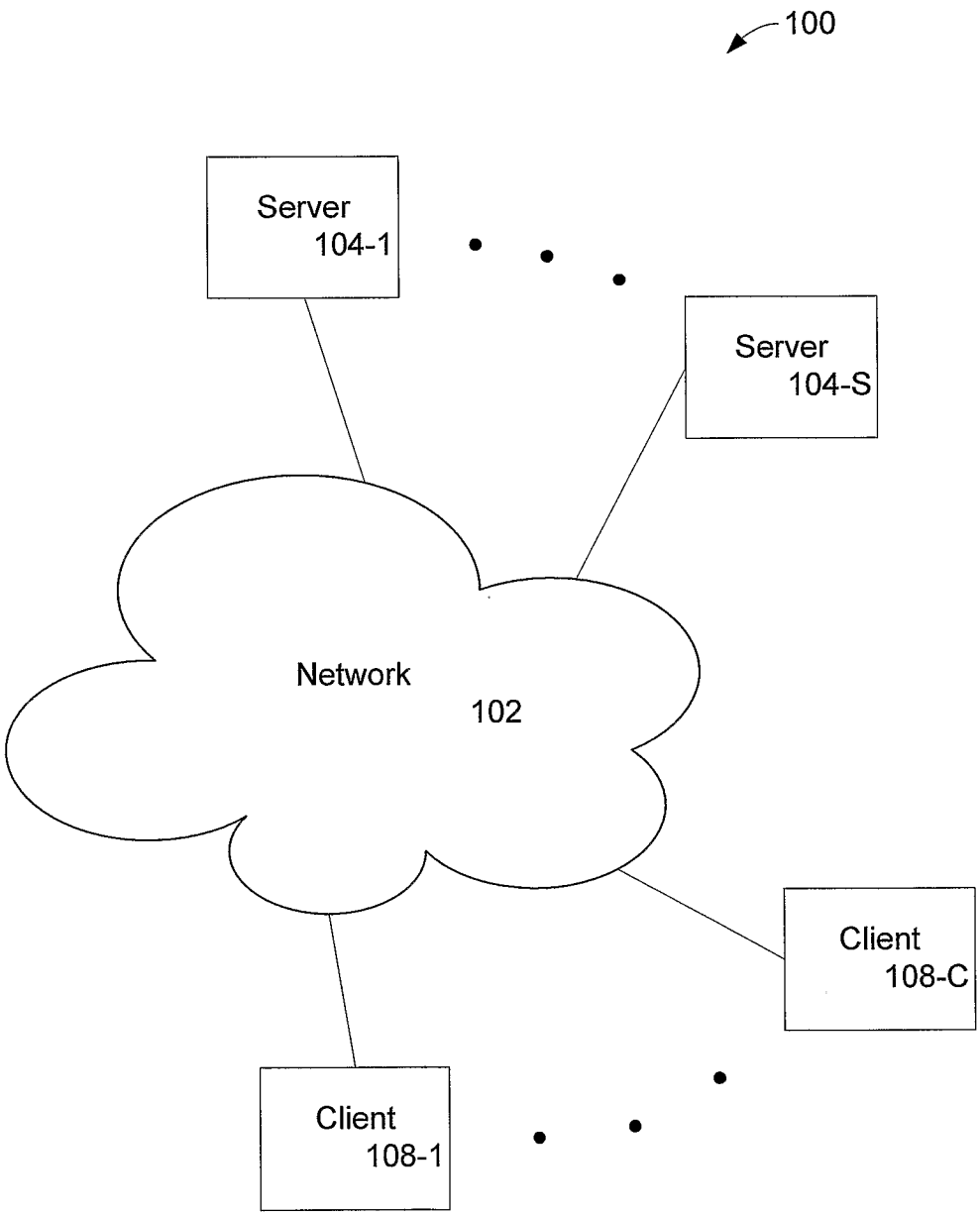

100
Server
104-1
Server
104-S
Network
102
Client
108-C
Client
108-1

FIG. 1

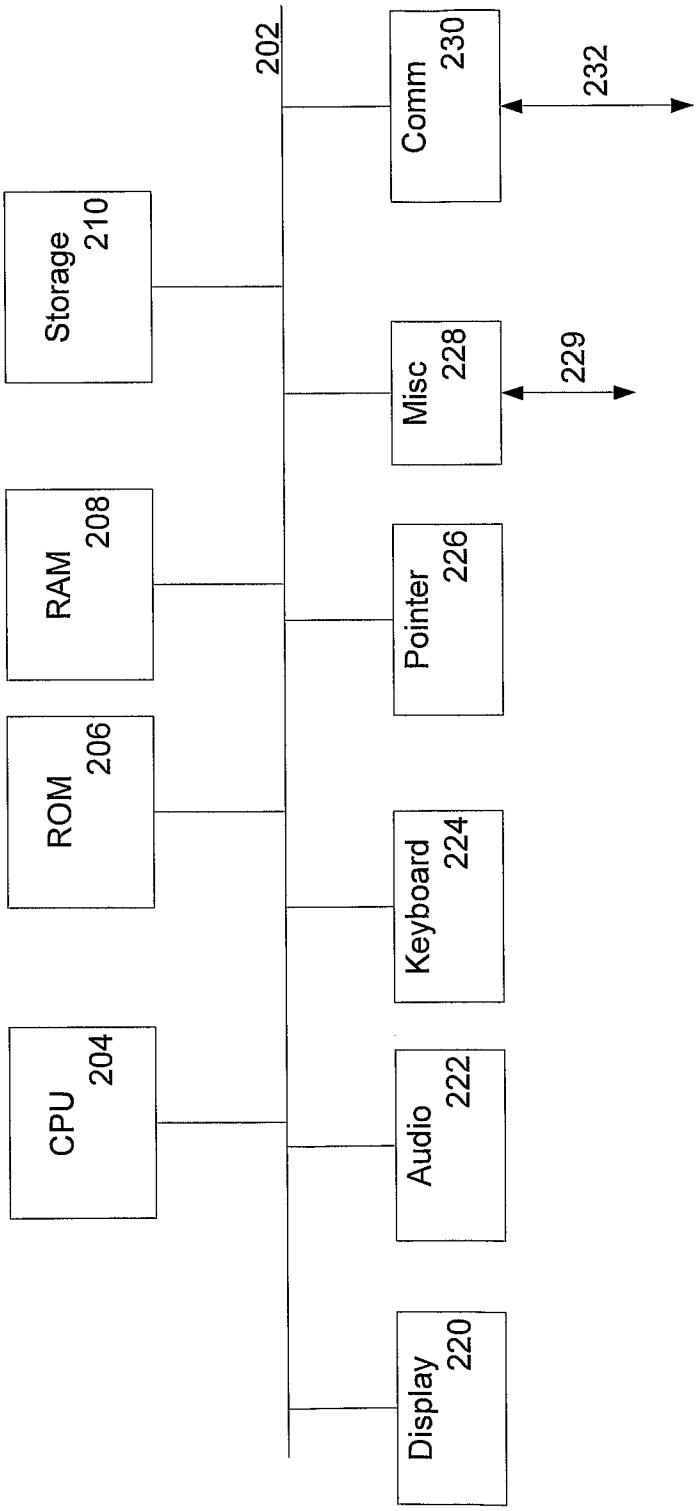
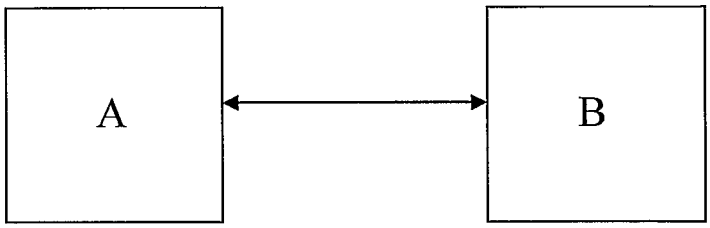
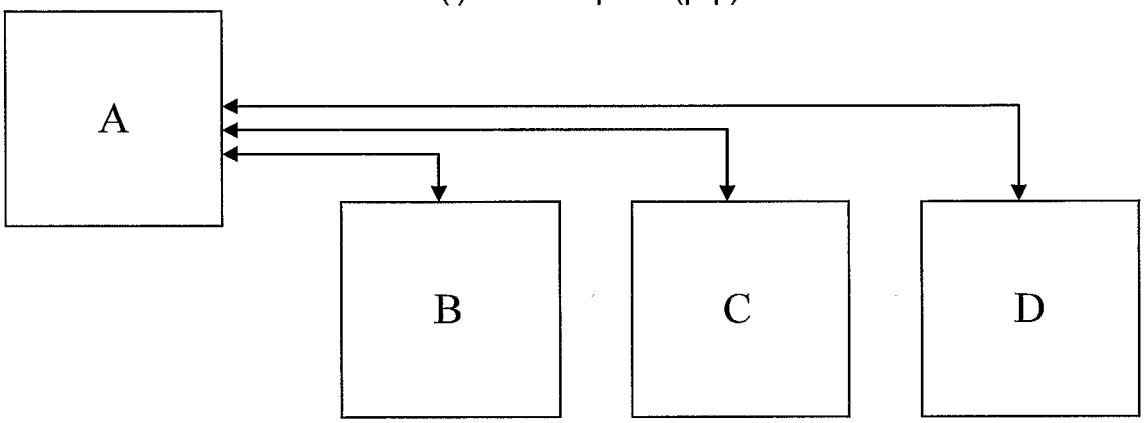

200
202
Storage 210
RAM 208
ROM 206
CPU 204
Comm 230
232
Misc 228
229
Pointer 226
Keyboard 224
Audio 222
Display 220

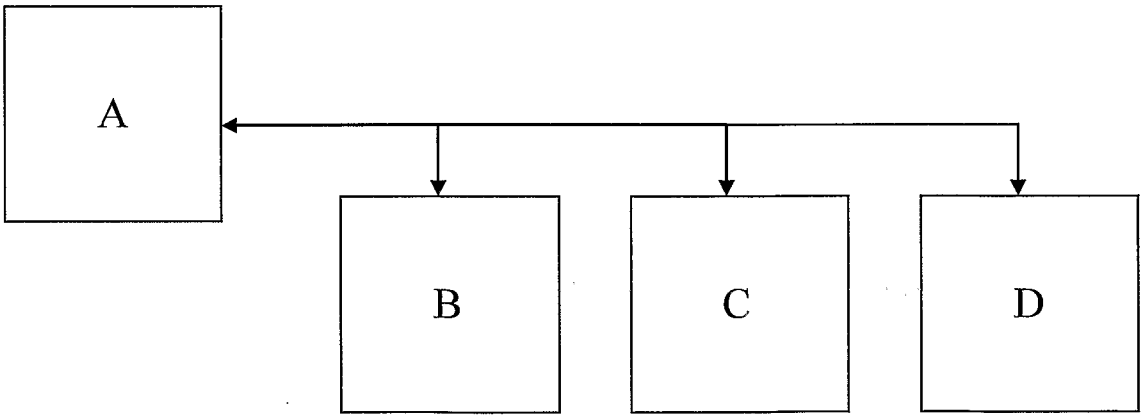
FIG. 2



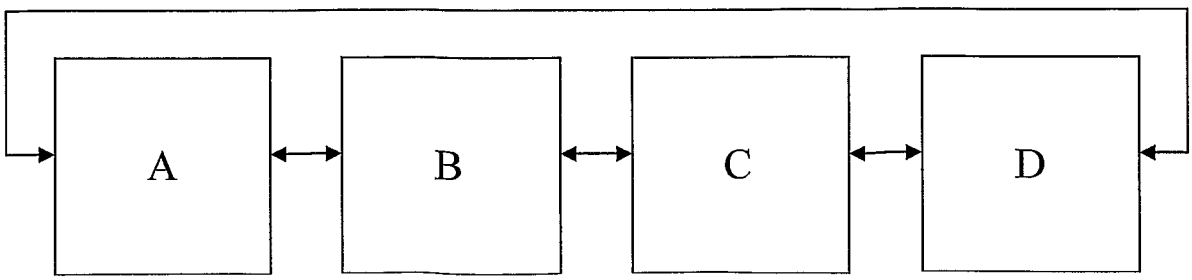
(i) Point to point (p-p)



(ii) Point to multipoint (p-mp)



(iii) Bussed



(iv) Daisy Chained

FIG. 3

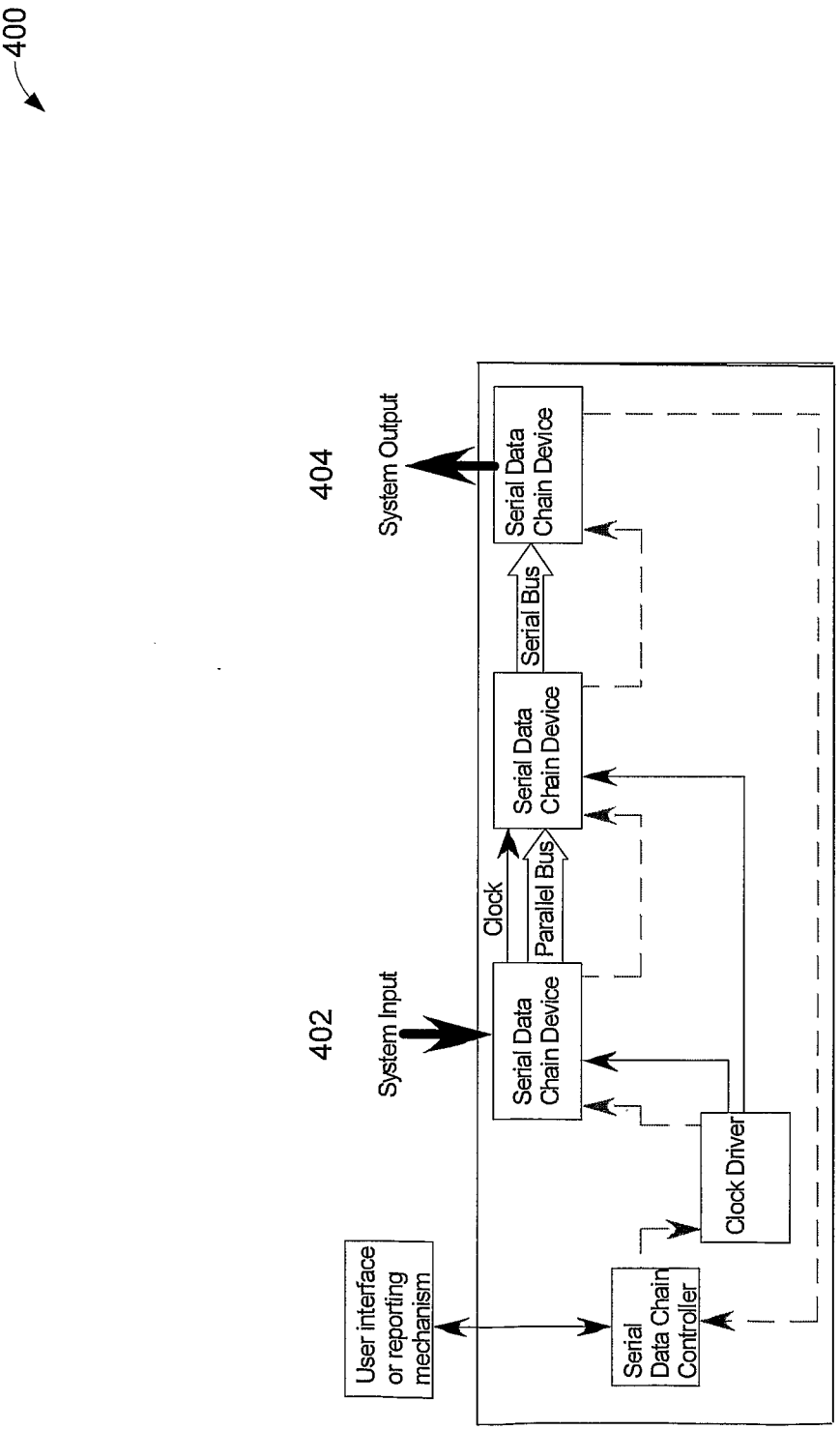

400
402
404
System Input
System Output
Clock
Parallel Bus
Serial Bus
Serial Data Chain Device
Serial Data Chain Device
Serial Data Chain Device
Clock Driver
Serial Data Chain Controller
User interface or reporting mechanism

FIG. 4

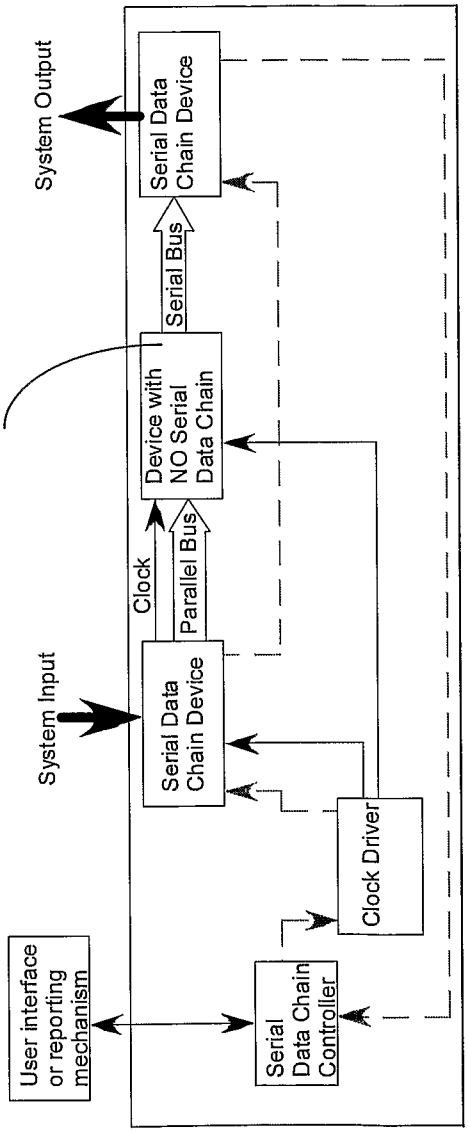

500
506
System Output
Serial Data Chain Device
Serial Bus
Device with NO Serial Data Chain
Clock
Parallel Bus
System Input
Serial Data Chain Device
Clock Driver
User interface or reporting mechanism
Serial Data Chain Controller

FIG. 5

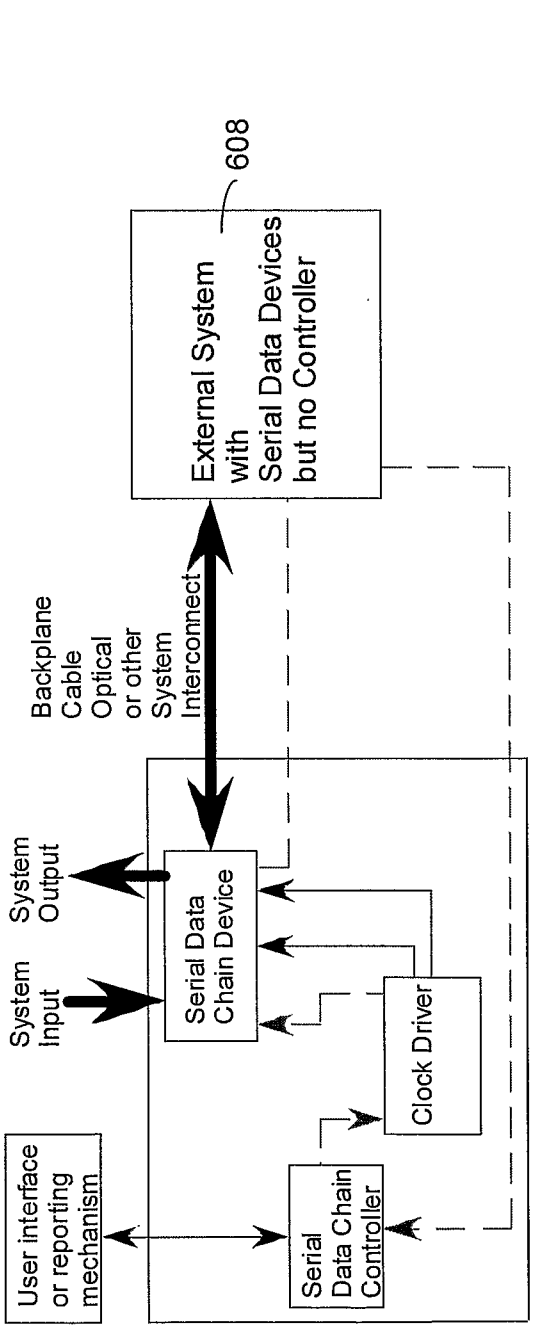

600
608
External System with Serial Data Devices but no Controller
Backplane Cable Optical or other System Interconnect
System Output
System Input
Serial Data Chain Device
Clock Driver
User interface or reporting mechanism
Serial Data Chain Controller

FIG. 6

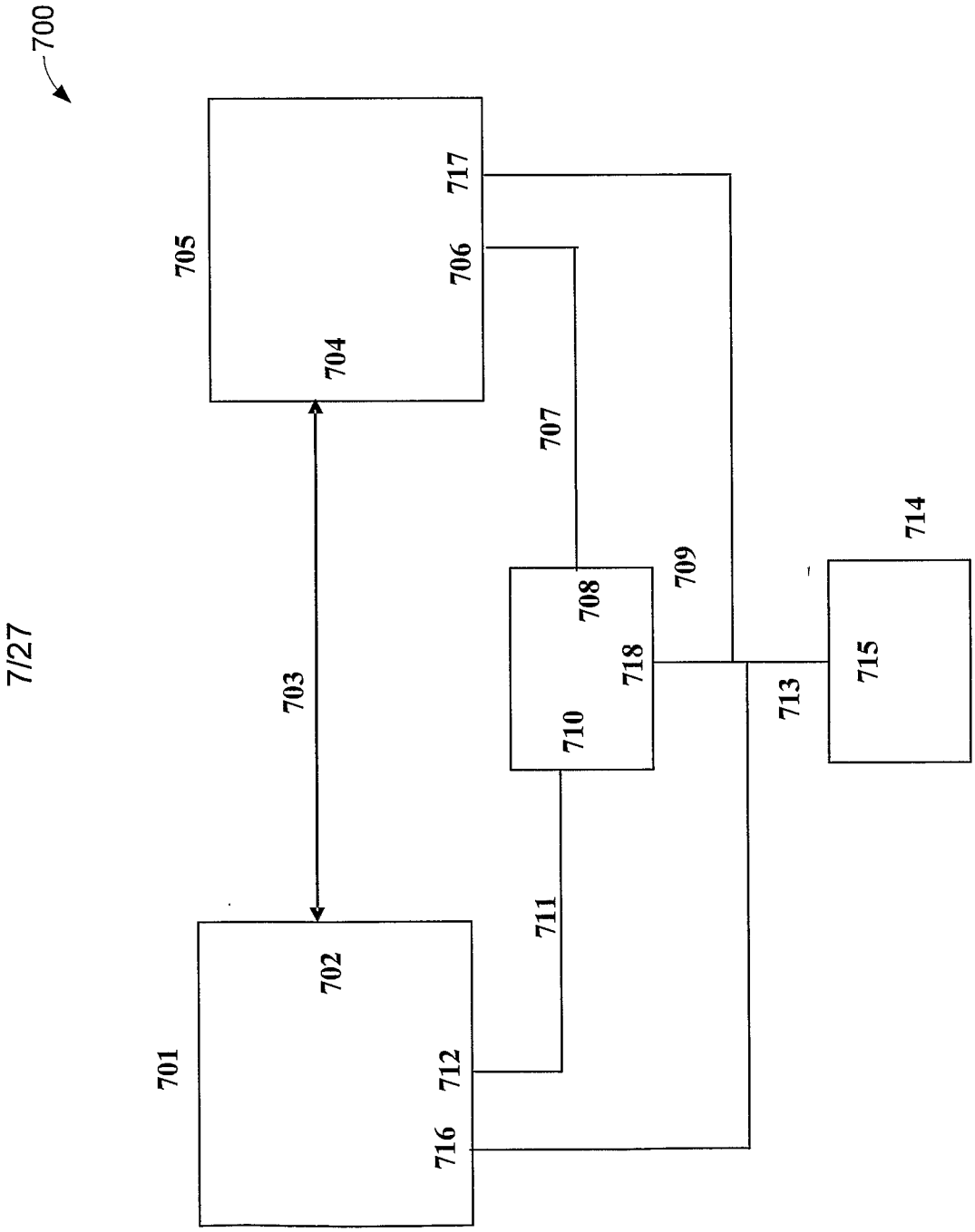

700
705
704
717
706
707
703
708
709
710
718
714
715
713
711
702
701
712
716

FIG. 7

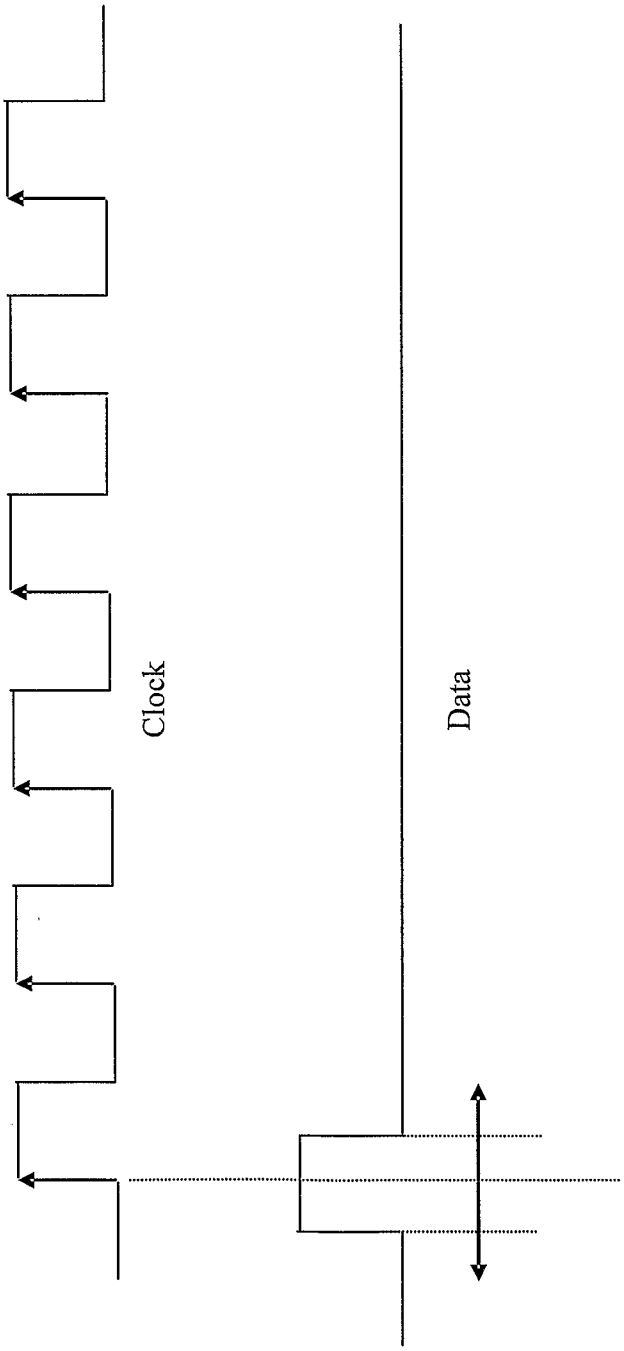


FIG. 8

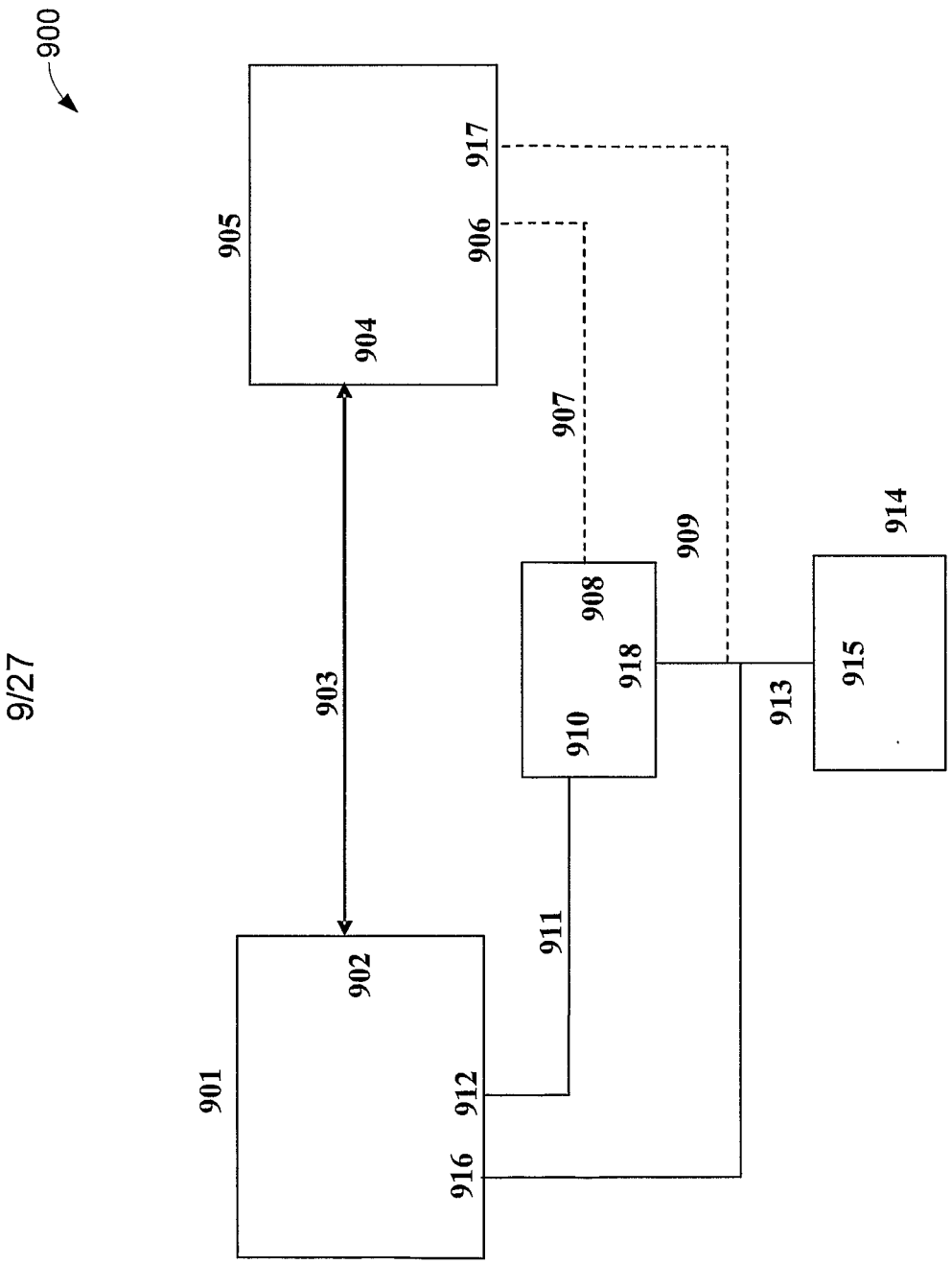

900
905
917
906
904
907
909
914
908
903
918
915
910
913
911
902
901
912
916

FIG. 9

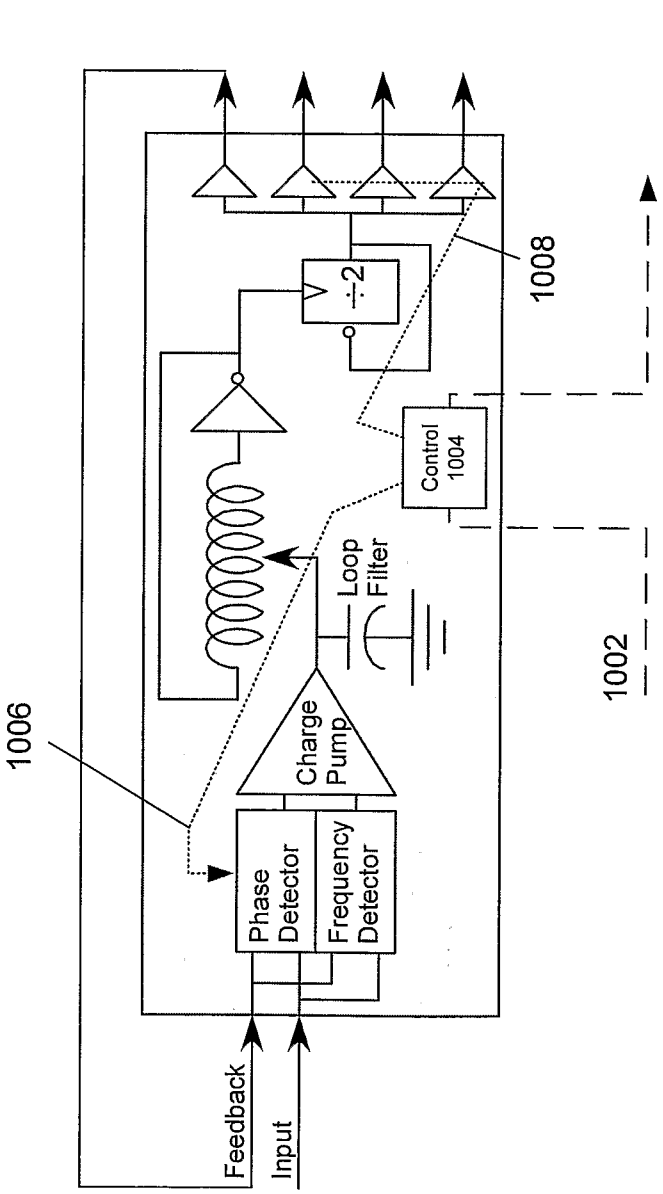

1000
1008
÷2
Control
1004
Loop
Filter
1002
1006
Charge
Pump
Phase
Detector
Frequency
Detector
Feedback
Input

FIG. 10

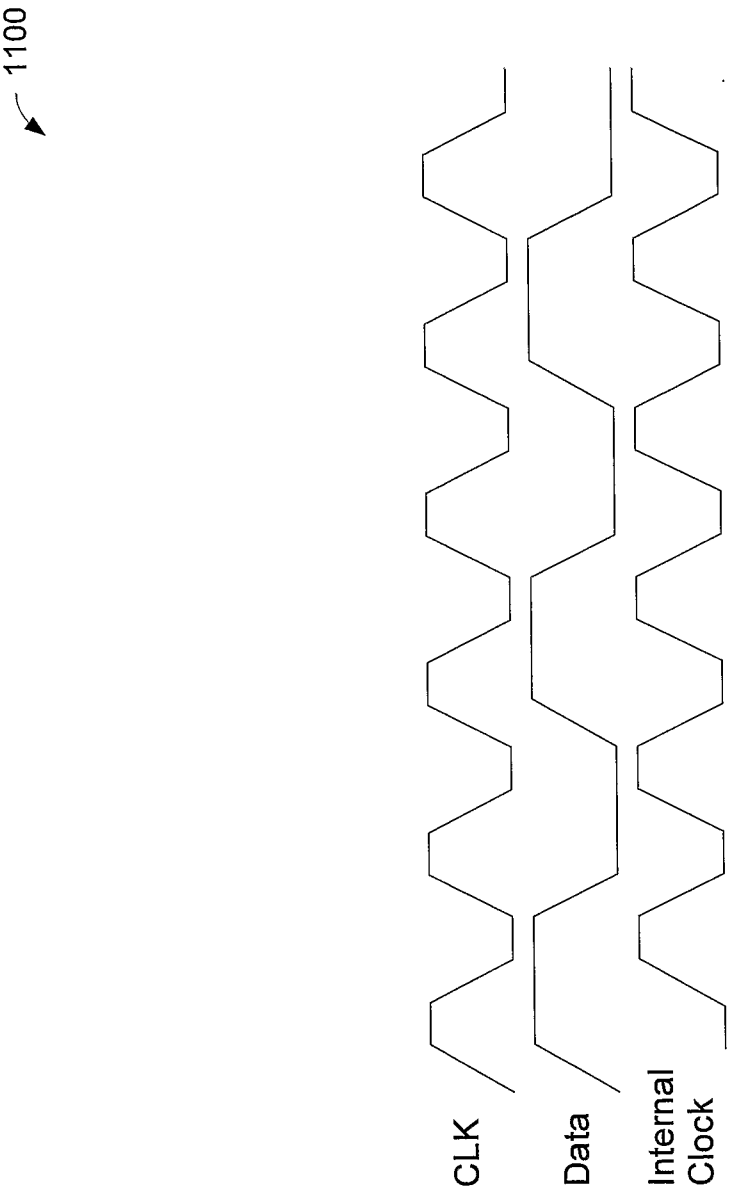


FIG. 11

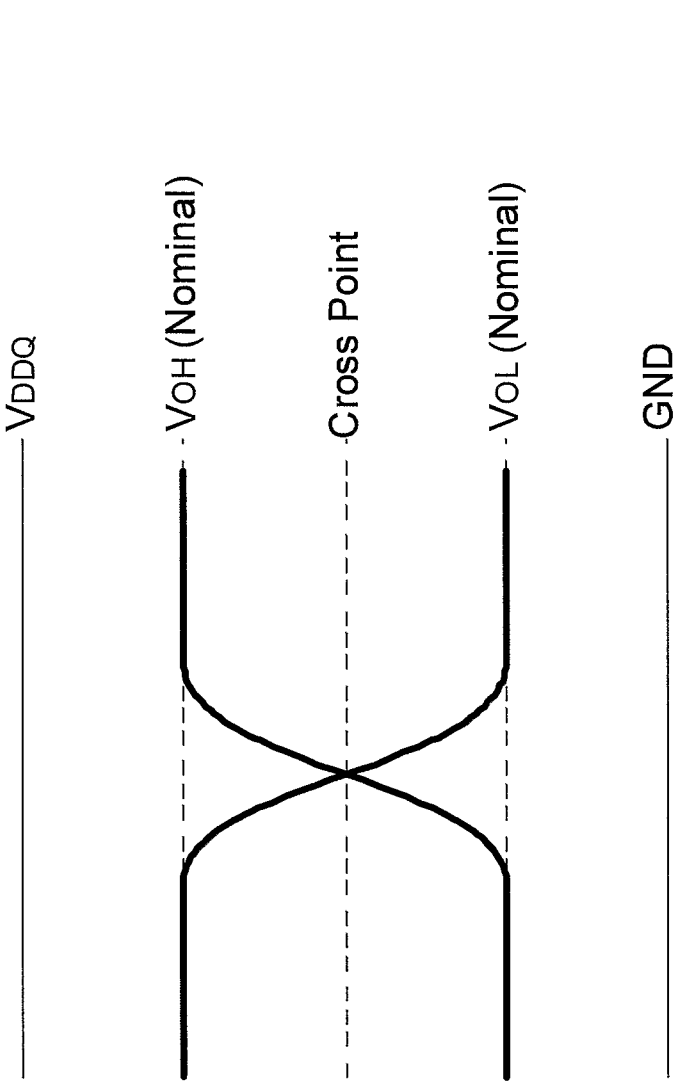


FIG.12

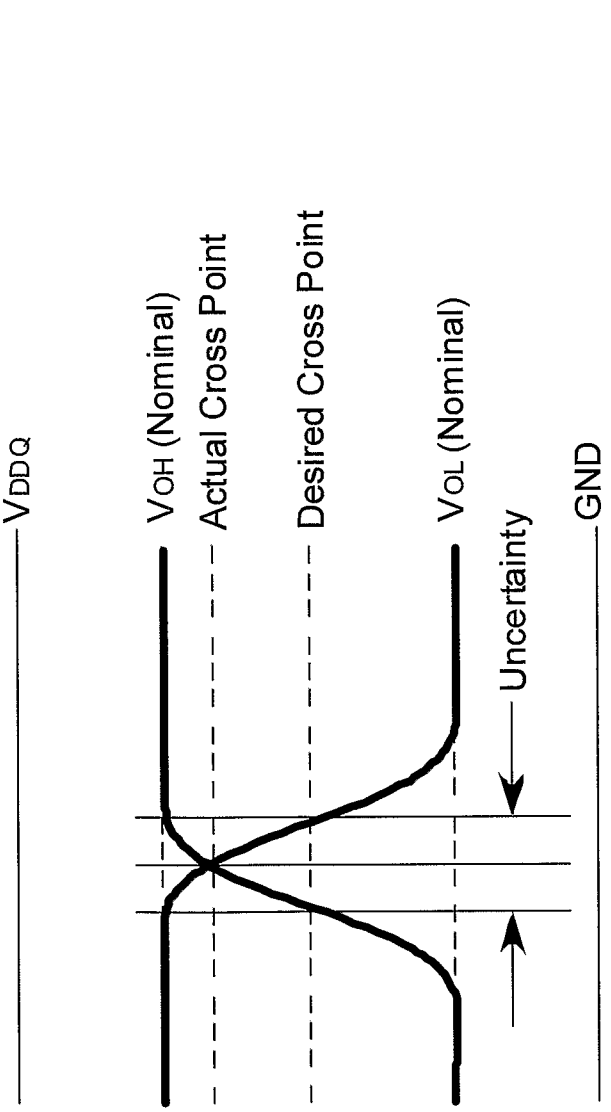

1300
VDDQ
VOH (Nominal)
Actual Cross Point
Desired Cross Point
VOL (Nominal)
Uncertainty
GND

FIG.13

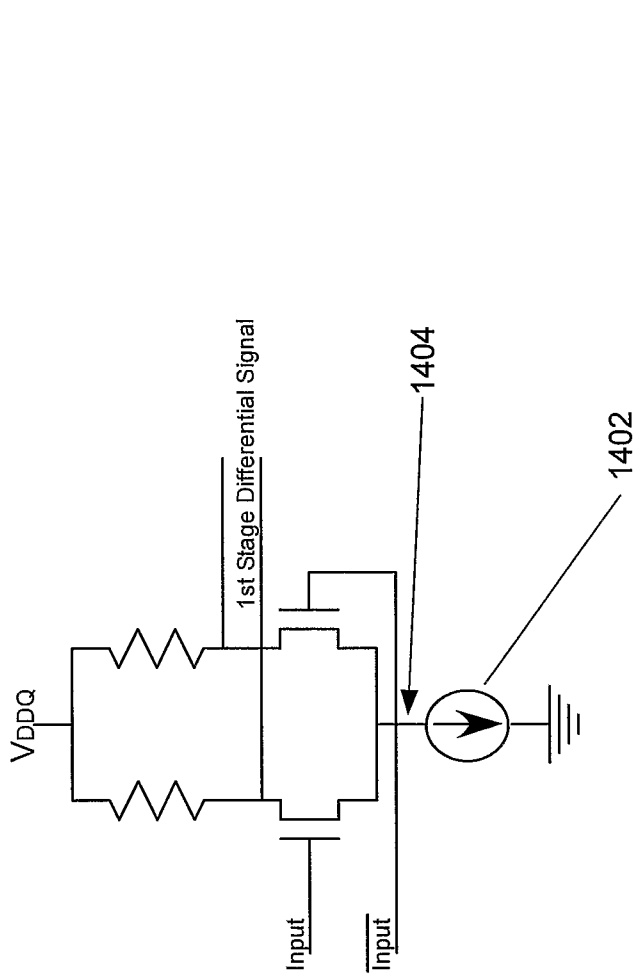

1400
1st Stage Differential Signal
1404
1402
VDDQ
Input
Input

FIG.14

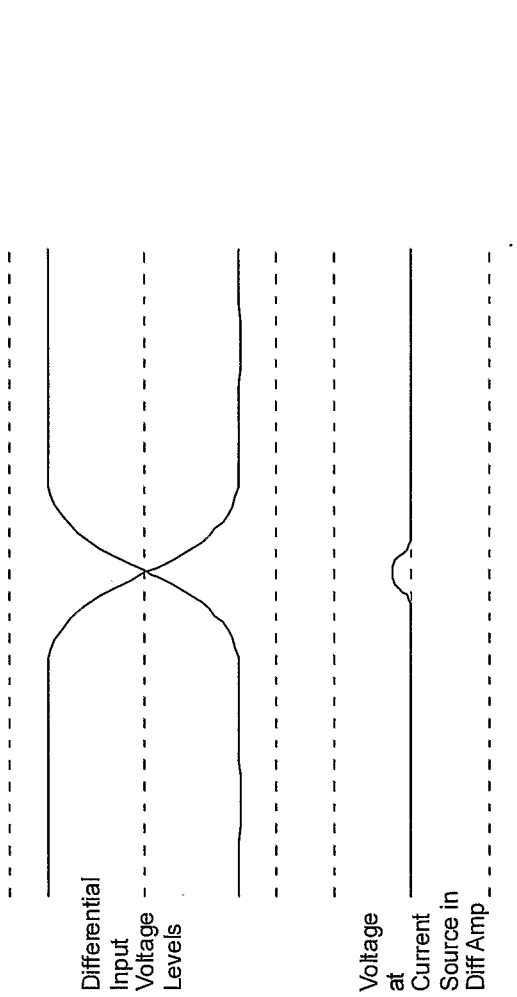

1500
Differential Input Voltage Levels
Voltage at Current Source in Diff Amp

FIG. 15

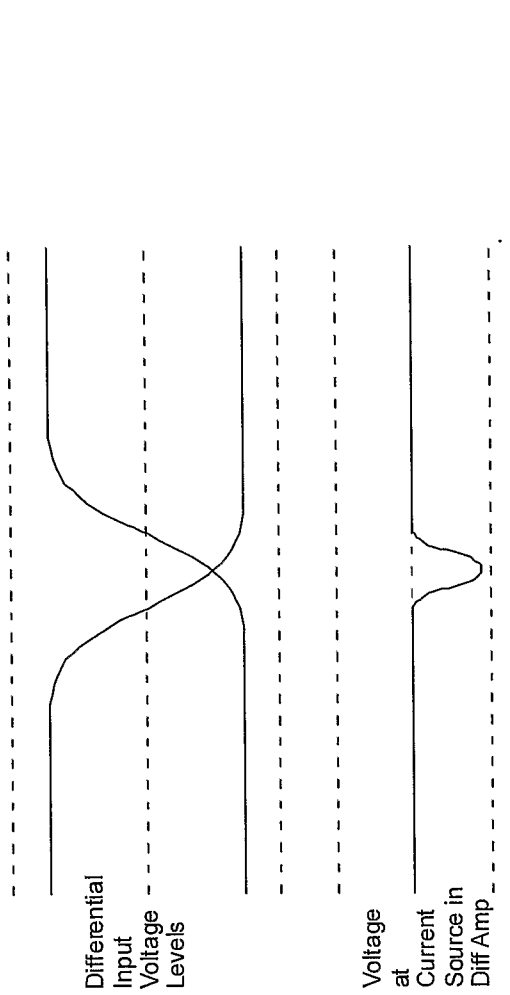

1600
Differential Input Voltage Levels
Voltage at Current Source in Diff Amp

FIG. 16

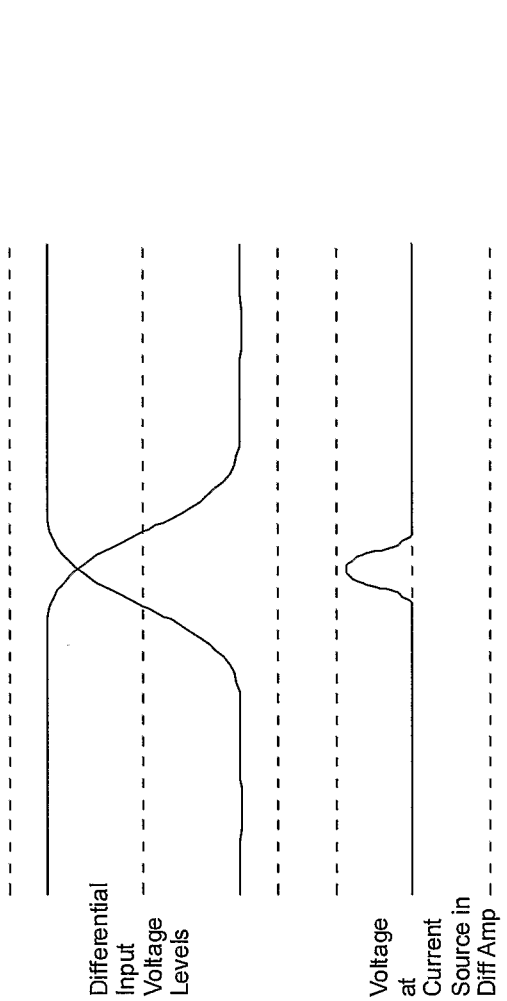

1700
Differential Input Voltage Levels
Voltage at Current Source in Diff Amp

FIG. 17

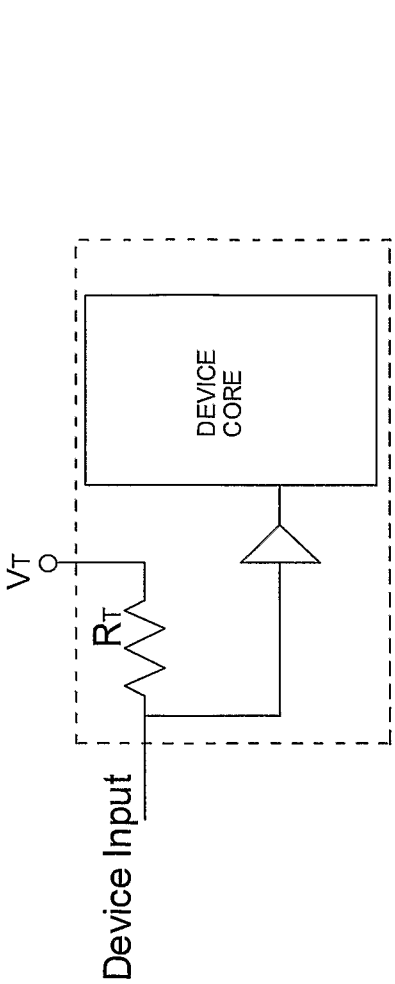


FIG. 18

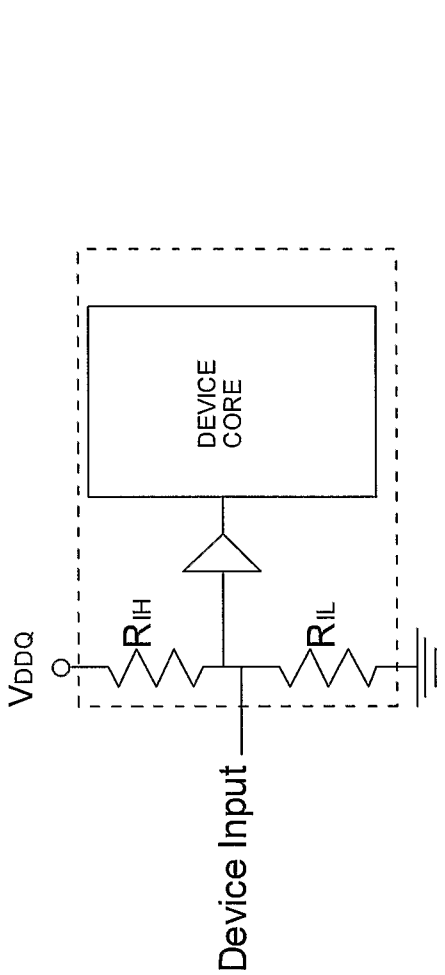


FIG. 19

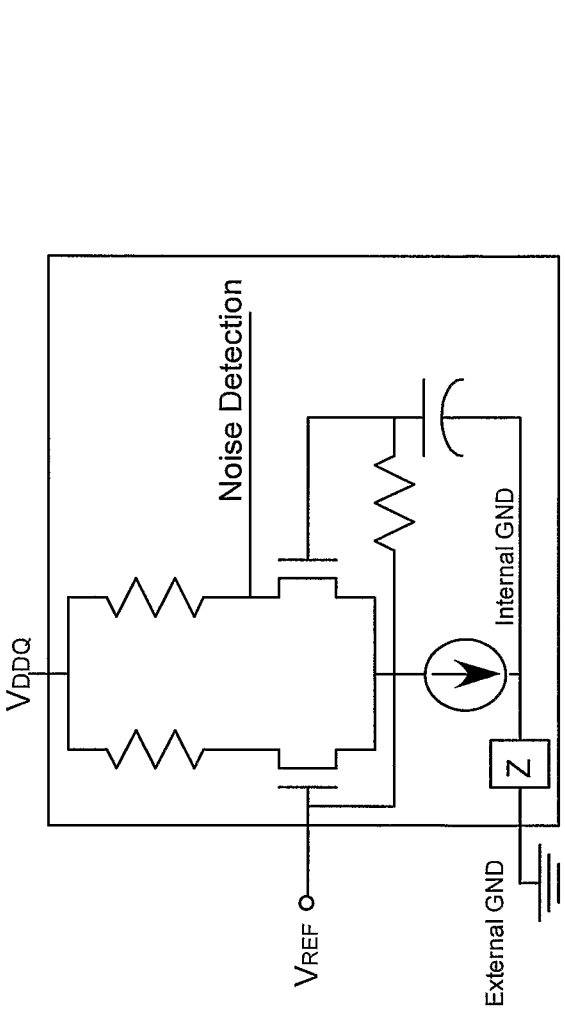


FIG. 20

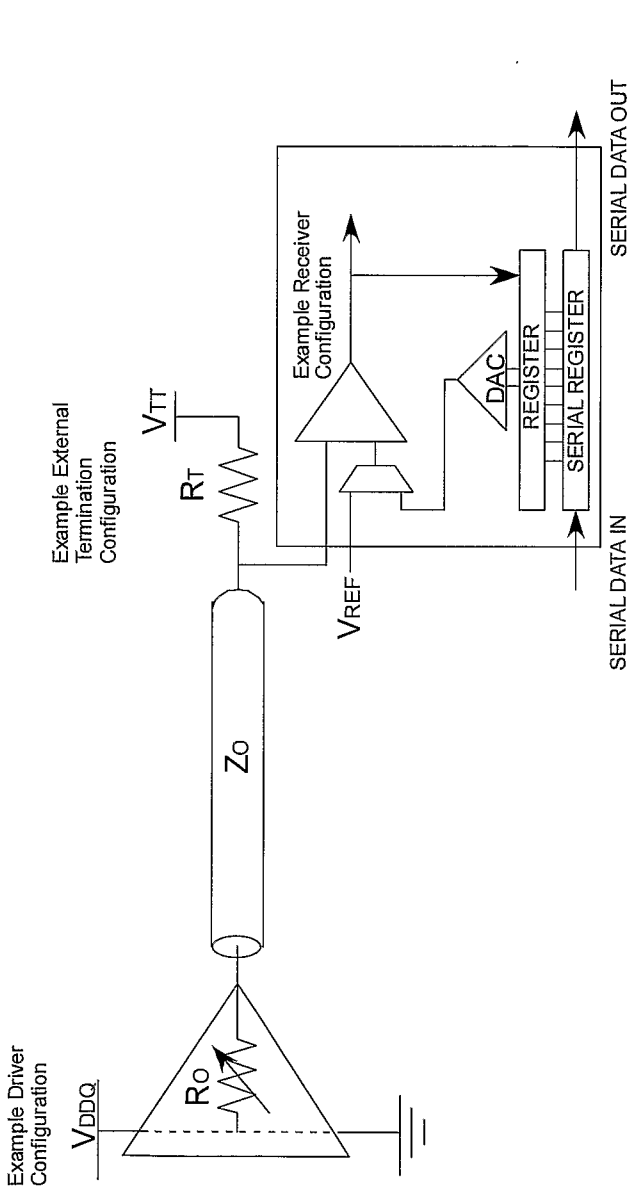

2100
Example Driver Configuration
VDDQ
RO
ZO
Example External Termination Configuration
VTT
RT
VREF
Example Receiver Configuration
DAC
REGISTER
SERIAL REGISTER
SERIAL DATA IN
SERIAL DATA OUT

FIG. 21

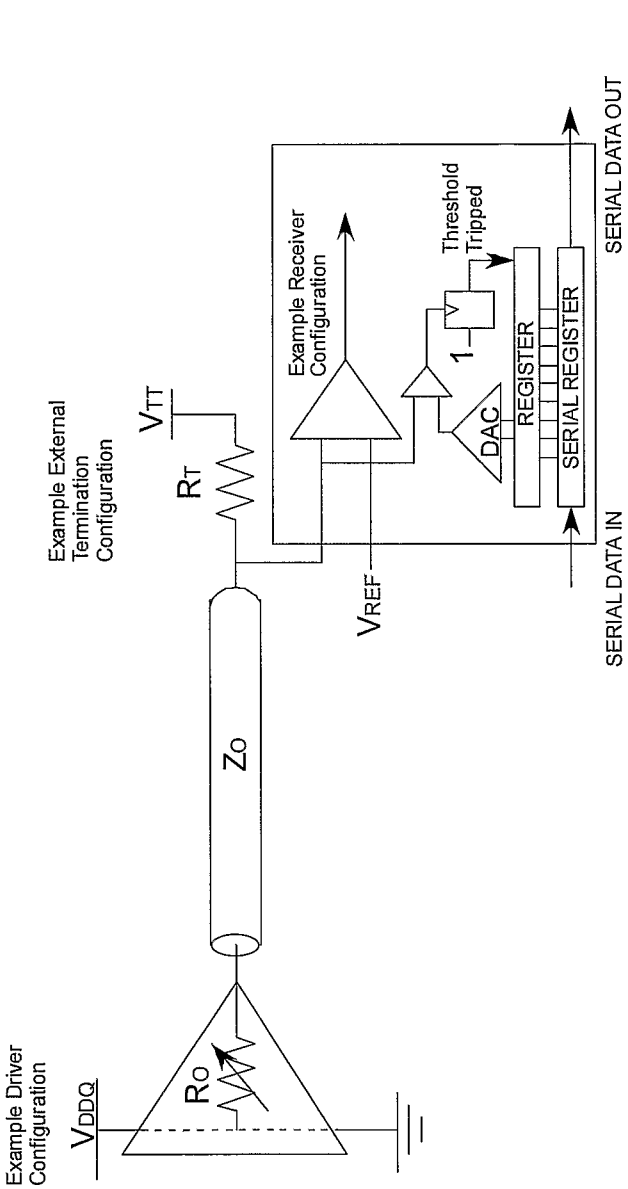

2200
Example Driver Configuration
VDDQ
RO
ZO
Example External Termination Configuration
VTT
RT
VREF
Example Receiver Configuration
Threshold Tripped
1
DAC
REGISTER
SERIAL REGISTER
SERIAL DATA IN
SERIAL DATA OUT

FIG. 22

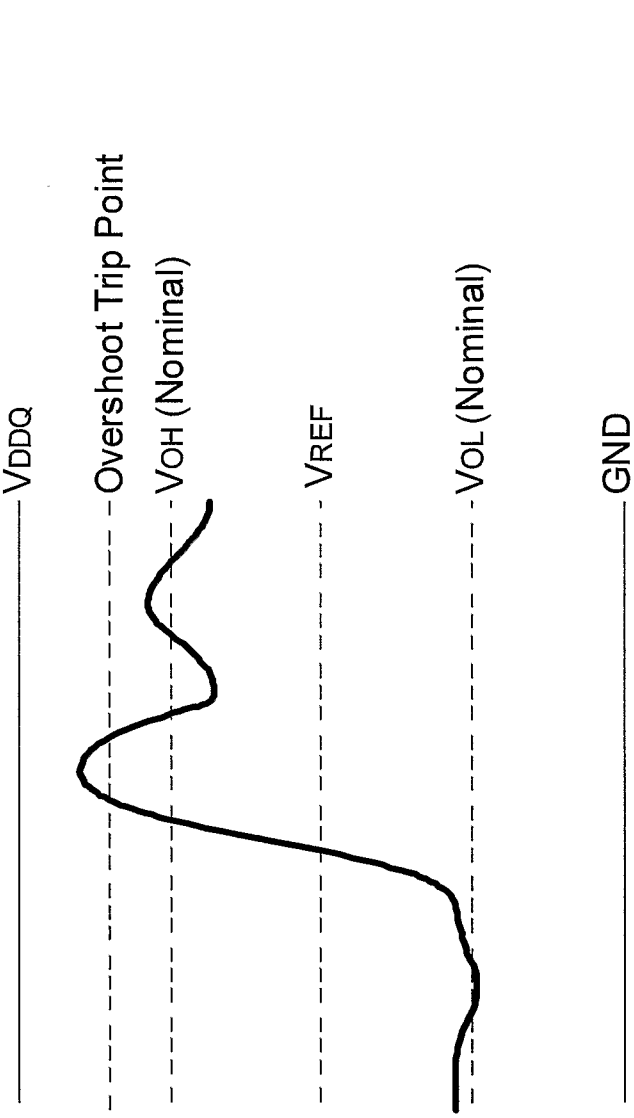

2300
VDDQ
Overshoot Trip Point
VOH (Nominal)
VREF
VOL (Nominal)
GND

FIG. 23

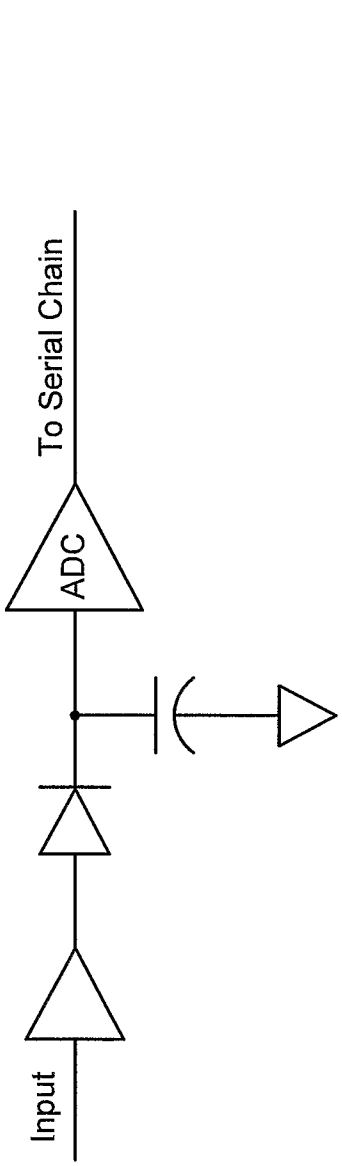


FIG. 24

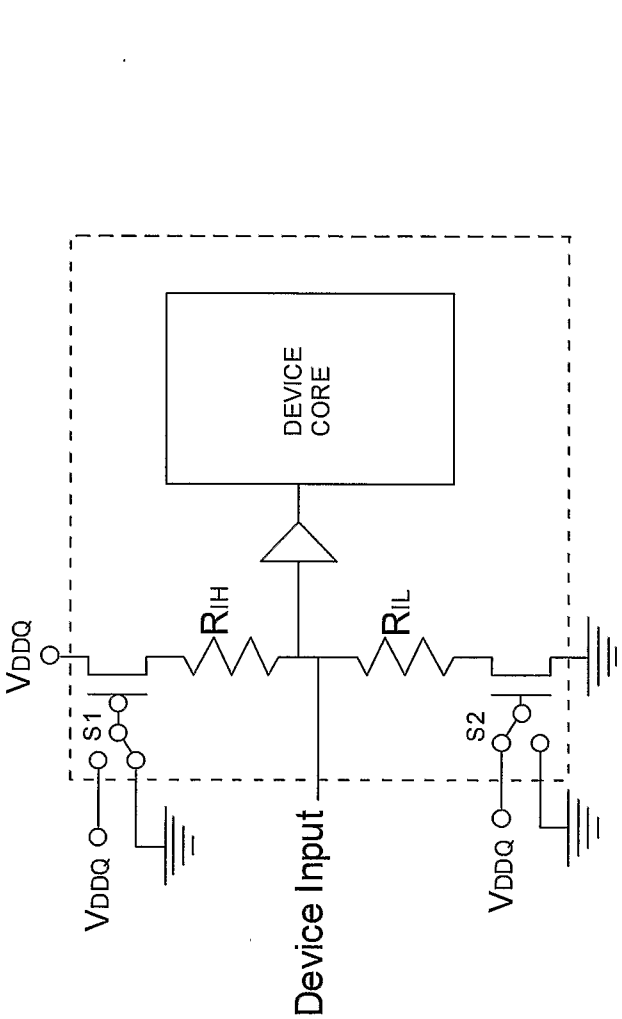


FIG. 25

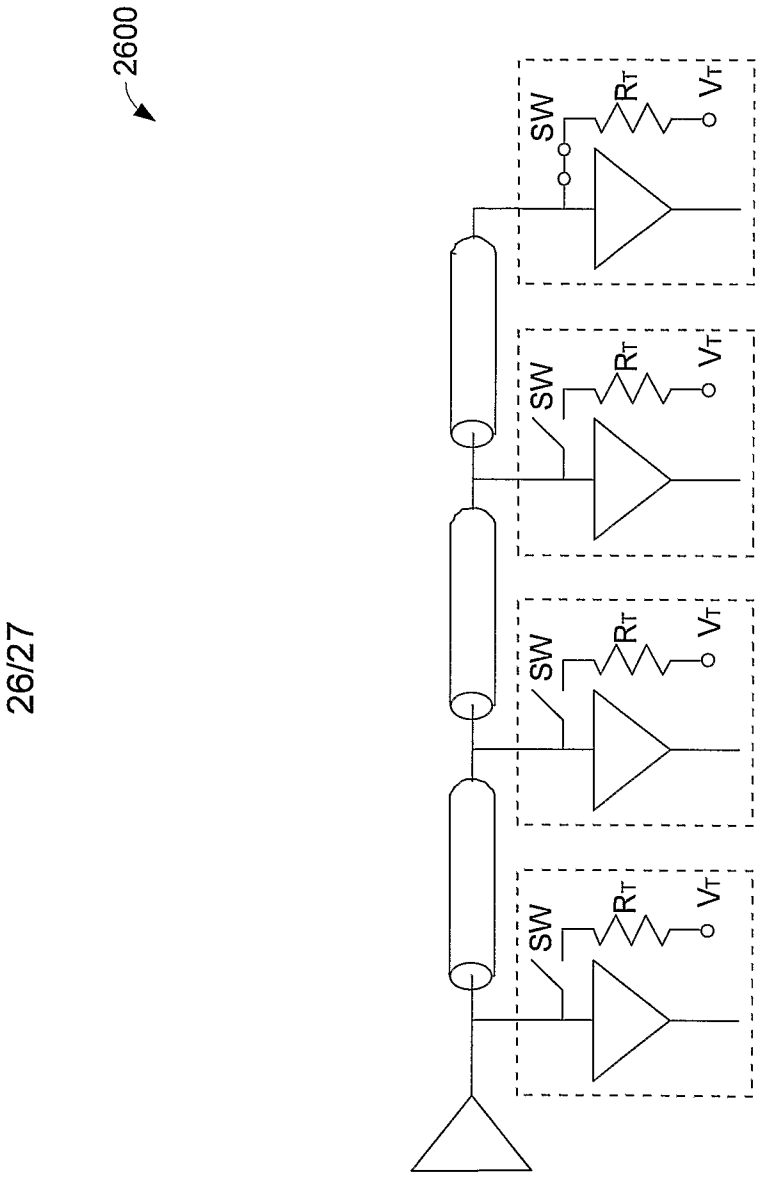


FIG. 26

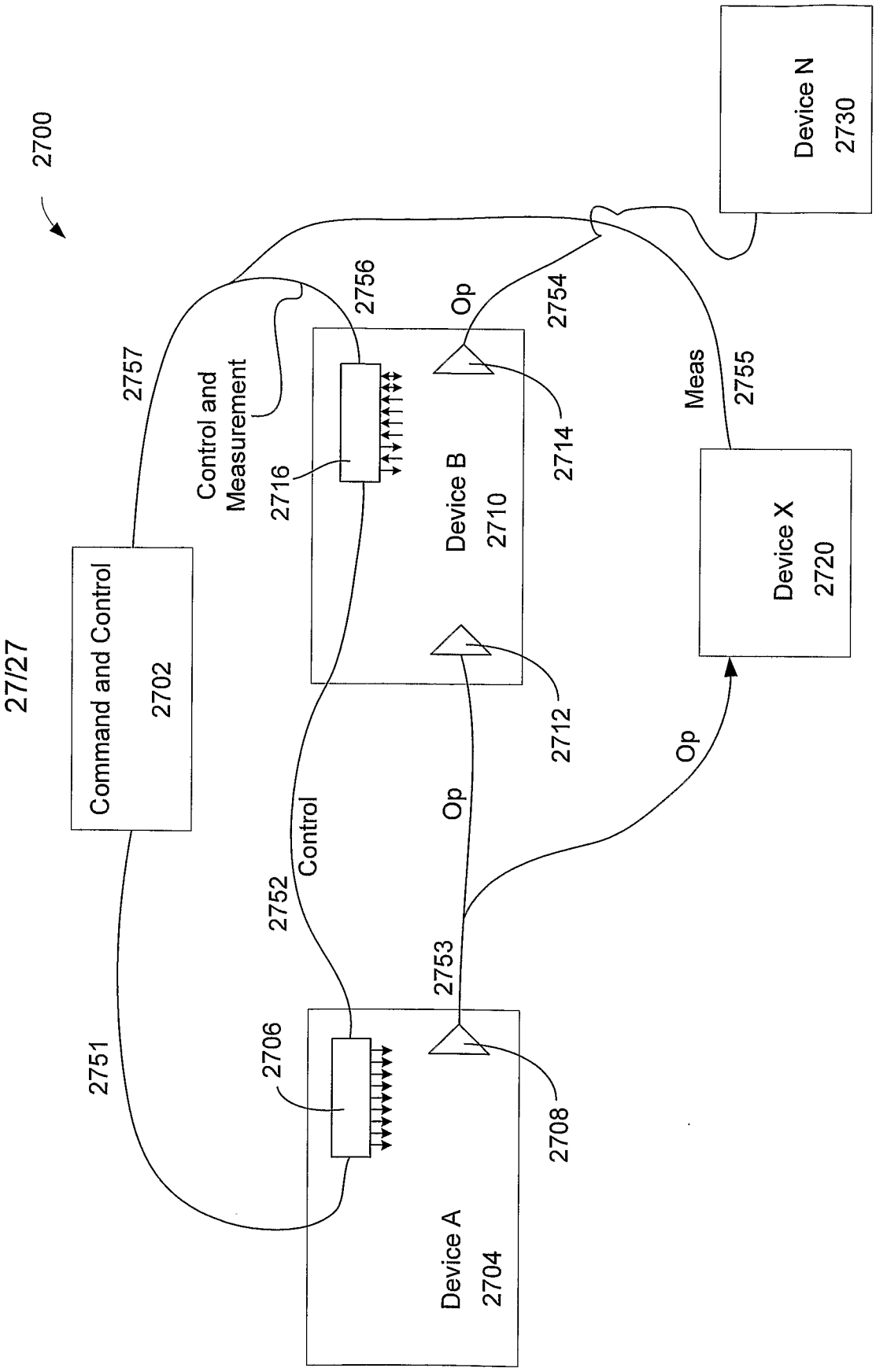

2700
Device N
2730
Command and Control
2702
2757
Control and
Measurement
2756
Op
2754
Meas
2755
Device B
2710
2716
2714
Device X
2720
2712
Op
Control
2752
Op
2753
2751
2706
2708
Device A
2704

FIG. 27