645923

P/00/001
Section 29

AUSTRALIA
Patents Act 1990

PATENT REQUEST : STANDARD PATENT

I/We, being the person(s) identified below as the Applicant(s), request the grant of a Standard Patent to the person(s) identified below as the Nominated Person(s), for an invention described in the accompanying complete specification.

Applicant(s) and Nominated Person(s): MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

Address: 1006, OAZA KADOMA
KADOMA-SHI
OSAKA
JAPAN

Invention Title: MOVING-IMAGE SIGNAL ENCODING APPARATUS

Name(s) of Actual Inventor(s): YUTAKA MACHIDA; TAKESHI YUKITAKE

Address for Service: GRIFFITH HACK & CO
509 ST KILDA ROAD
MELBOURNE VIC 3004

Attorney Code: HA

BASIC CONVENTION APPLICATION DETAILS

Application No:	Country:	Application Date:
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Drawing number recommended to accompany the abstract: 1

DATED: 26 January 1993

MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

GRIFFITH HACK & CO

Patent Attorney for and
on behalf of the Applicant

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Section 29(1)
Regulation 3.1(2)

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NOTICE OF ENTITLEMENT

I/We MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

of 1006, OAZA KADOMA
KADOMA-SHI
OSAKA
JAPAN

being the applicant(s) in respect of an application for a patent for an invention entitled MOVING-IMAGE SIGNAL ENCODING APPARATUS, state the following:

1. The nominated person(s) has/have, for the following reasons, gained entitlement from the actual inventor(s):

   THE NOMINATED PERSON IS THE ASSIGNEE OF THE ACTUAL INVENTORS.

2. The nominated person(s) has/have, for the following reasons, gained entitlement from the basic applicant(s) listed on the patent request:

   THE APPLICANT AND NOMINATED PERSON IS THE BASIC APPLICANT.

3. The basic application(s) listed on the request form is/are the first application(s) made in a Convention country in respect of the invention.

DATE: 26 January 1993

MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

GRIFFITH HACK & CO.

Patent Attorney for and
on behalf of the applicant(s)

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(71) Applicant(s)
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

(72) Inventor(s)
YUTAKA MACHIDA; TAKESHI YUKITAKE

(74) Attorney or Agent
GRIFFITH HACK & CO , GPO Box 1285K, MELBOURNE VIC 3001

(56) Prior Art Documents
AU 571899 34406/84 H04N 7/13 5/94 G11B 27/22

(57) Claim

1. A moving-image signal encoding apparatus characterized by comprising:

means for converting an input image signal into a binary signal;

means for converting said binary signal into a bitstream;

means for converting said bitstream into cells of a certain number of bits each; and

means for adding to within said cells positional information of a plurality of bits which indicates the position of a ~~particular meaning~~ carrying code word within said cells in said bitstream.

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COMPLETE SPECIFICATION

STANDARD PATENT

Applicant(s):

MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

Invention Title:

MOVING-IMAGE SIGNAL ENCODING APPARATUS

The following statement is a full description of this invention, including the best method of performing it known to me/us:

BACKGROUND OF THE INVENTION

This invention relates to a moving-image signal encoding apparatus which is used in video telephone and teleconference.

In general, the moving image signal has large spatial and temporal correlation. The conventional moving-image signal encoding apparatus calculates predicted error value for each pixel by making intraframe prediction and interframe prediction with motion compensation, and removes the correlation existing between the pixels. The moving image signal with the correlation removed has a narrow dynamic range, and takes particular values at a high frequency. If a proper variable length code (for example, huffman code) is assigned to the particular values which occur at a high frequency, the moving image signal can be coded to have a small amount of information.

Fig. 1 is a block diagram of the conventional encoding apparatus for the moving image signal. Referring to Fig. 1, when a digital moving-image signal is applied to an input terminal 101, a motion vector detector 102 detects a motion vector for each block which is a group of a plurality of pixels (for example, 8×8 pixels) by use of the reproduced pixel value of the previous frame read from a frame memory 103. A

prediction circuit 104 receives the motion vector and the reproduced pixel value of the previous frame read from the frame memory 103, and makes interframe prediction with motion compensation, thereby calculating a predicted value. A subtracter 105 subtracts the predicted value from the digital moving-image signal supplied via the input terminal 101 to produce a prediction error value. An encoding circuit 106 encodes the prediction error value at each block and supplies this prediction error value code to an information source encoding circuit 107. The information source encoding circuit 107 receives positional information of the block within the current frame from a block position information generator 108, the motion vector of the block from the motion vector detector 102, and the prediction error value code from the encoding circuit 106, and makes optimum information source encoding according to the appearance probabilities of these values to produce a variable length code. A buffer 109 converts the variable length code into a bitstream. A channel encoding circuit 110 divides the bitstream into units of a plurality of bits each and produces them as cells on a transmission path 111. On the other hand, a decoder 112 locally decodes the prediction error value code produced from the encoding circuit 106, thus reproducing the prediction error value. In addition, an adder 113 adds this reproduced prediction error value and the predicted value from the prediction circuit 104,

thus reproducing the pixel value. This pixel value is written in the frame memory 103.

Therefore, according to this conventional example, the moving image can be encoded to have a small amount of information. In addition, by converting the transmitted information into cells, it is possible to efficiently transmit the moving image at a variable rate.

In the conventional moving-image signal encoding apparatus, however, if a cell is lost on the transmission path, part of the corresponding bitstream is also lost. Thus, since the bitstream is a sequence of variable length codes, the code word included in the bitstream following the lost cell cannot be correctly decoded. In addition, information is lost in the bitstream following the lost cell until the unique code word which can always be recognised appears.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the invention to provide a moving-image signal encoding apparatus in which, when a cell is lost in the transmission path, the lost information can be restricted to the minimum.

The invention provides a moving-image signal encoding apparatus characterised by comprising:

means for converting an input image signal into a binary signal;

means for converting said binary signal into a bitstream;

means for converting said bitstream into cells of a certain number of bits each; and

means for adding to within said cells positional information of a plurality of bits which indicates the position of a carrying code word within said cells in said bitstream.

Therefore, according to this invention, since the positional information of a carrying code word is added to the cells, even if a cell is lost in the transmission path,

it can be decoded from a carrying code word which first appears in the bitstream following the lost cell, thus the lost information being suppressed to the minimum. In addition, since the positional information of a carrying code word is not added to the cells in the transmission path in which no cell is lost, but only the information that the positional information is not added to the cells is added to within the cells, the transmission efficiency can be prevented from being reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic block diagram of the conventional moving-image signal encoding apparatus;

Fig. 2 is a schematic block diagram of one embodiment of the moving-image signal encoding apparatus of the invention;

Fig. 3 is an explanatory diagram to which reference is made in explaining the operation of a cell assembler in the first embodiment of the invention;

Fig. 4 is an explanatory diagram to which reference is made in explaining the operation of the cell assembler in the first embodiment of the invention;

Fig. 5 is an explanatory diagram to which reference is made in explaining the operation of the cell assembler in the second embodiment of the invention;

Fig. 6 is an explanatory diagram to which reference is made in explaining the operation of the cell assembler in the second embodiment of the invention,

DESCRIPTION OF THE PREFERRED EMBODIMENTS

(Embodiment 1)

Embodiments of the invention will be described with reference to the accompanying drawings. Fig. 2 is a block diagram of a first embodiment of the moving-image signal encoding apparatus of the invention. Figs. 3 and 4 are diagrams to which reference is made in explaining the operation of the encoding apparatus shown in Fig. 2.

The operation of the first embodiment will be described below. Referring to Fig. 2, when a digital moving-image signal is supplied to an input terminal 201, a motion vector detection circuit 202 detects a

motion vector of each block which is formed of a group of a plurality of pixels (for example, 8×8 pixels) by use of the reproduced pixel values of the previous frame read from a frame memory 203. A prediction circuit 204 makes interframe prediction with motion compensation and calculates predicted values by use of the motion vector and the reproduced pixel values of the previous frame read from the frame memory 203. A subtracter 205 subtracts the predicted value from the input digital moving-image signal at the input terminal 201, thus producing a prediction error value. An encoding circuit 206 encodes the input prediction error value into a code at each block, and supplies it to an information source encoding circuit 207. The information source encoding circuit 207 receives the positional information of the block within the current frame from a block position information generating circuit 208, the motion vector of this block from the motion vector detection circuit 202, and the code of the prediction error value from the encoding circuit 206, and makes optimum information source encoding in accordance with the appearance probabilities of these information so as to produce a variable length code. A buffer 209 converts the variable length code into a bitstream. A cell assembler 214 divides the bitstream into cells of bits each, divides each cell into a plurality of small regions, and adds to within each cell the positional information indicating the small region from which the information

of a certain pixel block begins. A channel encoding circuit 210 produces cells on a transmission path. The code of the prediction error value produced from the encoding circuit 206 is locally decoded by a decoding circuit 212. An adder 213 adds this reproduced prediction error value and the predicted value from the prediction circuit 204, and thus produces a pixel value, which is written in the frame memory 203.

The operation of the cell assembler 214 in the first embodiment will be described with reference to Fig. 3. The bitstream produced from the buffer 209 is divided into cells of, for example, 352 bits each by the cell assembler 214. Of the 352 bits, for example the first seven bits indicate the positional information, and the remaining 345 bits constitute the bitstream. At the same time, the cell assembler 214 divides the 345-bit bitstream into 115 small regions of, for example, 3 bits, and assigns numbers such as 1, 2, ... 115 to the small regions, respectively. When information of a certain pixel block begins from the K-th small region of a certain cell, K is expressed by a binary value of seven bits and added to the beginning of the corresponding cell as the positional information. In this case, it is assumed that the information of a certain pixel block begins from the first bit of the K-th small region. If the information of a certain pixel block begins from another bit than the first bit of the K-th small region, a bit of, for example, 1 is added

thereat, as shown in Fig. 4, shifting one bit so that the information of a certain pixel block begins from the first bit of the (K+1)-th small region. Such bit shifting is performed so that the information of pixel block corresponds to the first bit of the region. Then, since this pixel block information contains the positional information of the pixel block within the frame, it can be decoded from the same pixel block. When there are two or more pixel blocks within one cell, the number of the small region in which the pixel block information begins and which is closer to the beginning of the cell is added to the beginning of the cell.

Therefore, according to the first embodiment, since the number of the small region in which the information of a certain pixel block begins is added to the beginning of the cell as the positional information, the bitstream following the cell lost in the transmission path can be decoded beginning with the first appearing pixel block. Thus, the loss of information can be minimized.

(Embodiment 2)

A second embodiment will be mentioned. The construction of the second embodiment is the same as that of the first embodiment shown in Fig. 2. The operation of the second embodiment is different in the operation of cell assembler 214 from that of the first embodiment. Only the cell assembler 214 will be described with reference to Figs. 5 and 6.

The bitstream produced from the buffer is divided into cells of, for example, 352 bits each by the cell assembler as shown in Fig. 5. Of the 352 bits, the first bit is the flag bit which indicates whether the positional information is contained within the corresponding cell. If the flag is 0 (reset) as shown in Fig. 5, the positional information is not contained in the corresponding cell, and the 351 bits except the flag bit constitute the bitstream. If the flag bit is 1 (set) as shown in Fig. 6, the seven bits following the flag bit is the positional information. The remaining 344 bits constitute the bitstream. At the same time, the cell assembler 214 divides the bitstream of 344 bits into 86 small regions of, for example, 4 bits each, which are sequentially numbered as 1, 2, ..., 86, respectively. When information of a certain pixel block begins from the K-th small region of a certain cell, K is expressed by a binary value of seven bits and added after the flag bit of the corresponding cell as the positional information. In this case, it is assumed that the information of a certain pixel block begins with the first bit of the K-th small region. If the information of a certain pixel block begins with another bit than the first bit of the K-th small region, for example, a bit of 1 is added thereat to shift one bit so that the information of a certain pixel block can be started from the first bit of the (K+1)-th small region as is similar to the first embodiment as shown in Fig.

4. Such bit shifting is performed so that the information of pixel block corresponds to the first bit of the region. Thus, since the pixel block information contains the positional information within the frame, it can be decoded from the pixel block. When there are two or more pixel blocks within one cell, the number of the small region which is closer to the beginning of the cell and in which the pixel block begins is added to the back of the flag bit that is positioned at the beginning of the cell. The cell assembler properly sets or resets the flag bit to the transmission path in which a cell is lost or not.

Therefore, according to the second embodiment, since the number of the small region in which the information of a certain pixel block starts is added to the back of the flag bit as the positional information, the bitstream can be decoded beginning with the first appearing pixel block which follows the cell lost in the transmission path. Thus, the loss of information can be minimized. In the transmission path in which no cell is lost, only the flag bit is reset, or no positional information is added, and thus the transmission efficiency is not reduced.

While the positional information to be added to the beginning of the cell or the back of the flag bit is expressed by the number of the small region in which the information of a certain pixel block starts as in the first and second embodiments, it may be the number

of the small region in which particular-meaning carrying information such as frame information and pixel information starts as well as the pixel block information.

Moreover, while the number of a small region is used to indicate the position of particular-meaning carrying information within a cell as in the first and second embodiments, the position of the particular-meaning carrying information within a cell may be indicated by other means.

According to this invention, as will be obvious from the embodiments, since the positional information of a plurality of bits is added within the corresponding cell so as to indicate the position of a particular-meaning carrying code word in a certain cell within the bitstream, the bitstream following the lost cell in the transmission path can be decoded beginning with the first appearing particular-meaning carrying code word. Thus, the loss of information can be minimized. In addition, since the information indicating whether the positional information of a particular-meaning carrying code word is added to within a cell is added to within the corresponding cell, the positional information of the particular-meaning carrying code word is not added within the cell in the transmission path in which no cell is lost and thus the transmission efficiency can be prevented from being reduced.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A moving-image signal encoding apparatus characterized by comprising:

means for converting an input image signal into a binary signal;

means for converting said binary signal into a bitstream;

means for converting said bitstream into cells of a certain number of bits each; and

means for adding to within said cells positional information of a plurality of bits which indicates the position of a ~~particular-meaning~~ carrying code word within said cells in said bitstream.

2. A moving-image signal encoding apparatus according to claim 1, characterized by further comprising means for adding to within said cells additional information which indicates the presence or absence of said positional information indicative of the position of said particular-meaning carrying code word contained within said cells in said bitstream.

3. A moving-image signal encoding apparatus according to claim 1, characterized in that said positional information is formed of seven bits.

4. A moving-image signal encoding apparatus according to claim 2, characterized in that said additional information is formed of one bit.

DATED THIS 26TH DAY OF JANUARY 1993
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
By its Patent Attorneys: GRIFFITH HACK & CO
Fellows Institute of Patent Attorneys of Australia

ABSTRACT OF THE DISCLOSURE

A moving-image signal encoding apparatus is provided in which information to be lost is suppressed to a minimum extent when a cell is lost in a transmission line. A cell assembler divides a bitstream into cells of bits and adds to the cells positional information of encoded words having particular meaning within the cell. When the cells are lost in the transmission line, a decoding is allowed from the encoded words having particular meaning which appears at a first bit of bitstream succeeding to the lost cells.

FIG. 1

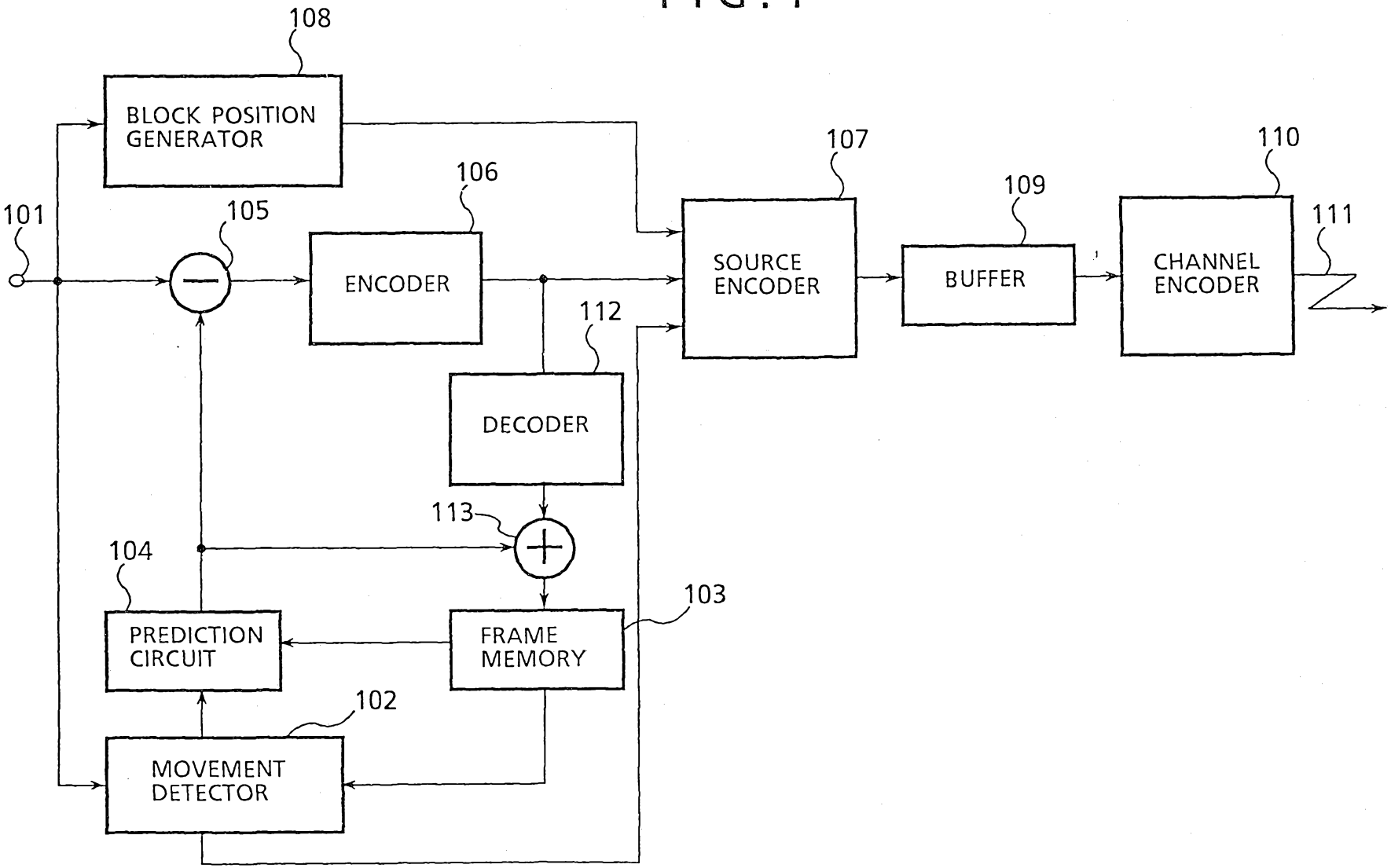

108
BLOCK POSITION GENERATOR
101
105
106
ENCODER
107
SOURCE ENCODER
109
BUFFER
110
CHANNEL ENCODER
111
112
DECODER
113
104
103
PREDICTION CIRCUIT
FRAME MEMORY
102
MOVEMENT DETECTOR

FIG. 2

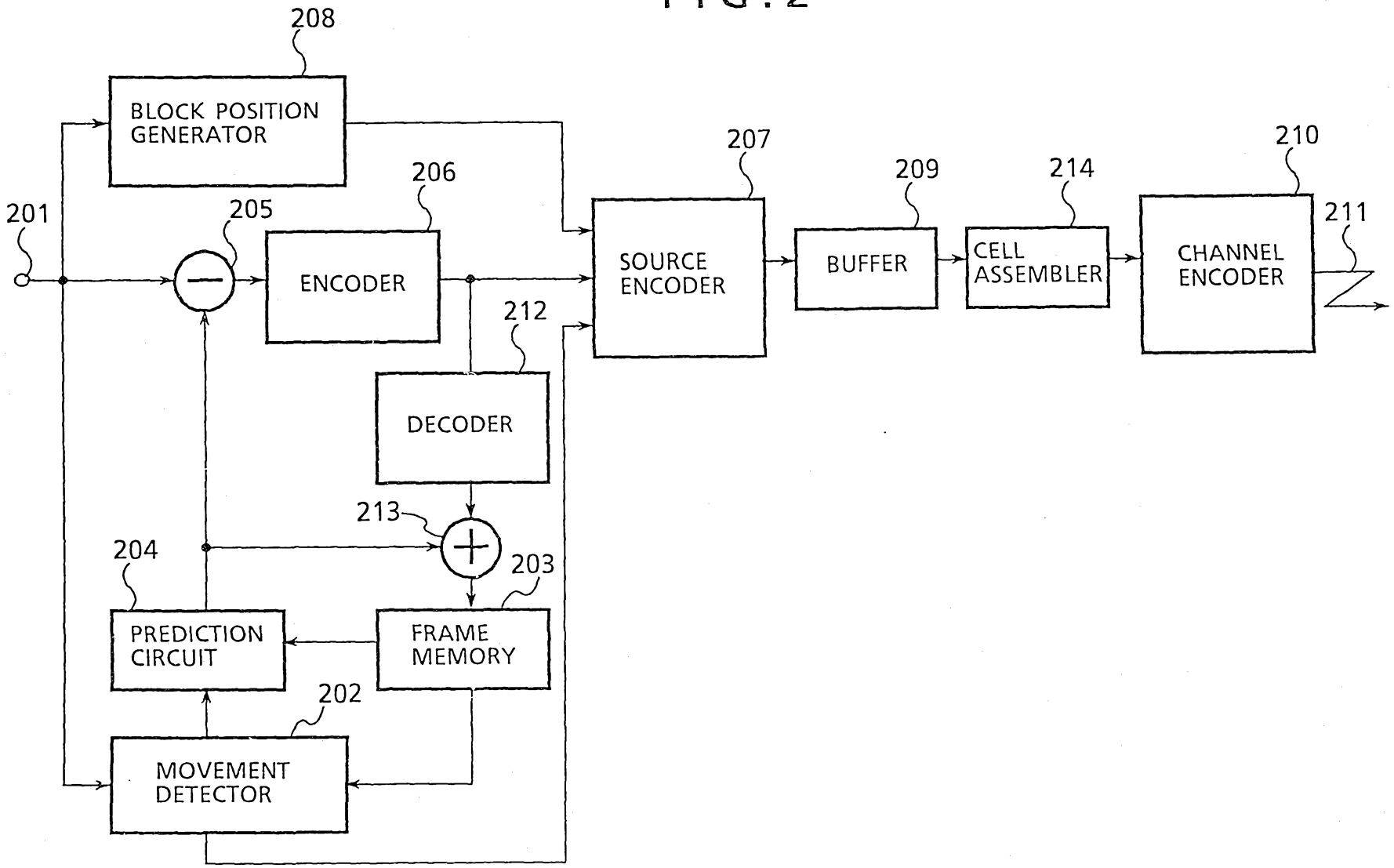


FIG. 3

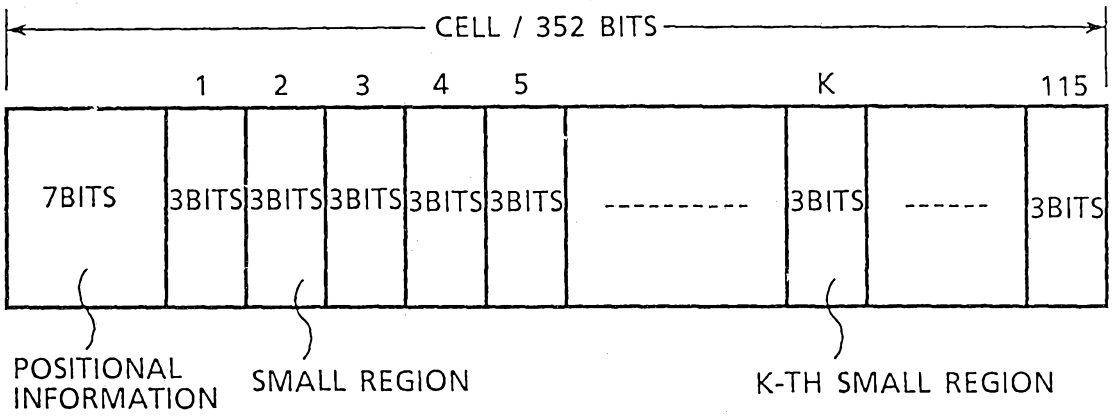

CELL / 352 BITS
1
2
3
4
5
K
115
7BITS
3BITS
3BITS
3BITS
3BITS
3BITS
3BITS
3BITS
POSITIONAL INFORMATION
SMALL REGION
K-TH SMALL REGION

FIG. 4

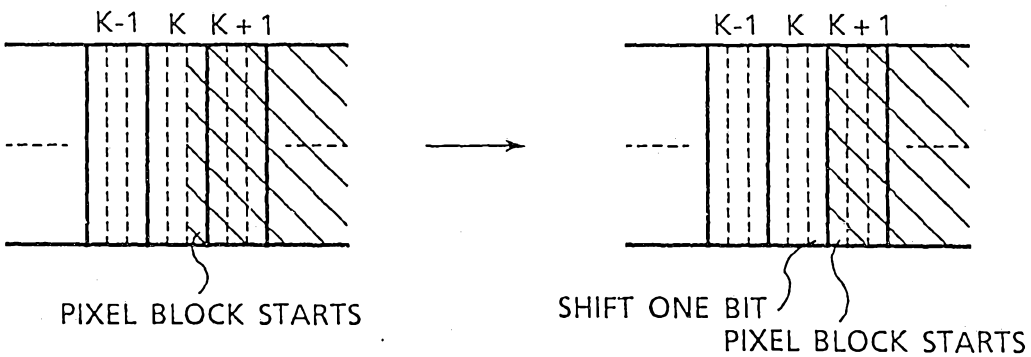

K-1
K
K+1
PIXEL BLOCK STARTS
K-1
K
K+1
SHIFT ONE BIT
PIXEL BLOCK STARTS

FIG. 5

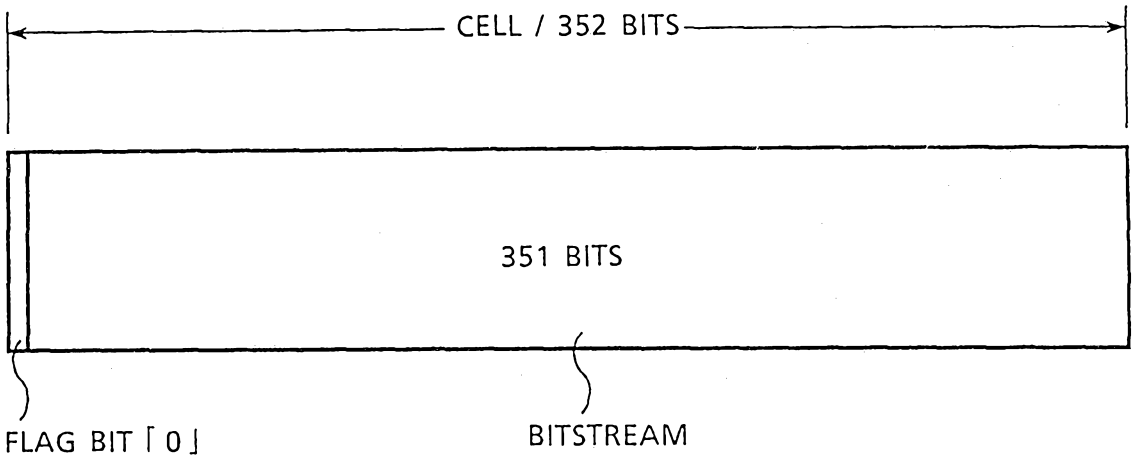
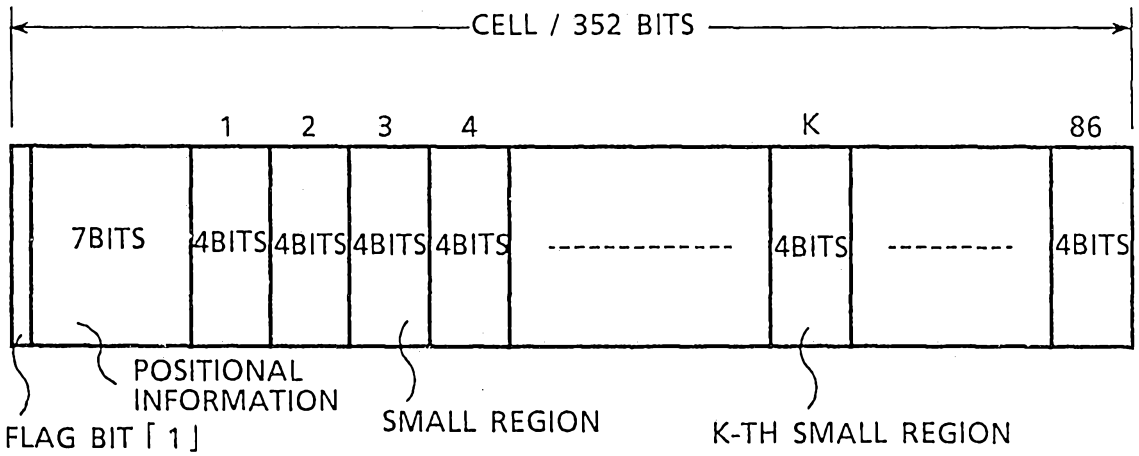

CELL / 352 BITS
351 BITS
FLAG BIT「0」
BITSTREAM

FIG. 6


CELL / 352 BITS
1
2
3
4
K
86
7BITS
4BITS
4BITS
4BITS
4BITS
4BITS
4BITS
POSITIONAL INFORMATION
FLAG BIT「1」
SMALL REGION
K-TH SMALL REGION