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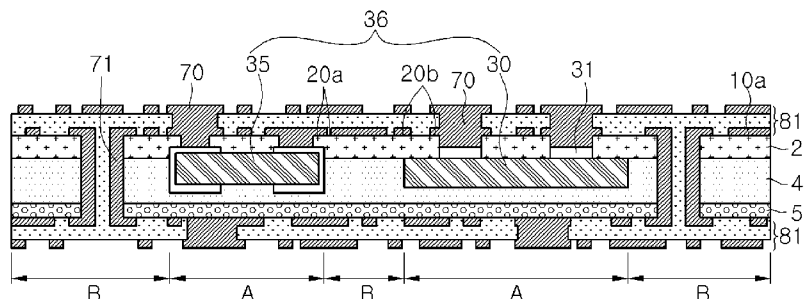
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(54) Title: PRINTED CIRCUIT BOARD AND METHOD OF MANUFACTURING THE SAME

[Fig. 10]



(57) Abstract: Disclosed are a printed circuit board and a method of manufacturing the same. The method includes preparing a metal layer formed with an adhesive layer on which first and second regions are defined; attaching an electronic element to the first region of the adhesive layer; forming an insulating layer on the second region of the adhesive layer to surround the electronic element; and forming a circuit pattern by patterning the metal layer.

Description

Title of Invention: PRINTED CIRCUIT BOARD AND METHOD OF MANUFACTURING THE SAME

Technical Field

- [1] The disclosure relates to a printed circuit board and a method of manufacturing the same.

Background Art

- [2] Recently, as current tendency has tended toward the lightweight, slim structure and small size, a thickness of a printed circuit board (PCB) is gradually reduced. Since the PCB is manufactured with a thin thickness and has lots of elements in a compact size, various problems may occur.
- [3] For instance, due to difference in coefficient of thermal expansion (CTE) among a chip, a circuit pattern, an adhesive layer and an insulating layer of the PCB, cracks or warpage may occur in the PCB.
- [4] In particular, according to the related art, an adhesive layer is locally formed on a region corresponding to a chip, so that the region formed with the adhesive layer may have the characteristic different from the characteristic of other regions. For this reason, severe crack or warpage may occur in the PCB.
- [5] In addition, air bubbles are generated between the adhesive layer and the insulating layer, thereby causing the electric short.

Disclosure of Invention

Technical Problem

- [6] The embodiment provides a PCB for minimizing crack or warpage and a method of manufacturing such a PCB.
- [7] The embodiment provides a PCB manufactured through a simple process and a method of manufacturing such a PCB.

Solution to Problem

- [8] A method of manufacturing a printed circuit board according to the embodiment includes preparing a metal layer formed with an adhesive layer on which first and second regions are defined; attaching an electronic element to the first region of the adhesive layer; forming an insulating layer on the second region of the adhesive layer to surround the electronic element; and forming a circuit pattern by patterning the metal layer.
- [9] A printed circuit board according to the embodiment includes a circuit pattern; an adhesive layer on the circuit pattern; an electronic element on a first region of the adhesive layer; and an insulating layer formed on a second region of the adhesive layer

while surrounding the electronic element, wherein the second region is defined as a region besides the first region, and the adhesive layer is formed over the first and second regions.

Advantageous Effects of Invention

- [10] According to the embodiment, the adhesive layer is formed on the second region as well as the first region where the electronic element is positioned, so that the adhesive layer can be uniformly formed in a large area. Thus, the PCB may have uniform characteristics over the whole area thereof, thereby preventing the crack or warpage from occurring in the PCB.
- [11] In addition, since the adhesive layer is formed over the whole area of the metal layer, the manufacturing process can be simplified as compared with a case in which the adhesive layer is locally formed on the region where the electronic element is positioned.

Brief Description of Drawings

- [12] FIGS. 1 to 10 are sectional views showing a method of manufacturing a PCB according to the embodiment.

Mode for the Invention

- [13] In the description of an embodiment, it will be understood that, when a layer (or film), a region, a pattern, or a structure is referred to as being on or under another substrate, another layer (or film), another region, another pad, or another pattern, it can be directly or indirectly on the other substrate, layer (or film), region, pad, or pattern, or one or more intervening layers may also be present. Further, on or under of each layer is determined based on the drawing.
- [14] The thickness and size of each layer shown in the drawings can be exaggerated, omitted or schematically drawn for the purpose of convenience or clarity. In addition, the size of elements does not utterly reflect an actual size.
- [15] Hereinafter, a PCB and a method of manufacturing the same according to the embodiment will be described in detail with reference to FIGS. 1 to 10.
- [16] As shown in FIG. 1, a first metal layer 10 having a first adhesive layer 20 is prepared.
- [17] According to the embodiment, the first adhesive layer 20 is formed over first regions A where electronic elements 36 (see, FIGS. 3 to 5) are positioned and second regions B besides the first regions A. The first regions A may include a region where the electronic element 36 is actually positioned and a region located around the electronic element 36 by taking the process tolerance into consideration. The second regions B may include a region interposed between the electronic elements 36, a region around a via hole 61 (see, FIG. 7), and a margin region, which is inevitably formed.

- [18] According to the embodiment, the first adhesive layer 20 is formed on a part or a whole area of the second regions B as well as the first regions A such that the first adhesive layer 20 can be formed over 80% of the whole area of the first metal layer 10. In this case, the crack or warpage of the PCB can be minimized.
- [19] The first adhesive layer 20 can be formed over the whole area of one surface of the first metal layer 10. The expression formed over the whole area of the first metal layer 10 may include a situation in which the first adhesive layer 20 is not formed on specific regions of the first metal layer 10, inevitably.
- [20] The first metal layer 10, for example, includes at least one selected from the group consisting of copper (Cu), gold (Au), silver (Ag), aluminum (Al), nickel (Ni) and tin (Sn). In addition, the first adhesive layer 20 may include semi-cured (B-stage) resin material having adhesive property, such as epoxy resin or phenol resin.
- [21] The thickness of the first adhesive layer 20 may vary depending on applications. If the first adhesive layer 20 is too thin, leakage current or electric short may occur. Thus, the first adhesive layer 20 must have the thickness sufficient for preventing the leakage current or electric short. For instance, the first adhesive layer 20 may have the thickness of about 10 to 25.
- [22] The first adhesive layer 20 can be obtained by laminating an adhesive film having a predetermined thickness onto the first metal layer 10. In addition, the first adhesive layer 20 can be obtained by roll coating adhesive material onto one surface of the first metal layer 10. Thus, the manufacturing process is simplified while improving the reliability and precision of the PCB.
- [23] In more detail, according to the related art, the adhesive layer is locally formed on the region where the chip is attached through the printing scheme or the distribution scheme. In this case, air bubbles may be generated when the adhesive layer is formed, so that leakage current or electric discharge may occur due to the air bubbles, causing the electric short. In addition, in order to locally form the adhesive layer, an alignment process and/or a patterning process is necessary to form the adhesive layer on the desired region with the desired shape, so that the manufacturing process is complicated.
- [24] In addition, the thickness difference may occur between the region having the adhesive layer and the region having no adhesive layer, so that the adhesive layer may not be uniformly formed. For this reason, when the adhesive layer is cured, the crack or warpage may occur in the PCB due to difference in coefficient of thermal expansion (CTE). As a result, the chip may be damaged during the manufacturing process and failure of electric connection may occur. In addition, the circuit pattern, which will be formed later, may be misaligned, so that the degree of precision may be degraded.
- [25] Meanwhile, according to the present embodiment, the first adhesive layer 20 is

laminated or roll-coated onto the first metal layer 10, so that air bubbles generated during the manufacturing process can be minimized. In addition, since the first adhesive layer 20 is formed over the whole area of the first metal layer 10, the alignment process and the patterning process may be omitted. Therefore, the manufacturing process can be simplified.

- [26] Further, since the first adhesive layer 20 is formed over the whole area of the first metal layer 10, the crack or warpage occurring in the PCB due to the difference in CTE can be minimized. In addition, the first adhesive layer 20 can be formed with the uniform thickness, so that the electronic element 36 is prevented from being damaged and the degree of precision for the circuit pattern can be improved.
- [27] Then, as shown in FIG. 2, the electronic elements 36 are attached onto the first adhesive layer 20. The electronic element 36 may include at least one of a chip 30 and a passive element 35.
- [28] The chip 30 may include a bare chip or a wave level package (WLP) chip obtained by forming a redistribution layer of the bare chip, but the embodiment is not limited thereto. The chip may include a connection terminal 31 electrically connected to other circuit pattern, chip or passive element.
- [29] Referring to FIG. 2, the connection terminal 31 of the chip 30 is attached to the first adhesive layer 20, but the embodiment is not limited thereto. That is, according to another embodiment, a surface of the chip 30 having no connection terminal 31 can be attached to the first adhesive layer 20. That is, the attachment surface of the chip 30 to the first adhesive layer 20 may vary depending on applications.
- [30] The passive element 35 may include a resistor, an inductor or a capacitor. The passive element 35 can also be freely attached to the first adhesive layer 20 depending on applications.
- [31] The first adhesive layer 20 is under the B stage and has adhesive property, so that the electronic elements 36 can be easily attached to the first adhesive layer 20 by pressing the electronic elements 36 against the first adhesive layer 20 while applying heat or pressure to the electronic elements 36. In addition, after the electronic elements 36 have been attached to the first adhesive layer 20, the first adhesive layer 20 is cured to securely fix the electronic elements 36. For instance, the first adhesive layer 20 can be cured by applying heat or ultraviolet ray onto the first adhesive layer 20.
- [32] Then, as shown in FIGS. 3 and 4, an insulating layer 40 is formed on the second regions B of the first adhesive layer 20 in such a manner that the electronic elements 36 are surrounded by the insulating layer 40. The insulating layer 40 may be under the B stage. In addition, a second metal layer 50 having a second adhesive layer 51 can be formed on the insulating layer 40.
- [33] For instance, as shown in FIG. 3, the insulating layer 40 includes a first layer 41

having openings 41a corresponding to the electronic elements 36 and thickness corresponding to that of the electronic elements 36, and a second layer 42 covering the electronic elements 36 and the first layer 41.

[34] Although one first layer 41 and one second layer 42 are shown in FIG. 3, the embodiment is not limited thereto. According to the embodiment, a plurality of first and second layers 41 and 42 can be prepared.

[35] Selectively, as shown in FIG. 4, the insulating layer 40 may include a recess having a shape corresponding to the electronic elements 36.

[36] Selectively, as shown in FIG. 5, the insulating layer 40 may include an opening 40a corresponding to the electronic elements 36 and have a thickness corresponding to that of the electronic elements 36.

[37] According to the embodiment, the insulating layer 40 may include resin material having adhesive property, such as epoxy resin or phenol resin. The insulating layer 40 may include an ABF (Ajinomoto buildup film) or a polyimide film. In addition, the insulating layer 40 may include a prepreg which can be obtained by infiltrating thermosetting resin into glass fiber.

[38] The second metal layer 50 formed with the second adhesive layer 51 may be identical to the first metal layer 10 formed with the first adhesive layer 20 and aligned on the insulating layer 40 such that the top surface of the second metal layer 50 can be exposed.

[39] As shown in FIG. 6, the insulating layer 40 and the second metal layer 50 formed with the second adhesive layer 51 are placed on the first adhesive layer 20 and pressed against the first adhesive layer 20. Thus, the insulating layer 40 is formed on the first adhesive layer 20 and the electronic elements 36, the second adhesive layer 51 is formed on the insulating layer 40, and the second metal layer 50 is formed on the second adhesive layer 51.

[40] Referring to FIG. 6, the insulating layer 40 is formed on the electronic elements 36 based on the structure shown in FIGS. 3 and 4. Although not shown in the drawings, the electronic elements 36 may directly make contact with the first adhesive layer 51 based on the structure shown in FIG. 5.

[41] At this time, since the insulating layer 40 is under the B-stage, the electronic elements 36 can be securely fixed by curing the insulating layer 40 after the pressing process. In order to cure the insulating layer 40, heat and ultraviolet ray may be applied to the insulating layer 40.

[42] Meanwhile, referring to FIGS. 3 to 6, the second metal layer 50 formed with the second adhesive layer 51 is pressed against the insulating layer 40, but the embodiment is not limited thereto. According to another embodiment, only the second metal layer 50 can be aligned on the insulating layer 40 or RCC (resin coated Cu-foil) is aligned on

the insulating layer 40 to press the second metal layer 50 or the RCC against the insulating layer 40. In this case, the second metal layer or the RCC is formed on the insulating layer 40. If the RCC is formed on the insulating layer 40, a resin layer (not shown) is formed on the insulating layer 40 and a second metal layer 50 including Cu-foil is formed on the resin layer.

[43] Then, as shown in FIG. 7, first via holes 60 are formed to partially expose the electronic elements 36. If it is necessary to electrically connect a circuit pattern 80 (see, FIG. 9), which will be formed on both surfaces of the PCB, second via holes 61 can be formed. The PCB is turned over in FIG. 7 for the purpose of explanation.

[44] The first and second via holes 60 and 61 can be formed through laser drilling, selective etching or chemical etching.

[45] After that, as shown in FIG. 8, a plating process is performed with respect to the first and second via holes 60 and 61 to form first and second conductive vias 70 and 71. In order to form the first and second conductive vias 70 and 71, a seed layer is formed through an electroless plating process and then an electroplating process is performed.

[46] The first and second conductive vias 70 and 71 can be formed by using metal including at least one selected from the group consisting of copper (Cu), gold (Au), silver (Ag), aluminum (Al), nickel (Ni) and tin (Sn).

[47] Then, as shown in FIG. 9, the circuit pattern 80 is formed by selectively removing the first and second metal layers 10 and 50. In order to form the circuit pattern 80, a photoresist pattern (not shown) is formed on the first and second metal layers 10 and 50 and the metal layers 10 and 50 are selectively etched by using the photoresist pattern as a mask. The method of forming the metal layers 10 and 50 is generally known in the art, so detailed description thereof will be omitted.

[48] Referring to FIGS. 9 and 10, a circuit pattern unit 81 can be formed by repeatedly forming the insulating layer, the circuit pattern and the conductive via on the circuit pattern 80 according to the circuit design of the PCB. That is, the circuit pattern unit 81 may include a plurality of insulating layers, circuit patterns and conductive vias. The method for forming the circuit pattern unit 81 is generally known in the art, so detailed description thereof will be omitted. The circuit pattern unit 81 shown in FIG. 10 is illustrative purpose only, and the circuit pattern unit 81 may be designed with various configurations.

[49] Then, a solder mask or a solder ball can be formed on the circuit pattern unit 81 according to the circuit design of the PCB to make electric connection with other circuit pattern unit, electronic elements or substrates.

[50] Referring to FIG. 10, in the PCB according to the embodiment, the first adhesive layer 20 is positioned in a first circuit pattern 10a formed by the first metal layer 10, and the electronic elements 36 are positioned on the first adhesive layer 20.

- [51] The first adhesive layer 20 is formed on the second regions B having no electronic elements 36 as well as the first regions A having the electronic elements 36. For instance, the second regions B include a region between the electronic elements 36 (for instance, between the chip 30 and the passive element 35), and a region where the second conductive via 71 is formed.
- [52] The first adhesive layer 20 can be continuously formed on adjacent first and second regions A and B. For instance, a portion 20b of the first adhesive layer 20 for attaching the chip 30 serving as a first electronic element may be integrally formed with a portion 20a of the first adhesive layer 20 for attaching the passive element 35 serving as a second electronic element in the second region B shown in the center of FIG. 10. In contrast, according to the related art, in which the adhesive layer is locally formed on the region where the chip is provided, the adhesive layer is divided to attach the electronic elements spaced apart from each other.
- [53] The above structure of the embodiment can be achieved because the first adhesive layer 20 is formed over the whole area (80% or more) of the first metal layer 10 when the first metal layer 10 having the first adhesive layer 20 is prepared. For example, the first adhesive layer 20 may occupy 80% or more relative to the whole area of the PCB.
- [54] Although the exemplary embodiments of the present invention have been described, it is understood that the present invention should not be limited to these exemplary embodiments but various changes and modifications can be made by one ordinary skilled in the art within the spirit and scope of the present invention as hereinafter claimed.

Industrial Applicability

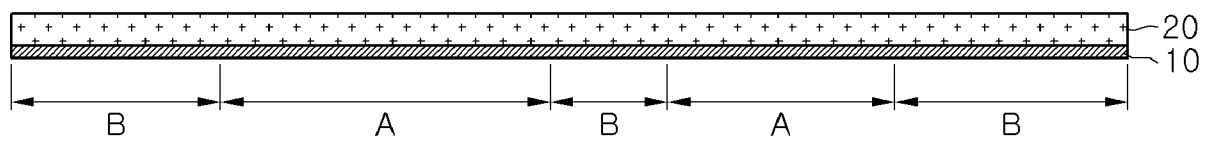
- [55] The embodiments are applicable to the PCB and the method of manufacturing the same.
- [56]
- [57]

Claims

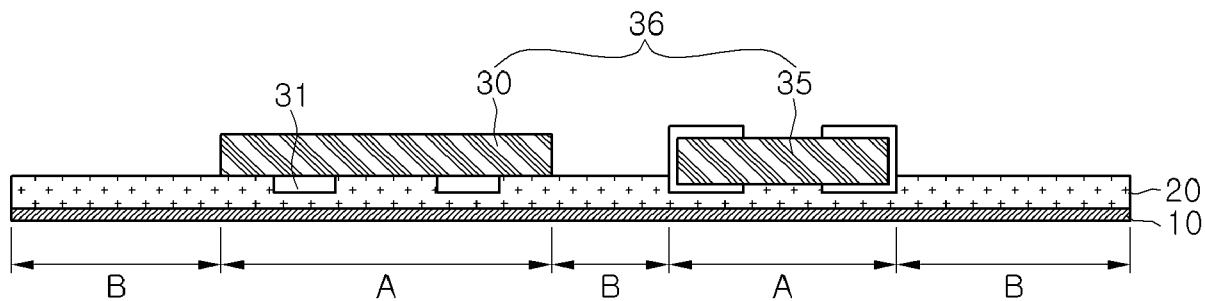
- [Claim 1] A method of manufacturing a printed circuit board, the method comprising:
preparing a metal layer formed thereon with an adhesive layer on which first and second regions are defined;
attaching an electronic element to the first region of the adhesive layer;
forming an insulating layer on the second region of the adhesive layer such that the electronic element is surrounded by the insulating layer;
and
forming a circuit pattern by patterning the metal layer.
- [Claim 2] The method of claim 1, wherein the adhesive layer has an area corresponding to 80% or more relative to a whole area of the metal layer in the preparing the metal layer.
- [Claim 3] The method of claim 2, wherein the adhesive layer is formed over a whole area of one surface of the metal layer in the preparing the metal layer.
- [Claim 4] The method of claim 1, wherein the electronic element includes first and second electronic elements spaced apart from each other, and a first portion of the adhesive layer, to which the first electronic element is attached, and a second portion of the adhesive layer, to which the second electronic element is attached, are integrally formed.
- [Claim 5] The method of claim 1, wherein the adhesive layer includes B-stage resin in the preparing the metal layer, and the adhesive layer is cured after the attaching electronic element to the adhesive layer.
- [Claim 6] The method of claim 1, wherein the adhesive layer has a thickness of about 10 to 25.
- [Claim 7] The method of claim 1, wherein the adhesive layer is laminated or roll-coated on the metal layer in the preparing the metal layer.
- [Claim 8] The method of claim 1, wherein an additional metal layer is formed simultaneously with the insulating layer in the forming the insulating layer, and the metal layer is patterned together with the additional metal layer in the forming the circuit pattern.
- [Claim 9] The method of claim 1, wherein an additional adhesive layer and an additional metal layer are formed simultaneously with the insulating layer in the forming the insulating layer, and the metal layer is patterned together with the additional metal layer in the forming the circuit pattern.

- [Claim 10] The method of claim 1, wherein the insulating layer formed on the adhesive layer is pressed against the adhesive layer in the forming the insulating layer.
- [Claim 11] The method of claim 1, wherein the insulating layer includes an opening corresponding to the electronic element.
- [Claim 12] The method of claim 1, wherein the insulating layer includes a first layer having an opening corresponding to the electronic element and a second layer covering the first layer and the electronic element.
- [Claim 13] The method of claim 1, wherein the insulating layer includes a recess corresponding to the electronic element.
- [Claim 14] A printed circuit board comprising:
a circuit pattern;
an adhesive layer on the circuit pattern;
an electronic element on a first region of the adhesive layer; and
an insulating layer formed on a second region of the adhesive layer while surrounding the electronic element,
wherein the second region is defined as a region besides the first region, and the adhesive layer is formed over the first and second regions.
- [Claim 15] The printed circuit board of claim 14, wherein a first portion of the adhesive layer aligned in the first region is integrally formed with a second portion of the adhesive layer aligned in the second region.
- [Claim 16] The printed circuit board of claim 14, wherein the adhesive layer has an area corresponding to 80% or more relative to a whole area of the printed circuit board.
- [Claim 17] The printed circuit board of claim 14, wherein the electronic element includes first and second electronic elements spaced apart from each other, and a first portion of the adhesive layer, to which the first electronic element is attached, and a second portion of the adhesive layer, to which the second electronic element is attached, are integrally formed.

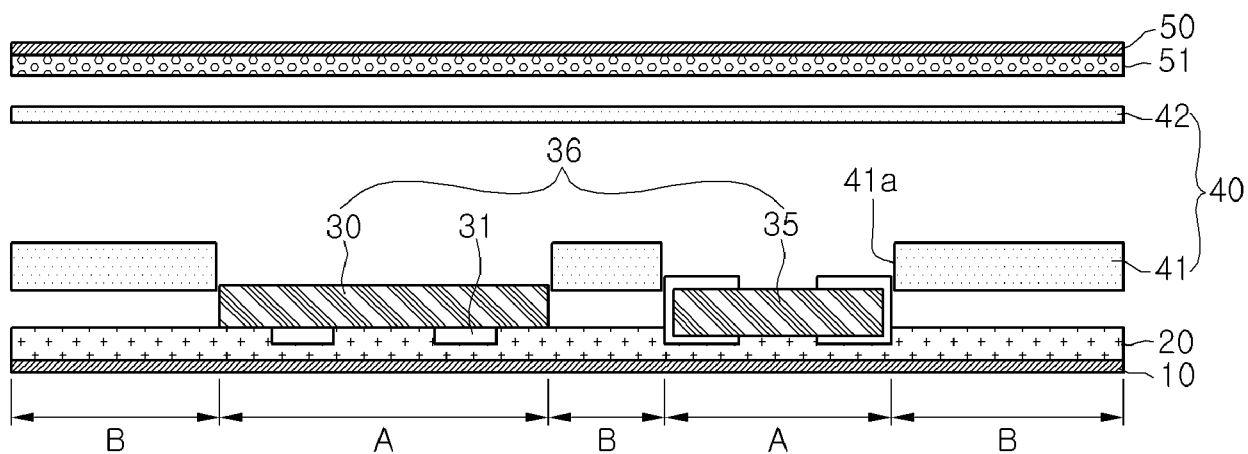
[Fig. 1]



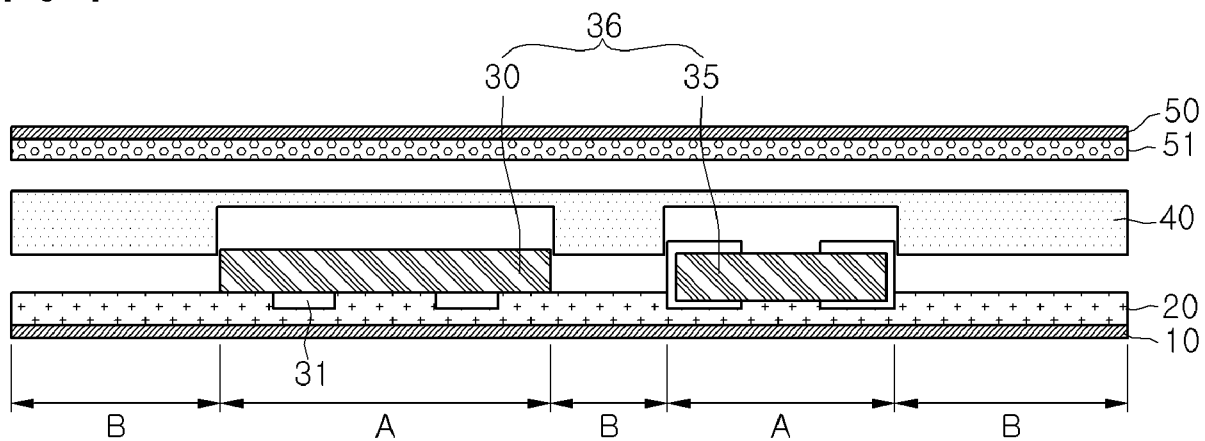
[Fig. 2]



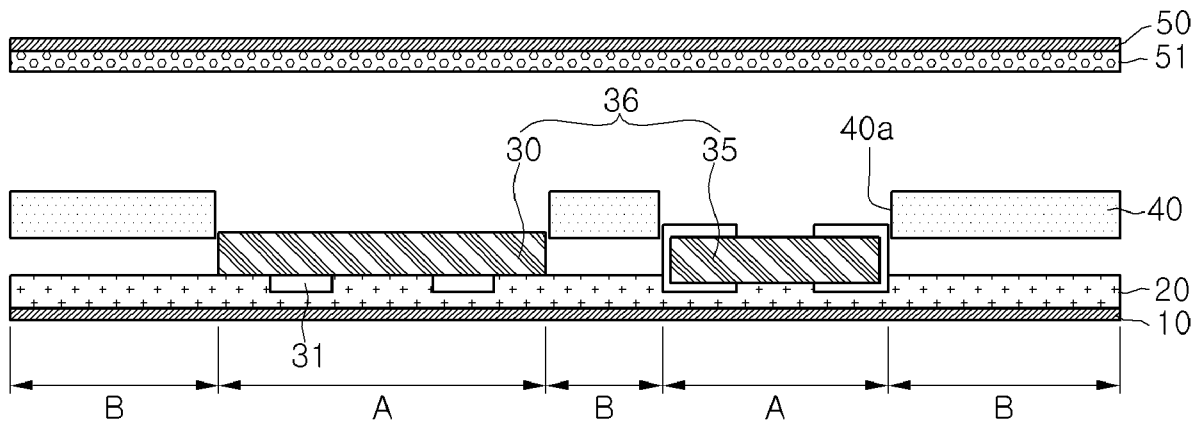
[Fig. 3]



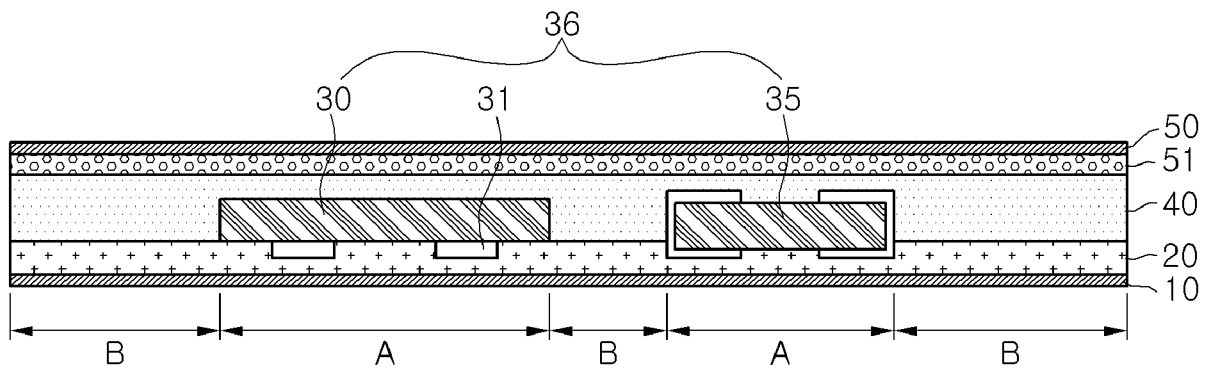
[Fig. 4]



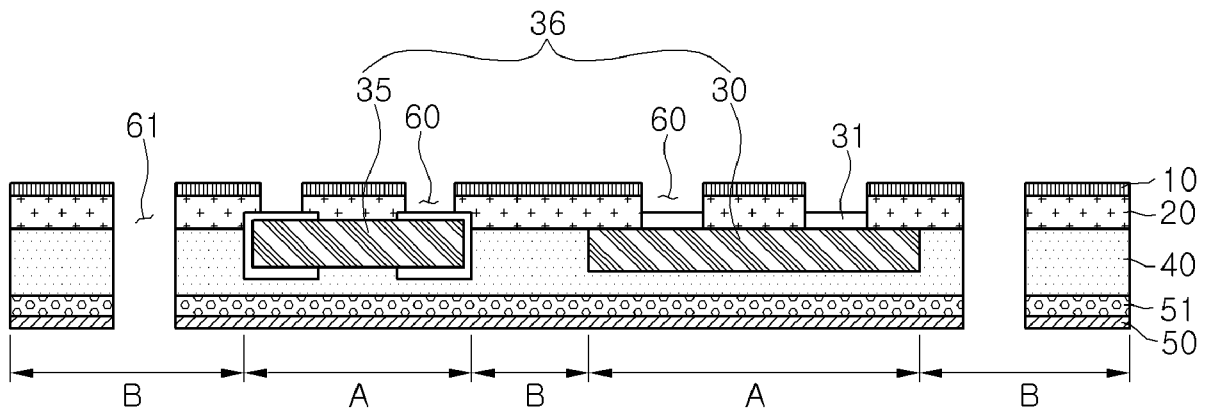
[Fig. 5]



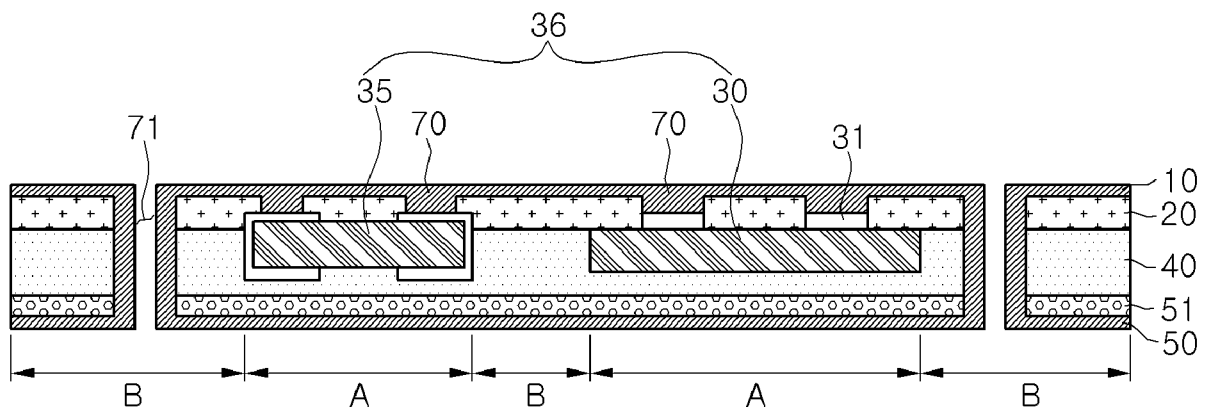
[Fig. 6]



[Fig. 7]



[Fig. 8]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2010/004460**A. CLASSIFICATION OF SUBJECT MATTER****H05K 1/18(2006.01)i, H05K 3/30(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H05K 1/18; H05K 3/30

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: embedded, PCB, adhesive**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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Date of the actual completion of the international search

29 MARCH 2011 (29.03.2011)

Date of mailing of the international search report

01 APRIL 2011 (01.04.2011)

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Telephone No. 82-42-481-8500



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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