

March 28, 1967

D. I. URQUHART-PULLEN

3,311,707

TIME ASSIGNMENT SPEECH INTERPOLATION SYSTEM

Filed June 26, 1963

8 Sheets-Sheet 1

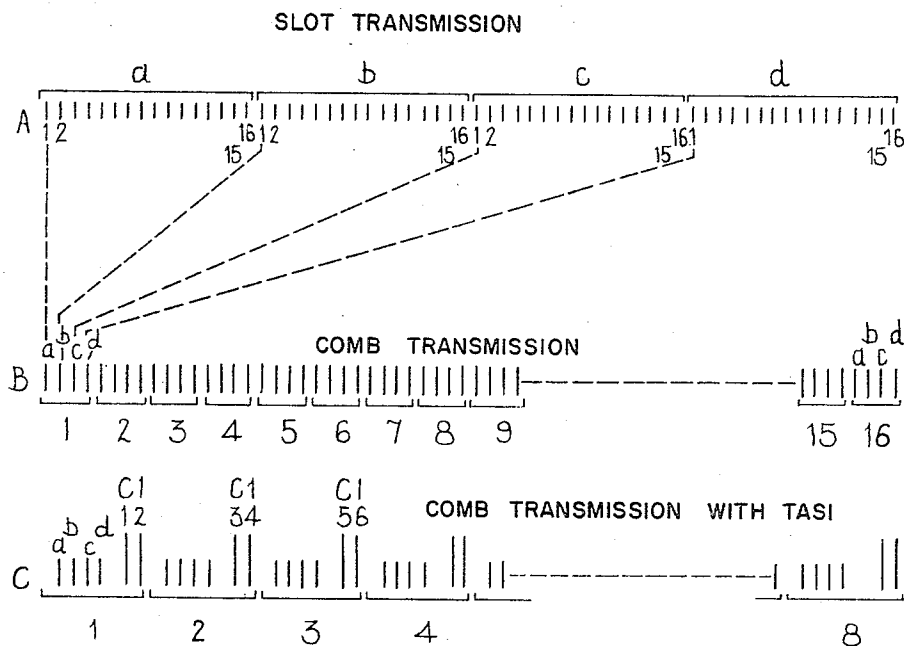


Fig. 1. PRIOR ART

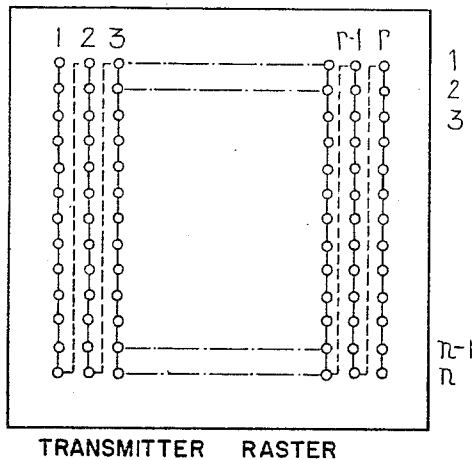


Fig. 2. PRIOR ART

March 28, 1967

D. I. URQUHART-PULLEN

3,311,707

TIME ASSIGNMENT SPEECH INTERPOLATION SYSTEM

Filed June 26, 1963

8 Sheets-Sheet 2

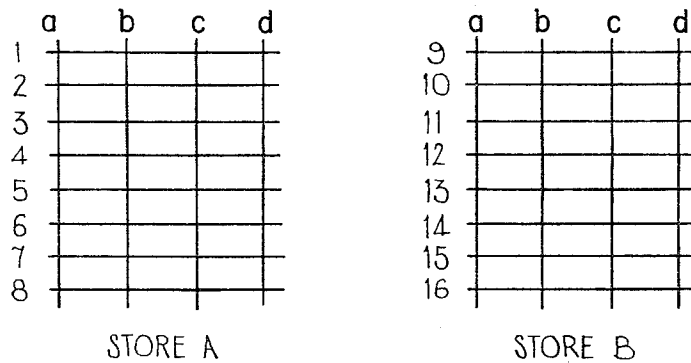
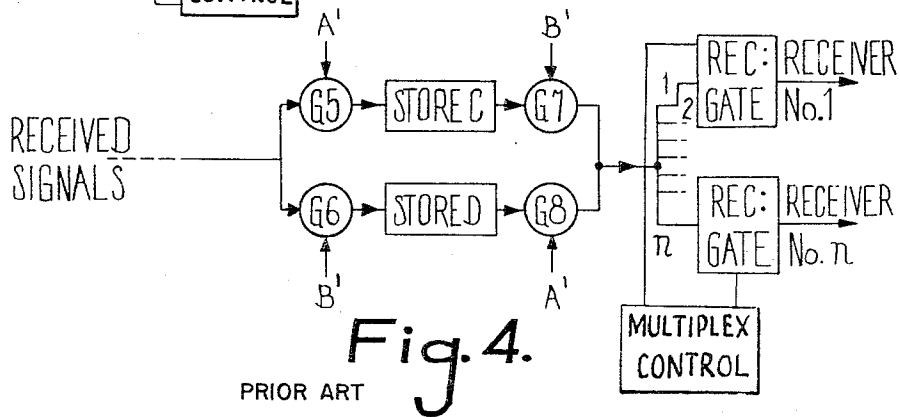
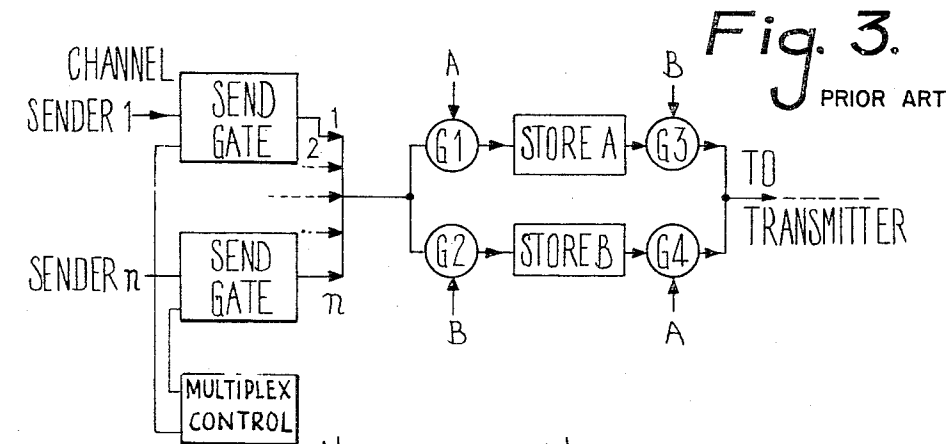


Fig. 5.

March 28, 1967

D. I. URQUHART-PULLEN

3,311,707

TIME ASSIGNMENT SPEECH INTERPOLATION SYSTEM

Filed June 26, 1963

8 Sheets-Sheet 3

STORE A		STORE B	
READ	WRITE	READ	WRITE
1b, 1c, 1d, 1a	a1, a2, a3, a4, a5, a6, a7, a8	15a, 15b, 15c, 15d	a9, a10, a11, a12, a13, a14, a15, a16
3c, 3d, 3a, 3b	b1, b2, b3, b4, b5, b6, b7, b8	9b, 9c, 9d, 9a	b9, b10, b11, b12, b13, b14, b15, b16
4d, 4a, 4b, 4c	c1, c2, c3, c4, c5, c6, c7, c8	10c, 10d, 10a, 10b	c9, c10, c11, c12, c13, c14, c15, c16
6a, 6b, 6c, 6d	d1, d2, d3, d4, d5, d6, d7, d8	13d, 13a, 13b, 13c	d9, d10, d11, d12, d13, d14, d15, d16

Fig. 6.

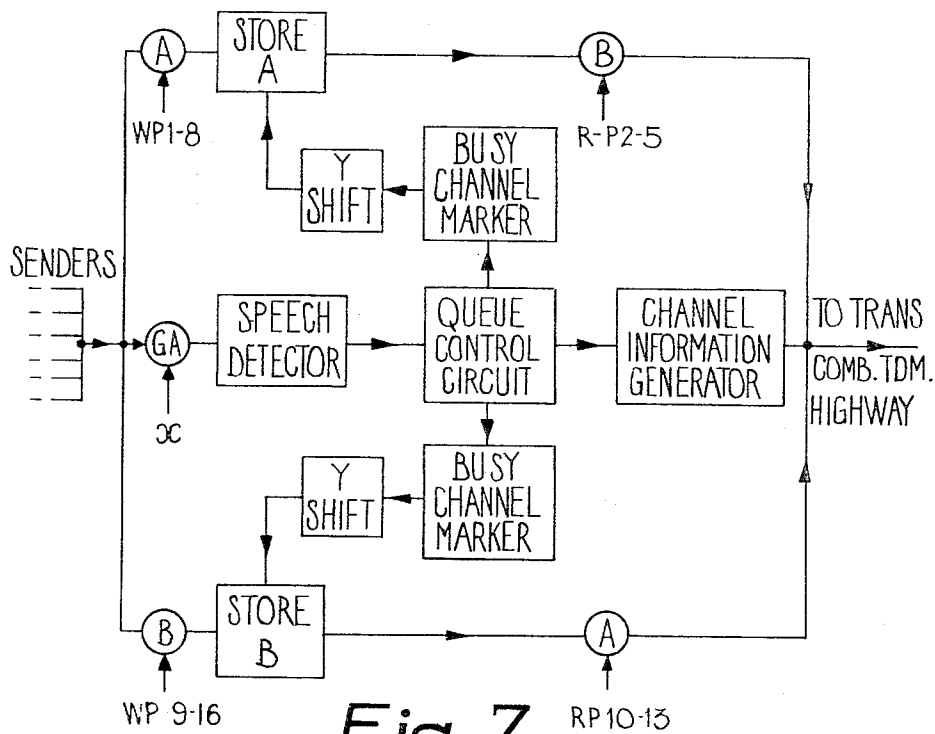
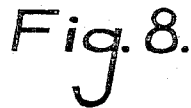


Fig. 7.

3,311,707

8 Sheets-Sheet 4



March 28, 1967

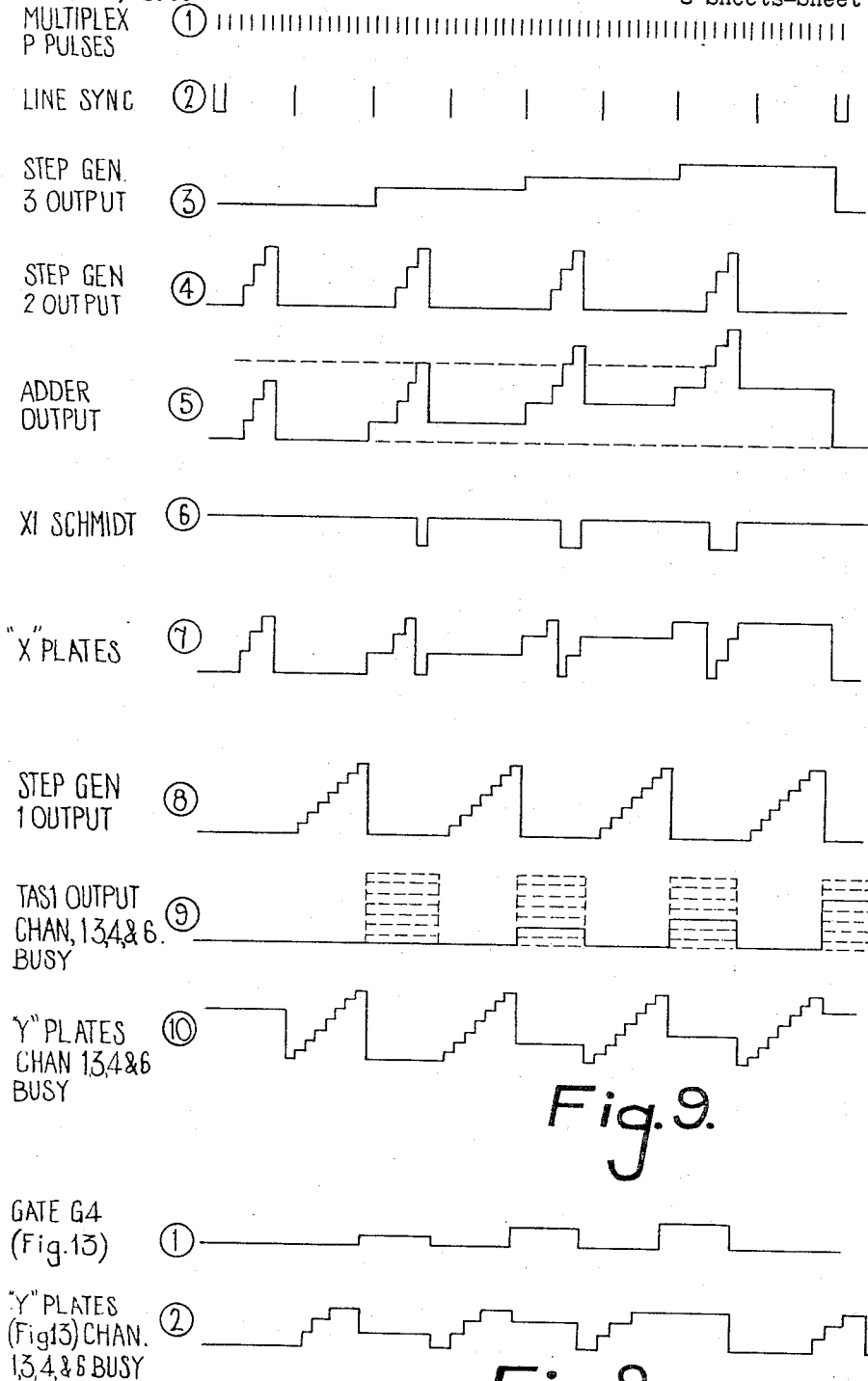
D. I. URQUHART-PULLEN

3,311,707

TIME ASSIGNMENT SPEECH INTERPOLATION SYSTEM

Filed June 26, 1963

8 Sheets-Sheet 5



March 28, 1967

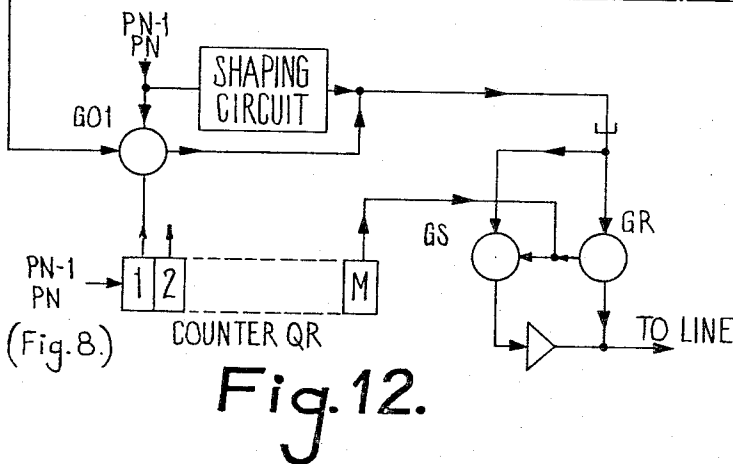
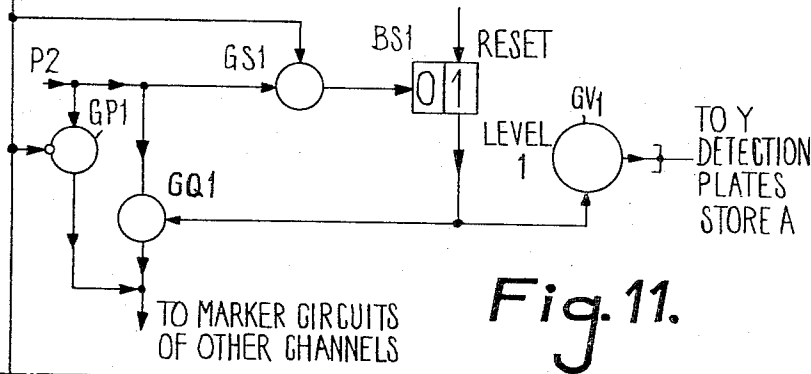
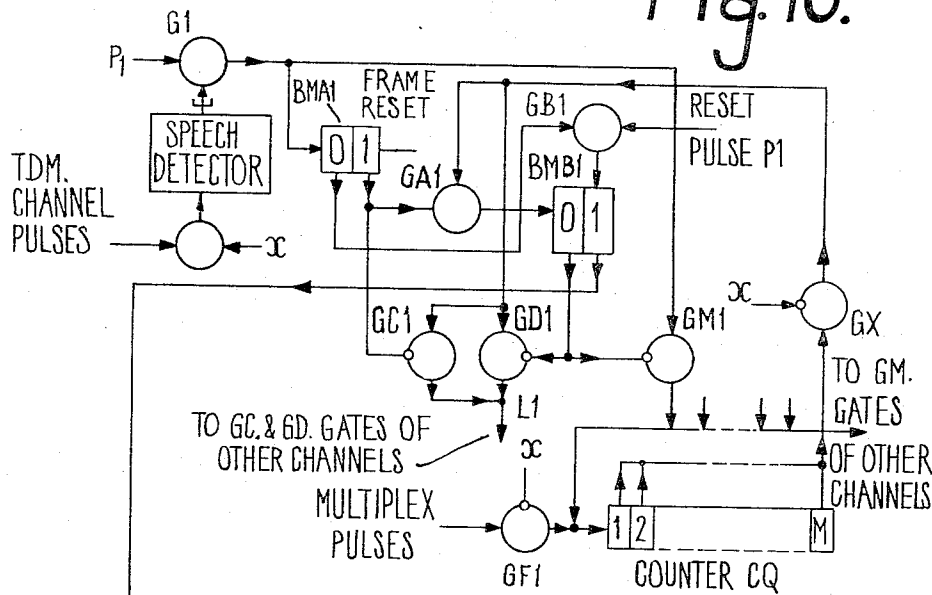
D. I. URQUHART-PULLEN

3,311,707

TIME ASSIGNMENT SPEECH INTERPOLATION SYSTEM

Filed June 26, 1963

8 Sheets-Sheet 6



March 28, 1967

D. I. URQUHART-PULLEN

3,311,707

TIME ASSIGNMENT SPEECH INTERPOLATION SYSTEM

Filed June 26, 1963

8 Sheets-Sheet 7

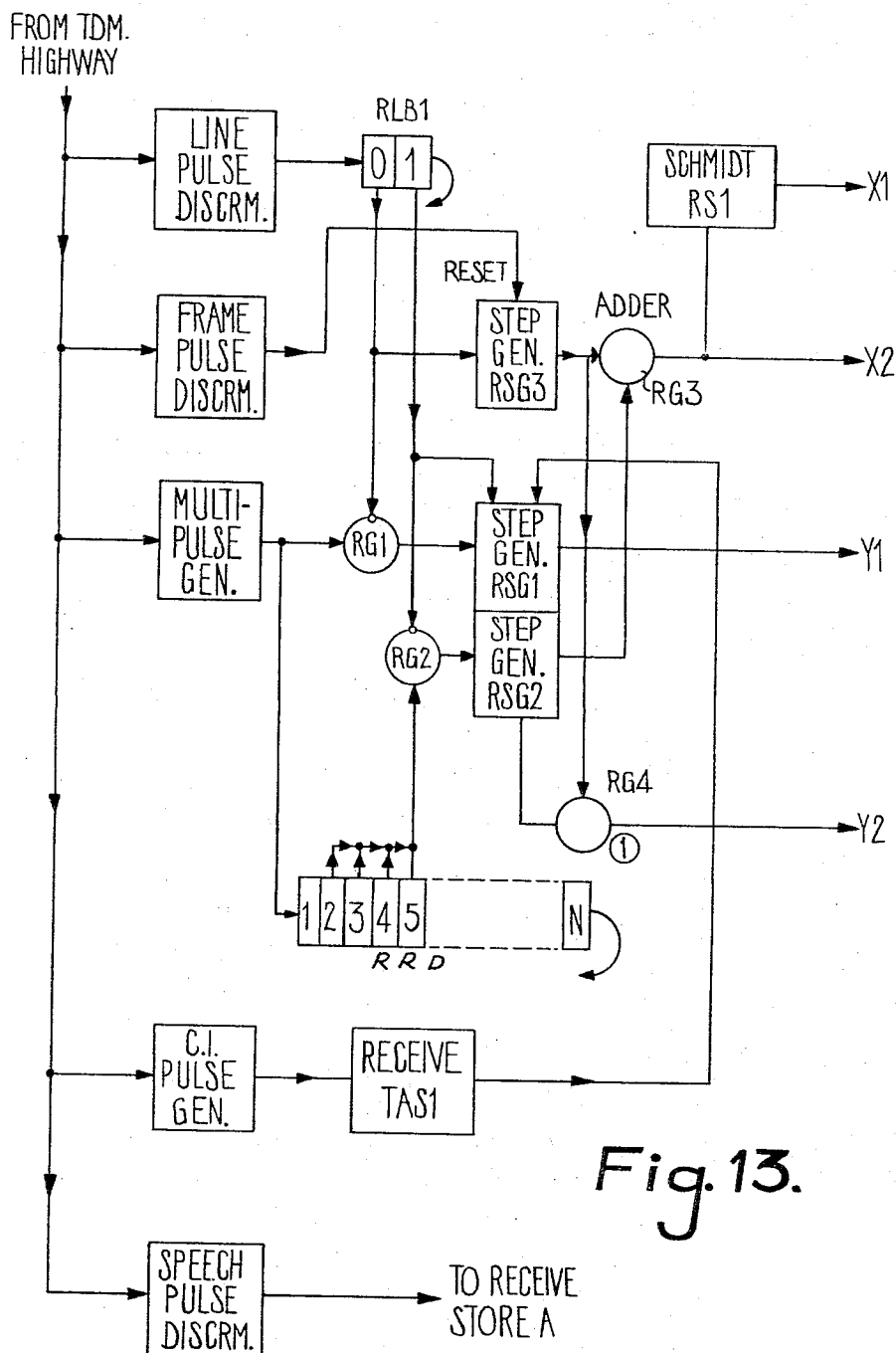


Fig. 13.

March 28, 1967

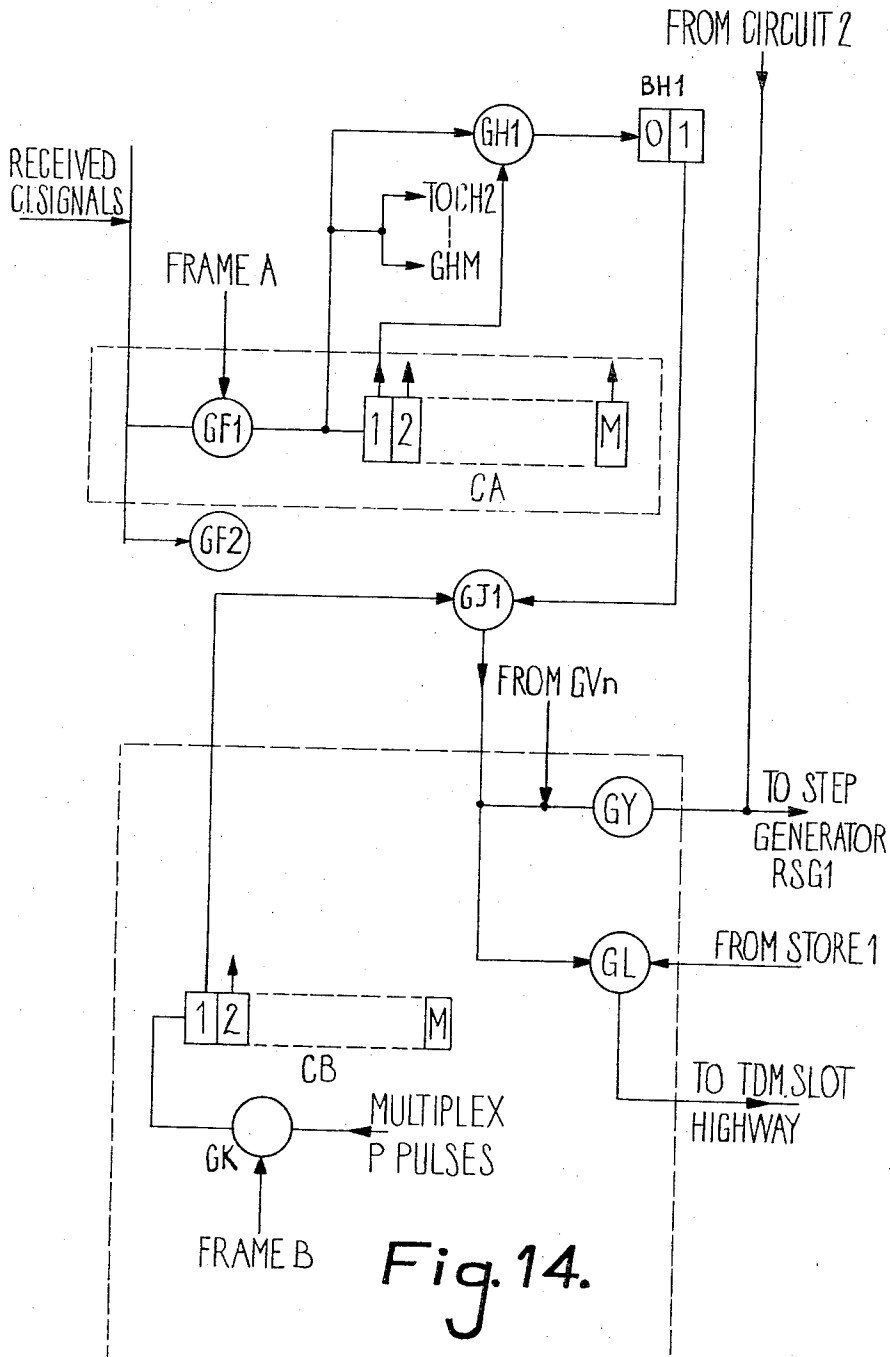
D. I. URQUHART-PULLEN

3,311,707

TIME ASSIGNMENT SPEECH INTERPOLATION SYSTEM

Filed June 26, 1963

8 Sheets-Sheet 8



1

2

3,311,707

TIME ASSIGNMENT SPEECH INTERPOLATION SYSTEM

David Ian Urquhart-Pullen, Ascot, England, assignor to Associated Electrical Industries Limited, London, England, a British company

Filed June 26, 1963, Ser. No. 290,797

Claims priority, application Great Britain, June 27, 1962, 24,722/62

5 Claims. (Cl. 179—15)

This invention relates to time division multiplex transmission systems in which signals of a number of independent information channels are transmitted over a single transmission path in a recurrent sequence.

The invention is applicable both to telephone systems for transmitting speech signals and also to systems transmitting information other than telephone signals such, for example, as video signals and data signals, e.g. in telemetry. It is applicable to transmission over lines and also to transmission over radio links.

The invention is especially applicable to transmission systems of the kind in which a burst of information, i.e. a train of pulses of each information channel, is transmitted in turn and is to be distinguished from systems in which single pulses of each information channel are transmitted in turn.

Such transmission systems may include storage means at the transmitter into which the signals of a number of channels can be written recurrently and then read out in bursts or trains for transmission to the receiver which is provided with a complementary arrangement for distributing signals to the respective receivers, such for example as the systems described in co-pending U.S. applications No. 833,020 now Patent No. 3,084,222 and No. 206,808 now Patent No. 3,213,201.

It is well known that in multiplex transmission it is not necessary to provide as many transmission channels between a transmitter and a receiver as there are information channels as it is unlikely that people will wish to transmit on all the information channels at the same time.

However if there are fewer transmission channels than information channels the problem arises of selecting which information channels are to be transmitted at any time.

The present invention comprises a multiplex transmission system provided with a transmitter having signal storage means into which signals from a plurality of information channels are fed in recurrent cycles, and from which signals are read and transmitted in the intervening alternate cycles. Channel selection means having information storage means, are provided with means for interrogating the signals of each information channel in the signal storage means. The information storage means are each provided with two devices—the first of which is set if the channel carries information during the present cycle, which in turn sets the second device which retains its setting until the next cycle. When both devices are in the "set" state, the signals of the associated information channel are transmitted.

Preferably the storage means includes separate zones for each channel and information is fed recurrently to each zone, the contents of each zone is then transmitted as a short train of information pulses.

The condition of each information channel may be compared with its condition during the previous cycle and priority for transmission is given to channels having information during successive cycles.

According to one embodiment of the invention there is provided a queue counter having a number of stages corresponding to the number of transmission channels, means for interrogating the storage zone for stepping the

counter or stage for each zone having information during two successive cycles and means whereby the counter is then stepped on through its remaining stages and pulses are fed back to activate a further information channel for transmission for each unfilled queue counter stage, the channels activated being those containing information during the current frame.

In order that the invention may be more clearly understood reference will now be made to the accompanying drawings, in which:

FIG. 1 explains the comb system of transmission,

FIG. 2 shows diagrammatically the arrangement of the store matrix at the transmitter,

FIG. 3 shows in block form the store switching arrangement at the transmitter,

FIG. 4 similarly shows the store switching arrangement at the receiver,

FIG. 5 shows for purposes of explanation a modified arrangement of a store matrix having four rows and four columns,

FIG. 6 shows a switching sequence for a modified arrangement in which writing and reading are carried out with line interlace,

FIG. 7 shows the general arrangement of time assignment apparatus for use with the transmission apparatus of FIG. 3,

FIG. 8 shows the switching circuit for applying deflection voltages to the storage devices,

FIGS. 9 and 9A show graphically the voltage changes occurring in the circuit of FIG. 8,

FIG. 10 shows the queue control circuit,

FIG. 11 shows the busy channel marker circuit,

FIG. 12 shows the channel information pulse generator,

FIG. 13 shows the receive store control circuit, and

FIG. 14 shows the TASI circuit at the receiver schematically.

The arrangement to be described is one in which information channel pulses are grouped together in short pulse trains for transmission, the pulse trains belonging to different information channels being interleaved, and recurrent cycles of such interleaved pulse trains being transmitted to a receiver where the pulse trains are distributed to respective demodulators. This method of time division multiplexing is often referred to as "comb" transmission as distinct from "slot" transmission in which individual T.D.M. pulses from each transmission channel are interleaved and transmitted in recurring cycles. Comb transmission has the advantage over slot transmission that, other things being equal, the bandwidth required for comb transmission is less than that required for slot transmission since with comb transmission cross-talk is restricted to that occurring between successive trains of pulses, whereas slot transmission is susceptible to cross-talk between any successive pair of pulses since these will always be of different channels.

It is a well known fact that it is not necessary to provide a transmission channel between the transmitter and the receiver for the full number of information channels which are fed to the transmitter and fed from the receiver since it is unlikely that everybody will want to speak at the same time, and systems providing fewer transmission than information signals are known as Time Assignment Speech Interpolation Systems, referred to as T.A.S.I. for short. The arrangement to be described concerns the application of T.A.S.I. to a comb transmission system, and for the purposes of explanation, a transmitting and receiving system has been assumed in which there are 16 information channels and only 8 transmission channels. It is to be appreciated however, that this is by way of example only and that the principles described are applicable to considerably more information and transmis-

sion channels. With such systems it is necessary to provide means for selecting for transmission, information channels that are busy, i.e. actually carrying speech or like signals, up to 8 in number at any time, and for transmitting these signals with suitable identification signals to indicate to the receiver the information channels to which the transmitted speech signals belong.

Referring to the drawings, FIG. 1 shows for purposes of comparison four cycles *a*, *b*, *c*, *d* of a 16 channel time division multiplex transmission. The row A illustrates slot transmission, the row B comb transmission and the row C illustrates comb transmission with T.A.S.I. and indicates the method of inserting the identification signals between trains of channel signals. It will be observed that the application of T.A.S.I. to the simple comb transmission shown in row B has resulted in the pulse trains being more widely spaced, this enables a correspondingly reduced bandwidth to serve for transmission without degradation of the cross-talk factor. It will be appreciated, of course, that where a greater bandwidth is available, the pulse trains could be compressed in time so as to permit a greater number of channels to be transmitted for a given cross-talk factor than would otherwise be possible.

Slot to comb conversion can be effected in a number of ways, the example described herein is of the kind described in co-pending U.S. application No. 833,020 employing storage matrices at the transmitter and receiver. In the following description it will, for convenience be assumed that at the transmitter writing will be carried out in columns and reading in rows and at the receiver writing effected in rows and reading in columns. It will be understood, however, that converse arrangements could equally well be employed and of course that rectangular matrices is only one example of application.

FIG. 2 shows the arrangement of a raster at the transmitter in which, as above mentioned, it is assumed that writing is carried out in vertical sweeps down each of the columns in turn passing from left to right. During writing sample signals from each of the sources are written in turn into the store, the writing being sequentially downwards and the displacement between samples being uniform so that in each row of the raster all the signals will be associated with the same channel.

The writing of a column is followed by reading of a row in which the storage tube is scanned horizontally as shown in FIG. 2. Reading and writing alternate in a manner which will be described subsequently. Since each row contains signals of the same channel the result will be that a short train of signals from each of the channels in turn will be transmitted, and thus slot to comb conversion is achieved.

FIG. 3 shows in block form the store switching arrangement at the transmitter. Half the input information channels, i.e. channels 1-8 in the example considered, are fed through associated end gates on the left of the figure and Gate G1 to store A, the send gates being operated sequentially so that each information channel in turn is connected to the store. Similarly the remaining information channels, i.e. channels 9 to 16, are connected through send gates and gate G2 with store B. Stores A and B read and write alternately during successive line scans and are controlled by the gates G1, G2, G3 and G4. Control signals A and B are applied alternately to the gates so that opening of gates G1 and G4 alternates with G2 and G3. When G1 and G4 are open during one line scan a column of incoming signals is fed through gate G1 and written into store A. At the same time a row of signals in store B is read and fed through the gate G4 to the transmission path. At the end of the line scan, signal A is removed and signal B applied. Gates G3 and G2 will now be opened and G1 and G4 blocked. Thus a row of information in store A will be read out and transmitted while at the same time a column of information is being written into store B.

FIG. 4 shows the corresponding arrangement at the

receiver which operates in a similar manner, but in this case since information channel distribution and not selection is involved, each store need accommodate only four transmission channels. Thus, store C is associated with transmission channels 1 to 4 and store D with transmission channels 5 to 8. The incoming signals are fed alternately into store C and store D, whilst information is being written into store C and information is being read out from store D and passed through the appropriate receiver gates associated with the respective channels. The control is obtained by means of signals A and B which control the gates G5, G6, G7 and G8. The signals A and B are approximately synchronised with signals A and B at the transmitter and it follows that, with the arrangement shown each transmitter store will always transmit signals to the same receiver store.

An important advantage of the proposed arrangement is the reduction of noise in the transmission and this is achieved by so arranging the transmitter and receiver that the same channels always are written on to the same store, this avoids the noise caused by switching from one store to the other such as is liable to occur if the writing occurs frame by frame.

FIG. 5 shows a transmitting matrix employing four columns and eight rows for the purposes of explanation. It will be observed that the columns are designated by small letters representing the pulse cycles, and the rows by numerals designating the information channels.

In the T.A.S.I. system to be described, a row is scanned only if the corresponding information channel is busy, and not more than four rows may be scanned during any frame, the rows corresponding to quiescent information channels being skipped in the scanning process.

FIG. 6 shows the sequence of switching which would be carried out in the case, for example, of information channels 1, 3, 4, 6, 9, 10, 13 and 15 being busy, the remaining channels being quiescent for the time being.

In FIG. 6, a column is written into store A, information signals being stored in the *a* storage elements 1*a*, 3*a*, 4*a* and 6*a*, the remaining *a* storage elements of Store A being empty. At the same time, a busy row of previously stored information is read out from Store B. In order, however, that the reading scan shall not try to read a store position before any information has been written into it, it is necessary to stagger the reading so that the reading of a row commences at the column following that column which has just been written and finishes up at the column which has just been written.

To perform the T.A.S.I. operation described above, it is necessary to sample the lines to ascertain which information channels are carrying speech and in the actual arrangement to be described the sampling is effected by investigating the first column during writing. It is also necessary to generate channel information pulses to indicate which of the information channels are being transmitted at any time, and as indicated in FIG. 1, these pulses are generated in pairs and inserted in gaps between adjacent trains of speech channel pulses. To avoid this arrangement causing difficulty due to a speech train being transmitted in advance of the corresponding information pulse, it is arranged that the information pulses received during one frame are stored at the receiver and utilised for the subsequent frame.

Referring now to FIG. 7, which shows the general arrangement of the T.A.S.I. apparatus, signals from the information channels (senders) are fed in at the left hand side in slot formation, i.e. as in FIG. 1A. The information channel pulses are fed alternately to stores A and B where they are written according to the matrix shown in FIG. 2. At the same time the pulses are fed in turn through a gate GA to a speech detector which during the first column of writing of a raster samples each information channel and passes a pulse to the queue controller if it receives a signal from the channel concerned. A sampling A pulse X, which lasts throughout the first column of writing on both stores, i.e. for the duration of

5

a full pulse cycle such as *a* FIG. 1, is applied to open the gate GA for the duration of the first writing column only.

In the queue control circuit the busy information channels in the present frame as shown by the signals from the speech detector are compared with those in the previous frame so as to ensure that the channels which are registered as busy in both the previous and present frames have priority in the allocation of a transmission channel over other information channels which have become busy after having been inactive in the previous frame. This arrangement minimises the possibility of speech being cut-off by the T.A.S.I. circuit. Otherwise, free transmission channels are allocated in the order of reading the information channels into the main stores.

From the queue control circuit, information is passed over separate leads for each channel to the busy channel markers and to the channel information generator. Each busy channel marker contains a marking element for each channel served by its associated main store, i.e. A or B. Thus the busy channel marker for Store A is associated with one half of the queue control circuit, while the busy channel marker for store B is associated with the other half of the queue control circuit. The busy channel markers operate in conjunction with the queue controller to control the Y shift of the appropriate store so as to select the row containing the next busy channel to be read out onto the outgoing transmission line. The function of the channel information generator is to send out signals regarding the identity of the transmitted information channels, these being generated, in batches, i.e. pairs in the present example, and transmitted between the speech pulse trains. In this arrangement, the input gates A and B are controlled by clock pulses from a central timing control and referred to as "write P" pulses 1-8 and 9-16 respectively, while the output gates A and B are controlled by "read P" pulses 2-5 and 10-13 respectively, the "read P" pulses being displaced from the "write P" pulses by half a cycle period. Thus while information channels 9-16 are being written into store B, information signals are being read out from store A on to transmission channels 1-4, the latter being effected in time periods 2-5, similarly when channels 1-8 are being written into store A, information signals are being read out from store B on to transmission channels 5-8 in time periods 10-13. This timing of the transmission channels ensures the requisite gaps in the transmitted signal trains and isolates the stores from the highway while information is being written into them.

FIG. 8 shows, for store A only, the control circuit in block form for controlling the deflection system of the store. At the top left hand corner, LB1 is a line binary counter which operates the gates G1 and G2 alternately. The line synchronising pulse recurrence frequency is an exact sub-multiple of the multiplex rate and occurs at the start of each writing line scan. The line and frame synchronising pulses are also passed to a frame discriminating circuit which separates out the frame synchronising pulses and uses them to reset SG3. Unmodulated multiplex P pulses are fed to the gate G1, to the T.A.S.I. circuits and to a read pulse distributing chain RD.

FIG. 9 shows graphically the voltage changes occurring in FIG. 8 for the 16/8 channel system being described. The numerals in circles in FIG. 8 refer to the graphs in FIG. 9 as showing the voltage changes at these points.

In FIG. 9 it is assumed that horizontal reading sweeps and vertical writing sweeps alternate.

With the line binary circuit LB1 set to its 0 state, the line synchronizing pulse passes over the 0 output lead and triggers the step generator SG3 which produces on its output lead the bias waveform 3. Multiplex pulses are applied to the cyclic counter RD and pulses 2-5 are passed by gate G2 to step generator SG2 which produces waveform 4 on its output lead. This controls the horizontal sweeps along rows selected by the deflections. The

6

outputs from step generators SG2 and SG3 are combined in the adding gate G3 to produce the composite waveform 5, which is fed to the X2 deflection plate and also to the schmidt trigger circuit. This latter circuit is arranged to trigger at the level indicated by the dotted line in graph 5. The output of the schmidt circuit is shown in Graph 6 and this is applied to the X1 deflection plates. The resultant deflection produced is indicated in Graph 7, which gives the staggered read scan required. The output 2-5 from the counter RD is also fed to the A store read gate B shown in FIG. 7 so that any output from the main store other than that at these times is prevented from reaching the transmission highway.

When the line binary LB1 is set to its 1 state, gate G2 is inhibited and gate G1 is primed to pass the multiplex pulses to the step generator SG1 which produces the step waveform shown in Graph 8. This controls the vertical deflection. The line synchronizing pulse is also passed to the T.A.S.I. circuit which produces bias output levels which are applied to the Y plates during the horizontal sweeps and select the rows containing information channels selected for transmission. For the purposes of explanation, it will be assumed that of the information channels 1-8 served by store A channels 1, 3, 4 and 6 are busy and have been selected for transmission. The process of selection will be described in full below, when the T.A.S.I. circuits are considered in detail. The result is that the levels 1, 3, 4, 6 shown in Graph 9 are applied in turn to the Y2 deflection plate, and the resultant waveform applied between plates Y1 and Y2 is shown in Graph 10 which shows that after each vertical writing scan, the Y deflection is successively positioned on rows 1, 3, 4 and 6, in readiness for the reading scan.

The store control circuit for store B is the same as for store A described above, with the exception that the X and Y scans are reversed in time. This may be achieved by simply reversing the output connections from the line binary gate, so that while store A is being written into, store B is being read, and vice versa.

FIGS. 10, 11 and 12 show the T.A.S.I. circuits in logical detail. FIG. 10 shows the queue control circuit, FIG. 11 shows the busy channel marker circuit while FIG. 12 shows the channel information pulse generator.

Referring to the queue control circuit of FIG. 10, with the exception of the counter CQ the speech detector and the gates GA and GX which are common to all channels of both stores, the equipment shown is associated with one information channel only, i.e. channel 1. The suffix numeral shown with the component designations in this equipment refers to the channel with which the equipment is associated, i.e. BMA1 belongs to channel 1, while channel 2 has a separate bistable element BMA2 etc. (not shown in the drawing).

For each information channel a pair of stores BMA and BMB is provided. These comprise simple bistable elements. Each BMA store has its input coupled to the output from the speech detector over a distributing gate G1. Each of these distributing gates is primed by a different successive multiplex P pulse, so that the gates are opened sequentially by the incoming T.D.M. channel slots. Between the BMA1 and BMB1 stores is a set of three gates GA1, GC1, GD1. The gate GA1 is a selecting gate. It is open when BMA1 is "set", i.e. is in the 1 state, and allows a pulse from the counter CQ to "set" BMB1 to the 1 state. Thus BMB1 will act as a memory store and have the same state that BMA 1 had during the previous frame irrespective of the state of BMA1 during the present frame as described more fully below. The gates GC1 and GD1 which are NOT gates are searching gates forming a chain with the corresponding searching gates belonging to other channels. These gates are controlled by the counter chain CQ which is common to all channels, and the operation of the circuit is as follows.

Assume initially that the BMB stores are set up with a number, up to 8, of busy channels. Therefore the BMB

storage elements corresponding to the busy channels will be in the 1 or set state and all the other BMB stores will be in the 0 or reset state. This is the state of affairs which can exist at the end of a frame period. During the first writing line scan of the new frame period the BMA memory units are set up according to the information from the speech detector. The separate busy channel pulses set the corresponding BMA storage elements and are also passed to counter CQ, via gates GM. These gates are primed by the BMB stores, so that the counter CQ only steps when both BMA1 and BMB1 are set. Therefore, considering channel 1, at the end of the first writing line, scan memory BMA1 can store "busy" information relating to the present state of channel 1, BMB1 contains "busy" information relating to the previous state of channel 1, and CQ contains comparative information about channel state changes. The output of CQ is blocked off during this setting up scan by pulse x applied to gate GX. Pulse x is of the same duration as the line scan and can be generated in the store-scan waveform generating equipment to occur during the first writing line scan.

The first line sync pulse of the next line period, i.e. pulse p_1 is used to reset memory store BMB1. Only those units are reset to zero in which the speech channel has become vacant. Gates GB ensure that this rule is followed, as they only permit the reset pulse to reach the associated BMB store if its corresponding BMA unit is "reset," i.e. in the 0 state. As pulse x has now vanished, the input of counter CQ is connected to the multiplex pulses and its output through GX to the memory chain. If there has been a change of channel state since the last frame, CQ will not have stepped its m positions, and the multiplex pulses will be able to step it on until stage m is reached. Each step produces an output pulse which is fed via GX to the selecting and searching gates of the memory stores BMB.

Suppose that channel 1 was busy in the previous frame and is unchanged. BMA1 will be "set" and so will BMB1. Gate GA1 will be open, but ineffective as BMB1 has already been set, GC1 will be shut due to the inhibit 1 from BMA1 and GD1 will be open. Therefore, the pulse from CQ (if there is one) will pass through GD1 to the second stage, L1 being connected to the upper sides of GC2 and GD2, it being assumed that successive stages are identical with the stage shown. Assume both BMA2 and BMB2 are "off". In this case gate GA2 is shut, GC2 is open and GD2 is shut. Therefore, the pulse passes through this stage without affecting it, via gate GC2 to the next stage. In the third stage assume that the speech channel has changed from busy to vacant. BMA3 will be reset, i.e. in the 0 state, and BMB3 will also be reset, i.e. in the 0 state, as the reset pulse will have reset it from its previous "on" state. Therefore the CQ pulse continues via GC3 to the fourth stage. Assume that channel 4 has become busy, whereas previously it was vacant, BMA4 will be set and BMB4 will be reset. So gate GA4 is open, GC4 is shut and GD4 is shut. The CQ pulse is diverted from the main line by GA4 and triggers BMB4 into the set state. This action opens gate GD4 so that a second CQ pulse could pass on the stage 5 and any remaining CQ counter output pulses can set up any remaining BMB units to a total of m units maximum. After the m th CQ pulse, the chain counter is saturated and cannot produce any more pulses until it is reset by the frame pulse. This frame pulse also resets the BMA units ready to receive the next train of "channel state" pulses from the speech detector.

As described earlier, the Queue Controller can only discriminate for one frame period at a time, however, it will be apparent that this discrimination could be extended by the incorporation of an additional memory chain for each additional frame period to be remembered.

Referring now to the busy channel marker circuit of FIG. 11, the function of this circuit is to feed out the appropriate bias voltage to the Y2 plate of the Y deflection

system of the main store at the start of each reading line scan. Thus if channel No. 2 is the first busy channel during a frame period, the busy channel marker must feed out voltage level 2 to the Y deflection system.

In FIG. 11, only the equipment for one channel has been shown. The gates GS, GP and GQ are selecting and searching gates similar to the gates GA, GC and GD in FIG. 10, the gates GP and GQ for each channel being serially connected in pairs to form a chain.

It will be observed that there is a connection from the one side of store BMB1 of FIG. 10 to the gate GS1 of FIG. 11. Similar connections exist between the one side of the BMB stores for other channels and the corresponding GS gates not shown.

There is a separate Busy Channel marker circuit as shown in FIG. 11 for each information channel and each has its gate GS connected to its associated queue control store BMB1-BMB16. The busy channel marker circuits each serve to apply an appropriate deflection to the Y2 deflection plate of its associated transmitting store. It will be recalled that by the time the first P1 pulse of the reading line scan is completed, the earliest busy channel to be transmitted has had its BMB memory set to the one state. At the beginning of the first read pulse the busy channel marker locates this channel and applies the appropriate Y2 voltage to the Y deflection system. The P2 pulses at the start of each line scan are applied to prime the gates GS. Assume the first channel has been marked busy from the queue control circuit an operating signal will be applied from the store BMB1 to open gate GS1 and allow the next pulse to set the bistable switch BS1 to its one state. This operates gate GV1 to apply Level 1 to the deflection plate Y2. The signal from BMB1 also inhibits the gate GP1. The gate GQ1 which was closed while the switch BS1 was in its 0 condition, is primed by the switch BS1 in its "one" condition in readiness for the next line scan pulse. Although the gates GS associated with other busy channels will also have received input signals from their associated BMB stores, these gates are not primed by the applied P2 pulse since the gates GP1 and GQ1 were both closed during receipt of this pulse and hence its passage beyond the first stage was blocked. At the next line scan however, the gate GQ1 will already be primed by the signal from switch BS1 now in its one state, and consequently the P2 pulse will pass via GQ1 to the next stage. Assume now that channel 2 is inactive, i.e. BMB2 is in its 0 condition. In this case, there is no signal to operate gate GS2, but GP2 will be primed since there is no inhibition signal from the BMB2 store. Consequently the P2 pulse is able to pass through the second busy marker stage and will in fact, progress along the chain of GP and GQ gating pairs until the next busy channel is encountered when the GS gate of that channel will be opened and the corresponding BS switch actuated to bring about the application of the appropriate voltage level to the Y2 deflection plates. This action continues for each line scan of the frame until all the busy channels have been transmitted.

Referring now to FIG. 12, the channel information pulse generator will now be described. It will be recalled that the function of this circuit is to transmit pulse signals to indicate at the receiver the identity of the channels being transmitted, these signals being transmitted in batches between the pulse trains transmitted from the transmitting stores. In the particular example being considered the channel information signals are transmitted by pairs of pulses according to a code and the scheme adopted employs a full height pulse to denote a busy channel and a half height pulse to denote an inactive channel, positive pulses to denote line periods and a negative pulse to denote the end of a frame. Of the equipment shown in FIG. 12, the gate GO1 and the pulse shaping circuit are provided for information channel 1 only, similar gates and pulse shaping circuits are provided for the remaining information channels, these not being shown. The

counter QR and gates GS and GR are common for all information channels. The operation of the circuit is as follows.

At the end of the first reading line period, pulse p_{n-1} triggers the counter to its first output position which primes gate GO1. If the bistable circuit BMB1 is set showing that channel 1 is busy, gate GO1 is also primed by this output. So pulse p_{n-1} can pass through gate GO1 on to the common output lead. However, if BMB1 is in its 0 condition, (i.e. channel 1 is vacant) gate GO1 remains shut, and pulse p_{n-1} cannot get through. Instead, an attenuated p_{n-1} pulse is fed onto the common lead via the shaping network. Because a "busy" pulse from the counter GR is of greater amplitude than a "vacant" pulse, there is no need to gate the "vacant" pulses as they will be swamped whenever a "busy" pulse is passed on to the common lead. The pulses p_{n-1} etc. are fed to the gates GO in accordance with the number of C.I. pulses in each transmitted batch.

In the system proposed, the frame synchronising pulse is of reverse polarity. Therefore a polarity-reversal circuit in inserted between the positional pulse common lead and the transmission line. This circuit is actuated by the final pulse of the chain counter. When the counter reaches its final position it primes gate GO_n and at the same time switches the P-pulse common lead from direct connection to the transmission line to connection via a "minus-one" amplifier. This reversal is achieved by means of the simple two gate system shown in FIG. 12 in which gate GR is normally open but gate GS is opened to pass the pulses through the amplifier. The next pulse into the counter switches it back to position 1, which switches out the minus-one amplifier by cutting out gate GS and priming gate GR and makes the pulse polarity revert to normal again.

Turning now to the apparatus for T.A.S.I. reception, as explained above the main receiving stores need accommodate only the transmitted channels and consequently in the present example each receiving store is arranged to store only 4 channels each at any one time. It is also arranged in the present example that writing into the received stores is effected horizontally and reading, vertically. The writing scans are staggered with respect to one another. This results in a receive store control circuit which is very similar to the transmit store control circuit. In the receive store control circuit however, although no Y deflection is no longer dependent upon channel activity, the start of each Y scan has to be controlled since the time for which the Y scan remains at each step during the read-out process is dependent upon channel activity.

The function of the receiving apparatus, it will be recalled, is to restore the incoming time assigned channel comb signals to their original non time assigned T.D.M. slot signals. Thus, for example, if at the transmitting end the information channels 1 and 3 are busy, then at the receiver in the process of restoring the transmitted comb signals for channels 1 and 3 to the original slot formation, a gap of one time slot must, during reading, be inserted between the time slots read from the main store for channels 1 and 3.

FIG. 13 shows the receive store control circuit for store 1 only. The line pulse discriminator feeds line synchronizing pulses to the line binary counter RLB1. In its 0 condition this counter applies a signal to set the step generator RSG3 and the gate RG2 is primed due to the absence of an inhibit signal from the "one" output of the counter and this gate passes pulses at times p_2 to p_5 from the counter RRD, causing the step generator RSG2 to step at these times. The step generators RSG2 and RSG3, the adder and the gates RG1 and RG2 operate in the same way as described above in connection with the send store control circuit of FIG. 8 and the waveforms produced are the same as those shown in FIG. 9, Graphs 3, 4, 5, 6 and 7. The gate RG4 is also primed at this time and

passes the waveform shown in FIG. 9A, Graph 1 to the Y2 plate of the deflection system. When the binary counter RLB1 changes to its "one" condition the gate RG2 is closed and RG1 opened, allowing the multiplex pulses to pass to the step generator RSG1. This corresponds to the step generator SG1 of FIG. 8, but instead of producing a regularly stepped waveform as in FIG. 9, Graph 8, it has an over-riding control exerted upon it from the receive T.A.S.I. circuit, which causes the stepping to be restricted to only four steps, corresponding to the four information channels stored in the associated receiving store, and the duration of each step to be determined by the channel activity as indicated by the received channel information pulses. For example, Graph 2 of FIG. 9A shows the composite waveform that would be applied to the Y deflection plates in the case where channels 1, 3, 4 and 6 are indicated as busy. Thus at the start of a line scan the first storage element of a column is scanned for two multiplex time periods, at the end of which the second storage element is scanned for one multiplex time period whereupon the third storage element is scanned for two multiplex time periods when the fourth storage element is scanned for a period of three multiplex time periods. The output signals thus reproduced by the store are applied to a gate GL (FIG. 14) also controlled by the T.A.S.I. circuit to terminate each such reproduced pulse at the end of its proper multiplex time period, thus inserting the required time gaps between the non-adjacent busy channels.

It will be appreciated that the individual information receivers will be connected to the circuit in a recurrent sequence under the control of the multiplex pulses which are synchronised with those at the receiver. The purpose of the time gaps is to ensure that the information is fed out at the instant when the correct information receiver is connected up. This result is achieved by the T.A.S.I. circuit.

FIG. 14 shows the receive T.A.S.I. circuit in schematic form. The components BH1, GH1 and GJ1 are for one information channel only and are repeated for each information channel. The parts in the dash line rectangles are common to all the channels but are only concerned with one store and are repeated for the other store.

Channel information pulses fed into the gate GF which is opened by frame pulse A and gate GF2 of the next circuit by frame pulse B. The frame pulses are generated by a binary counter triggered from the frame synchronising pulses. It is necessary to have A and B frame periods as the Channel Information pulses transmitted during any frame period are not used until the following frame period when they will be associated with the stored channel signals also transmitted during the previous frame. Therefore the channel information pulse memory units (bistable circuits BH1 etc.) are filled up during frame A and read out during frame B. An equivalent circuit associated with receive store 2 is filled up during frame B and read out during frame A.

Assuming that gate GF is open, the channel information pulses feed into gates GH1 to GHn and to counter CA. CA switches to output 1 at the arrival of channel information pulse 1 and gate GH1 opens so that channel information pulse 1 passes to bistable unit BH1. The bistable units are arranged such that they only switch on if the incoming channel information pulse is of more than half its maximum amplitude, i.e. indicating a busy channel. Thus, at the end of the first line scan period, $n/m=2$ (in the present example) bistable units will have been presented with either busy or vacant pulses and will have switched on or remained off accordingly. At the end of frame period 1, all the memory units BH1 to BHn will have been set up and gate GF shuts, as frame pulse 1 collapses.

Now frame pulse B appears and opens gate GK. The multiplex pulses immediately start triggering counter CB. The outputs from CB are connected to gates GJ1-GJn

which connect the outputs of BH1-BH_n to the common output line. As CB counts in synchronism with the multiplex pulses, pulses or gaps will appear on the common line to gate GL. Therefore gate GL will open every time a busy channel is read by the store, and shut during the pause periods when the store is standing at vacant channel positions.

The common line from GJ1-GJ_n is also connected to gate GY, which passes multiplex pulses through to the Y scan step-generator. The step-generator steps every time a multiplex pulse is presented to it. The application of the multiplex pulses is, however, controlled by gate GY such that they are only applied to the step generator for a busy channel position. The connections to the receivers will continue to be stepped during the gaps until the receiver associated with the next busy channel is reached when gate GL will open and information be passed.

At the end of frame period B all the bistable units BH1-*n* are reset by the frame pulse ready to be filled with fresh information by the incoming C.I. pulses. The counter CA is also reset ready to count down again. The identical equipment associated receive store 2 operates to the alternate frame periods, with all the frame A and frame B pulses interchanged. After having been set up as described above, the common-line equivalent to the output of GJ1-*n* operates a gate in parallel with GY. Therefore, the multiplex pulses can step the same step-generator during each frame period. A similar gate in parallel with GL is operated by the same common line and connects the store output to the output line. Thus, the step generator for the Y scan continuously steps in accordance with the incoming T.A.S.I. instructions.

It will be appreciated that a station having this equipment will operate in conjunction with a corresponding distant station. Thus, the near station will comprise both a transmitter and also a receiver operating with a receiver and transmitter respectively at the distant station.

What I claim is:

1. In a multiplex transmission system having a smaller number of transmission channels than information channels, a transmitter, signal storage means in said transmitter, means for writing signals from each of the information channels into the store in recurrent cycles and means for reading from the store information to be transmitted during the intervals between the writing cycles, together with channel selection means including means for interrogating each channel during writing, a first device which is set if the channel carries information during the present cycle, a second device which is set by the first device and retains its setting until the next cycle and means for reading from the store signals of those information channels whereof both associated devices are in the set state.

2. In a multiplex transmission system having a smaller number of transmission channels than information channels, a transmitter, signal storage means in said transmitter, means for writing signals from each of the information channels into the store in recurrent cycles and means for reading from the store information to be transmitted during the intervals between the writing cycles, together with channel selection means including means for interrogating each channel during writing, a first device which is set if the channel carries information during the present cycle, a second device which is set by the first device and retains its setting until the next cycle and means for reading from the store signals of those information channels whereof both associated devices are in the set state.

3. In a multiplex transmission system having a smaller

number of transmission channels than information channels, a transmitter, signal storage means in said transmitter, means for writing signals from each of the information channels into the store in recurrent cycles, and means for reading from the store information to be transmitted during the intervals between the writing cycles, together with channel selection means including means for interrogating each channel during writing, a first device which is set if the channel carries information during the present cycle, a second device which is set by the first device and retains its setting until the next cycle and means for transmitting from the store signals of those information channels whereof both associated devices are in the set state, means for transmitting signals identifying the information channels together with a receiver, signal storage means in said receiver, means for writing received signals into said store, means for writing said stored signals and means for connecting the output cyclically to a plurality of receivers in accordance with the identifying signals received.

4. In a multiplex transmission system a transmitter, signal storage means in said transmitter, means for writing signals from a plurality of information channels in recurrent cycles into said storage means, means for reading and transmitting stored signals in the intervals between the writing cycles, means for interrogating the signals of each information channel held in said store, information storage means for each information channel interrogator, said information storage means including a first bistable device, means for setting said device if there is information in the channel during the present cycle, a second bistable device associated with each channel, means whereby said second device is set by said first device when said first device is itself set, said second device being arranged to retain its setting during the following cycle irrespective of the state of the first device and means for transmitting signals of a channel whereof both associated bistable devices are in the set state.

5. In a multiplex transmission system a transmitter, signal storage means in said transmitter, means for writing signals from a plurality of information channels in recurrent cycles into said storage means, means for interrogating the signals of each information channel stored in said information channel and means for reading and transmitting from the store those channels carrying information in the intervals between writing cycles, together with a queue counter having a number of stages corresponding to the number of transmission channels, means for interrogating each information channel and for stepping the counter a stage for each zone having information during two successive cycles and means whereby the counter is then stepped on through its remaining stages and pulses are fed back to activate a further information channel for transmission in each unfilled queue counter stage, the channels activated being those containing information during the present frame.

References Cited by the Examiner

UNITED STATES PATENTS

2,935,569	5/1960	Saal et al.	179—15
2,957,949	10/1960	James et al.	179—18.9
3,084,222	4/1963	Foot et al.	179—15
3,213,201	10/1965	Flood et al.	179—15

FOREIGN PATENTS

873,934 8/1961 Great Britain.

DAVID G. REDINBAUGH, *Primary Examiner*.

ROBERT L. GRIFFIN, *Examiner*.