

[54] VEHICLE SPEED CONTROL

[75] Inventors: William J. Walsh, Birmingham;
Joseph A. Livers, Roseville; Robert
S. Mueller, Southfield; Warren R.
Hill, Dearborn, all of Mich.

[73] Assignee: Eaton Yale & Towne Inc., Cleve-
land, Ohio

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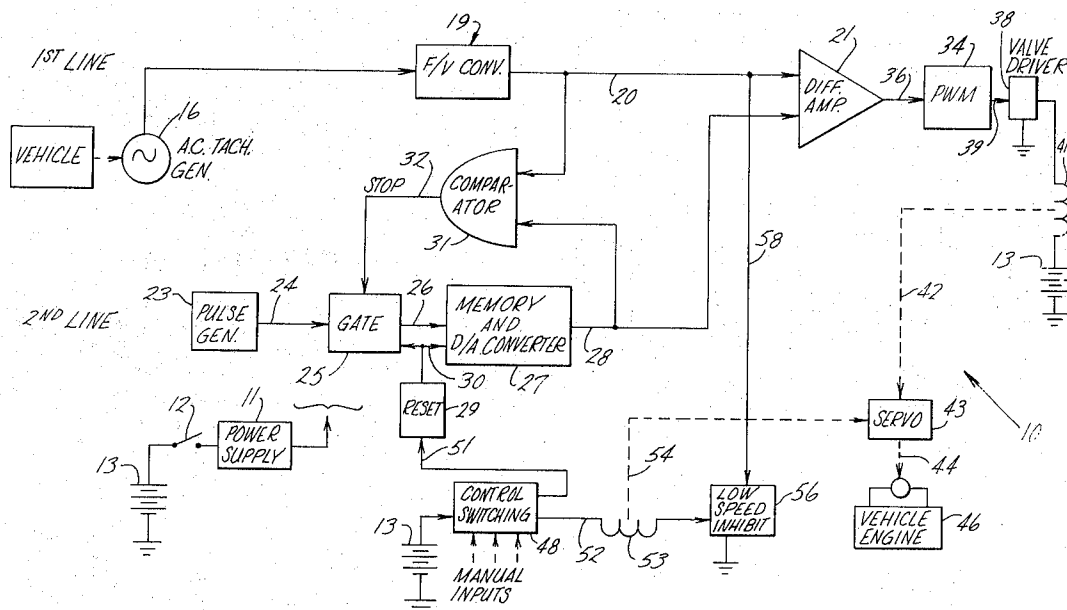
Primary Examiner—Kenneth H. Betts

Attorney—Woodhams, Blanchard and Flynn

[57] ABSTRACT

A device for automatically maintaining the speed of an automotive vehicle at, or substantially at, any currently existing value when same is suitably selected by the operator. The apparatus comprises means for remembering and producing a signal proportional to the speed of the vehicle at the moment the control mechanism is activated by the operator. It further comprises means for producing a signal proportional to a subsequent instantaneous speed of the vehicle. Said signals are then compared and caused to alter proportionately the duty cycle of an oscillator output. Such variations in said duty cycle are then utilized to control the vehicle throttle in a manner to adjust the speed toward the selected value.

27 Claims, 9 Drawing Figures



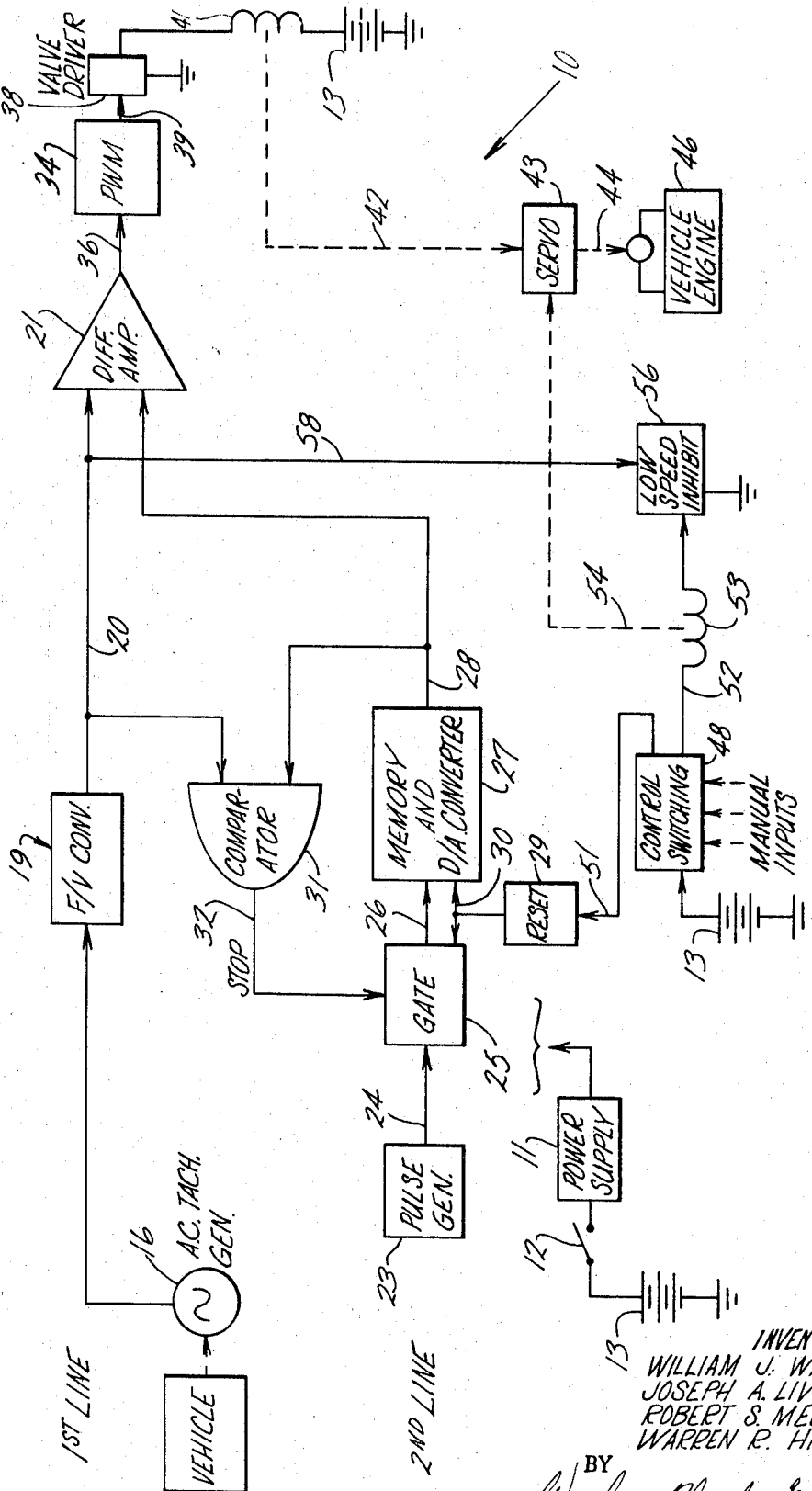
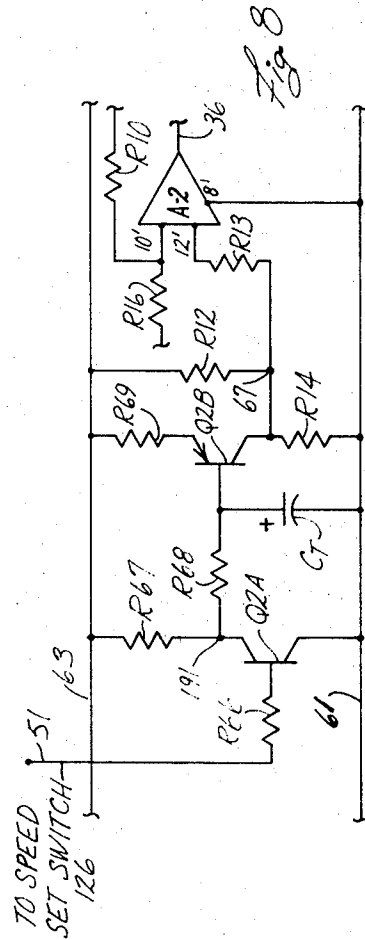
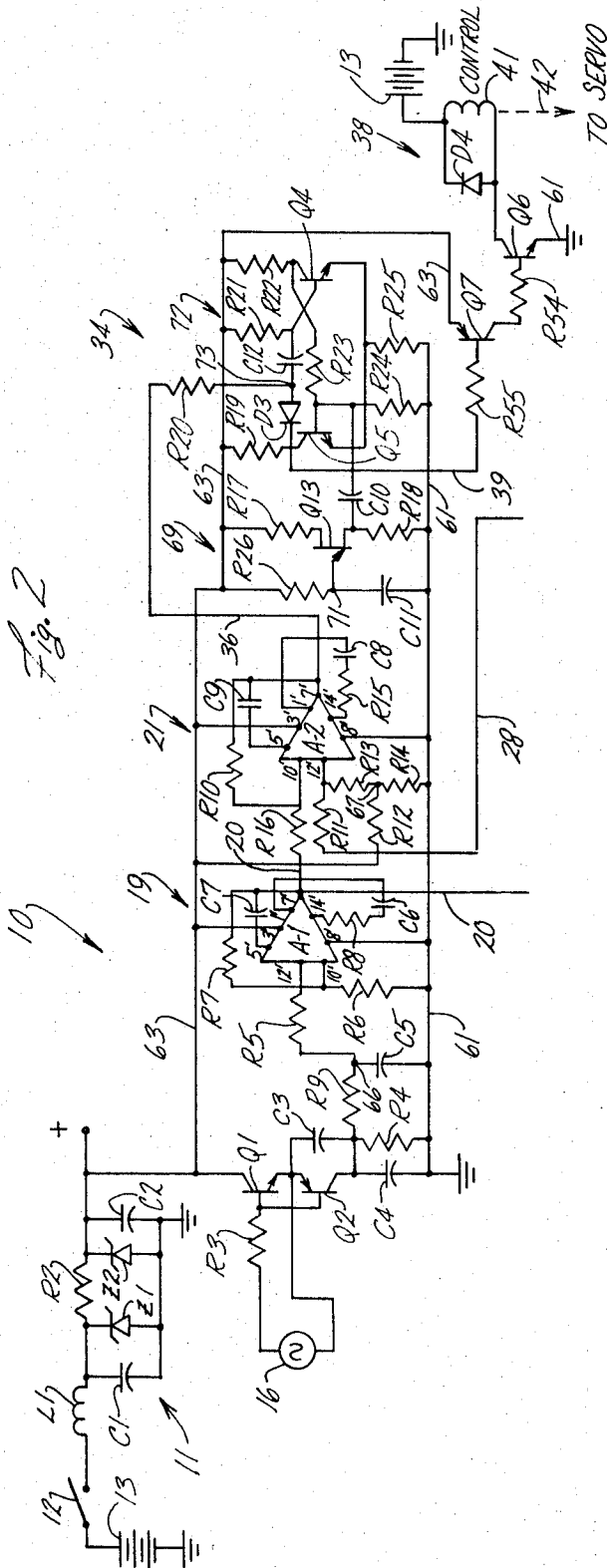


Fig. 1

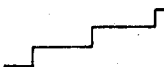
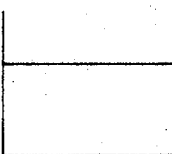
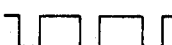
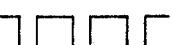
INVENTORS
 WILLIAM J. WALSH
 JOSEPH A. LIVERS
 ROBERT S. MEULLER
 WARREN R. HILL

BY
William J. Walsh & Flynn
 ATTORNEYS



INVENTORS
 WILLIAM J. WALSH
 JOSEPH A. LIVERS
 ROBERT S. MEULLER
 WARREN R. HILL
 BY
 Woodhams, Blanchard & Flynn
 ATTORNEYS

Fig. 4

	¹ TURN IGNITION ON (CAR MOVING)	² SET BUTTON DOWN	³ SET BUTTON RELEASED	⁴ MATCH
A-3, PIN 7'	HIGH	HIGH	HIGH	LOW
COLLECTOR, Q8	HIGH	HIGH	HIGH	LOW
MEMORY PT. 108	LOW PT. ≈ 1.5V.	0		
GATE 81 (OUTPUT LINE 26)	+ CONSTANT			
GATE 82 (PULSE GENER- ATOR LINE 24)				
GATE 83	0	+	+	0
GATE 84	0	+	+	0
GATE 86	+	0	0	+
GATE 87 (RESET LINE 30)	+	0	+	+
GATE 92	+	0	0	+
GATE 94 (COMPARATOR OUTPUT LINE 32)	0	+	+	0
GATE 95	0	+	+	0

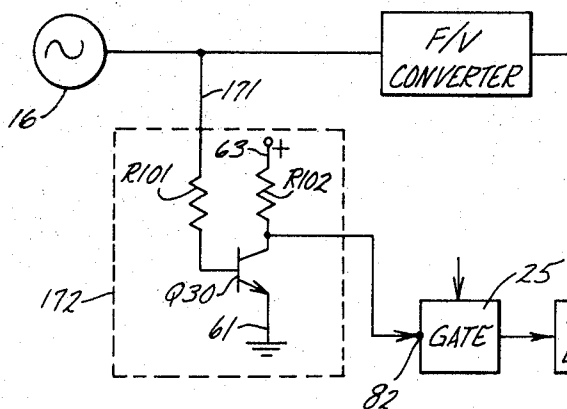


Fig. 6

INVENTORS
WILLIAM J. WALSH
JOSEPH A. LIVERS
ROBERT S. MEULLER
WARREN R. HILL

BY
Woodhams, Blanchard & Flynn
ATTORNEYS

Fig. 5

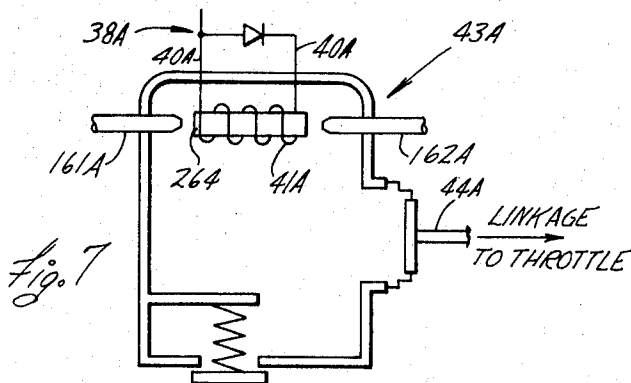
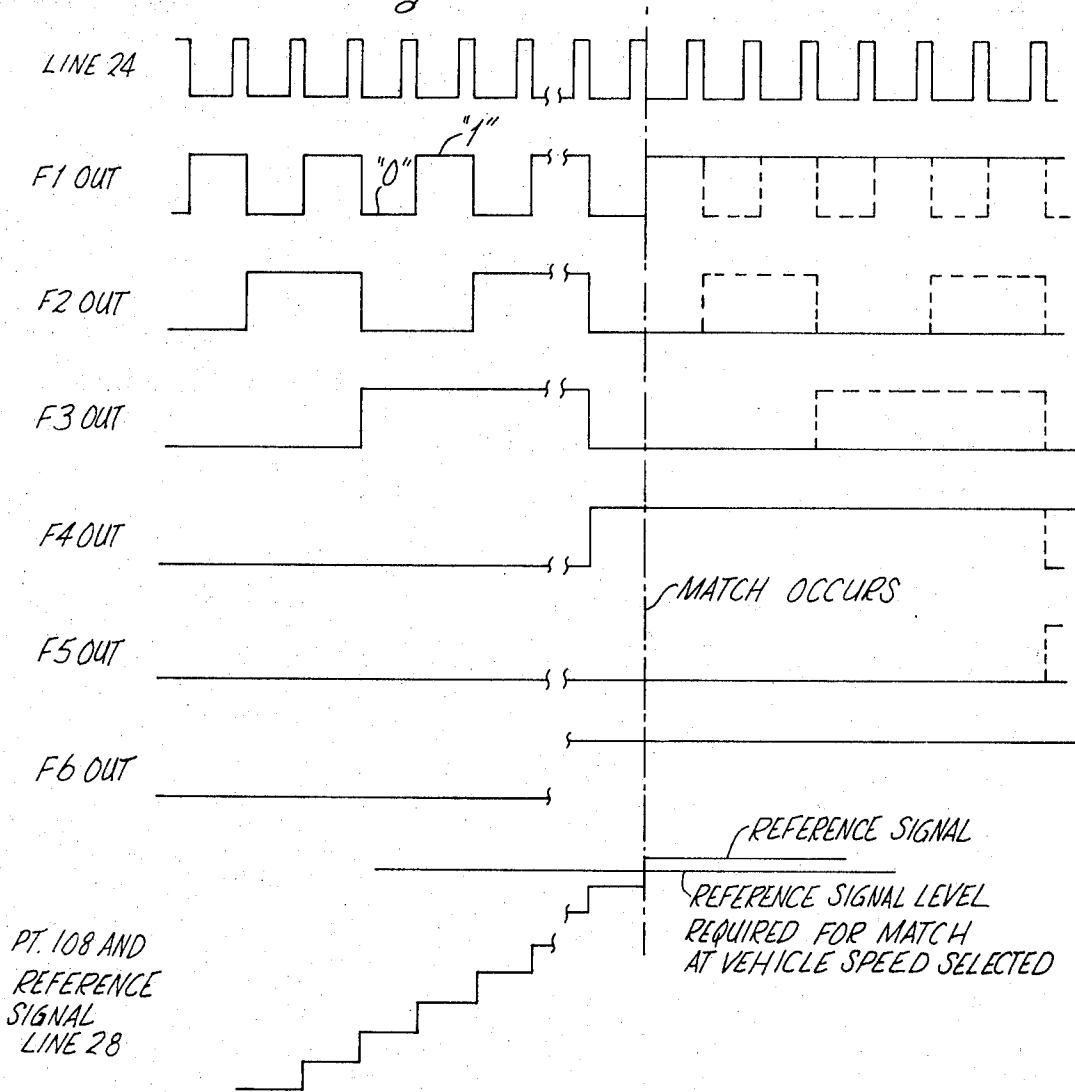


Fig. 7

INVENTORS
 WILLIAM J. WALSH
 JOSEPH A. LIVERS
 ROBERT S. MEULLER
 WARREN R. HILL

BY
 Woodhams, Blanchard & Flynn
 ATTORNEYS

VEHICLE SPEED CONTROL

FIELD OF THE INVENTION

The invention relates to apparatus for automatically maintaining the speed of an automotive vehicle as determined by an operator. Operation of selection means when the vehicle is running at a speed which it is desired to maintain actuates means producing a signal proportional to such selected speed. Such signal is maintained at a constant value and becomes a reference signal which is then compared to another signal proportional to a subsequent instantaneous speed of the vehicle. The product of such comparing is then utilized to modify the setting of the vehicle throttle as needed to adjust the vehicle speed toward the selected value.

BACKGROUND OF THE INVENTION

Automatic speed control devices for automotive vehicles have been known for a long period of time, have operated upon a wide range of operating principles and have taken a large number of different forms. However, such apparatus has in the past had only limited customer acceptance for a variety of reasons which is the broad objective of this invention to correct.

In the past, most devices for this purpose have been of mechanical nature. To meet the necessary control requirements, the devices have been relatively complex and have had many moving parts. These characteristics have made them relatively expensive to manufacture and have further subjected them to considerable expense in maintaining same in good operating condition. Further, while the known mechanical devices for this purpose could under carefully controlled conditions be made to operate within satisfactory limits of accuracy, when such devices are made under production conditions and at acceptable cost limits, the accuracy thereof diminishes and sometimes becomes unacceptable. Experimentation with electronic apparatus for this purpose indicates that while same may be no more accurate than mechanical devices when the latter are operated under highly controlled, such as laboratory, conditions, they can under production conditions be made at an accuracy substantially exceeding the accuracy of mechanical units at comparable cost.

A further problem with the mechanical units previously known is that their characteristics have frequently required the routing of the speedometer cable first into the engine compartment to operate the control mechanism and then out therefrom to the speedometer head on the vehicle's instrument panel. This not only requires additional speedometer cable and results in additional cost at this point but further requires additional space within the engine compartment and requires additional assembly time with resulting costs. It is accordingly desirable to provide a speed control device in which the speedometer cable goes only to a single point, preferably the indicator head in the vehicle's instrument panel and further connections are then made solely by electric wires.

A further problem of the mechanical device is that since the device must be positioned operably with respect to both the engine throttle and the speedometer head, it has certain positioning limitations which are often inconvenient to meet. Contrastingly, since the

electrical device is mechanically related only to the throttle, it being only electrically related to the speedometer head, it needs to be located in a given positional relationship only with respect to the throttle. This makes such positioning easier and more open to such variations as may be desirable for other reasons of design.

It is realized that the foregoing objections to mechanical control devices have been recognized in the past and some attempts have been made to correct same by the use of electrical speed control devices. However, these devices have not been wholly satisfactory for a variety of reasons and it is accordingly the purpose of the present invention to overcome the problems existing in previously known electrical speed control devices.

For example, one such problem has originated in that many of such devices have utilized capacitors which are charged to a level proportional to either the selected or instantaneous speed and the charge so created is then utilized for effecting the comparing step. This procedure leads to some inaccuracies, particularly where the equipment is permitted to stand idle for a substantial period of time and it is therefore desirable if possible to avoid this source of inaccuracy. Further in such units the necessity of providing a relatively large capacitor precludes the system from being embodied in relatively small semiconductor chips. It is accordingly desirable to provide a speed control device of electrical nature whose circuitry is such that it becomes possible to apply same to such chips and thereby effect satisfactory miniaturizing thereof.

A further problem with previous electrical units is that they could not be automatically and conveniently locked at a given vehicle speed by simple actuation of a control member when the vehicle is traveling at such speed. Instead, most previous electrical units with which I am acquainted utilize a dial which the operator was required to set to select the desired vehicle speed to be maintained prior to the desired operation of the speed control apparatus. This requires more time and attention on the part of the operator than many such operators are desirous of giving or safely capable of giving while driving the vehicle.

Some previous electrical devices utilize an electrical signal which is modulated in response to a given speed, or to the relationship of a given speed to a preselected speed, and the modulated signal is then used to effect a progressive alteration of the control apparatus. This is relatively expensive, sometimes leads to inaccuracy and therefore it is desirable to arrange the mechanical portion of the apparatus for simple on-off operation.

Accordingly, the objects of the invention include:

1. To provide a speed control device primarily adaptable to an automotive vehicle enabling the operator to select a speed at which the vehicle is then operating and which will then maintain the vehicle at or substantially at such speed.

2. To provide apparatus, as aforesaid, which is of electrical nature and thereby obtain manufacturing and installation economies and operating accuracy more advantageously than with presently known mechanical or electrical units for the same purpose.

3. To provide apparatus, as aforesaid, which will be capable of manufacture at a commercially acceptable

price and in sufficiently small size to make it possible to utilize same without excessive requirement for space.

4. To provide apparatus, as aforesaid, which can be made under production conditions at a lower cost than previously known devices for the same purpose, both mechanical and electrical.

5. To provide apparatus, as aforesaid, which provides for a simple installation including a requirement that the speedometer cable be connected only to the indicator head.

6. To provide apparatus, as aforesaid, which will be capable of utilizing integrated circuits and thereby obtain the economies characteristic thereof.

7. To provide apparatus, as aforesaid, which has a minimum amount of moving mechanical parts whereby to simplify installation and minimize inaccuracies due to wear.

Other objects and purposes of the invention will be apparent upon reading the following specification and inspecting the accompanying drawings.

In the drawings:

FIG. 1 is a block diagram of a speed control device embodying the invention.

FIG. 2 is a circuit diagram disclosing in detail a portion of the block diagram of FIG. 1.

FIG. 3 is a circuit diagram disclosing a further portion of the block diagram of FIG. 1.

FIG. 4 is a table disclosing conditions appearing at various points in the circuitry of FIGS. 2 and 3.

FIG. 5 is a waveform diagram disclosing waveforms appearing in the memory portion of the apparatus of FIG. 1.

FIG. 6 is a schematic diagram disclosing a modified portion of FIG. 1.

FIG. 7 is a schematic diagram showing a modified servo mechanism.

FIG. 8 is a schematic diagram disclosing a modified reference signal generator for the operational amplifier in the differential amplifier circuitry.

FIG. 9 is a schematic diagram of a modified low speed inhibit circuit.

GENERAL DESCRIPTION

In general, the objects and purposes of this invention are met by providing a speed control apparatus for a vehicle comprising means for providing a speed signal corresponding to any instantaneous speed of the vehicle. Means responsive to manual initiation when the vehicle is at a speed desired to be maintained, accumulate and store digital information to produce and maintain a reference signal having a preselected relation to said speed signal. Means responsive to changes in the relationship between said reference signal and subsequently occurring speed signals to vary the power setting of the vehicle engine so as to maintain the vehicle speed at, or at least acceptably close to, a constant value despite varying road and/or load conditions.

DETAILED DESCRIPTION

Turning first to FIG. 1 for a generalized illustration of one embodiment of the invention, the speed control apparatus 10 embodying the invention includes a power supply 11 which is energized through a switch 12, preferably the ignition switch of the vehicle, from the vehicle battery 13. The speed control apparatus 10

includes an a.c. source 16, here a tachometer generator, of any conventional type capable of producing an alternating voltage of frequency proportional to the speed of the vehicle to be controlled. The a.c. generator 16 is driven by any convenient means from a portion of the vehicle moving at a rate proportional to the vehicle speed, such as a wheel thereof or a portion of the drive train following the change speed gearing in the power transmission line thereof. More particularly, the a.c. source 16 may be a tachometer mechanically driven from the vehicle speedometer cable or head or may be an electrical pickup driven by an electrical connection to a vehicle speedometer of a type generating an a.c. signal proportional to vehicle speed.

The output of the a.c. source 16, hereinafter termed the a.c. speed signal, is fed to a frequency-to-voltage converter 19 which converts the a.c. speed signal into a d.c. voltage of amplitude proportional to the instantaneous vehicle speed and which is termed the d.c. speed signal. The d.c. speed signal is applied to one input of a differential amplifier 21 through a line 20.

A pulse source 23, comprising a pulse generator capable of supplying fixed amplitude and frequency pulses, is connected through a pulse line 24, gate 25 and gate output line 26 to the input of a memory unit 27. The counter portion, hereinafter described, of unit 27 counts pulses supplied thereto through the gate 25. The digital-to-analog converter (D/A converter) portion hereinafter described supplies a d.c. reference signal, the amplitude of which is proportional to the number of pulses counted, to a line 28.

A comparator 31 has two inputs to which are respectively connected the reference signal line 28 and the d.c. speed signal line 20. In response to a predetermined correspondence between these two inputs, the comparator 31 changes state and hence the potential on the output line 32 thereof. The line 32 connects to the gate 25 and said change in state blocks further conduction through the gate.

The reference voltage on line 28 also connects to a second input of the differential amplifier 21. The differential amplifier 21 provides a signal to a pulse width modulator 34 through a line 36 which signal varies with changes in the relationship of the d.c. speed signal and the reference signal.

The pulse width modulator 34 generates a constant frequency signal, the pulse width, i.e., duty cycle, of which varies with variations in the output of the differential amplifier 21. The pulse width modulated signal is applied to a valve driver 38 through a line 39. A control solenoid 41 is connected in a series loop with a d.c. source, preferably the vehicle battery 13 and a portion of the valve driver 38. The valve driver allows conduction through the control solenoid 41 at the duty cycle of the pulse width modulator 34. The control solenoid 41 controls, through a suitable linkage generally indicated at 42, a servo 43 of any convenient type.

The servo 43 through any convenient linkage indicated at 44 controls the power setting of the vehicle engine generally indicated at 46 to maintain the vehicle speed at least approximately constant despite changes in terrain, load or other operating conditions. In the embodiment shown the variation from the precise selected speed is of the order of plus or minus one or two miles per hour and this is commercially acceptable.

Control switching 48 responsive to suitable manual inputs, e.g., actuation of the vehicle brake and manually operated push buttons as hereinafter described, is connected in series with the vehicle battery 13 for controlling current flow therefrom through a line 51 to a reset unit 29. The reset unit 29 is thereby actuable for applying a reset signal to the memory unit 27 and gate 25 through a reset line 30. The control switching 48 also controls current flow through a line 52 to a venting solenoid 53.

The venting solenoid is mechanically connected as indicated at 54 to the servo 43 in a manner that energization of the venting solenoid 53 is required for servo control of vehicle engine power output. The venting solenoid 53 is connected through a low speed inhibit unit 56 to the other or ground side of the battery 13. The low speed inhibit circuit 56 requires a predetermined minimum potential on line 58 connecting the d.c. speed signal line 20 to the low speed inhibit unit 56. The low speed inhibit unit 56 responds to a d.c. speed signal above a predetermined minimum level to allow energization of the venting solenoid 53. The low speed inhibit unit 56 can be set to thus inhibit energization of the venting solenoid 53 and hence the servo 43 below a desired vehicle speed, e.g., 25 miles per hour.

Turning now to the detailed circuitry of the apparatus 10, attention is directed to FIG. 2.

REGULATED POWER SUPPLY 11

The regulated supply 11 provides a regulated positive operating potential to remaining portions of the apparatus 10. In the preferred embodiment shown, the regulated supply comprises an inductor L1 and capacitor C1 connected in series as a filter network. The free end of the inductor L1 is connected through the ignition switch 12 to the positive side of the d.c. source or vehicle battery 13 and the free end of the capacitor C1 is connected to negative or ground side of the d.c. source 13 through a conductor 61 hereinafter termed the ground line. The ground line 61 may be a conductor connected directly to the battery 13 or, as will in many cases be convenient, may include conductively connected portions of the vehicle. A Zener diode Z1 connects across the capacitor C1 to limit the maximum transient voltage thereacross to a predetermined value. A resistor R2 connects from a point 62 intermediate the Zener Z1 and conductor L1 to a positive supply line 63. A further Zener diode Z2 connects the positive supply line 63 and ground line 61 to regulate the potential appearing thereacross. A capacitor C2 parallels the Zener Z2 to further stabilize the potential across the positive supply and ground lines 63 and 61, respectively. The positive supply line 63 supplies regulated positive potential to portions of the apparatus 10 as hereinafter described.

FREQUENCY TO VOLTAGE CONVERTER 19

The frequency to voltage converter 19 comprises an NPN transistor Q1 and a PNP transistor Q2 connected emitter-to-emitter. The collector of transistor Q1 connects to the positive supply line 63 and the collector of transistor Q2 connects through a capacitor C4 to the ground line 61. One side of the a.c. source 16 connects through a resistor R3 to the bases of the transistors Q1 and Q2. The other side of the a.c. source 16 connects to the common emitters of said transistors. A capacitor

C3 connects across the emitter and collector terminals of transistor Q2. A resistor R4 parallels the capacitor C4. An RC filter comprising a series resistor R9 and capacitor C5 is connected across the resistor R4 with the capacitor C5 being connected to the ground side of resistor R4. The aforementioned circuitry of the frequency-to-voltage converter 19 converts the variable frequency a.c. source 16 to a d.c. voltage, the amplitude of which is proportional to frequency of the a.c. source. This d.c. signal is applied from a junction point 66 intermediate resistor R9 and capacitor C5 through a resistor R5 to the noninverting input 12' of a high gain d.c. operational amplifier A1.

The operational amplifier A1 may be of any conventional construction and, hence, its internal circuitry need not be described in detail. For example, the preferred embodiment of the invention utilizes an operational amplifier A1 commercially available as Part No. PA-238 from General Electric as shown in their semiconductor Specification Sheet No. 85.27 (dated Oct., 1967) the operational amplifier pin numbers 1', 3', 5', 7', 8', 10', 12', 14' of FIG. 2 corresponding to pin numbers 1, 3, 5, 7, 8, 10, 12 and 14, respectively, of the aforementioned specification sheet.

Positive operating potential is supplied from the positive supply line 63 to the pin 3' and ground potential is supplied from the ground line 61 to the pin 8'. Operating bias for the negative input 10' is supplied by connection thereof through a resistor R6 to the ground line 61. The operational amplifier A1 provides an output voltage at pin 7' for driving succeeding circuitry without loading prior circuitry and hence without degrading the signal appearing at junction point 66. To limit the gain of the operational amplifier A1, to enhance the stability thereof and to provide for frequency compensation, further connections are provided. These include a series resistor R8 and capacitor C6 connected from the pin 1' to the pin 14', a capacitor C7 connected from the output pin 7' to pin 5' and a resistor R7 connected also from the output pin 7' to the negative input pin 10'.

The output of the operational amplifier A1 appearing on pin 7' comprises the d.c. speed signal and is applied through line 20 to one input of the differential amplifier 21 and to one input of the comparator 31 (FIG. 3).

DIFFERENTIAL AMPLIFIER 21

The differential amplifier circuit 21 includes a high gain d.c. operational amplifier A2 which may be of any conventional type. However, in the preferred embodiment shown, the operational amplifier A2 is identical to the operational amplifier A1 and the catalogue references as to the internal circuitry terminating in pins 1', 3', 5', 7', 8', 10', 12' and 14' given above with respect to the operational amplifier A1 applies to the operational amplifier A2 as well. Hence, a detailed discussion of the internal circuitry and the operational amplifier A2 is not believed required.

The d.c. speed signal line 20 connects through a resistor R16 to the inverting input pin 10' of the operational amplifier A2. The reference signal from the memory and digital-to-analog converter unit 27 is applied through the line 28 and a resistor R11 to the noninverting input pin 12' of the operational amplifier

A2. A voltage divider comprising series resistors R12 and R14 connects between the positive supply line 63 and the ground line 61. A resistor R13 connects the noninverting input pin 12' of the operational amplifier A2 to a junction point 67 intermediate resistors R12 and R14 for providing operating bias to the noninverting input pin 12'. The power, frequency compensation and feedback connections to the operational amplifier A2 are similar to those above described with respect to the operational amplifier A1, resistors R10 and R15 and capacitors C8 and C9 of the operational amplifier A2 corresponding to the resistors R7 and R8 and capacitors C6 and C7, respectively, of the operational amplifier A1. The output of the differential amplifier circuit 21 is taken from pin 7' of the operational amplifier A2 through the line 36 and is applied as a variable amplitude d.c. voltage to the pulse width modulator 34.

PULSE WIDTH MODULATOR 34

The pulse width modulator 34 includes oscillator circuitry generally indicated at 69 capable of generating a constant frequency pulse train comprising a series of constant amplitude, short duration positive pulses. The oscillator 69 comprises a unijunction transistor Q13 having its upper base connected through a resistor R17 to positive source line 63 and its lower base connected through a resistor R18 to the ground line 61. The positive source line 63 connects to the ground line 61 through a series resistor R26 and capacitor C11. The emitter of the unijunction Q13 connects to a junction point 71 intermediate said resistor and capacitor. Output from the oscillator 69 is taken from the lower base of the unijunction Q13 through a capacitor C10.

The pulse width modulator 34 further includes a monostable multivibrator 72. The multivibrator 72 comprises a pair of NPN transistors Q4 and Q5. The emitters of transistors Q4 and Q5 connect through a common resistor R25 to the ground line 61. The collectors of transistors Q4 and Q5 connect through respective resistors R22 and R19 to the positive supply line 63. Operating bias is supplied to the bases of the transistors Q4 and Q5 by resistors R21 and R24 connected, respectively, to the positive source line 63 and to ground line 61. A resistor R23 connects the base of the transistor Q5 to collector of transistor Q4. The base of transistor Q4 connects through a series capacitor C12 and diode D3 to the collector of transistor Q5, the diode D3 being oriented with its cathode toward said collector.

The oscillator output capacitor C10 connects the lower base of unijunction Q13 to the base of transistor Q5 for applying positive spike pulses thereto at the fixed frequency of the oscillator 69 for rendering the transistor Q5 conductive upon initiation of conduction through the unijunction Q13. The differential amplifier output line 36 connects through a resistor R20 to a junction point 73 between the diode D3 and capacitor C12. Variations in the voltage on the line 36 vary the time required for charging the capacitor C12 through the resistor R21, diode D3 and conductive transistor Q5 to a level sufficient to turn on transistor Q4 and thus turn off transistor Q5. The latter remains nonconductive until unijunction Q13 again fires whereupon the multivibrator 72 repeats its cycle of operation. The output of the pulse width modulator 34, termed the duty

cycle signal, is taken from the collector of transistor Q5 and applied through line 39 to the valve driver 38. The duty cycle signal is of square waveform, of constant frequency equal to that of oscillator 69 and of pulse width varying with the output of differential amplifier 21.

VALVE DRIVER 38

The valve driver 38 comprises a current amplifier including an NPN transistor Q6 and a PNP transistor Q7. Transistor Q7 connects at its emitter to the positive source line 63 and at its collector through a resistor R54 to the base of transistor Q6. The duty cycle line 39 connects through a resistor R55 to the base of transistor Q7. The emitter of transistor Q6 connects to the ground line 61. The collector of transistor Q6 is connected through the control solenoid 41 and thence to the d.c. source 13 at its positive end. A diode D4 connects across the control solenoid 41, with the anode thereof toward the transistor Q6, as a reverse current shunt.

PULSE GENERATOR 23

Turning now to FIG. 3, the pulse generator 23 comprises a unijunction transistor Q15. The upper base of unijunction Q15 connects through a resistor R58 to the positive source line 63 and the lower base thereof connects through a resistor R59 to the ground line 61. Positive source line 63 is connected through a series resistor R1 and capacitor C13 to the ground line 61. The emitter of unijunction Q15 connects to a junction point 76 between said resistor and capacitor. Output is taken from the lower base of unijunction Q15 through a resistor R60 to the base of an NPN transistor Q3 functioning as an amplifier inverter. The emitter of transistor Q3 connects to the ground line 61 and the collector thereof connects through a resistor R61 to the positive potential line 63. The output of the pulse generator 23 appears on the collector of transistor Q3 and consists of a pulse train of fixed frequency and square waveform comprising a potential at the level of the positive supply line 63 interrupted by periodic, short duration intervals of approximately ground potential. Pulse line 24 applies this pulse train to the gate unit 25.

GATE 25

The gate unit 25 comprises NAND gates N1, N2 and N3 of any conventional type. NAND gate N1 has an output terminal 81 and input terminals 82 and 83. NAND gate N2 has an output terminal 84 and input terminals 86 and 87. NAND gate N3 has an output terminal 92 and input terminals 94 and 95.

The pulse line 24 connects to input 82 of NAND gate N1, the output terminal 81 of which connects through gate output line 26 to the input of the memory unit 27. The comparator output line 32 connects to input 94 of NAND gate N3. The line 30 from the reset portion 29 connects to input 87 of NAND gate N2.

Considering the internal connections between the NAND gates in the unit 25, the output 84 of NAND N2 connects to input 83 of NAND N1 and input 95 of NAND N3. The output 92 of NAND N3 connects to the input 86 of NAND N2. In response to proper poten-

tials on the lines 30 and 32, the gate unit 25 will transfer and invert pulses from the pulse generator line 24 through the line 26 to the memory unit 27.

RESET UNIT 29

The reset unit 29 comprises an NPN transistor Q10, the emitter of which is connected to the ground line 61 and the collector of which is connected through a resistor R33 to the positive source line 63. A resistor R62 and a capacitor C16 connect in parallel between the collector of said transistor and the ground line 61. The capacitor C16 delays briefly, by the time required for its charging, the rise of collector potential of the transistor Q10 when the ignition switch 12 is closed, for purposes appearing hereinafter. The base of the transistor Q10 is coupled to the line 51 from the control switching 48, hereinafter described in detail, through a resistor R34. The reset line 30 connects to the collector of transistor Q10 and is normally held by the normally nonconductive state of the latter at the potential of the positive supply line 63. The reset line 30 is the output line of the reset unit 29 and connects to the gate unit 25 as above described and to the counter portion 97 of the memory unit 27.

MEMORY UNIT 27

The counter portion 97 of the memory unit 27 comprises a digital counter and more particularly a binary counter for counting pulse supplied thereto from the gate 25. The counter 97 comprises a series of flip-flop circuits F1, F2, F3, F4, F5 and F6. Said flip-flops may be of any conventional construction. In the particular embodiment shown, the flip-flop pairs F1, F2 and F3, F4 and F5, F6 comprise dual JK flip-flop units generally indicated as FF1, FF2 and FF3, respectively and of the type generally indicated on Data Sheet 6004, dated Jan. 1968 of the Amelco Data Book, Volume 1 published by Amelco Semiconductor, 1300 Terra Bella Avenue, Mountain View, California. Terminals 2'', 4'', 7'', 8'' and 9'', 12'', 14'' and 16'' of each of the flip-flop units FF1, FF2 and FF3 correspond to terminals 2, 4, 7, 8, 9, 12, 14 and 16 of the corresponding flip-flop unit disclosed in the aforementioned reference.

The units FF1, FF2 and FF3 are preferably identical and thus the following description of the internal connections of the unit FF1 will be understood to apply to the units FF2 and FF3 as well. The leading flip-flop F1 of the unit FF1 has an input terminal 4'' connected to the gate output line 26. Output is taken from terminal 2'' of flip-flop F1 and applied through line 98 to the input terminal 12'' of trailing flip-flop F2. The output of the flip-flop F2 appears at terminal 14'' thereof. The flip-flops F1 and F2 of unit FF1 connect at terminals 7'' and 9'', respectively, to the reset line 30.

As to the interconnections of the flip-flop units FF1, FF2 and FF3, output is taken from terminal 14'' of trailing flip-flop F2 of unit FF1 and applied to the input terminal 4'' of leading flip-flop F3 of unit FF2. The flip-flops F1 through F6 thus described constitute a binary counter of the upcounter type. The pulse count stored by the counter 97 appears on the output terminals 2'' and 14'' of the flip-flops F1-F6 in binary representation.

Turning now to the D/A converter portion 106 of the memory unit 27, same includes a resistive network 123

including a voltage divider consisting of resistors R35, R38, R41, R44, R47 and R50 connected in series from the ground line 61 to a junction point 108. Series resistor pairs R36 and R37, R39 and R40, R42 and R43, R45 and R46, R48 and R49, respectively, connect from the positive supply line 63 to junction points 111 through 115 between successive ones of the aforementioned resistors R35, R38, R41, R44, R47, R50. In addition, a series pair of resistors R51 and R52 connects from the positive source line 63 to the junction point 108. The intermediate output terminals 2'' of the units FF1, FF2 and FF3 connect to junction points 117, 119 and 121, respectively, intermediate the resistor pairs R36 and R37, R42 and R43, R48 and R49, respectively. Also, the output terminals 14'' of the units FF1, FF2, FF3 connect to junction points 118, 120 and 122, respectively, intermediate the resistor pairs R39 and R40, R45 and R46, R51 and R52, respectively. The network 123 converts the binary count represented by the state of the outputs of the flip-flops F1-F6 to a corresponding d.c. potential level on point 108 which varies in proportion to the number of pulse counted, i.e., to the binary count stored.

The D/A converter 106 further comprises an NPN transistor Q12, the emitter of which is connected through a resistor R53 to the ground line 61 and the collector of which is connected to the positive source line 63. The base of said transistor connects to the junction point 108. The emitter potential of transistor Q12 varies in proportion to the potential on point 108. Output, comprising the reference signal, is taken from the emitter of transistor Q12 and is applied through the reference signal line 28 to the comparator 31 and to the differential amplifier 21.

COMPARATOR 31

The comparator circuit 31 (FIG. 1) includes an operational amplifier A3 which may be of any conventional type but preferably is identical to operational amplifiers A1 and A2 above described. Thus, the terminal numbers 1', 3', 5', 7', 8', 10', 12', 14' correspond to similarly numbered terminals of the aforementioned operational amplifier A1 and the internal circuitry of the operational amplifier A3 is thus believed to require no further disclosure. In a manner similar to the operational amplifiers A1 and A2, positive operating potential is supplied to pin 3' of the operational amplifier A3 from the positive source line 63 and ground potential is applied to the terminal 8' thereof from the ground line 61. Also a frequency compensating capacitor C14 connects from the output terminal 7' to the terminal 5' and a frequency compensation connection comprising a series resistor R27 and capacitor C15 connects from the terminal 1' to the terminal 14'. However, no feedback connection is made from the output connection 7' of operational amplifier A3 to either of the inputs 10' and 12' thereof. As a result, the effective d.c. voltage gain from the input to the output of the operational amplifier A3 is much greater than in the case of the operational amplifiers A1 and A2. Thus, when the potential on input 10' rises past a level near that of input 12' (in the present embodiment 150 millivolts therebelow) the potential on output terminal 7' will switch from a maximum level corresponding to the level of the positive supply line 63 to a minimum or near ground potential.

The d.c. speed signal on line 20 is applied through a series diode D1 and resistor R31 to the positive input terminal 12' of operational amplifier A3. The reference signal is taken from the output of the memory unit 27 through line 28 and a diode D2 and resistor R32 in series therewith and applied to the negative input terminal 10' of operational amplifier A3.

The comparator 31 further includes transistor switching responsive to a switching of the output of the operational amplifier A3 and comprising transistors Q9 and Q8. PNP transistor Q9 is driven at its base from the output terminal 7' of operational amplifier A3 and connects at its emitter through a resistor R28 to the positive source line 63 and at its collector through a resistor R30 to the ground line 61. NPN transistor Q8 connects at its base to the collector of transistor Q9, at its emitter directly to the ground line 61 and at its collector through a resistor R29 to the positive source line 63. Comparator output, alternatively one of two discrete potentials, is taken from the collector of transistor Q8 and applied through line 32 to input terminal 94 of the gate unit 25.

CONTROL SWITCHING 48

Turning now to the control switching 48, same includes a speed set switch 126. This switch has stationary contacts 127 and 128 and a manually actuatable push button 129 for actuating the movable contact thereof. Said movable contact is normally biased open by any convenient means schematically indicated by a spring 131. Closure of the contacts 127 connects the positive terminal of the battery 13 to the line 51 and thence to the reset circuit 29. Closure of contacts 128 connects the positive terminal of battery 13 through line 52 to the upper end 132 of the venting solenoid 53.

A resume switch 134 has stationary contacts 136 connected in a parallel circuit with the stationary contacts 128 of the speed set switch 126, the movable contact of switch 134 being normally biased to an open position by any convenient means here schematically indicated as a spring 137. Resume switch 134 further includes a push button 138 manually actuatable to close the connection between the battery 13 and line 52.

A normally closed single pole brake switch 141 is connected as indicated schematically by the broken line 140 to the vehicle brake system so that actuation of the vehicle brakes results in opening of the brake switch 141. Brake switch 141 is connected in series with a normally open single pole, single throw contact K1 between the positive terminal of the vehicle battery 13 and the upper end 132 of the venting solenoid 53. The contact K1 is closed by energization of the venting solenoid 53 through suitable linkage generally indicated at 143.

LOW SPEED INHIBIT CIRCUIT 56

The low speed inhibit circuit 56 comprises switching transistors Q14 and Q11. NPN transistor Q14 connects at its collector to the positive source line 63 and at its emitter through a resistor R56 to the ground line 61. The base of transistor Q14 is connected to the d.c. speed signal line 20. NPN transistor Q11 is connected at its emitter to the ground line 61 and at its collector to the free end of the venting solenoid 53. A diode D5 is connected across the venting solenoid with its anode toward the transistor Q11 for shunting reverse current

around the venting solenoid 53. A series resistor 57 and Zener diode Z3 connect between the emitter of transistor Q14 and the base of transistor Q11. The Zener is oriented with its anode toward transistor Q11 to prevent actuation thereof in the absence of a d.c. speed signal above a minimum level. This minimum level may be set by appropriate selection of the Zener Z3 to correspond to a desired minimum vehicle speed, for example, 25 miles per hour.

SERVO 43

Although any convenient servo 43 may be used, FIG. 3 discloses schematically one particular embodiment which has been found effective.

More particularly, the servo 43 comprises an airtight housing 151 including an axially movable wall or diaphragm 152. A spring 153 urges the diaphragm 152 outwardly of the chamber 154 defined within the housing 151. The diaphragm 152 is connected by any suitable and preferably flexible linkage 44 to a throttle lever 156 which controls the opening of the throttle plate 157 in the carburetor throat 158 of a gasoline internal combustion engine. A conventional throttle return spring 159 urges the throttle to its closed position. It will be apparent that the apparatus 10 may be used with other forms of engine and in such case that the linkage 44 may connect to the corresponding engine power control means thereof.

Opposed conduits 161 and 162 are connected respectively to a suitable vacuum source 163 and to the atmosphere. The vacuum source 163 may be of any convenient type, for example, the inlet manifold of the engine. A flapper valve plate 164 is supported at one end thereof within the housing 151, the free end thereof being disposed between the opposed ends of the conduits 161 and 162. The flapper 164 is adapted to alternatively block the opposed ends of said conduits. In the particular embodiment shown, the flapper 164 is pivotally mounted on the housing and is spring biased toward the vacuum conduit for normally closing same. The control solenoid connects through the linkage 42 to the flapper 164 in a manner that current flow through the control solenoid moves the flapper 164 to open the vacuum conduit 161 and close the atmosphere conduit 162.

A vent valve 166 is normally urged open by a spring 167. The linkage 54 from the venting solenoid connects to the vent valve 166 so that upon energization of the venting solenoid the vent valve 166 will close. When the vent valve 166 is closed, movement of the flapper 164 away from the vacuum conduit 161 and its closing contact with the atmosphere conduit 162 reduces the pressure within the chamber 154 below atmospheric pressure causing the diaphragm 152 to move inwardly of the housing 151 and open the throttle 157 to an extent directly related to the period of energization of the control solenoid 41.

OPERATION

Ignition on, vehicle at rest

When the ignition switch 12 (FIG. 2) of the vehicle is closed, battery potential is applied to the regulated supply 11 which, as above described, furnishes a regulated positive voltage to the positive source line 63. Where a 12 volt battery is used, the source line 63 is in

the present embodiment maintained at about 11 volts positive with respect to the ground line 61. Thus, operating potential from the supply 11 is applied to the system 10.

Although closure of the ignition switch 12 results in application of operating potential to the memory unit 27 and reset unit 29 (FIG. 3), the capacitor C16 is in a discharged condition as a result of prior discharge through the resistor R62. Charging of the capacitor C16 through resistor R33, though rapid, is not instantaneous. Thus, the reset line 30 remains momentarily at a low potential during the initial charging of capacitor C16 to apply an initial reset signal to the counter portion 97 and thus insure resetting of the counter portion 97 to zero count. This momentary initial reset signal is also applied by reset line 30 to the input 87 of NAND N2 of the gate unit 25.

At this point, the speed set switch 126, the resume switch 138 and the contacts K1 are open, whereby the venting solenoid is de-energized. As a result, the vent valve 166 is open and the servo 43 exercises no control over the throttle 157 which is thus completely subject to manual control by the vehicle operator.

With the positive supply line 63 energized, current passes through the resistor R1 to charge capacitor 13 of the pulse generator 23 at a preselected rate controlled by the resistor R1. When this charge has increased sufficiently, it fires the unijunction Q15, the capacitor C13 then rapidly discharging through said unijunction and through the resistor R59 to provide a positive spike pulse through the resistor R60 to the base of transistor Q3. Transistor Q3 is thus briefly rendered conductive through the resistor R61. Thus, the potential of the collector of transistor Q3 drops momentarily to a value near ground potential, thereafter returning the positive source potential. This process repeats regularly with the result that the normal positive supply potential on line 24 is interrupted by a series of negative going pulses of fixed frequency and width. In the particular embodiment shown, this frequency is one kilohertz, a value found to be sufficiently slow for reliable operation of the gate 25 and counter 97 and yet sufficiently rapid for rapid establishment of a reference signal. This pulse train is applied to input 82 of the NAND N1 in gate unit 25.

Inasmuch as the vehicle speed is zero, the output of the frequency-to-voltage converter 19 on the d.c. speed signal line 20 is at its minimum level. With no counts registered by the memory counter 97, the output on the line 28 of the memory unit 27 will be at its minimum level (in the present embodiment approximately 1.5 volts). This minimum reference signal level is preferably sufficiently high to convince the comparator 31 that a match between the d.c. speed and reference signals exists. Thus, the comparator will switch (if it had not previously done so as a result of a prior stopping of the vehicle) and a low potential appears on the collector of the output transistor Q8 thereof. This low potential is applied through comparator output line 32 to input pin 94 of NAND N3. In the following discussion of the operation of the gate unit 25, the following terminology will be adopted for convenience in reference: a relatively high potential will be termed a "+" (plus) signal and a relatively low potential will be termed a "0" (zero) signal. The NAND's N1-N3 of the

present embodiment produce a "0" output only in response to a "+" at both inputs thereof and for all other combinations of inputs ("0," "0" and "0", "+" and "+", "0") produce a "+" output.

The initial momentary reset signal on line 30 produces a momentary "0" at input 87 of NAND N2. This, coupled with a "+" on input 94 of NAND N3, as later discussion of the operation of the gate unit 25 in more detail will make apparent, would enable the gate unit 25 to conduct (with inverted polarity) the pulse train from pulse generator 23 to the counter portion 97. However, the comparator 31 has sensed a match, switched and applied a low or "0" potential through line 32 to the input 94. Thus, the gate unit 25 remains nonconductive and the counter portion 97 remains at zero count.

On the other hand, should the circuit parameters be such that the minimum d.c. speed signal be sufficiently greater than the minimum reference signal that the comparator sees no initial match condition, the result will merely be, as indicated by discussion hereinafter in greater detail of intentional initiation of speed control of the vehicle in motion, that the gate 25 will supply one or a few pulses to the memory unit 27 causing the reference signal to rise sufficiently that the comparator 31 senses a match condition, switches and shuts off the gate 25.

Since the speed of the vehicle at rest is necessarily below the minimum required for conduction of the low speed inhibit unit 56, the apparatus 10 cannot control the engine power setting, whatever the count stored in the memory 27 and the resulting reference signal, despite an inadvertent actuation of the speed set or resume switch at this time.

VEHICLE IN MOTION

When the vehicle operator places the vehicle in motion, the a.c. source 16 generates an a.c. voltage of frequency proportional to the instantaneous vehicle speed. This a.c. speed signal is applied across the base-emitter junctions of the transistors Q1 and Q2. During the half cycle in which said bases are positive in respect to said emitters, termed the positive half cycle, the transistor Q1 conducts from the positive source line 63 through capacitors C3 and C4 to the ground line 61, charging said capacitors. During the negative half cycle of the a.c. source 16, the bases of transistors Q1 and Q2 are rendered negative with respect to the emitters thereof with the result that the capacitor C3 discharges through the transistor Q2 while the capacitor C4 discharges at a predetermined rate through shunt resistor R4. As the frequency of the a.c. speed signal increases with vehicle speed, the period of each cycle thereof decreases and capacitor C4 discharges to a lesser extent through resistor R4 in each negative half cycle. Conversely, as vehicle speed is reduced, the period of the a.c. speed signal increases and capacitor C4 discharges to a greater extent through resistor R4 during the negative half cycle. Consequently, a rippling d.c. potential appears across the capacitor C4 the average value of which is, by appropriate selection of the values of the circuit elements, proportional to the vehicle speed. The RC network comprising resistor R9 and capacitor C5 smooths the ripple superimposed on the d.c. potential appearing across capacitor C4 and

applies the resulting d.c. potential, of amplitude proportional to the vehicle speed, to the input 12' of operational amplifier A1. As the result, the d.c. speed signal appears on the output line 20 of operational A1 for application to the differential amplifier 21 and the comparator 31.

The operational amplifier A1 supplies sufficient current to drive the differential amplifier and comparator without loading the transistors Q1 and Q2 and the RC circuitry driven thereby. Thus, the d.c. speed signal appearing on line 20 will in direct proportion follow the vehicle speed as it rises, falls or remains constant. The d.c. speed signal in the present embodiment lies in the range of 2.5 to 8.0 volts positive.

Referring to FIG. 3 and FIG. 4, column 1 and assuming that the speed set switch 126 has not been actuated and the vehicle is in motion, the gate 25 will normally be in a nonconductive condition as a result of a prior match condition occurring on closure of the ignition switch. As a result, no pulses from the pulse generator 23 are applied to the memory 97 and the reference signal remains at or at least near its lowest potential. Thus, the comparator 31 will be in its normal nonmatch condition as a result of difference between the minimum reference signal from the memory unit 27 and the nonminimum d.c. speed signal applied thereto. As will be apparent from the detailed discussion of the operation of the comparator circuit 31 given hereinafter, in this nonmatch condition a high positive potential appears on the collector of transistor Q8 which is applied through line 32 to the gate 25 rendering input 94 of NAND N3 "+". This condition cannot in the absence of a concurrent reset signal (low potential) on reset line 30 cause conduction of the gate.

As will be apparent from the detailed discussion of their operation hereinafter, the differential amplifier 21, pulse width modulator 34 and valve driver 38 respond to the difference between the nonminimum d.c. speed signal and the minimum reference signal applied by energizing the control solenoid 41 and hence the flapper 164 of the servo 43 at a duty cycle which if the servo 43 was in control of the engine would minimize the difference therebetween. However, since neither the speed set switch 126 or resume switch 134 has been actuated, the vent solenoid 53 must be unenergized whereby the servo 43 exerts no control over the vehicle power setting. Thus, the control solenoid is not energized, since it has positive voltage applied only when contacts K1 of the venting coil are closed. Complete manual control of the vehicle engine power setting thus remains with the operator.

SPEED CONTROL — GENERAL

To render the apparatus 10 operative to maintain the speed of the vehicle at a desired speed automatically and despite changes in load or terrain, the operator first, by use of the vehicle throttle, brings the vehicle to the speed which is desired to be maintained and then momentarily presses the speed set switch 126 and releases same. Thereupon the apparatus 10 assumes control of the vehicle throttle and thereafter adjusts same as required to maintain the vehicle speed at the desired value.

SPEED CONTROL - DEPRESSION OF SPEED SET SWITCH 126

The following discussion refers to FIGS. 2 and 3 and to FIG. 4, column 2. Momentary depression of the speed set switch 126 closes the stationary contacts 127 and 128 thereof. Closure of the contacts 127 applies positive potential from the vehicle battery 13 through resistor 34 to the base of transistor Q10 of the reset circuit 29 for energizing said reset circuit. The positive potential applied to the base of transistor Q10 renders same conductive from the positive source line 63 to the ground line 61, the capacitor C16 discharging therethrough, and rapidly dropping the potential of reset line 30 essentially to ground potential establishing the reset signal on reset line 30. This resets all of the flip-flops F1-F6 of the memory 97 to their unenergized or zero state and hence assures that the counter 97 registers a zero count.

As a result, the outputs 2'' and 14'' of said flip-flops are at, or substantially at, ground potential.

As long as the speed set switch is held closed, the flip-flops F1-F6 remain in their zero state and hold the point 108 at ground potential. This holds emitter follower transistor Q12 nonconductive and reference signal line 28 at ground potential.

Inasmuch as the reference signal is substantially lower than the d.c. speed signal, no match is sensed by the comparator unit 31 and as a result the high positive potential remains on the output line 32 thereof and hence on input 94 of NAND N3 of the gate unit 25.

The low potential reset signal on reset line 30 is also applied to the input 87 of NAND N2 of the gate unit 25. The resulting "0" on input 87 of NAND N2 results necessarily in a "+" at output 84 thereof and hence at input 83 of NAND N1. Thus, a "+" at input 82, corresponding to the absence of a negative going pulse from the pulse generator 23, results in a "0" at the output 81 of the NAND N1. Conversely, a "0" at input 82, corresponding to a negative going pulse from the pulse generator 23, results in a "+" at output 81. As a result, the aforementioned "+" at input 83 of NAND N1 enables same to conduct and invert the pulse train from the pulse generator 23 to the line 26. Thus, while the reset signal appears, a series of short duration positive pulses appear on line 26.

The signals at the remaining NAND terminals are shown in column 2 of FIG. 4.

The aforementioned pulse is applied by the line 26 to the input 4' of the leading flip-flop F1 of the binary counter 97. However, they are not registered by that counter since the reset line is still held by the reset unit 29 at a low potential. Thus, the reference signal on line 28 remains low.

Returning to the closed speed set switch 126, the closed contacts 128 thereof applies positive battery potential to the venting solenoid 53 at junction point 132.

If the vehicle is at a speed above the minimum required for actuation of the low speed inhibit unit 56, the d.c. speed signal applied by line 20 to the base of transistor Q14 will render same conductive. As a result, a positive potential will appear upon the emitter thereof which is proportional to vehicle speed and will exceed the Zener voltage of Zener Z3. Thereupon the

latter will conduct through the base emitter junction of transistor Q11 to enable same to conduct through the venting solenoid 53, the closed speed set contact 128 and the vehicle battery 13. The venting solenoid, thus actuated, closes its lock-in contact K1 to assure continuing current supply therethrough from the vehicle battery 13 and the closed brake switch, even after the speed set switch 126 is released. The energized venting solenoid also closes the vent valve 166 of the servo 43. As a result, the flapper 164, controlled by the differential amplifier 21, pulse width modulator 34 and valve driver 38 through the control solenoid 41, in its movement between the vacuum and atmosphere conduits 161 and 162, would normally drop the pressure within the chamber 154 tending to move the diaphragm 152 inwardly to assume control of the opening of the throttle 157. However, since the counter 97 is still reset, holding the reference signal at a low value (i.e. ground potential), the differential amplifier sees the vehicle speed as excessive and thus minimizes the duty cycle of the control solenoid 41. In the present embodiment, the minimum duty cycle is zero and thus the control solenoid remains unenergized. Consequently, the servo does not act to open the throttle and full manual throttle control is retained by the operator.

On the other hand, if the speed of the vehicle is below the predetermined low speed required for actuation of the low speed inhibit circuit, the Zener Z3 will not conduct and the transistor Q11 will remain nonconductive thus maintaining open the path between the venting solenoid and the vehicle battery. As a result, closure of the speed set contact 128 under such low vehicle speed conditions will not close the vent valve 166 and the servo will remain inoperative.

SPEED CONTROL - RELEASE OF SPEED SET SWITCH 126

The following discussion refers to FIGS. 2, 3 and 5 and to FIG. 4, column 3. When the speed set switch 126 is released, the opening of contacts 127 thereof breaks the connection from the positive battery terminal to the base of reset transistor Q10 whereon the transistor Q10 falls nonconductive. Thus, the collector potential thereof rises to the level of positive source line 63 as the capacitor C16 charges through the resistor R33. In consequence, the potential of the reset line 30 rises to the positive source level. This releases the counter 97 from the reset condition and enables it to start counting in response to pulses applied thereto from the gate on line 26.

The high potential on reset line 30 also is applied to input 87 of NAND N2 of the gate 25. This "+" condition of input 87 does not change the conductive condition of the gate 25, however. More particularly, the reset signal had resulted in "+" conditions on terminals 84 and 95 and, through the resetting of counter 97 and the consequent lack of a match in the comparator 31, a "+" condition on terminal 94. This in turn had established a "0" on NAND N3 output 92 and hence on NAND N2 input 86 which causes terminals 83 and 84 to remain "+" when the reset signal terminates and input 87 goes "+." Retention of the "+" on NAND N1 input 83 results in its conduction still being controlled by the pulse train applied to input 82 thereof. Hence, the gate 25 continues to provide the inverted pulse

train through gate output line 26 to the counter 97. Thus, train of narrow, positive pulses continues to appear on input 4'' of flip-flop F1.

The binary counter 97 is arranged in the conventional manner to switch each of the flip-flops thereof upon the drop in potential at the end of a positive pulse applied to the input of such flip-flop. Thus, at the end of the first positive pulse applied to the input 4'' of flip-flop F1, following termination of the reset signal, the flip-flop F1 changes state with the result that the output 2' thereof goes from ground potential to a high potential. This switching will be hereinafter termed a switching from a "0" output to a "1" output and establishes a count of one in the counter 97. At the end of the second positive pulse applied to the input 4'' of flip-flop F1, the latter again changes state and is thus restored to its reset state, the potential at the output 2' thereof falling from a high potential to ground potential and reestablishing a count of "0" at the output 2' thereof.

However, this drop in potential is applied to the input 12'' of flip-flop F2 causing same to switch from its reset state to its energized state, thereby causing the output 14'' to rise from ground potential to a high potential, that is, from "0" to "1." Thus, at this point the counter 97 has counted two pulses from the line 29 and therefore registers a binary "10."

Thus, as shown in FIG. 5, each of the flip-flops F1-F6 switches at one-half the rate of the flip-flop proceeding it, the flip-flop F1 switching once for each pulse applied thereto on line 26 and completing one switching cycle from reset condition through energized condition and back to reset condition once for every two pulses applied to the input thereof. This counting sequence continues for as long as pulses are applied to the counter by the line 26, up to the capacity of the counter. Each binary level stored in the counter 97 corresponds to a discrete reference speed at which it may be desired to have the vehicle maintained. It will be apparent that a greater number of flip-flops may be employed where the range of cruising speeds at which the vehicle may desirably be maintained is great or where the difference between reference speeds corresponding to successive binary counts is desired to be very small. However, the six flip-flop counter of the present embodiment will at its maximum count supply 64 discrete reference speed levels and is thereby capable of supplying reference signals level differences corresponding to actual vehicle speed differences of about one mile per hour depending upon the maximum speed at which the apparatus 10 is to be used. This maximum speed may be set to be the maximum speed of the vehicle or, for example, the maximum speed limit allowable on particular types of highways by variation in the increment of actual speed which each binary count stored corresponds to. It is further contemplated that the range of vehicle speeds at which the apparatus 10 will operate may shift upwardly or downwardly by varying the gain of speed voltage amplifier A.

Considering now the resistance network portion of the digital-to-analog converter, in the zero count state of the counter 97, ground or low potential appears on each of the junction points 117-122 and hence the point 108 and the reference signal line 28 are held at a minimum potential. Whenever one of the flip-flops

F1-F6 switches to an energized condition, the corresponding output thereof is switched to the potential of the positive source line 63 which positive potential appears on the corresponding one of the points 117 through 122.

Thus, for example, when only the flip-flop F1 is in its energized condition, only junction point 117 will be at the positive supply potential. Thus, the potential appearing on point 108 will be raised by an increment by reason of the positive potential on point 117. When the counter 97 registers two counts the junction point 118 will be in a high potential and the remaining junction points 117 and 119 through 122 will be at low potential. However, the potential of point 108 will be an increment higher than when the counter registered a one count due to loss of the voltage drop across resistor R38. The potential at point 108 will be increased by a further increment when the counter has stored three counts since high positive potential will appear at both the junction points 117 and 118. Thus, as the count stored by counter 97 increases incrementally, so will the potential at the point 108. Therefore, as pulses are applied to the input of the counter 97 and counted thereby, the potential at point 108 rises in a step-wise fashion from its minimum value toward its maximum value in the manner indicated in FIG. 5 and in column 3 of FIG. 4. In the particular embodiment shown, the range of reference signal levels varies from 1.5 to 8.0 volts positive. The potential appearing at junction point 108 is applied to the base of emitter follower transistor Q12 and thus appears at the emitter thereof and upon the line 28 as the reference speed signal.

As the potential on the reference signal line 28 is stepped upwardly by the counting of the counter 97, it raises the potential on the negative input terminal 10' of the comparator operational amplifier A3. This diminishes the potential difference between the positive and negative input terminals 12' and 10'. The operational amplifier has a high voltage gain and by remaining saturated, maintains its output at a high level, until the stepped signal on the reference line closely approaches the d.c. speed signal. In the particular embodiment shown, when the potential of the reference signal line 28 steps up to a level less than one step above, and here about 150 millivolts above, the d.c. speed signal level, the operational amplifier output switches to a low potential. The comparator 31 has thus sensed a match and is in its match condition. This switch drops the potential on the base of transistor Q9 and renders same conductive from the positive potential line 63 to the ground line 61. Such conduction takes place through the resistor R30 causing a potential drop thereacross and, in consequence, a rise in potential on the base of transistor Q8 rendering same conductive. In consequence, the collector of transistor Q8 drops in potential from that of the positive source line 63 essentially to that of the ground line 61.

This low potential is applied through line 32 to NAND N3 input 94. Thus, said input 94 goes from a "+" condition to a "0" condition. This causes NAND N3 output 92 to switch from its former "0" condition to a "+" condition which is applied to input 86 of NAND N2. In consequence, both inputs of NAND N2 are "+" so that its output 84 and NAND N1 input 83 must be "0." Therefore NAND N1 stops conducting

the inverted pulse train from the pulse generator 23 and its output 81 remains "+" thereafter. In this way, the achievement of match in the comparator 31 turns off the gate 25 and prevents further counting of the counter 97. Thereafter, the counter 97 stores the count previously achieved and output of the memory 27 on the line 28 is stabilized at the value which caused the comparator 31 to achieve the match and turn off the gate as above described, this potential on the line 28 being the stabilized reference speed signal.

It will be apparent that the parameters of the comparator circuit 31 may be adjusted so that a match condition may be achieved upon a condition other than a memory output 150 millivolts above the d.c. speed signal. That is, a greater or lesser differential may be used as desired to define a match. Moreover, it is contemplated that the comparator may be arranged to switch from its nonmatched mode to its matched mode upon a condition wherein the memory output equals or exceeds by a predetermined amount the d.c. speed signal. However, such would require revision or readjustment within the differential amplifier 21 and/or succeeding portions of the apparatus 10 to insure holding the vehicle at, or at least close to, the desired reference speed at which the match is made.

The stabilized reference signal on line 28 resulting after a match is applied to the positive input 12' of the operational amplifier A2 of differential amplifier 21. The operational amplifier A2 detects the difference between the reference signal and d.c. speed signal applied to the input 10' thereof and provides on output 7' thereof a d.c. signal which varies in magnitude in relation to the polarity and magnitude of said difference. Under conditions of match, the d.c. speed signal and reference signal as above described are approximately equal and the differential amplifier output on line 36 is at a medium value, in the present embodiment approximately 5.5 volts. Should the vehicle speed thereafter increase above the desired or reference speed which has been selected, the output of differential amplifier will decrease proportionately in amplitude. On the other hand, if the speed drops below the reference speed selected, the output of the differential amplifier will increase proportionately. In the present embodiment, the differential amplifier output lies in the range of 2.0 to 8.5 volts positive. The line 36 applies the output of the differential amplifier 21 through resistor R20 to junction point 73 in the multivibrator 72 of the pulse width modulator 34.

The oscillator 69 of the pulse width modulator 34 is energized from the regulated supply 11 through positive potential line 63 whereby current flow through resistor 26 charges the capacitor C11 at a preselected rate. When the charge reaches a sufficient level, that is, the firing point of the unijunction Q13, the latter conducts discharging the capacitor C11 through resistor R18. In the present embodiment, the frequency of the oscillator 69 is about 10 hertz. The resulting rise in potential on the lower base of the unijunction is applied as a positive spike pulse through capacitor C10 to the base of multivibrator transistor Q5 rendering same conductive and dropping the potential at the collector thereof. This drops the potential of both the plates of capacitor C12 and the base potential of transistor Q4 through the diode D3 causing said transistor to fall non-

conductive. The rise in collector potential of transistor Q4 is applied to the base of transistor Q5 to hold same conductive.

The capacitor C12 gradually charges from the positive source line 63 through resistor R21, diode D3, the conductive transistor Q5 and resistor R25 to the ground line 61. The rate of charge of the capacitor C12 is governed by the resistance in series therewith. However, the extent to which the capacitor C12 must charge to render transistor Q4 conductive is governed by the potential applied by the differential amplifier output line 36 to the junction point 73 and hence to the leftward plate of capacitor C12 prior to conduction of transistor Q5. Thus, if the potential so applied to junction point 73 is relatively high, the capacitor must be charged to a greater degree to render transistor Q4 conductive and the time required for such charging will be relatively long. On the other hand, if the junction point 73 is at a relatively low potential as a result of a low differential amplifier output potential, the amount of charging and hence the amount of time required for said charging will be decreased. When the capacitor C12 has charged to a sufficient level, transistor Q4 resumes conduction, its collector potential falls turning off transistor Q5 and the potential on the collector of transistor Q5 again rises. Sometime thereafter the oscillator 69 produces a further positive pulse and the above cycle of events repeats. Output is taken from the collector of transistor Q5 to line 39 and applied to the valve driver 38.

Thus, the output of the pulse width modulator 34 is a constant frequency square wave pulse signal of varying duty cycle. Hence, the time during which the transistor Q5 is conductive is proportional to the amplitude of the output of the differential amplifier 21. In the present embodiment, the pulse width modulator 34 is arranged to hold transistor Q5 conductive for up to 90 percent of the period of the oscillator for maximum differential amplifier output or for essentially 0 percent of the period for a minimum differential amplifier output. With the vehicle speed at the reference level, the duty cycle of transistor Q5 conductive time is about 25 percent of the period of oscillator 69.

When the pulse width modulator output on line 39 is at a low potential, during charging of capacitor C12, the low potential applied through resistor R55 to the base of PNP transistor Q7 renders same conductive from the positive source line 63 through resistor R54 and the base-emitter junction of transistor Q6. Such enables transistor Q6 to conduct from the battery 13 through the control solenoid 41 to the ground line 61, energizing said control solenoid. Conversely, when the pulse width modulator output on line 39 again rises after capacitor C12 is charged, transistors Q6 and Q7 fall nonconductive and the control solenoid is again de-energized. Hence, the period of energization of the control solenoid is proportional to the output of the differential amplifier and a short control solenoid duty cycle results from a vehicle speed which exceeds the reference speed and a long duty cycle results from a vehicle speed below the reference level.

The control solenoid when energized moves the flapper 164 to open the vacuum line 161 to the chamber 154. When the duty cycle of the control solenoid shortens due to an increase in vehicle speed

beyond the reference level, the vacuum line 161 opens for shorter periods in each cycle of the oscillator 69 and the pressure within servo chamber 154 increases allowing the diaphragm 152 to be moved outwardly by the spring 153 to lessen the opening of the throttle 157 to lessen vehicle speed. A decrease in vehicle speed below the desired speed lengthens the control solenoid duty cycle and the open time of the vacuum line 161, pulling in diaphragm 152 to increase the power setting of the vehicle engine so as to hold the vehicle speed near the reference value. Thus, the apparatus 10 maintains the vehicle at least near the desired speed by varying the power setting of the vehicle engine as speed changes tend to occur as a result of, for example, changes in terrain.

REFERENCE SPEED RESET

To change the speed reference speed setting of the apparatus 10, the speed set switch 126 is again closed, energizing the reset unit 29 and resetting the counter 97 to zero. As a result, the potential on the reference speed line 28 is reduced to its minimum level and the differential amplifier 21 sees this as an overspeed condition. The duty cycle of the control solenoid is thus reduced to its minimum level causing the servo 43 to allow the throttle to return to its minimum or idle setting returning throttle control to the operator. Thus, the vehicle operator by manually adjusting the throttle, shifts the vehicle speed upwardly or downwardly to the new desired speed. When this new desired speed is reached, the speed set switch 126 is released by the operator and the gate 25, memory 27 and comparator 31 operate in the manner above described to apply a new reference signal corresponding to the new desired speed to line 28. The differential amplifier 21, pulse width modulator 34, valve driver 38 and servo 43 operate in the manner above described to maintain the vehicle at the new desired speed.

RETURN TO MANUAL CONTROL

Should the vehicle operator desire to resume manual control of the engine power setting, the circuit from the battery 13 to the venting solenoid 53 may be opened. It is contemplated that this may be carried out by opening of a suitable switch, not shown, placed in circuit with the battery 13 and venting coil 53. However, in the particular embodiment shown this circuit may be broken merely by actuation of the vehicle brake which, through the connection 140, opens the brake switch 141 momentarily. This de-energizes the vent solenoid and thereby opens the contact K1 for maintaining the vent solenoid de-energized thereafter. The vent valve 166 then opens restoring the servo chamber 154 to atmospheric pressure whereby the spring 153 pushes diaphragm 152 to its outwardmost position allowing the throttle 157 to return to idle and allowing the vehicle operator to manually control the throttle.

Similarly, in an emergency requiring rapid stopping of the vehicle, the normal reaction of the vehicle operator in applying the vehicle brakes, opens the brake switch 141 de-energizing the venting solenoid and servo and allowing the throttle to return to its idle. It will be apparent that by appropriate arrangement of the vent valve 166, the de-energization of the servo can be made extremely rapid. The diode D5 shunting the vent-

ing solenoid allows essentially instantaneous de-energization of the venting solenoid. Hence the apparatus 10 in no way impedes the rapid deceleration of the vehicle in an emergency.

RESUME SPEED CONTROL

To resume automatic control of the vehicle speed by the apparatus 10 following de-energization of the venting solenoid, the vehicle operator momentarily closes the resume switch 134. Said switch completes the circuit through the venting solenoid 53 and battery 13 energizing the venting solenoid and locking same in energized condition by closure of the contacts K1. Since de-energization of the venting solenoid 53 has no effect upon the data stored in the memory 97 and hence no effect upon the reference speed signal appearing upon line 28, such reenergization of the venting solenoid allows the apparatus 10 to return the vehicle to the speed previously selected.

The above discussion assumes that the resume switch is actuated when the vehicle speed is above the minimum required for actuation of the low speed inhibit unit 56. If on the other hand, the vehicle is at a speed below that minimum, the operator of the vehicle by manual actuation of the throttle returns the vehicle speed to a level above the minimum before actuating the resume switch, since actuation of the resume switch below the inhibit threshold speed cannot actuate the venting solenoid because the transistor Q11 is not enabled for conduction.

Opening the ignition switch 12 de-energizes the apparatus 10 by removing the positive operating potential from the positive source line 63. This removes operating potential from the valve driver 38 and low speed inhibit circuit 56 preventing energization of the control and venting solenoids 41 and 53 and thereby deactuating the servo 43.

The apparatus 10 is fail-safe in operation. For example, failure of the vacuum source 163, rupturing of the chamber 154 of the servo or failure of energization of the control or venting solenoids cause the servo 43 to relinquish control of the throttle, allowing same to return to a closed condition and restoring control of the vehicle power setting to the operator.

MODIFICATIONS

FIG. 6 corresponding to a portion of the block diagram of FIG. 1 discloses a modification. More particularly, in this modified structure the pulse generator 23 of FIG. 1 is eliminated and replaced by a connection 171 from the output of the a.c. source 60 to the input 82 of the gate 25. A pulse-shaping circuit 172 is preferably interposed in the connection 171 for converting the a.c. output of the source 16 to a pulse train suitable in shape for driving the gate 25 and the succeeding memory 27. The pulse shaper 172 of the embodiment shown comprises an NPN transistor Q30 coupled at its base through a resistor R101 to the a.c. source 16, at its emitter to the ground line 61 and at its collector through a resistor R102 to the positive source line 63. Positive pulses at the frequency of the a.c. source 16 are applied by said collector to the gate input 82. The transistor Q30 switches from nonconduction to saturated conduction during the positive half cycle of the source 16, such nonconduction applies a positive

pulse to the gate 25. Although the modified embodiment has been found satisfactory in applications when speed range is not sufficiently great as to cause the pulses from the shaper 172 to exceed the switching rates of the gates and memory and where the output of the a.c. source is free of transients and capable of being shaped to a suitable pulse configuration, the embodiment of FIGS. 1-3 is preferred.

The servo mechanism 43 has been indicated above as being only one specific example of such mechanism which has been found to work effectively within the environment shown. Another such unit, likewise presented solely as a further example of apparatus effective for the purpose, is shown in FIG. 7. In this figure, many of the parts are identical to the parts shown in FIG. 3 and accordingly indicated by the same numerals as utilized in FIG. 3 with the suffix "A" appended thereto. Since these parts are fully and sufficiently described in connection with FIG. 3, no further description thereof is needed. However, in the unit of FIG. 7, the vacuum conduits 161A and 162A are positioned somewhat further apart than are their counterparts 161 and 162 and there is positioned in place of the flapper valve 164 therebetween the core 264 of the solenoid whose winding 41A is indicated at 41 in FIG. 2. Energization of winding 41A affects movement of core 264 in the same manner and for the same purpose as energization of winding 41 affects movement of flapper valve 164 in FIG. 2.

FIG. 8 relates to a modified reference voltage circuit for the operational amplifier A2 of the differential amplifier 21. In the circuit as shown above, there can sometimes be a slight decrease in vehicle speed when the automatic device assumes control due to the moment of time required for vacuum to accumulate in the chamber 154. This decrease is only momentary and is only slight (as 1 or 2 mph) but in some instances it is desirable to eliminate even this amount of irregularity. It is for this purpose that the circuitry of FIG. 8 is provided.

In this particular embodiment, the capacitor C_i is initially charged to the potential on positive source line 63 through the resistors R67 and R68. The collector-emitter circuit of a transistor Q2A is connected between a junction point 191 located between the resistors R67 and R68 and the ground line 61. The base electrode of the transistor Q2A is connected through a dropping resistor R66 to line 51 of the speed set switch 126 illustrated in FIG. 3.

The emitter circuit of a transistor Q2B is connected through a resistor R69 to the positive source line 63 and the collector circuit thereof is connected through the resistor R14 to the ground line 61. The collector of the transistor Q2B is further connected to the junction point 67. The remaining circuitry comprising resistors R12 and R13, operational amplifier A2 and resistors R10 and R16 are connected in the same manner as described above and illustrated in FIG. 2. Accordingly, further detailing of the remainder of the circuitry is unnecessary.

In operation, a closing of the contacts 127 (FIG. 3) of the speed set switch 126 results in the application of the potential from the battery 13 to the base of the transistor Q2A thereby rendering the same conductive. As a result, capacitor C_i discharges through resistor

R68 and the collector-emitter circuit of the transistor Q2A causing the base electrode of the transistor Q2B to become negative with respect to its emitter. Thus, transistor Q2B conducts. As a result, the voltage across resistor R14 increases. Thus, the reference potential to the positive input 12' of the operational amplifier A2 increases to a new value. As a result, the difference in potential between the inputs 10' and 12' of the operational amplifier A2 will be detected. In this particular embodiment, it is desired that the increase in the reference potential on the input 12' be higher than the input signal on the input 10' of the operational amplifier A2 so that the circuitry will attempt to increase the speed of the vehicle to the new reference potential. There will be no effective increase in speed of the vehicle since this modified circuitry only enhances the vacuum accumulation in the servo 43 to prevent a temporary decrease in vehicle speed upon an actuation of the speed set switch 126.

When the speed set switch 126 is released so that the contacts 127 become opened, the voltage across the resistor R14 does not immediately return to its previously low level. The delay is a result of the slowed charging of the capacitor C_i which is controlled by the R67-C_i time constant. As a result, the initial output on the line 36 to the pulse width modulator circuit 34 will be higher for a short period of time and this will cause a higher initial duty cycle and thereby enhance the vacuum accumulation in the servo 43.

A modified low speed inhibit circuit 56A is illustrated in FIG. 9. The low speed inhibit circuit comprises a Schmitt trigger consisting of transistors Q14A and Q14B. The Schmitt trigger prevents an actuation of the transistor Q11 in the absence of a d.c. signal above a minimum value. This was accomplished in the embodiment illustrated in FIG. 3 by the Zener diode Z3.

More specifically, transistor 14A is normally non-conducting and the base of transistor Q14B is biased by the voltage divider consisting of resistors R71, R72 and R73 to maintain the transistor Q14B in a conducting condition and as a result, the voltage applied to the base of the transistor Q11 is small and will prevent an actuation thereof. However, as the potential on line 20 approaches a critical value, transistor Q14A begins to conduct and regeneratively turns off transistor Q14B. Nonconduction of transistor Q14B will result in a potential, determined by the voltage divider consisting of resistors R75, R76 and R77, which is higher so that the transistor Q11 is turned on. As a result, the venting solenoid 53 is energized through the presumed temporary closing of the speed set switch 126 by a closing of the contacts 128. The Schmitt trigger can be set so that the transistor Q14A will become conductive at any desired level by an appropriate setting of the resistor R74 to correspond to any desired minimum vehicle speed, for example 25 miles per hour.

Although particular preferred embodiments of the invention have been described above for purposes of illustration, it will be apparent that modifications and variations of the disclosed embodiments, including the rearrangement of parts, lie within the scope of the present invention.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. In a vehicle speed control, the combination comprising:

means for providing a speed signal proportional to vehicle speed;

a pulse source;

a digital counter for counting said pulses;

a network associated with said counter for producing a reference signal proportional to the count stored in said counter;

a comparator responsive to matching of said reference signal and speed signal for generating a comparator signal;

a manually actuatable switch;

a reset unit responsive to actuation of said switch for resetting said counter and for generating a reset signal;

a gate responsive to said reset signal for conducting pulses from source to said counter and responsive to said comparator signal for isolating said counter from said source;

means responsive to the relationship of said speed signal and reference signal for adjusting vehicle speed to adjust said relationship to a desired condition.

2. The apparatus defined in claim 1 in which said means responsive to the relationship of said speed signal and said reference signal comprises:

a differential amplifier, said differential amplifier having an output variable in response to variation of said speed signal with respect to said reference signal, a pulse width modulator responsive to said differential amplifier for producing a variable duty cycle pulse train, the duty cycle of said pulse width modulator varying in relation to the said output of said differential amplifier; and

servo means adapted to vary the power setting of the vehicle in proportion to the length of said duty cycle.

3. The apparatus defined in claim 2 in which said pulse width modulator comprises a fixed frequency oscillator having a narrow width pulse output and a monostable multivibrator having a first state initiated by said oscillator and a second state; and

means connecting the output of said differential amplifier to said monostable multivibrator for causing same to assume said second state after a period related to said differential amplifier output whereby to determine the length of said duty cycle.

4. The apparatus defined in claim 2 in which said speed signal providing means comprises a source responsive to a vehicle speed and a first operational amplifier responsive thereto;

said differential amplifier comprises a second operational amplifier to which said speed signal and reference signal are applied and having an output variable in response to differences therebetween; and

said comparator circuit comprises a third operational amplifier responsive also to said speed signal and reference signal, said first and second operational amplifiers having feedback means to maintain the gain thereof at a level substantially less than that of said third operational amplifier, whereby said third operational amplifier provides a discrete two-level alternative output instead of the continuously vari-

able output of said first and second operational amplifiers.

5. In a vehicle speed control apparatus, the combination comprising:

- A. pulse means;
- B. memory means for counting said pulses and storing said count;
- C. gate means connected at one input thereof to said pulse means and at an output thereof to said counting means;
- D. means producing a vehicle speed signal;
- E. comparator means producing an inhibit signal in response to a preselected correspondence between said count and said vehicle speed signal;
- F. means applying said inhibit signal to another input of said gate for disabling conduction of said pulses to said counting means;
- G. power regulating means for changing the power setting of said vehicle; and
- H. control means responsive to subsequent changes in the correspondence between said count and said vehicle speed signal for adjusting said power regulating means in a manner to maintain said correspondence.

6. The apparatus of claim 5 including means manually operable for preventing said counting by said memory means.

7. The apparatus defined in claim 5, in which said vehicle speed signal means comprises means for producing an a.c. speed signal proportional to instantaneous vehicle speed; and including

frequency-to-voltage converter means responsive to said a.c. speed signal for producing a d.c. speed signal of amplitude proportional to instantaneous vehicle speed.

8. The apparatus defined in claim 7, in which said frequency-to-voltage converter means comprises:

- transistor switching means energizable by said a.c. speed signal;
- an RC network responsive to actuation of said transistor switching means for producing a d.c. signal proportional in amplitude to the frequency of said a.c. speed signal; and
- an operational amplifier responsive to said d.c. signal for producing said d.c. speed signal.

9. The apparatus defined in claim 5 wherein said gate means comprises:

- a first NAND gate connected at one input thereof to said pulse providing means and at an output thereof to said memory means; and
- enabling gating means interposed between another input of said first NAND gate and said comparator means for applying said inhibiting signal to said another input in response to sensing by said comparator means of said preselected correspondence to disable said first NAND gate from conduction of said pulse train therethrough.

10. The apparatus defined in claim 5 including reset means responsive to manual actuation by the vehicle operator for applying a reset signal to said memory means for resetting same at a minimum count level.

11. The apparatus defined in claim 10 in which said enabling gating means comprises:

- a second NAND gate having an output connected to said another input of said first NAND gate;

a third NAND gate having an input connected to said output of said second NAND gate and an output connected to an input of said second NAND gate, said second NAND gate having a further input connected to said reset means and said third NAND gate having a further input connected to said comparator means.

12. The apparatus defined in claim 5 in which said memory means comprises

means responsive to the count stored for producing a d.c. voltage proportional in amplitude to said count and for applying said d.c. signal to said comparator means.

13. The apparatus defined in claim 12 wherein said memory means comprises a series of flip-flops, an output of each of said flip-flop connecting to an input of the next succeeding one of said flip-flops, the initial one of said flip-flops being connected to said pulse providing means;

said d.c. reference signal producing means including a first voltage divider connected between a fixed potential point and an output point and a plurality of further voltage dividers each connected at one end thereof to a source of potential different from said fixed potential, intermediate the ends thereof to an output of a respective one of said flip-flops and at the remaining ends thereof being connected to points spaced along the intermediate portion of said first-mentioned voltage divider, said spaced points being in a sequence corresponding to the sequence of flip-flops, whereby a rising count in said memory means results in a rising potential on said output point whereby upcounting of said memory means results in a stepwise potential rise on said output point; and

current supply means responsive to the potential on said output point for generating said reference signal in correspondence thereto.

14. The apparatus defined in claim 5 in which said comparator means comprises high gain d.c. amplifier means, having a first input connected to said speed signal providing means and a second input connected to said memory means, for providing a rapid, large potential change at the output thereof in response to unidirectional approach of said reference signal toward the potential of said speed signal;

switching means responsive to said change of output of said amplifier means for switching to a state indicating a matched condition of said speed and reference signals and thereby for deactuating said gate means to stabilize the value of said reference signal.

15. The apparatus defined in claim 14 in which said amplifier means comprises an operational amplifier arranged for high gain, the speed and reference signal inputs thereto being arranged to provide a drop in operational amplifier output as the reference signal steps up to the level of the speed signal; and

said switching means comprises first and second transistors sequentially responsive to said drop for switching the potential applied thereby to said gate means for disabling same.

16. The apparatus defined in claim 5 in which said control means comprises differential means responsive to differentials between said speed and reference signals;

two-state means periodically switched to a first state and means responsive to said differential means for switching to a second state after a time controlled by said differential means;

said power regulating means being responsive to one of said first and second states of said two-state means for controlling vehicle power in accordance with the time length thereof.

17. The apparatus defined in claim 16 in which said two-state means comprises a monostable multivibrator having first and second valve means each having output electrodes and a control electrode, capacitive means connecting the output electrode of one of said valves to the control terminal of the other of said valves, means applying charging potential to one side of said capacitive means and means coupled to said differential means for applying a bias signal responsive to changes in the relationship between said speed and reference signals to the other side of said capacitive means, so that the time required to charge said capacitive means sufficiently to change the state of said second valve is related to the relationship of said speed and reference signals.

18. The apparatus defined in claim 5 including switch means responsive to manual actuation for enabling said power regulating means to change the power setting of said vehicle in response to adjustment of said power regulating means by said control means;

reset means responsive to actuation of said switch means for enabling said gate means to supply pulses to said memory means and for holding said memory means at a minimum count level.

19. The apparatus defined in claim 18 in which said switch means has first contact means actuatable for enabling of said power regulating means and second contact means connected to said reset means and deactuatable for returning control of said gate means to said comparator means and for allowing pulse accumulation by said memory means when said comparator means allows conduction of said gate means thereto.

20. The apparatus defined in claim 5 including means energizable for enabling said power regulating means to change the power setting of said vehicle in response to adjustment by said control means;

a manually actuatable switch;

inhibit means responsive to a speed signal above a preselected level for enabling energization of said enabling means upon actuation of said manually actuatable switch.

21. The apparatus defined in claim 20 in which said inhibit means includes a Zener diode to which a signal proportional to said speed signal is applied, the Zener voltage of which is selected to allow Zener conduction when the vehicle speed exceeds a predetermined minimum limit; and

means responsive to conduction of said Zener diode for enabling energization of said enabling means upon actuation of said manually actuatable switch.

22. The apparatus defined in claim 20 including brake switch means openable in response to actuation of the vehicle brake;

a lock-in contact in series therewith and with said enabling means and responsive to actuation of said enabling means for closing;

a source of potential connected to said enabling means through said brake switch and said lock-in

contact for energizing same, whereby actuation of the vehicle brake will open said brake switch and de-energize said enabling means;

resume switch means paralleling said brake switch means and lock-in contact and manually closable for energizing said enabling means to return control of the vehicle speed to said power regulating means subsequent to actuation of the vehicle brake.

23. A vehicle speed control for maintaining the vehicle at a preselected speed, said control comprising:

A. means to produce pulses;

B. means for counting said pulses and producing a first voltage representative of the number of pulses counted;

C. means for producing a second voltage representative of vehicle speed;

D. means for stopping the passage of said pulses to said counting means when said first and second voltages are substantially equal;

E. difference means for producing a third voltage representative of the difference between said first and second voltages;

F. two state means periodically switched to a first state, and then to a second state after a time controlled by said third voltage; and

G. means responsive to one of said first and second states for controlling the speed of said vehicle.

24. The speed control of claim 23, wherein said stopping means comprises:

A. means for producing a first signal when said second voltage is greater than said first voltage and a second signal when said second voltage is less than said first voltage; and

B. means allowing the passage of said pulses to said counting means when said first signal is produced and preventing said passage when said second signal is produced.

25. Apparatus actuatable for automatically controlling the speed of a vehicle comprising:

A. speed signal means for providing a speed signal related to instantaneous vehicle speed;

B. memory means for accumulating pulses for generating a reference signal corresponding to said pulse accumulation;

C. gate means positioned ahead of said memory means and deactuatable for preventing further pulse accumulation by said memory means;

D. pulse means supplying a train of pulses to said memory means;

E. comparator means responsive to a preselected correspondence between said speed signal and reference signal for deactuating said gate means whereby the output of said memory means stabilizes and becomes a reference standard;

F. differential means responsive to differentials between said speed and reference signals;

G. first and second state means comprising a monostable multivibrator having first and second valve means each having an output electrode and a control electrode, capacitive means connecting the output electrode of one of said valves to the control electrode of the other of said valves, means applying a changing potential to one side of said capacitive means and means coupled to said dif-

ferential means for applying a bias signal responsive to changes in the relationship between said speed and reference signals to the other side of said capacitive means, whereby said first and second state means is switched to one of said two states in response to the time required to charge said capacitive means sufficiently to change the state of said second valve as a function of the relationship between said speed and reference signals; and

H. power regulating means responsive to said first and second states for controlling the power setting of said vehicle.

26. In a vehicle speed control, the combination comprising:

- A. means of providing a speed signal proportional to vehicle speed;
- B. a pulse source;
- C. a digital counter for counting said pulses;
- D. a network associated with said counter for producing a reference signal proportional to the count stored in said counter;
- E. a comparator responsive to matching of said reference signal and speed signal for generating a comparator signal;
- F. a manually actuable switch;
- G. a reset unit responsive to actuation of said switch for resetting said counter and for generating a reset signal;
- H. a gate responsive to said reset signal for conducting pulses from said source to said counter and responsive to said comparator signal for isolating said counter from said source;
- I. means producing a variable amplitude signal in response to a difference between said speed and reference signals;
- J. means producing a variable duty cycle pulse train

having a duty cycle length proportional to the amplitude of said variable amplitude signal; and

K. means adapted to vary the power setting of the vehicle in proportion to the length of said duty cycle pulses.

27. In a vehicle speed control, the combination comprising:

- A. pulse means;
- B. memory means for accumulating pulses and generating a reference signal corresponding to said pulse accumulation;
- C. means for generating a vehicle speed signal;
- D. means comparing said reference signal and said speed signal and producing a signal representing a preselected correspondence between said reference and speed signals;
- E. gate means responsive to said comparing means for discontinuing said pulse accumulation, said gate means comprising
 - 1. a first NAND gate connected at one input thereof to said pulse means and at an output thereof to said memory means, and
 - 2. enabling gating means interposed between another input of said first NAND gate and said comparator means for applying an inhibiting potential to said another input in response to said correspondence signal to disable said first NAND gate from conduction of said pulses to said memory means;
- F. power regulating means for changing the power setting of said vehicle; and
- G. control means responsive to subsequent changes in the correspondence between said speed and reference signals for adjusting said power regulating means in a manner to maintain said correspondence.

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