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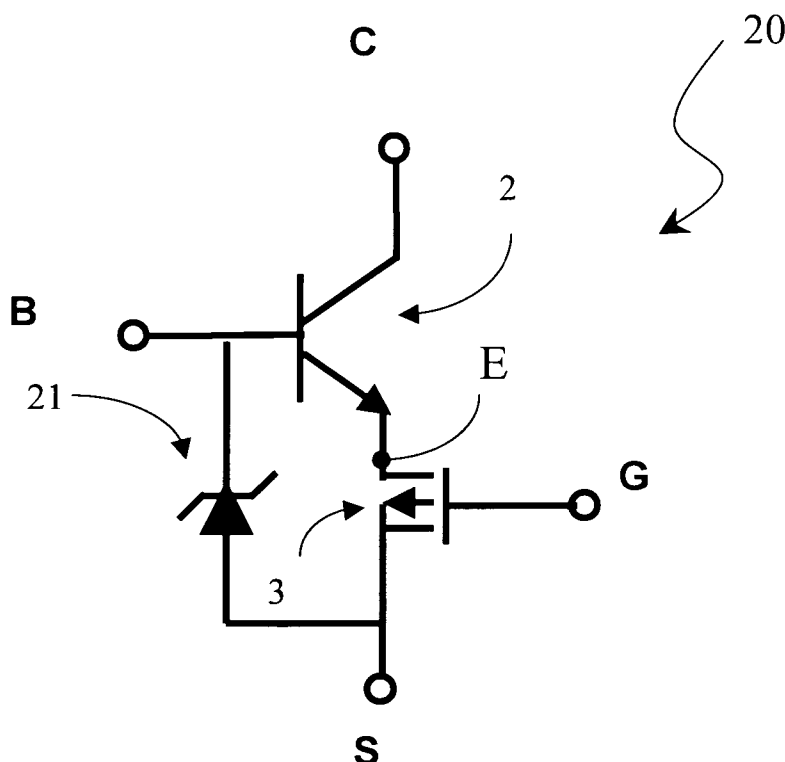
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(54) Title: POWER DEVICE HAVING MONOLITHIC CASCODE STRUCTURE AND INTEGRATED ZENER DIODE



(57) Abstract: A power actuator (20) of the emitter-switched type is described, the power actuator comprising at least one high voltage bipolar transistor (2) and a low voltage DMOS transistor (3) connected in cascode configuration between a collector terminal (C) of the bipolar transistor (2) and a source terminal (S) of the DMOS transistor (3) and having respective control terminals (B, G). Advantageously according to the invention, the power actuator (20) further comprises at least a Zener diode (21), inserted between the source terminal (S) of the DMOS transistor (3) and the control terminal (B) of the bipolar transistor (2).

**POWER DEVICE HAVING MONOLITHIC CASCODE STRUCTURE AND
INTEGRATED ZENER DIODE**

DESCRIPTION

Field of application

The present invention relates to a emitter-switched power actuator.

5 More specifically, the invention relates to a power actuator of the emitter-switched type and comprising at least one high voltage bipolar transistor and a low voltage DMOS transistor connected in cascode configuration between a collector terminal of said bipolar transistor and a source terminal of said DMOS transistor and having respective control
10 terminals.

Prior art

As it is well known, an emitter-switched power actuator is an electronic device able to supply a low voltage drop when conductive as well as a high operative frequency.

15 In particular, as schematically shown in Figure 1A, an emitter-switched power actuator, globally indicated with 1, essentially comprises a high voltage bipolar transistor 2 and a low voltage DMOS transistor 3 connected in "cascode" configuration. In such way, the power actuator 1 has a collector terminal C, a base terminal B, a gate
20 terminal G and a source terminal S. Such a power actuator is indicated with ESBT® and it is represented by the equivalent circuit of Figure 1B.

Thanks to the cascode configuration of the high voltage bipolar transistor 2 and of the low voltage DMOS transistor 3, the power actuator 1 shows a low voltage drop when conductive and a high
25 operative frequency, peculiarity which grows more as the "voltage rating" of the actuator itself increases.

It is possible to monolithically integrate a power actuator 1 of the type described, as schematically shown in Figure 2.

30 In particular, the monolithically integrated power actuator 1 comprises a substrate 5, made of a first layer 5a heavily doped with a first type of dopant, in particular N, overlapped by a second layer 5b slightly doped with the first type of dopant N, commonly indicated as drift layer.

35 Above the substrate 5 a first buried layer 6 of the second type of dopant, in particular P, is realised, corresponding to the base terminal

B of the high voltage bipolar transistor 2 of the power actuator 1.

In the first buried layer 6 a second buried layer 7 of the first type of dopant N is then realised whereon an epitaxial layer 8 is arranged always of the first type of dopant N.

5 A first 7a and a second well 7b of the first type of dopant N with low resistivity are realised in the epitaxial layer 8 suitable to contact the second buried layer 7.

10 Such second buried layer 7 and the regions 7a and 7b contain a portion 9 of the epitaxial layer 8 wherein a first 10a and a second islands 10b of the second type of dopant P are realised wherein active areas of elementary cells of the DMOS type are provided.

In particular, the islands 10a and 10b realise body regions of such elementary cells of the DMOS type, and they are overlapped by contact structures of the source S and gate G terminals.

15 The second buried layer 7 realises instead a buried emitter region E of the high voltage bipolar transistor 2, whose base terminal B is realised by the first buried layer 6, contacted by means of a first 6a and a second well 6b of the second type of dopant P.

20 In essence, the monolithically integrated power actuator 1 has a symmetrical structure.

Finally, the monolithically integrated power actuator 1 comprises a contact layer 11, below the substrate 5, suitable to realise the collector terminal C of the high voltage bipolar transistor 2.

25 The first 7a and the second well 7b of the first type of dopant N not only contain the elementary cells of the DMOS type in the portion 9 of the epitaxial layer 8, but also allow to inhibit a lateral parasitic transistor realised by the conductivity alternation of the wells 6a, 7a and of the islands 10a, respectively of the wells 6, 7b and of the islands 10b.

30 It should be noted that, since the low voltage DMOS transistor 3 is connected in series to the emitter of the high voltage bipolar transistor 2, it is a non negligible series resistance which increases the voltage drop during the conduction phase of the actuator as a whole as schematically shown in Figure 3B, where I_s is the current flowing
35 through said low voltage DMOS transistor 3.

In particular, the low voltage DMOS transistor 3 is in the ON state when the voltage V_{GATE} of the gate terminal G is higher than a threshold voltage value V_{th} , as shown in Figure 3A.

To decrease the resistance of the low voltage DMOS transistor 3 it is possible to increase the perimeter density of the channel. In such case it is however necessary to realise the power actuator 1 with a more sophisticated technology.

It is also possible to use, as DMOS transistor 3, a transistor MOS having an even lower voltage and a less resistive drain region. In such case, however, also a reduction can be obtained of the highest value of the current which can be switched by the power actuator 1.

In fact, during the turn-off of the actuator 1, all the collector current I_c of the high voltage bipolar transistor 2 is deviated on its base terminal B, as shown in Figure 4B.

In particular, the low voltage DMOS transistor 3 is in the OFF state when the voltage V_{GATE} of the gate terminal G is null, as shown in Figure 4A.

As a consequence, a voltage drop is generated on an external resistance R_b connected to the base terminal B which increases in turn the voltage value of the base terminal B of the high voltage bipolar transistor 2 substantially corresponding to the drain-source voltage of the low voltage DMOS transistor 3.

If this voltage value of the base terminal B overcomes a breakdown voltage value of the drain-source junction of the low voltage DMOS transistor 3, a portion of the collector current I_c will flow again through the base-emitter junction of the high voltage bipolar transistor 2. In such case, the power actuator 1 is under inverted secondary breakdown conditions.

The technical problem underlying the present invention is that of providing a power actuator having such structural and functional characteristics as to allow to overcome the limits still affecting the devices realised according to the prior art.

Summary of the invention

The solution idea underlying the present invention is that of inserting, in the power actuator, a Zener diode connected between the

source terminal of the low voltage DMOS transistor and the base terminal of the high voltage bipolar transistor.

Advantageously, the Zener diode is incorporated in a monolithic structure of the monolithically integrated power actuator.

5 On the basis of such solution idea the technical problem is solved by a power actuator as previously indicated and defined by the characterising part of claim 1.

The characteristics and advantages of the power actuator according to the invention will be apparent from the following
10 description of an embodiment thereof given by way of indicative and non limiting example with reference to the annexed drawings.

Brief description of the drawings

In such drawings:

Figures 1A and 1B show an equivalent circuit of a power actuator
15 ESBT® and its symbol;

Figure 2 schematically shows, in section, an elementary cell of the monolithically integrated power actuator of Figure 1;

Figure 3A and 4A schematically show gate voltage values at the power actuator of Figure 1A under different operative conditions;

20 Figures 3B and 4B schematically show the power actuator of Figure 1A under the different operative conditions of Figures 3A and 4A, respectively;

Figure 5 schematically shows a power actuator realised according to the invention; and

25 Figure 6 schematically shows the monolithically integrated power actuator of Figure 5.

Detailed description

With reference to such Figures, and in particular to Figure 5, a power actuator realised according to the present invention is globally
30 and schematically indicated at 20.

By way of illustration, elements being structurally and functionally identical with respect to the power actuator described with reference to the prior art will be given the same reference numbers.

Moreover, the Figures showing schematic views of portions of an
35 integrated structure are not drawn to scale, but they are instead drawn

so as to emphasise the important characteristics of the invention.

The power actuator 20 is of the emitter-switched type and it essentially comprises a high voltage bipolar transistor 2 and a low voltage DMOS transistor 3 connected in "cascode" configuration. In such way, the power actuator 1 has a collector terminal C, a base terminal B, a gate terminal G and a source terminal S.

Advantageously according to the invention, the power actuator 20 also comprises a Zener diode 21, inserted between the source terminal S of the low voltage DMOS transistor 3 and the base terminal B of the high voltage bipolar transistor 2.

Suitably, such Zener diode 21 is chosen so as to have a Zener voltage lower than a breakdown voltage of the low voltage DMOS transistor 3.

In this way, in fact, when the base voltage value of the high voltage bipolar transistor 2, during the turn-off phase, overcomes the value of the Zener voltage, a portion of the collector current I_c of the high voltage bipolar transistor 2 flows through the Zener diode 21 towards the source terminal S of the low voltage DMOS transistor 3, without however flowing through the base-emitter junction of the high voltage bipolar transistor 2.

The power actuator 20 according to the invention thus allows to avoid the inverted secondary breakdown conditions still affecting the actuators realised according to the prior art.

It should be noted that the power actuator 20 according to the invention thus allows to use as DMOS transistor 3, a MOS transistor having an even lower voltage and a less resistive drain region, however without incurring inverted secondary breakdown problems during the turn-off of the DMOS transistor 3 itself, thanks to the presence of the Zener diode 21.

In a preferred embodiment of the power actuator 20 according to the invention, the Zener diode 21 is incorporated in the monolithic structure of the actuator itself, in particular placed as close as possible to the base-emitter junction of the high voltage bipolar transistor 2.

In fact, it has been experimentally verified with simulations in transient that the speed of the Zener diode 21 should be enough as to

ensure its intervention before the low voltage DMOS transistor 3 enters avalanche conditions. Such intervention speed of the Zener diode 21 can be ensured by its monolithic integration with the power actuator 20.

5 As it will be better explained hereafter, advantageously according to the invention, it is possible to monolithically integrate a power actuator 20 as above described, as schematically shown in Figure 6, without adding process phases to a manufacturing process of a power actuator as described in relation with the prior art.

10 In particular, the monolithically integrated power actuator 20 comprises a substrate 5, made of a first layer 5a heavily doped with a first type of dopant, in particular N, overlapped by a second layer 5b slightly doped with the first type of dopant N, commonly indicated as drift layer.

15 A first buried layer 6 of a second type of dopant, in particular P, is realised above the substrate 5 corresponding to the base of the high voltage bipolar transistor 2 of the power actuator 1.

A second buried layer 7 of the first type of dopant N is then realised in the first buried layer 6, whereon an epitaxial layer 8 is
20 arranged, being always of the first type of dopant N.

Inside the epitaxial layer 8 the low voltage DMOS transistor 3 is integrated, as it has been seen in relation with the prior art, equipped with contact structures for the source S and gate G terminals.

The second buried layer 7, contacted by means of at least a first well 7a of the first type of dopant N, realises instead a buried emitter of
25 the high voltage bipolar transistor 2, whose base terminal B is realised by the first buried layer 6, contacted by at least a second well of the second type of dopant P.

The monolithically integrated power actuator 20 also comprises a
30 contact layer 11, below the substrate 5, suitable to realise the collector terminal C of the high voltage bipolar transistor 2.

Advantageously according to the invention, the Zener diode 21 is integrated in an end portion 15 of the integrated structure, the end portion being contiguous to the first well 7a, i.e. contiguous to a second
35 portion 16 wherein the high voltage bipolar transistor 2 and the low

voltage DMOS transistor 3 are integrated.

As shown in Figure 6, the source terminal is connected to ground and the Zener diode 21 is advantageously connected between the base terminal B of the low voltage DMOS transistor 3 and ground.

5 In particular, the Zener diode 21 is realised by using wells of the first N and of the second P type of dopant, corresponding to those realised during the integration process of the bipolar transistor 2 and of the DMOS transistor 3. In other words, the Zener diode 21 comprises wells of the first and second type of dopant simultaneously realised with
10 wells of the first and second type of dopant of the second portion 16.

The end portion 15 thus has a further buried layer 12, realised in the first buried layer 6 and delimited by a first 13a and by a second well 13b of the second type of dopant P. In particular, the second well 13b corresponds to the second contact well of the first buried layer 6 of the
15 monolithically integrated power actuator 20.

Moreover, such end portion 15 comprises a first 12a and a second wells 12b, realised above the further buried layer 12 and in contact therewith, containing a further well 14 of the second type of dopant P.

In such way, the Zener diode 21 is realised as a lateral transistor
20 with open base, indicated with dot lines in Figure 6.

In particular, such transistor with open base has, as emitter region, the wells 13a and 13b of the second type of dopant P, connected to the base region of the high voltage bipolar transistor 2, as base region the wells 12a and 12b of the first type of dopant N, under floating
25 condition and, as collector region, the further well 14 of the second type of dopant P, which is then electrically connected to the source terminal S of the low voltage DMOS transistor 3 by a metal track.

The Zener diode 21 so realised has a Zener voltage equal to the voltage BV_{ceo} of such transistor with open base, which is obviously
30 lower than a breakdown voltage value of the low voltage DMOS transistor 3 of the power actuator 20 since the distances between the wells realising such transistor with open base, i.e. the Zener diode 21, are far more reduced than the distances between the wells realising the low voltage DMOS transistor 3.

35 In such way, it is immediate to verify how the integration of the

Zener diode 21 does not require the introduction of further process phases in a flow suitable to integrate the high voltage bipolar transistor 2 and the low voltage DMOS transistor 3 of the power actuator 20.

It should be also noted that, advantageously according to the invention, since the power actuator 20 comprises a Zener diode 21 monolithically integrated in the end portion 15, it is possible to integrate a DMOS transistor having a lower breakdown voltage with respect to the known solutions and thus having a even lower resistances when conductive.

Moreover, to obtain an adequate speed of the Zener diode 21, the end portion 15 is chosen in correspondence with the source pad of the power actuator 20, and in particular of the corresponding bus.

In other words, the cross section shown in Figure 6 corresponds to one part of the terminal of the so called emitter finger near the source pad bus, while the unchanged portion corresponding to the portion of the emitter/source finger in the rest of the power actuator 20 is not shown.

In summary, the present invention provides for a monolithically integrated structure comprising a power actuator 20 of the emitter-switched type and a Zener diode 21 inserted between the source terminal S of the low voltage DMOS transistor 3 and the base terminal B of the high voltage bipolar transistor 2 of the emitter-switching device.

More particularly, the Zener diode 21 "routes" a portion of the collector current of the high voltage bipolar transistor 2 during its turn-off phase towards the source terminal S of the low voltage DMOS transistor 3, thus avoiding inverted secondary breakdown conditions still affecting the prior art actuators.

Advantageously, the Zener diode 21 have a Zener voltage lower than the breakdown voltage of the low voltage DMOS transistor 3 in order to "drawn" such a portion of the collector current.

CLAIMS

1. Power actuator (20) of the emitter-switched type and comprising at least one high voltage bipolar transistor (2) and a low voltage DMOS transistor (3) connected in cascode configuration between a collector terminal (C) of said bipolar transistor (2) and a source terminal (S) of said DMOS transistor (3) and having respective control terminals (B, G) characterised in that it further comprises at least a Zener diode (21), inserted between said source terminal (S) of said DMOS transistor (3) and said control terminal (B) of said bipolar transistor (2).

2. Power actuator (20) according to claim 1, characterised in that said Zener diode (21) has a Zener voltage lower than a breakdown voltage of said DMOS transistor (3).

3. Power actuator (20) according to claim 1, characterised in that said Zener diode (21) is incorporated in a monolithic structure of said power actuator (20).

4. Power actuator (20) according to claim 3, characterised in that said Zener diode (21) is integrated near a base-emitter junction of said bipolar transistor (2).

5. Power actuator (20) according to claim 4, characterised in that said Zener diode (21) is integrated in an end portion (15) of said monolithic structure of said power actuator (20), said end portion being contiguous to a second portion (16) wherein said bipolar and DMOS transistors (2, 3) are integrated.

6. Power actuator (20) according to claim 5, characterised in that said Zener diode (21) comprises wells of a first type and of a second type of dopant (12a, 12b; 13a, 13b) which wells are simultaneously realised with wells of the first and second types of dopant of said second portion (16).

7. Power actuator (20) according to claim 6, characterised in that said end portion (15) comprises a buried layer (12), realised in a first buried layer (6) of said second portion (16) and delimited by said wells of the second type of dopant (13a, 13b).

8. Power actuator (20) according to claim 7, characterised in that said end portion (15) further comprises said wells of the first type

of dopant (12a, 12b) realised above said buried layer (12) and in contact therewith.

9. Power actuator (20) according to claim 8, characterised in that said wells of the first type of dopant (12a, 12b) contain a further well (14) of said second type of dopant.

10. Power actuator (20) according to claim 5, characterised in that said end portion (15) is in correspondence with a pad of said source terminal (S).

11. Power actuator (20) according to claim 1, characterised in that said DMOS transistor (3) is a low voltage MOS transistor with a little resistive drain region.

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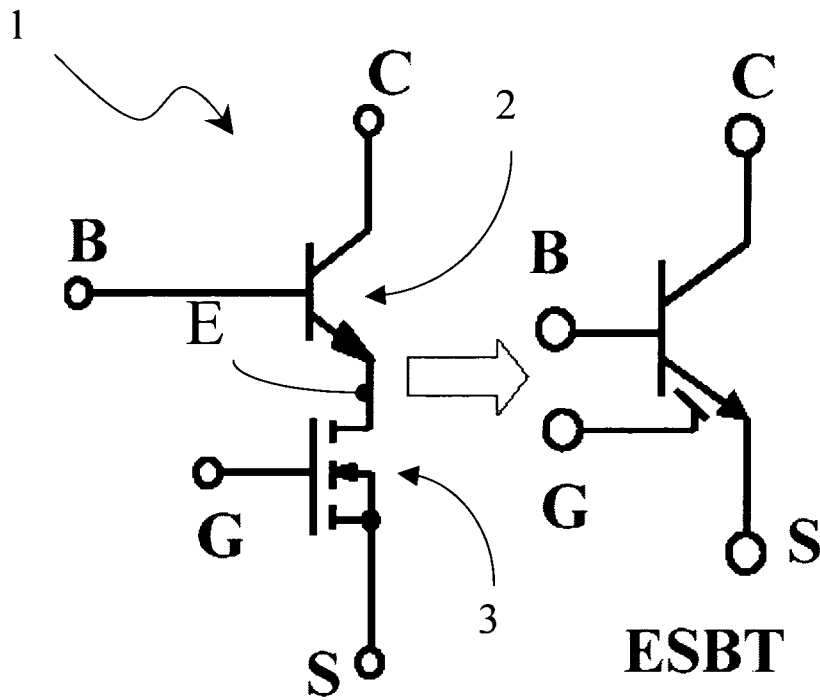


FIG. 1A
PRIOR ART

FIG. 1B
PRIOR ART

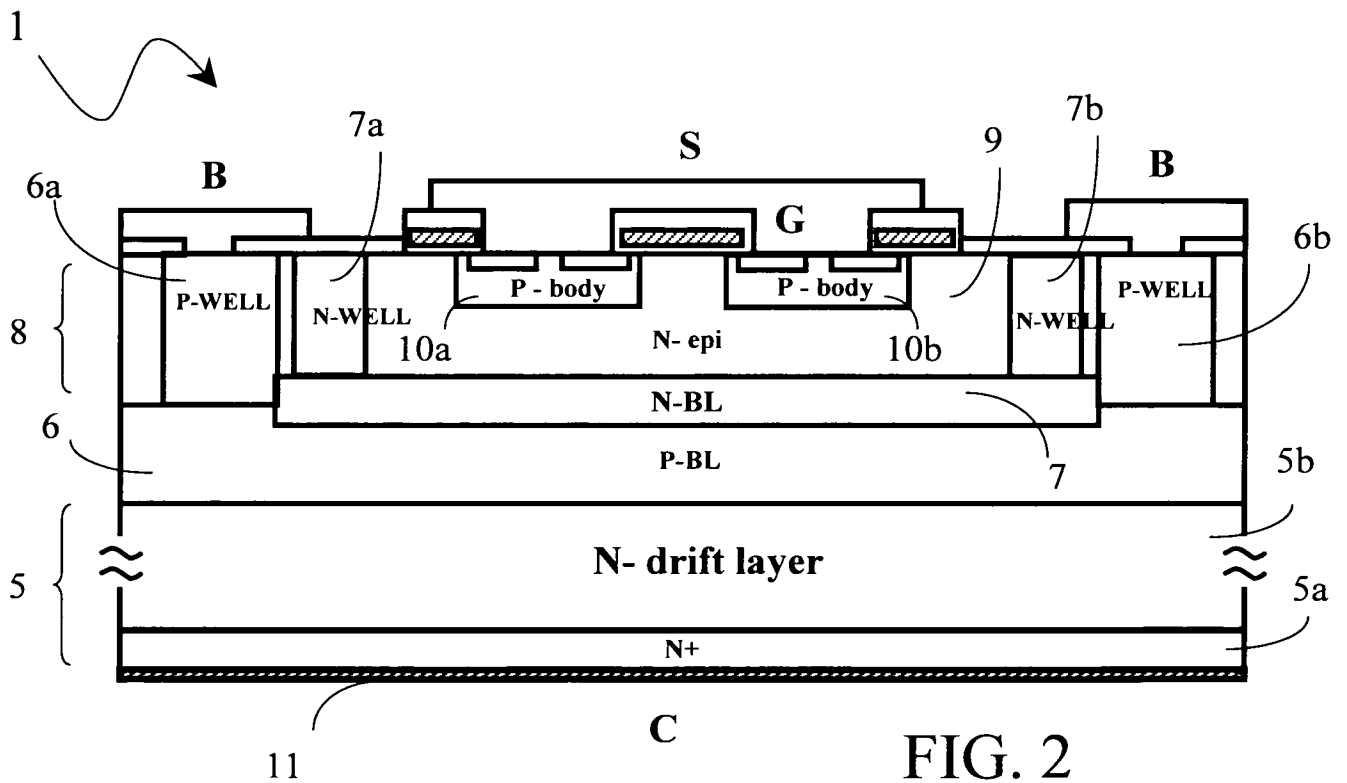


FIG. 2
PRIOR ART

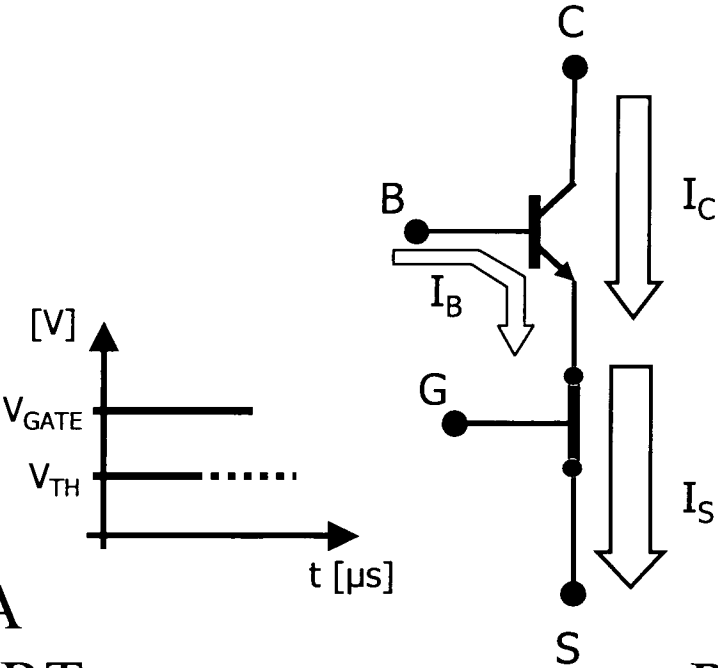


FIG. 3A
PRIOR ART

FIG. 3B
PRIOR ART

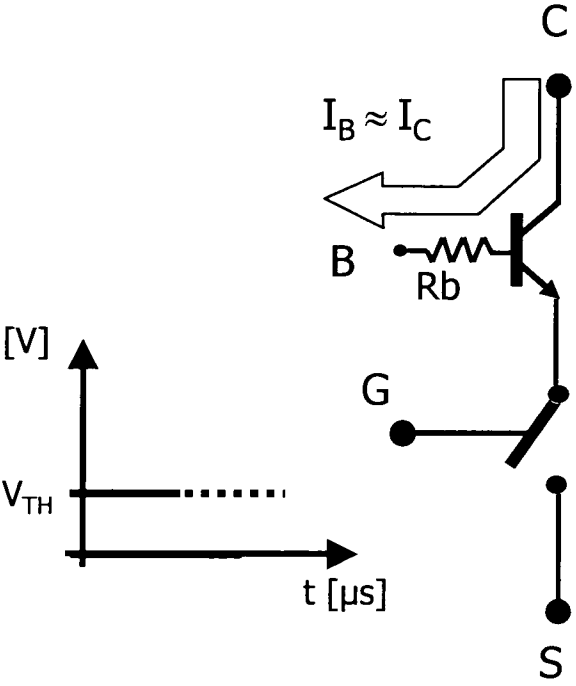


FIG. 4A
PRIOR ART

FIG. 4B
PRIOR ART

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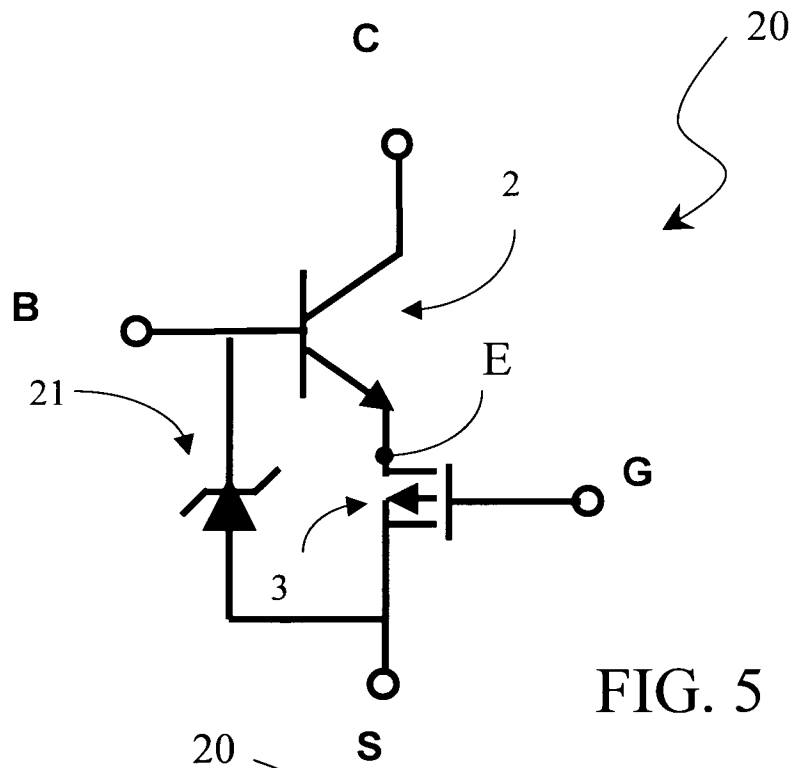


FIG. 5

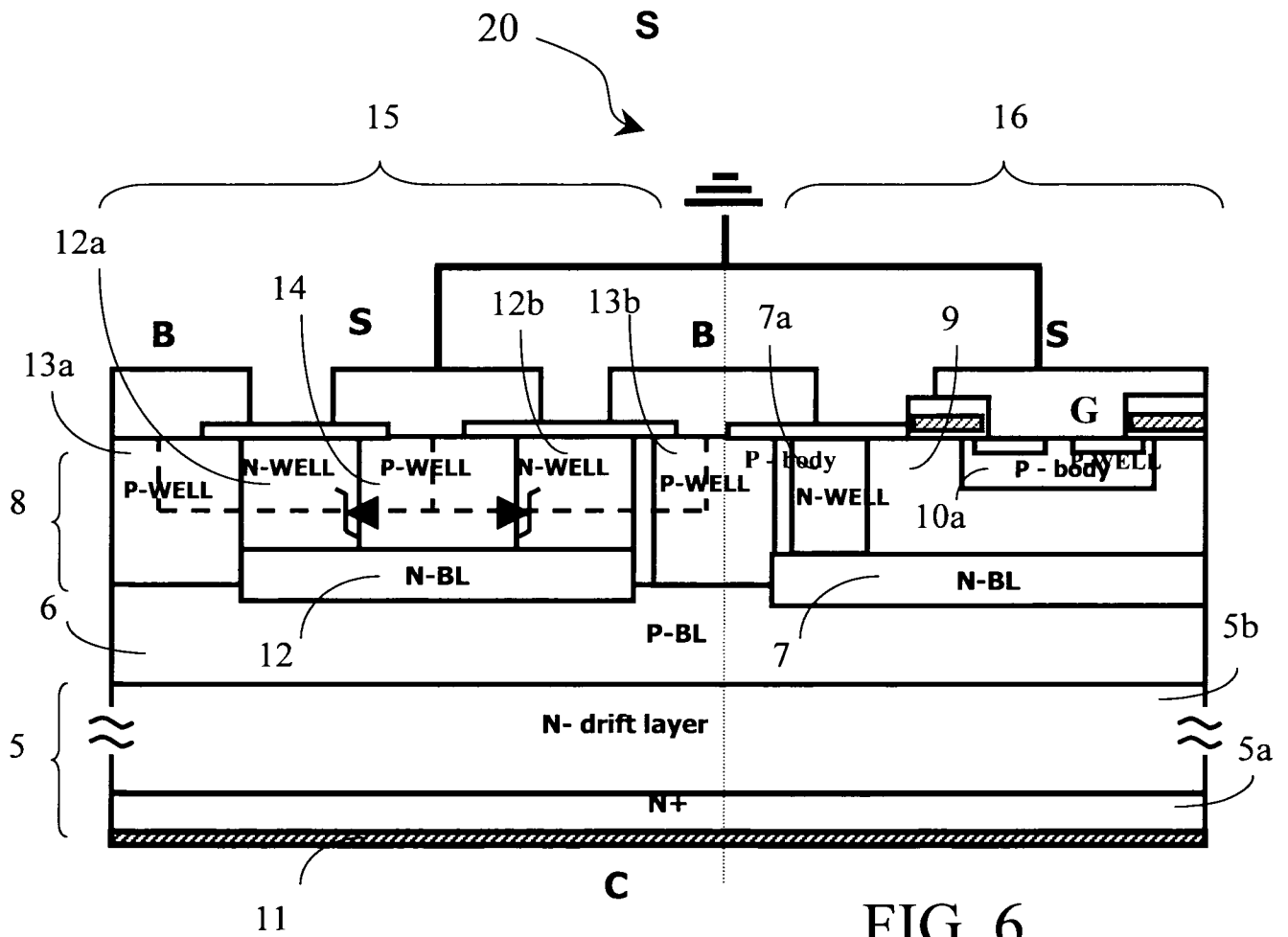


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No
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A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/78
ADD. H01L27/07

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, COMPENDEX, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 966 042 A (STMICROELECTRONICS S.R.L) 22 December 1999 (1999-12-22)	1-8, 10, 11
Y	paragraphs [0024] - [0036], [0069] - [0080] figures 5, 11	9
Y	US 3 739 238 A (HARA H) 12 June 1973 (1973-06-12) column 3, line 42 - column 4, line 25 figures 2, 3	9

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2006/006670

Patent document cited in search report		Publication date		Patent family member(s)	Publication date
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