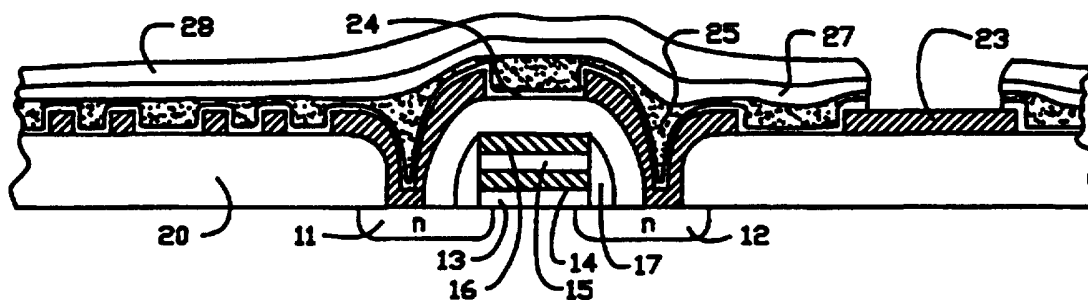




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(54) Title: INTEGRATED CIRCUIT PASSIVATION PROCESS AND STRUCTURE



(57) Abstract

A method for forming a UV transmission passivation coating on an integrated circuit, such as an EPROM, after completion of the active device and metal routing circuitry (11-17 and 20-22) comprising a first barrier dielectric layer (24) over the integrated circuit; smoothing out underlying features by applying a layer of flowable dielectric (25) over the first dielectric layer; and depositing a second dielectric layer over the flowable dielectric, which is composed of a first protective dielectric (27), such as silicon oxynitride, and a phosphorus doped silica layer (28) to provide a stress buffer.

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INTEGRATED CIRCUIT PASSIVATION PROCESS AND STRUCTURE

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present invention relates to integrated circuit passivation structures and processes, and more particularly to a passivation process and structure adapted for UV erase EPROMs.

Description of Related Art

10 An integrated circuit passivation layer coats the device with a protective covering. The protective covering performs a number of functions, including protecting the device from stress which may occur during package molding or otherwise, and protecting the device from contamination and moisture in the environment. Thus, passivation
15 structures should be resistant to thermal and mechanical stress, non-porous to mobile ions which may appear on the surface of the device particularly in moist conditions, and electrical insulating. For some devices, which include UV erase EPROM cells, the passivation layer must also be transmissive to the ultraviolet radiation.

20 The passivation layer, in addition to providing a protective coating for the device, must be opened over contact pads formed on the device. The contact pads are used for connecting wiring in the package to the metal layers on the integrated circuit. Thus, the passivation process must support a technique for making openings in the passivation layer to
25 expose contact pads.

 All of these features have led to significant development in the field of passivation layers for integrated circuits. The following U.S. Patents provide background information for the present invention: U.S. Patent No. 4,581,622 entitled UV ERASABLE EPROM WITH UV

TRANSPARENT SILICON OXYNITRIDE COATING; U.S. Patent No. 5, 260,236 entitled UV TRANSPARENT OXYNITRIDE DEPOSITION IN SINGLE WAFER PECVD SYSTEM; U.S. Patent No. 5,010,024 entitled PASSIVATION FOR INTEGRATED CIRCUIT STRUCTURES; U.S. Patent No. 4,618,541 entitled METHOD OF FORMING SILICON NITRIDE FILM TRANSPARENT TO ULTRAVIOLET RADIATION AND RESULTING ARTICLE; U.S. Patent No. 5,306,946 entitled SEMI-CONDUCTOR DEVICE HAVING A PASSIVATION LAYER WITH SILICON NITRIDE LAYERS; U.S. Patent No. 4,665,426 entitled EPROM WITH ULTRAVIOLET RADIATION TRANSPARENT SILICON NITRIDE PASSIVATION LAYER; and U.S. Patent No. 4,986,878 entitled PROCESS FOR IMPROVED PLANARIZATION OF THE PASSIVE LAYERS FOR SEMI-CONDUCTOR DEVICES.

Notwithstanding substantial development in the art of passivation layers, it is desirable to provide an improved structure. Particularly, it is desirable to provide a passivation structure and process which can completely fill the voids in underlying structures as the design rules for integrated circuits shrink, which provides protection against moisture and mobile ion penetration, which involves a process which does not degrade device reliability, which has high UV light transparency for efficient UV erase of EPROM cells, and which is cost-effective and manufacture worthy.

SUMMARY OF THE INVENTION

The present invention achieves the goals stated above for providing a improved passivation process and coating. It can be characterized as a method for forming a passivation coating on an integrated circuit, after completion of the active device and metal routing circuitry. These precursor processes result in an integrated circuit

having a non-planar features, and at least one conductive pad for providing connection to the packaging. The method comprises the following steps:

- 5 depositing a first dielectric layer over the integrated circuit;
 smoothing out underlying features by applying a layer of flowable dielectric over the first dielectric layer;
 depositing a second dielectric layer over the flowable dielectric;
 establishing a protective pattern layer, such as photoresist, over the second dielectric coating, and defining an opening in the protective
10 pattern layer over the at least one conductive pad;
 using a wet etch process to remove portions of the second dielectric layer exposed by the opening;
 using a dry etch process to remove portions of the remaining layers exposed through the opening, including the remaining portions of
15 the second dielectric layer, the flowable dielectric layer and the first dielectric layer, down to the conductive pad; and
 removing the protective pattern layer.

 According to one aspect of the invention, the first dielectric layer, composed of silicon oxynitride, is deposited using a plasma enhanced
20 chemical vapor deposition to form a dielectric layer resistant to mobile ion penetration, and having high quality.

 The step of smoothing out the underlying features is accomplished by spin coating and curing a flowable glass over the first dielectric layer to smooth out the underlying features. The flowable
25 glass is coated using a process which results in a thickness over the conductive pad of less than 0.1 micron in a preferred process. Further, there is no etch back process used to thin out the cured flowable glass.

 According to another aspect of the present invention, the second dielectric layer is composed of a first protective dielectric such as silicon

oxynitride deposited using plasma enhanced chemical vapor deposition, to protect the flowable dielectric layer from the subsequent wet etch process. The second dielectric layer also includes a top layer deposited using plasma enhanced chemical vapor deposition and comprising
5 phosphorus doped silica glass to provide a stress buffer and ion capture layer to prevent penetration of mobile ions to the first dielectric layer. The phosphorus doped silica layer is deposited using both high frequency and low frequency power for plasma formation during the deposition to increase the quality of the layer.

10 The top layer thus has a characteristic wet etch rate faster than the wet etch rate of the bottom layer. The wet etch process is timed so that it stops when it reaches the protective dielectric layer. This prevents the wet etch materials from penetrating to the flowable dielectric layer in the wet etch process. The dry etch is used to
15 complete the opening of the contact pad.

According to yet another aspect of the invention, the dry etch process includes a first plasma etch to expose the at least one conductive pad, and a second plasma etch to minimize dielectric residues on the at least one conductive pad. The wet etch process
20 according to this aspect of the invention is used to minimize the amount of time that plasma etching needs to be applied to the device during the passivation process. A smaller amount of plasma etch time reduces the possibility that the integrated circuit will suffer defects during the contact pad opening process.

25 The present invention can also be characterized as a passivation layer made according to the methods described above. Thus, the structure will provide a passivation layer which comprises a dielectric barrier layer resistant to penetration by moisture and mobile ions. A planarization layer is placed on the dielectric barrier layer, smoothing out

underlying features. A stress buffer and ion capturing layer is deposited over the planarization layer. The stress buffer and ion capturing layer may also include an underlying protective layer which prevents wet etch processes used for exposing the contact pads from reaching the planarization layer.

According to yet another aspect of the present invention, the passivation structure outlined above is used on an integrated circuit which includes UV erasable EPROM cells. According to this aspect, the passivation structure is transparent to the UV radiation used for erasing the EPROM cells.

Accordingly, the present invention provides a planarization process particularly suited to use with UV erase EPROMs. The planarization process of the present invention achieves substantially voidless gaps between the metal spaces, provides protection against moisture and mobile ion penetration, does not degrade device reliability, has high UV light transparency, and provides a cost-effective, manufacture worthy process.

Other aspects in and advantages of the present invention can be seen upon review of the Figures, the detailed description, and the claims which follow.

BRIEF DESCRIPTION OF THE FIGURES

Fig. 1 is a cross sectional view of an integrated circuit including an EPROM cell with a high quality barrier dielectric formed thereon.

Fig. 2 is a cross sectional diagram of the integrated circuit of Fig. 1, having a spin-on-glass layer over the barrier dielectric.

Fig. 3 is a cross sectional diagram of the integrated circuit of Fig. 1, having a protective, etch stop dielectric coating over the spin-on-glass.

Fig. 4 is a cross sectional diagram of the integrated circuit of Fig. 1, having a phosphorus doped glass over the protective etch stop dielectric.

5 Fig. 5 is a cross sectional diagram of the integrated circuit of Fig. 1, having a patterned photoresist layer over the phosphorus doped glass.

Fig. 6 is a cross sectional diagram of the integrated circuit of Fig. 1, after a wet etch process.

10 Fig. 7 is cross sectional diagram of the integrated circuit of Fig. 1, after a plasma etch process.

Fig. 8 is a cross sectional diagram of the integrated circuit of Fig. 1, having the completed passivation structure formed thereon.

Fig. 9 is a graph showing changes in threshold voltages dV_T of programmed EPROM cell after the wafer level retention bake.

15 Fig. 10 is a graph like that of Fig. 10, except after die level retention bake.

Fig. 11 is a graph showing UV erase capability of the inventive passivation structure, where $V_T(\text{min})$ for uncharged cells has a tight distribution around 3.8 volts.

20 Fig. 12 is a graph showing poor UV erasable passivation structure that has wide spread $V_T(\text{min})$.

DETAILED DESCRIPTION OF THE FIGURES

25 A detailed description of the present invention is described with reference to Figs. 1-12, which provide a step by step illustration of the process, and the structure used for passivation according to the present invention.

In Fig. 1, a cross sectional diagram of the EPROM structure is shown, where the line 10 represents the surface of an integrated circuit

substrate. A UV erase EPROM cell is formed therein having n-type buried diffusion regions 11 and 12 providing the source and drain for the memory cell. A thin insulator 13 is formed over the channel region of the EPROM device. A floating gate 14 is formed over the thin insulator 13. An insulator 15 is formed over the floating gate, and a control gate, or word line, polysilicon layer 16 is formed over the insulator 15. A side wall dielectric spacer 17 is formed on the side of the stack composed of the dielectric 13, the floating gate 14, the dielectric 15 and the control gate line 16. An insulating layer 18 is formed over the stack to isolate the polysilicon 16 from the metal layers following. This insulating layer also extends in the regions 19 and 20 to cover the semiconductor substrate. A metal contact 21 is formed in an opening established through the insulating material 18 down to the buried diffusion region 11. Also, metal lines 22 are patterned on the surface of the device for a variety of reasons. The device may have metal line spacings "X" on the order of six tenths of a micron. Also disposed on the integrated circuit over the dielectric 19 is a metal contact pad 23.

According to the present invention, a high quality dielectric barrier 24 is formed over the underlying metal structures (21, 22, 23). The barrier dielectric 24 is formed of silicon oxynitride SiON in this example, or silicon nitride, using a plasma enhanced CVD process targeted to have the following properties:

thickness: 3000 to 4000 Angstroms,

UV transmittance at 254nm wavelength: >70% at 4000

Angstroms,

stress: $1.0 \text{ E}9 - 1.5 \text{ E}10$ dynes/cm² compressive

total H content: $1.0 - 2.0 \text{ E}22$ per cubic centimeter

SiH content: $0.5 - 2.5 \text{ E}21$ per cubic centimeter

refractive index: 1.75 - 1.92

The result of this process is a high quality barrier which blocks out moisture and mobile ions from reaching the underlying metal or other semiconductor structures.

5 After the growth of the high quality barrier dielectric 24, the opening over the metal contact 21 may be as narrow as 0.1 microns wide and 1.2 microns or more deep.

Fig. 2 illustrates the next step in the process of defining a passivation layer according to the present invention. According to the next step, a flowable dielectric layer 25 is deposited. This dielectric layer is laid down using a spin coat of flowable glass to fill the gaps between the metal lines and to smooth out the wafer surface. The flowable glass is then cured at about 420 C° to solidify the glass. The targeted properties of the spin-on-glass SOG after curing are as follows:

15

thickness (Angstroms): 2000 to 5500

refractive index: 1.3 - 1.4

gap fill: complete fill of 0.1 μm wide and $> 1.2 \mu\text{m}$ deep gaps.

planarity: $>90\%$ at large metal spacings ($> 40 \mu\text{m}$ metal spacing)

20 SOG thickness on top of large metal pad (Angstroms): <1000

stress: $2 \text{ E}8 - 7 \text{ E}8 \text{ dynes/cm}^2$ tensile

25 Thus, the flowable dielectric fills the gaps between the metal lines and the dimples within the contact holes and generally planarizes the underlying topography.

The spin-on-glass layer is not etch backed. Further it is applied using a process which minimizes the thickness of the spin on dielectric in the region generally 26 over the metal contact pad 23.

The spin-on-glass coating process consists of a dispense step, a spread step, and a dry setting step. In the dispense step, a controlled amount of flow glass is dispensed under optimized dispense arm movement and wafer rotation speeds. A moveable cap, making an enclosed compartment around the wafer, is then used to control the ambient above the wafer during the spin-spreading step. During the spreading step, the pressure, temperature, and ambient gas composition can be controlled within the enclosed compartment. Typically, a saturated vapor ambient is kept inside the enclosed compartment to keep the glass under a highly flowable state during spreading. The centrifugal force due to the wafer rotation assists in the global smoothing of the flow glass. A high speed rotation is needed at the end of the spreading step to spin off the excess flow glass and reduce the flow glass thickness on top of large metal pads. At the last dry setting step, the ambient is exhausted to dry and set the flow glass.

The base line recipe for the SOG coating process is as follows:

1. Dispense SOG: Time (sec): 0-2

Spin Speed (rpm): 0-200

Acceleration (rpm/s): 500-2000

Exhaust (lpm): 0-200

Cup: open

2. Close Cap: Time (sec): 0-5

Spin Speed (rpm): 0

Acceleration (rpm/s): 2000-3000

Exhaust (lpm): 0-200

Cup: closing

3. Spread/Flow-in: Time (sec): 0-30
Spin Speed (rpm): 0-500
Acceleration (rpm/s): 1000-3000
Exhaust (lpm): 0-200
Cup: closed
- 5
4. Open Cap: Time (sec): 0-5
Spin Speed (rpm): 0
Acceleration (rpm/s): 2000-3000
Exhaust (lpm): 0-400
Cup: opening
- 10
5. Spinoff: Time (sec): 0-20
Spin Speed (rpm): 3000-5000
Acceleration (rpm/s): 5000-10000
Exhaust (lpm): 0-400
Cup: open
- 15
- 20
- 25
- Thus, the first step involves dispensing the SOG material such as commercially available siloxane polymer based materials, like Allied Signal 512, 214 or 314, or others sold by Hitachi. This step takes less than about 2 seconds with a final spin speed of less than about 200 revolutions per minute. The final spin speed is set rapidly with an acceleration rate of about 500-2000 rpm. Exhaust in the SOG chamber is set at less than about 200 liters per minute (lpm) with the cap open.
- After the dispense step, the cap is closed. This process takes up to 5 seconds. The spin speed is set with a rapid deceleration from

2000-3000 rpm per second to 0 rpm. The exhaust during the cap closing step remains set at up to about 200 lpm.

After the cap is closed, the SOG material is spread and flowed in. This process takes up to about 30 seconds, preferably greater than
5 about 20 seconds, with a relatively low spin speed of up to about 500 rpm, preferably less than about 250 rpm. The spin speed is set with a acceleration rate of about 1000 - 3000 rpm per second with the exhaust in the outside chamber remaining at a value up to about 200 lpm. During this process, the cap is closed, isolating the space inside the
10 closed cap from the external exhaust, so that the evaporation rate of the SOG solvent is slowed down.

In the next step, the cap is opened. This step takes about up to 5 seconds with a 0 rpm spin speed. The spin speed is set with a deceleration in a range of 2000-3000 rpm per second. The exhaust is
15 increased to a value of up about 400 lpm while the cap is being opened.

The final step is the spin off step which takes up to about 20 seconds. During spin off, the wafer rotates at a value between 3000-5000 rpm. The final spin speed is reached with rapid acceleration in the range of 5000-10000 rpm/s. The exhaust in the chamber is up to about
20 400 lpm with the cap open.

The equipment utilized consists of a standard SOG coating chamber modified to include a closeable cap structure which is rotated synchronously with the wafer support, such as a mechanism described in published German patent application 4203913, filed 11 February,
25 1992, invented by Gabriel, *et al.*, except modified for use with silicon wafers.

This process allows much longer spread/flow-in time and a much lower spread/flow-in rotation speed compared to prior art systems to

achieve system planarity, and accomplishes a thin SOG layer over the metal contact pads without an etch back step.

5 Fig. 3 illustrates the next step in the process. According to the next step, a plasma enhanced CVD dielectric layer 27 is deposited over the spin-on-glass 25. The resulting film is targeted to have the following properties:

10 wet etch rate in 10:1 BOE (Angstroms/min): ≤ 800
thickness: 2000 to 3000 Angstroms,
UV transmittance at 254nm wavelength: $> 70\%$ at 4000
Angstroms
stress: $2.0 \text{ E}9$ to $1.5 \text{ E}10$ dynes/cm²
total H content: $1.0 - 2.0 \text{ E}22$ /cm³
SiH content: $0.5 - 2.5 \text{ E}21$ /cm³
15 refractive index: 1.75 - 1.92

20 The 10:1 BOE listed above refers to wet, isotropic etch chemistry consisting of a 10 to 1 ratio of NH₄F to HF solutions. The HF solution has a concentration 5% HF in distilled water solution and the NH₄F has a concentration of 36% NH₄F in distilled water.

25 Thus layer 27 provides a protective covering, silicon oxynitride in this example, or silicon nitride, for the spin-on-glass 25. It acts as a wet etch stop layer because its composition has a relatively low wet etch rate. Thus, the wet etch steps used to make openings over the contact 23 do not reach the spin-on-glass layer 25.

Fig. 4 illustrates a next step in the process of the present invention. In particular, a phosphorus doped silica glass (PSG) layer 28 is deposited over the protective layer 27. The phosphorus doped silica

glass 28 is deposited using a dual frequency plasma enhanced chemical vapor deposition. The film properties are targeted as follows:

thickness (Angstroms): 10000 to 16000

5 UV transmittance: > 65% at 10000 Angstroms thickness,

stress (dynes/cm²): 2 E8 to 1 E9 compressive

total phosphorus content (weight %): 2 - 4

refractive index: 1.45 - 1.55

wet etch rate in 10:1 BOE (Angstroms/min): 1500 - 3000

10

The phosphorus containing glass top layer 28 provides a stress buffer and captures mobile ions, so that the mobile ions do not reach the underlying layers of the device.

15 The phosphorus glass layer process uses both high frequency (13.56 MHz) and low frequency (350 KHz) power for high quality film deposition.

20 The high and low frequency plasma are used at the same time in the deposition step. The high frequency plasma produces less charge bombardment to the wafer surface during film growth. The low frequency plasma introduces more energetic reactant on wafer surface for higher surface mobility. The high mobility of reactants on wafer surface improves the film density and its conformity to underlying topography. The desired PSG film properties, such as density, stress, wet etching rate, et cetera, can be engineered by adjusting the balance
25 between the high and low RF frequency powers.

After depositing the passivation structure, openings must be made to metal contact pads 23 on the integrated circuit. Thus, Fig. 5 illustrates the first step in establishing the openings to the contact pads 23. In particular, a photoresist layer 30 or other protective patterning

layer is deposited over the top layer 28 of the passivation structure. One creates the photoresist layer 30 by applying the photoresist, exposing the pattern desired, and developing resist to define the bond pad openings. As can be seen, there is an opening in the region, generally 26, over the metal contact pad 23.

Next, as shown in Fig. 6, the circuit is exposed to an isotropic wet etch process using a 10:1 BOE to etch the topmost phosphorus doped silica glass layer 28 and part of the wet etch stop layer 27. The wet etch stop layer 27 has a low enough wet etch rate so that it behaves as an etch stop during this process. This prevents wet etching of the underlying flowed glass layer 25. Thus, a structure having tapered walls, e.g. 35, 36, and slightly undercutting the photoresist 30 is formed over the contact pads 23.

The isotropic etch process is timed with enough control that the wet etch process does not cut through the wet etch stop layer 27 or otherwise reach the spin-on-glass layer.

As illustrated in Fig. 7, the next step involves an etch of the remaining passivation layers, which is anisotropic, including the remaining portions of the wet etch stop layer 27, the flowed glass 25, and the high quality barrier dielectric 24. The anisotropic etch process results in the vertical walls, e.g. wall 37, in the opening over the contact pad 23. The etch chemistry consists of CHF_3 , SF_6 and He. The dry etch is done in a plasma environment first with a main etch step. After the majority of the bonding pads on the wafer are opened by the main etch, an overetch process is added to ensure that all pads are open and that no oxide residue remains on the pads. Both the main etch and the overetch steps may induce charging damage to the device due to the high power plasma used. It is found that a device may fail if the dry etch time is over a maximum allowable dry etch time. Thus, the present

invention provides use of a wet etch step as described above with reference to Fig. 6, to substantially reduce the amount of time needed for the dry etch step. Thus, the wet etch stop layer may be used to avoid a wet etch attack of a flowed glass layer 25.

5 The final step in the process is the stripping of the photoresist mask 30, which according to the recipe described above is done using an O₂ plasma gas process.

The following process parameters and settings are typical for the passivation process described above:

10

15

20

Parameter	Layers 24, 27 (SiON)	Layer 28 (PSG)
pressure (torr)	1 - 6	1 - 4
13.56 MHz (Watt)	200 - 650	30 - 800
350 Hz RF (Watt)		30 - 500
temperature (C)	350 - 430	350 - 430
susceptor spacing (mil)	200 - 650	200 - 500
SiH ₄ flow rate (sccm)	50 - 120	20 - 180
N ₂ O flow rate (sccm)	0 - 300	500 - 2000
NH ₃ flow rate (sccm)	60 - 120	
N ₂ flow rate (sccm)	1000 - 5000	
PH ₃ (sccm)		20 - 180

25

The resulting structure is shown in Fig. 8. Thus, an integrated circuit which includes an EPROM cell having the floating gate 14, the source 11 and the drain 12 as shown includes a passivation structure according to the present invention. A first high quality dielectric layer composed of silicon oxynitride is formed over the metal structures 21,

22. A flowed dielectric 25 is deposited over the high quality dielectric 24 to smooth out the underlying features. A wet etch stop layer 27 composed of silicon oxynitride, which protects the underlying flowed glass 25 from subsequent wet etch processes is then applied. Finally, the phosphorus doped glass (PSG) 28 overlies the wet etch stop layer 27. The openings over the metal contact 23 are reliably formed. The gaps in the underlying metal structures are filled without voids. Excellent protection against moisture and mobile ion penetration is provided. Device reliability does not degrade due to the passivation processes, such as charge retention loss or gain failures, temperature cycling failures, pressure cooking failures, et cetera. Furthermore, all of the layers deposited according to the present invention have a high UV light transparency for efficient UV erase of programmed EPROM cells.

Furthermore, a cost effective, manufacture worthy process has been created for use in very small geometry integrated circuit design.

Accordingly, the present invention provides a passivation process by which after completion of the active device in metal routing circuitry, the following steps are performed:

- 1) deposit a high quality plasma enhanced CVD dielectric barrier;
- 2) coat with a spin-on-glass layer;
- 3) deposit a plasma enhanced CVD dielectric with a low etching rate;
- 4) deposit a plasma enhanced CVD phosphorus containing glass top layer;
- 5) apply photoresist and expose the photoresist to define the bond pad pattern;
- 6) perform the wet etch portion of the pad etch process;

- 7) perform the dry etch portion of the pad etch process; and
- 8) remove the photoresist.

An EPROM cell consists of a floating gate 14 of Fig. 8, and a control gate 16 of Fig. 8. The electrical passage between the source and drain active regions 11, 12 of Fig. 8 is determined by the status of the floating and control gates. When charge is intentionally added onto a floating gate, the charge will increase the threshold voltage V_T required on the control gate to open the electrical passage between the source and drain. For one binary state, the amount of charge added on the floating gate 14 is adjusted that the V_T is about 12 volts. As long as the charge remains on the floating gate, the V_T will remain at around 12 volts. The uncharged cells, representing the other binary state, will have a lower threshold voltage V_T of about 4 volts. During a "read" cycle, the control gate voltage will be set at 8 volts, so that the charged cells will not conduct current (passage shut) and the uncharged cells will (passage open). The proper function of the EPROMs depends on the capability of floating gates to keep the correct amount of charge on them.

During the operation of EPROMs, moisture and mobile ions can penetrate a poor quality passivation and induce charge loss (or gain) on the floating gate 14 of Fig. 8. The charge loss/gain will result in a change of control gate V_T and the degradation of the EPROM cells. The barrier quality of a passivation is usually tested before shipment through a procedure called retention bake, where the EPROMs under test will go through an extended baking, usually at 250 C° temperature, and the change in threshold voltage dV_T is monitored at specific time intervals. The change in V_T is a direct indication of device degradation. This retention bake can be done either at the wafer level or after the

packaging at the die level. Typically the sample size will be a few hundred dies, each with millions of memory cells. The wafer level and die level retention bake test results are summarized in Fig. 9 and Fig. 10 for the passivation structure of the present invention. The dV_T data shown here is well within commercially acceptable specifications (<1.5 V).

One main function of passivation on integrated circuit (IC) is to protect the IC from damage due to severe temperature, humidity, and abrasive mechanical stress through packaging and IC usage life. The reliability of an IC is usually tested through various accelerated tests, known as quality assurance. Extensive reliability tests on the proposed passivation structure have been conducted. The tests include temperature cycle, pressure cook test (PCT), thermal shock, electrical static discharge, low temperature storage, and temperature humidity tests. The proposed passivation structures have passed all these reliability tests. It is found that the proposed passivation affects the PCT test the most. During PCT test, the devices are subjected to 121°C , 100% humidity, and 2 atmosphere pressure ambient for 168 hours. The functionality of the samples is measured before and after the pressure cook for % yield comparison. It is found that with the proposed passivation, the yield lost is about 2%. The prior art passivation failed catastrophically ($>90\%$ lost) in this test. This is a significant advantage of the proposed passivation structure.

The UV light transparency of the passivation structure should be high enough for easy erasure of programmed cells. The EPROM cell erasability test consists of the following steps:

- 1) shine 254 nm UV light to make sure that all EPROM cells have no residue charge on the floating gates before start testing. (The

UV light provides enough excitation to the charge on the floating gate that charge can escape from the floating gate).

2) measure the minimal threshold voltage $V_T(\text{min})$ that is required to turn on all non-programmed cells in each die, and tabulate the number of dies that fall into each bin of $V_T(\text{min})$ (see Fig. 11).

3) program all the cells by adding charge on the floating gates.

4) shine 254 nm UV light onto device through passivation.

5) remeasure the $V_T(\text{min})$ for each die and compare the $V_T(\text{min})$ bin distribution with that obtained in step 2. If the charges on the floating gates were not completely erased at step 4 due to poor UV transmittance of the passivation layers, a tailing towards higher $V_T(\text{min})$ distribution will occur.

Figs. 11 and 12 compare the $V_T(\text{min})$ bin distributions of the passivation based on the present invention, and a poor UV erasable passivation. Fig. 11 is clean at >4.0 volts, but the prior art process had a wide tail at the large $V_T(\text{min})$ end (Fig. 12).

The additional cost of the proposed passivation is mainly due to the addition of flowed glass coating. Since no etch back step is used, the additional cost per wafer is relatively low and is well justified by the excellent reliability provided. The manufacturability is optimized by limiting the pad dry etch time with the addition of a wet etch step and by adding a wet etch stop layer on top of the flow glass.

The foregoing description of a preferred embodiment of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to

the precise forms disclosed. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. It is intended that the scope of the invention be defined by the following claims and their equivalents.

5

What is claimed is:

CLAIMS

1. A method for forming a passivation coating on an integrated circuit, the integrated circuit having non-planar features and at least one conductive pad, comprising:

5 depositing a first dielectric layer over the integrated circuit;
smoothing out the non-planar features by applying a flowable dielectric layer over the first dielectric layer;

10 depositing a second dielectric layer over the flowable dielectric layer;

establishing a protective pattern layer over the second dielectric coating, and defining an opening in the protective pattern layer over the at least one conductive pad;

15 using a process which is isotropic to remove portions of the second dielectric layer exposed by the opening;

using a process which is anisotropic to remove portions of remaining layers exposed through the opening, including the remaining portions of the second dielectric layer, the flowable dielectric layer and the first dielectric layer, down to the conductive pad; and

20 removing the protective pattern layer.

2. The method of claim 1, wherein the step of depositing a first dielectric layer includes using plasma enhanced chemical vapor deposition to form a dielectric layer resistant to mobile ion penetration.

25

3. The method of claim 1, wherein the step of applying a flowable dielectric layer includes spin coating and curing a flowable glass over the first dielectric layer to smooth out underlying features.

4. The method of claim 3, wherein the step of applying a flowable dielectric layer does not include an etch back to thin out the cured flowable glass.

5 5. The method of claim 3, wherein the cured flowable glass has a thickness over the conductive pad of less than 0.1 micron.

10 6. The method of claim 1, wherein the step of depositing a second dielectric layer includes using a plasma enhanced chemical vapor deposition to form a protective dielectric layer to protect the flowable dielectric layer from the subsequent wet etch process.

15 7. The method of claim 6, wherein the plasma enhanced chemical vapor deposition used for the protective dielectric layer includes applying silicon oxynitride.

20 8. The method of claim 1, wherein the step of depositing a second dielectric layer includes using a plasma enhanced chemical vapor deposition to form a phosphorous doped silica layer providing a stress buffer and preventing penetration of mobile ions to the first dielectric layer.

25 9. The method of claim 8, wherein the plasma enhanced chemical vapor deposition used for the phosphorous doped silica layer includes applying both high frequency and low frequency power for plasma formation during the deposition.

10. The method of claim 1, wherein the second dielectric layer includes a top layer having a characteristic etch rate for isotropic etch, and a bottom layer having a characteristic etch rate slower than the top layer for the isotropic etch, and the isotropic etch process is timed to prevent etch materials from penetrating the bottom layer to protect the flowable dielectric layer from the isotropic etch step.

11. The method of claim 1, wherein the first dielectric layer, the flowable dielectric layer and the second dielectric layer comprise materials transmissive to ultraviolet radiation.

12. The method of claim 1, wherein the anisotropic etch step includes plasma etching.

13. The method of claim 1, wherein the anisotropic etch step includes a first plasma etch to expose the at least one conductive pad, and a second plasma etch to minimize dielectric residues on the at least one conductive pad.

14. A method for forming a passivation coating on an integrated circuit, the integrated circuit having non-planar features and at least one conductive pad, comprising:

depositing a first dielectric layer over the integrated circuit using plasma enhanced chemical vapor deposition;

spin coating and curing a flowable glass over the first dielectric layer;

depositing a second dielectric layer comprising silicon oxynitride over the cured flowable glass using plasma enhanced chemical vapor deposition;

depositing a third dielectric layer comprising phosphorous doped silica over the second dielectric layer using plasma enhanced chemical vapor deposition;

5 establishing a protective pattern layer over the third dielectric coating, and defining an opening in the protective pattern layer over the at least one conductive pad;

 using an etch process which is anisotropic to remove portions of the third dielectric layer exposed by the opening down to the second dielectric layer;

10 using an etch process which is isotropic to remove portions of remaining layers exposed through the opening, including the second dielectric layer, the cured flowable glass layer and the first dielectric layer, down to the conductive pad; and

 removing the protective pattern layer.

15

15. The method of claim 14, wherein the plasma enhanced chemical vapor deposition used for the third dielectric layer includes applying both high frequency and low frequency power for plasma formation during the deposition.

20

16. The method of claim 14, wherein the third dielectric layer has a characteristic isotropic etch rate faster than the second dielectric layer, and the isotropic etch process is timed to prevent etch materials from penetrating the second dielectric layer to protect the cured flowable glass layer from the isotropic etch step.

25

17. The method of claim 14, wherein the integrated circuit includes UV erasable EPROM cells, and the first dielectric layer, the cured flowable glass layer, the second dielectric layer and the third dielectric layer comprise materials transmissive to ultraviolet radiation used to erase the EPROM cells.

18. The method of claim 14, wherein the anisotropic etch process includes plasma etching.

19. The method of claim 14, wherein the anisotropic etch process includes a first plasma etch to expose the at least one conductive pad, and a second plasma etch to minimize dielectric residues on the at least one conductive pad.

20. The method of claim 14, wherein the step of spin coating and curing a flowable glass does not include an etch back to thin out the cured flowable glass.

21. The method of claim 20, wherein the cured flowable glass has a thickness over the conductive pad of less than 0.1 micron.

22. An integrated circuit having a passivation structure comprising:

a dielectric barrier layer resistant to penetration by mobile ions and moisture;

a planarization layer on the dielectric barrier layer, smoothing out underlying features; and

a stress buffer and ion capturing layer over the planarization layer.

23. The integrated circuit of claim 22, further including a protective layer between the planarization layer and the stress buffer and ion capturing layer, which protects the planarization layer from etch processes used on the stress buffer and ion capturing layer.

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24. The integrated circuit of claim 23, wherein the dielectric barrier layer comprises silicon oxynitride, the planarization layer comprises glass, the protective layer comprises silicon oxynitride, and the stress buffer and ion capturing layer comprises phosphorous doped silica.

10

25. An integrated circuit including UV erasable EPROM cells, and having a passivation structure comprising:

a dielectric barrier layer resistant to penetration by mobile ions and moisture and transmissive to ultraviolet radiation used to erase the EPROM cells;

15

a planarization layer on the dielectric barrier layer, smoothing out underlying features and transmissive to ultraviolet radiation used to erase the EPROM cells; and

20

a stress buffer and ion capturing layer over the planarization layer and transmissive to ultraviolet radiation used to erase the EPROM cells.

26. The integrated circuit of claim 25, further including a protective layer between the planarization layer and the stress buffer and ion capturing layer and transmissive to ultraviolet radiation used to erase the EPROM cells, which protects the planarization layer from etch processes used on the stress buffer and ion capturing layer.

25

27. The integrated circuit of claim 26, wherein the dielectric barrier layer comprises silicon oxynitride, the planarization layer comprises glass the protective layer comprises silicon oxynitride, and the stress buffer and ion capturing layer comprises phosphorous doped silica.

5

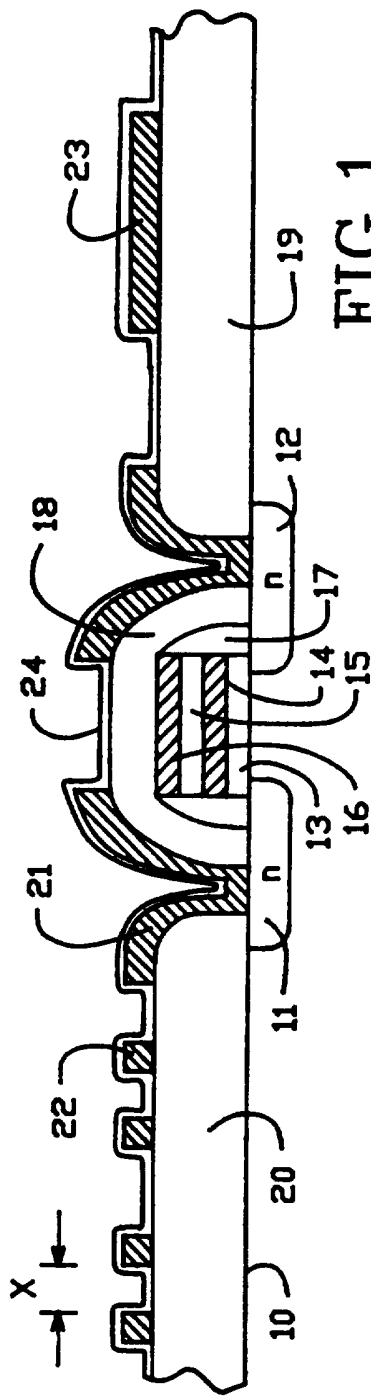


FIG. 1

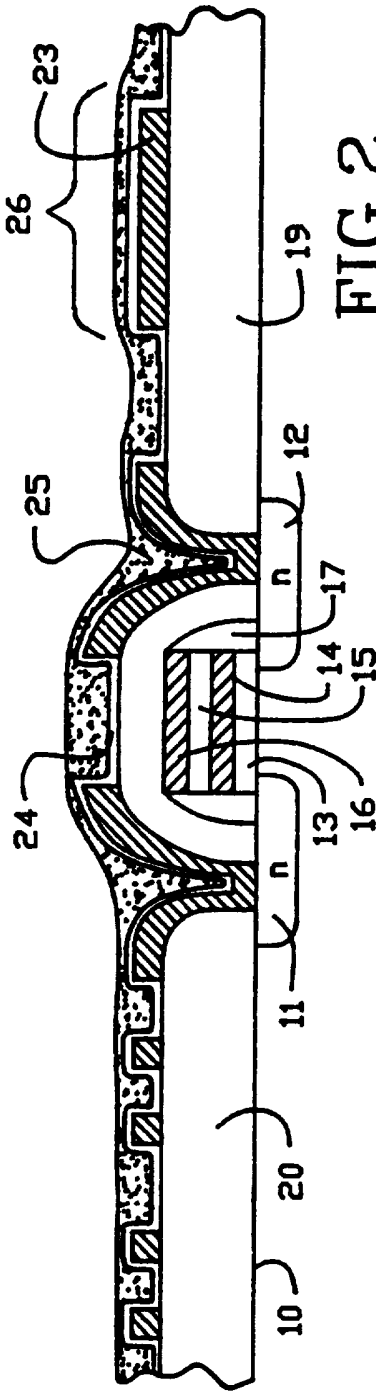


FIG. 2

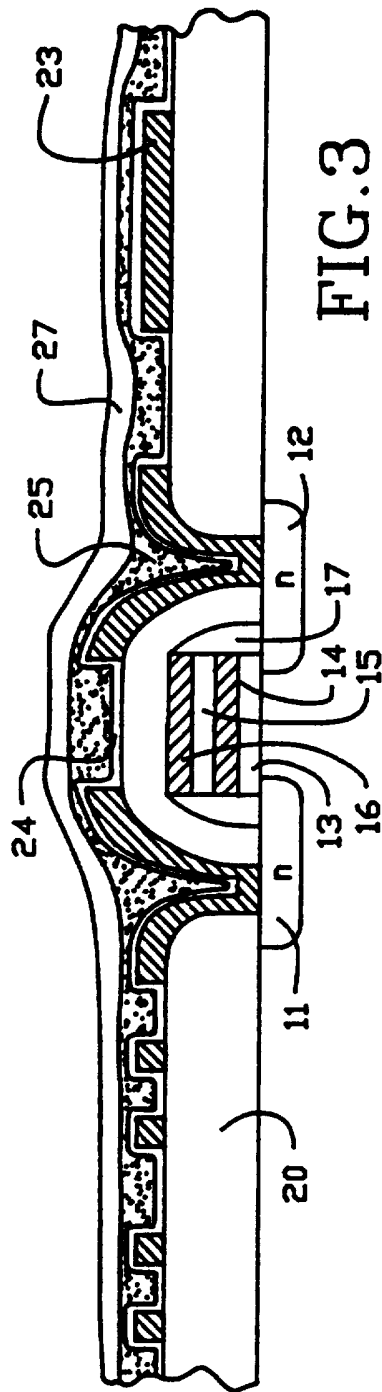
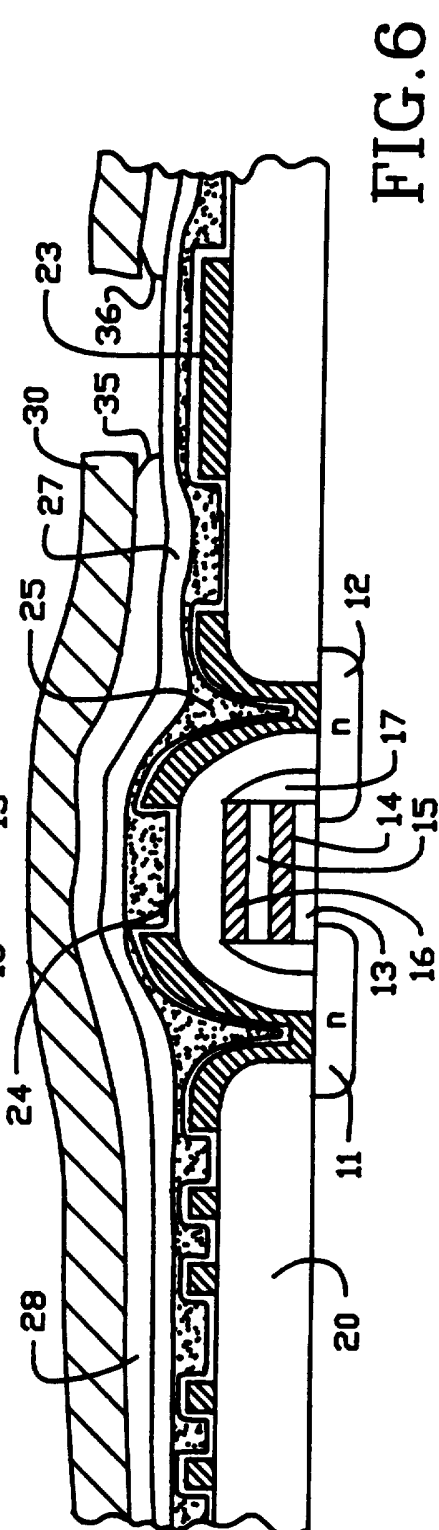
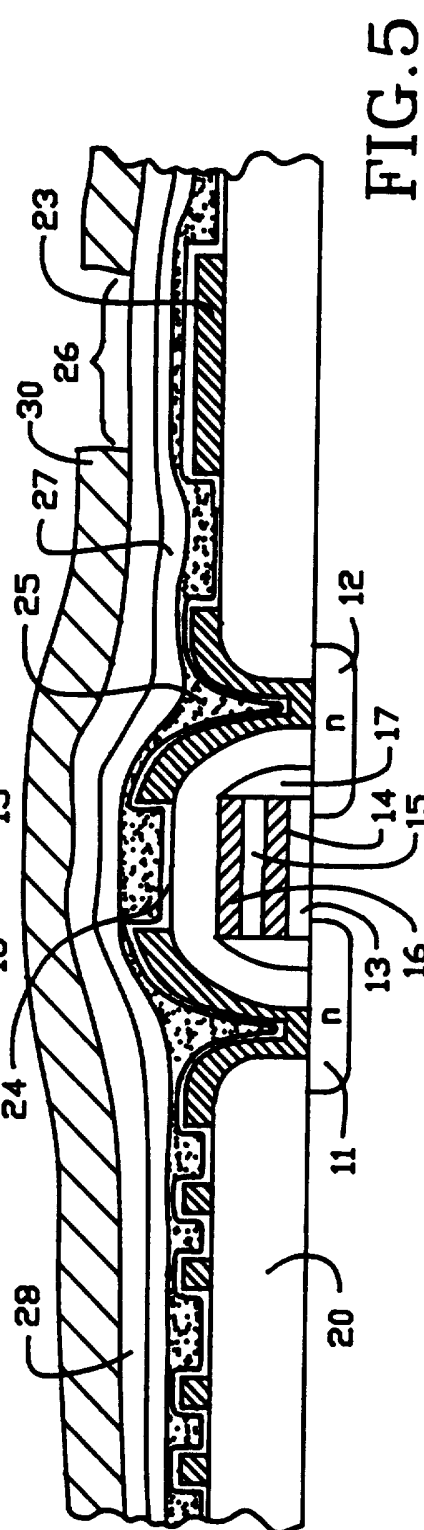
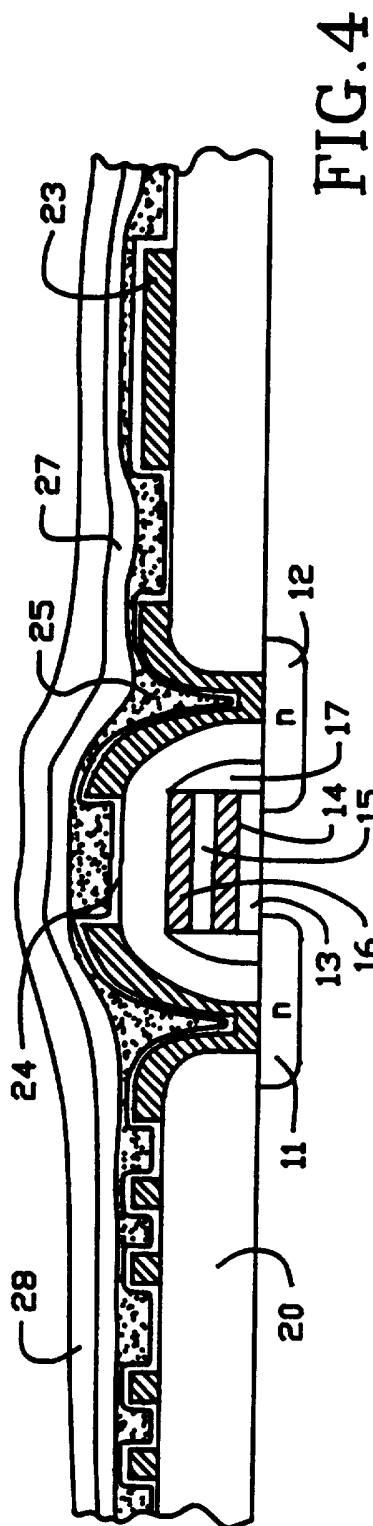


FIG. 3



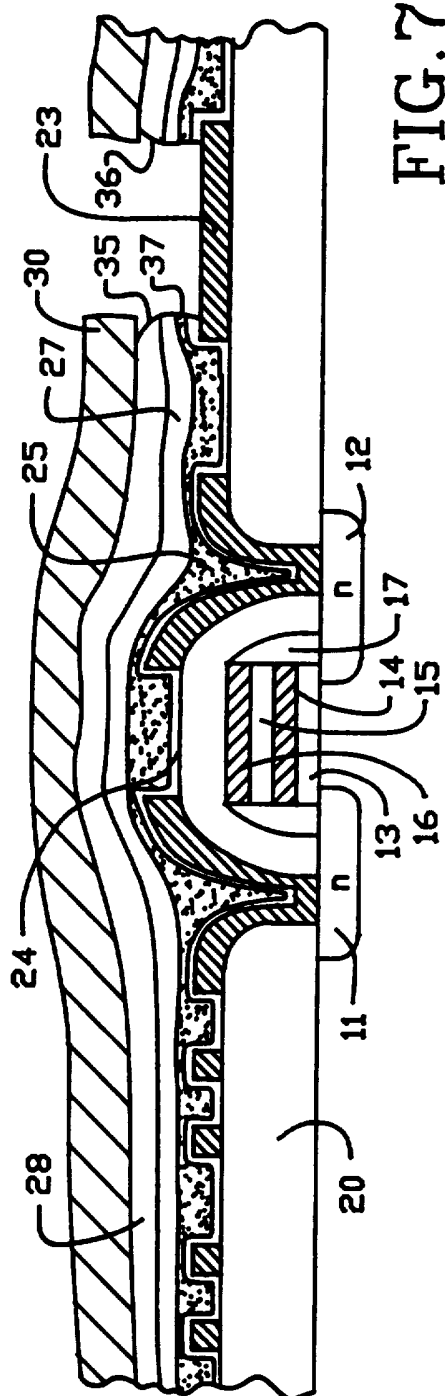


FIG. 7

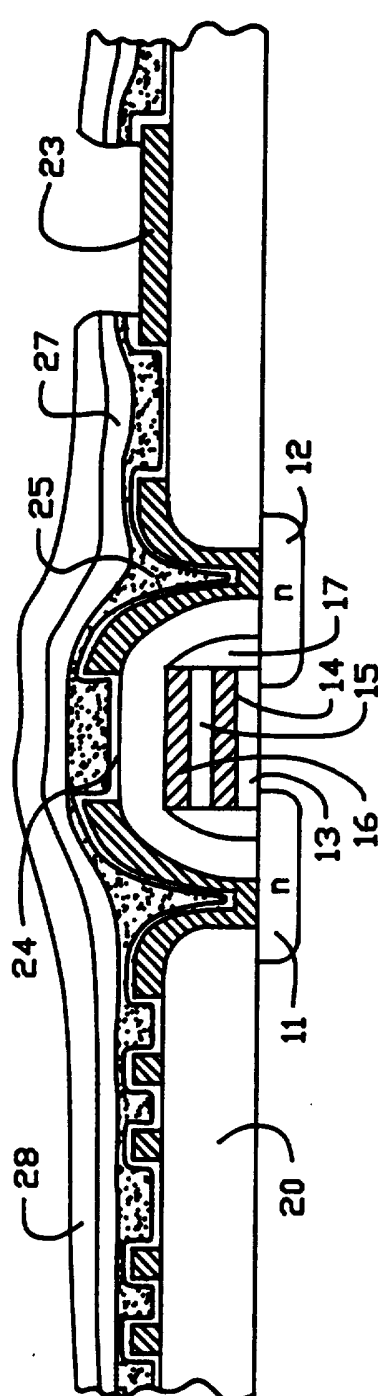


FIG. 8

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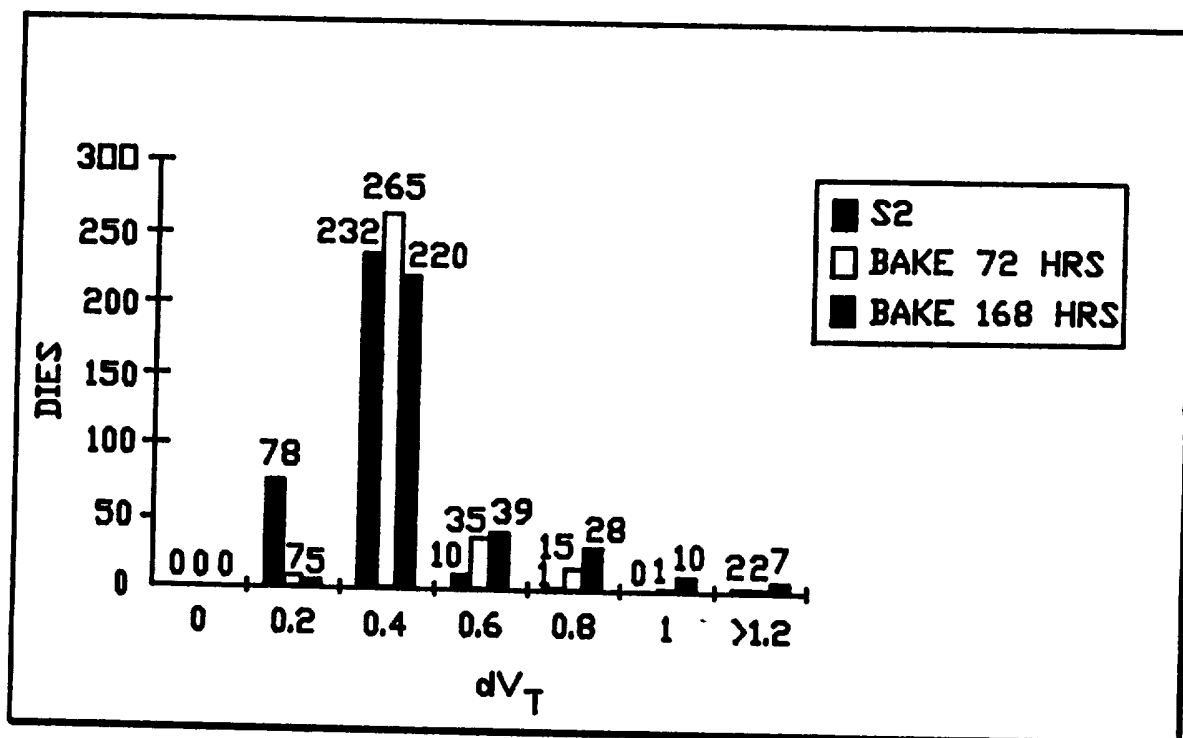


FIG.9

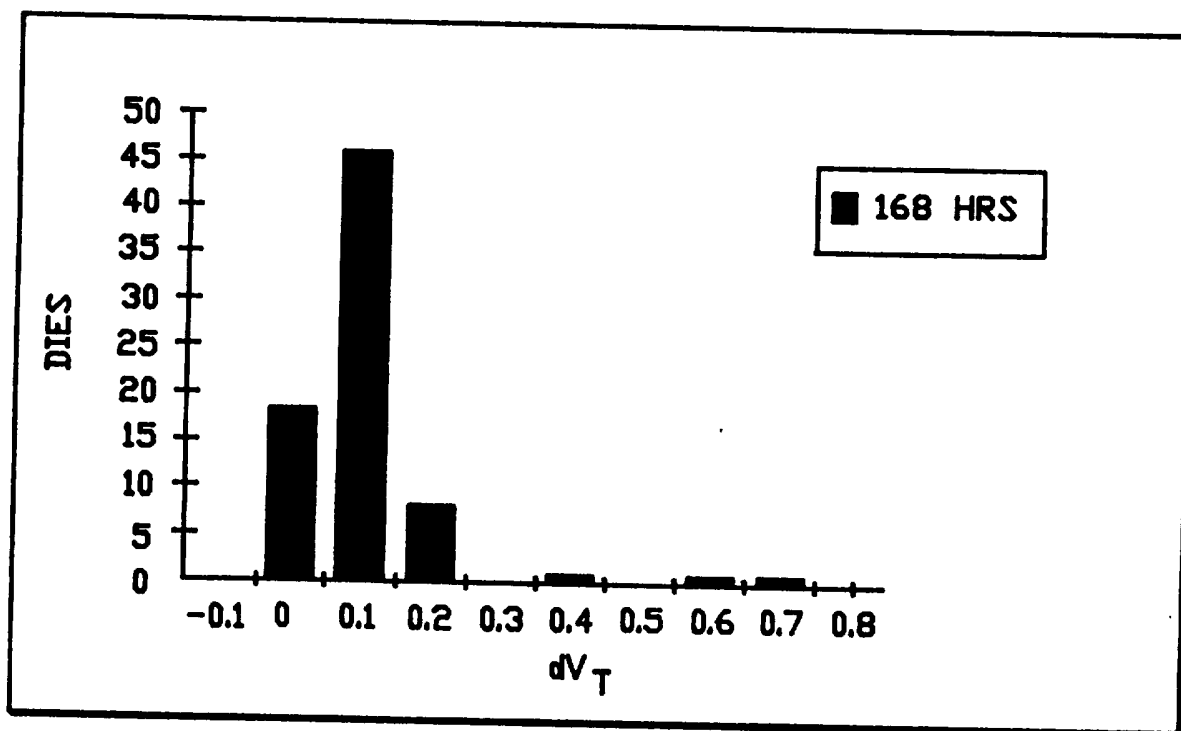


FIG.10

SUBSTITUTE SHEET (RULE 26)

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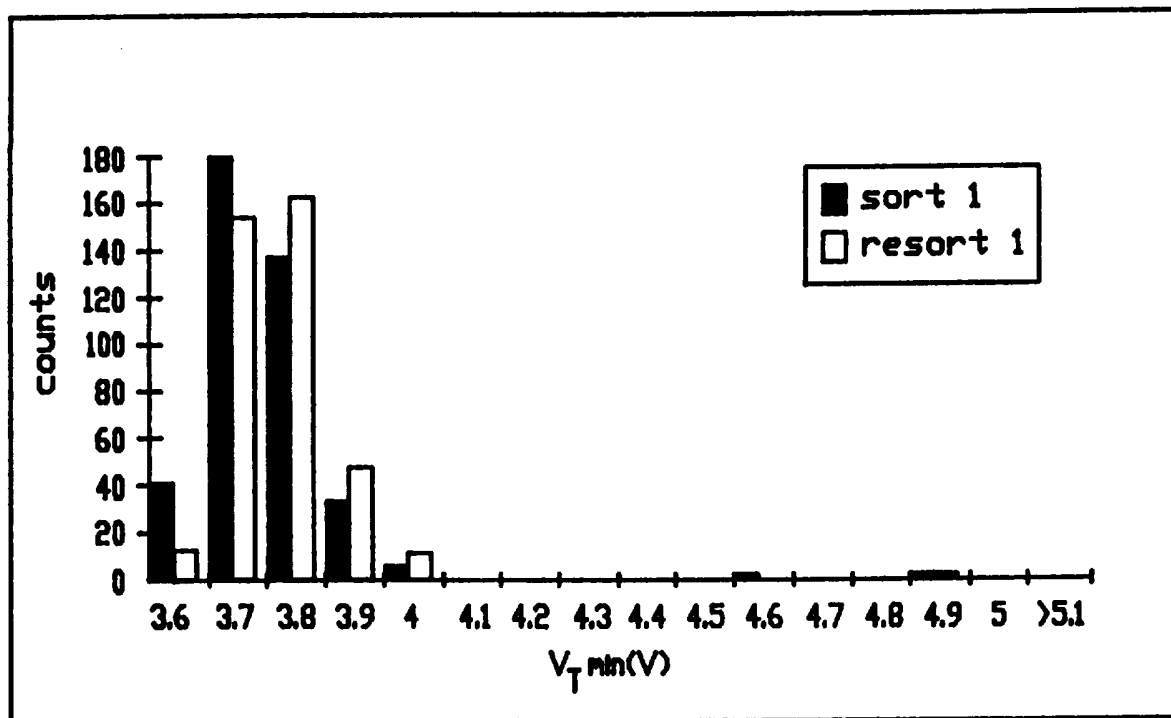


FIG. 11

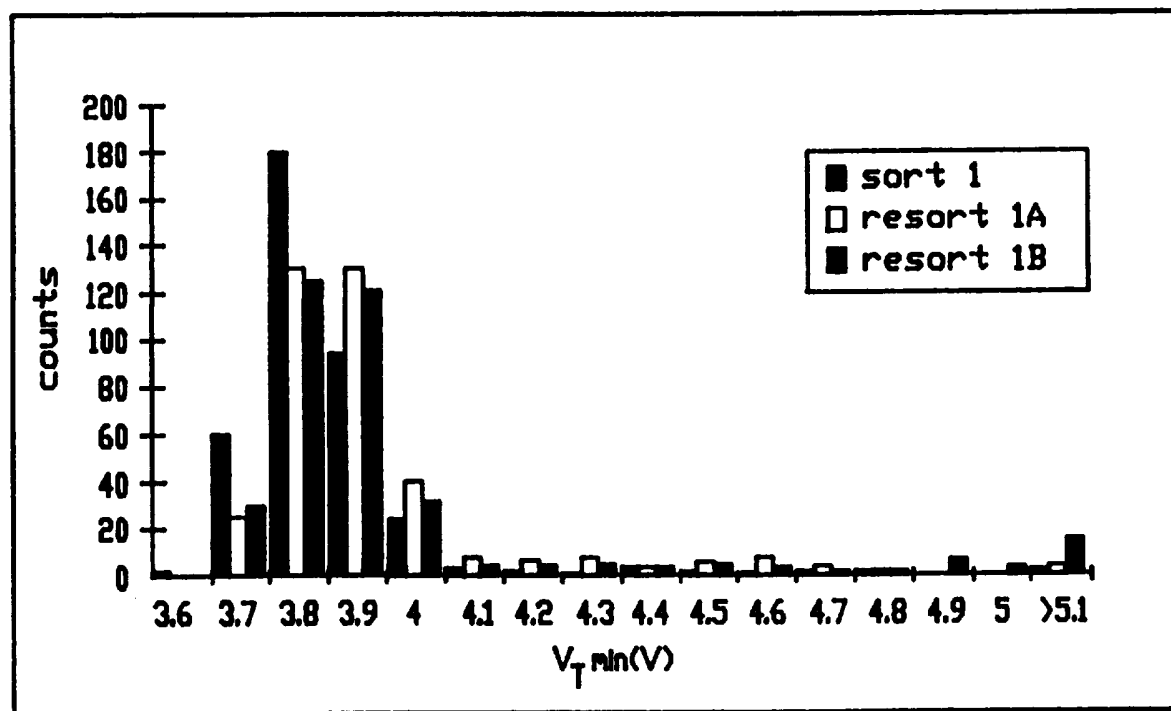


FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/12780**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(6) : H01L-21/02

US CL : 437/43, 235, 238, 241; 257/323, 324, 639, 641, 649

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 437/43, 235, 238, 241; 257/323, 324, 639, 641, 649

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

search terms: UV erasable eprom, eprom, passivation, planarize, smooth, flat, oxynitride, bpsg, psg, glass

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,372,034 (BOHR) 8 FEBRUARY 1983, ABSTRACT AND SUMMARY	1 AND 14
Y	US, A 4,816,115 (HÖRNER ET AL) 28 MARCH 1989, ABSTRACT	1 AND 14
Y,E	US, A, 5,376,590, (MACHIDA ET AL) 27 DECEMBER 1994, FIGURE 2 AND COL. 4, LINES 20-63; COL. 5, LINES 42-56	1 AND 14
Y	US, A, 5,362,686, (HARADA) 8 NOVEMBER 1994, ABSTRACT	2, 6, 7
Y	US, A, 5,306,936 (GOTO) 26 APRIL 1994, ABSTRACT	1 AND 14
Y	US, A, 4,962,063 (MAYDAN ET AL) 09 OCTOBER 1990, COL. 4-8	1, 7, 14

☒ Further documents are listed in the continuation of Box C.
 ☐ See patent family annex.

* Special categories of cited documents:	*T	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
A document defining the general state of the art which is not considered to be of particular relevance	*X*	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
E earlier document published on or after the international filing date	*Y*	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*A*	document member of the same patent family
O document referring to an oral disclosure, use, exhibition or other means		
P document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

09 MARCH 1995

Date of mailing of the international search report

03 APR 1995

Name and mailing address of the ISA/US
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/12780

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	- Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 5,252,515 (TSAI ET AL) 12 OCTOBER 1993, ABSTRACT AND COL. 5-6	1 AND 14
Y	US, A, 4,775,550 (CHU ET AL) 04 OCTOBER 1988, COL 4	1, 7, 14
Y	US, A, 5,260,236 (PETRO ET AL) 09 NOVEMBER 1993, TITLE AND ABSTRACT	7, 17
Y	US, A, 4,885,262 (TING ET AL) 05 DECEMBER 1989, COL 3	1 AND 14
Y	US, A, 5,003,062 (YEN) 26 MARCH 1991, ABSTRACT	1 AND 14
Y	US, A, 4,581,622 (TAKASAKI ET AL) 08 APRIL 1986, ABSTRACT, SUMMARY, COL. 3-4	7, 17
Y	US, A, RE.32,351 (DAWSON ET AL) 17 FEBRUARY 1987, ABSTRACT	8
Y	US, A, 4,097,889 (KERN ET AL) 27 JUNE 1978, ABSTRACT AND COL. 3-4	1, 7, 14