



(51) International Patent Classification:

H01L 27/108 (2006.01) H01L 29/78 (2006.01)
H01L 21/768 (2006.01) H01L 29/66 (2006.01)

(21) International Application Number:

PCT/US2016/063458

(22) International Filing Date:

23 November 2016 (23.11.2016)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

14/978,305 22 December 2015 (22.12.2015) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: NON-UNIFORM GATE OXIDE THICKNESS FOR DRAM DEVICE

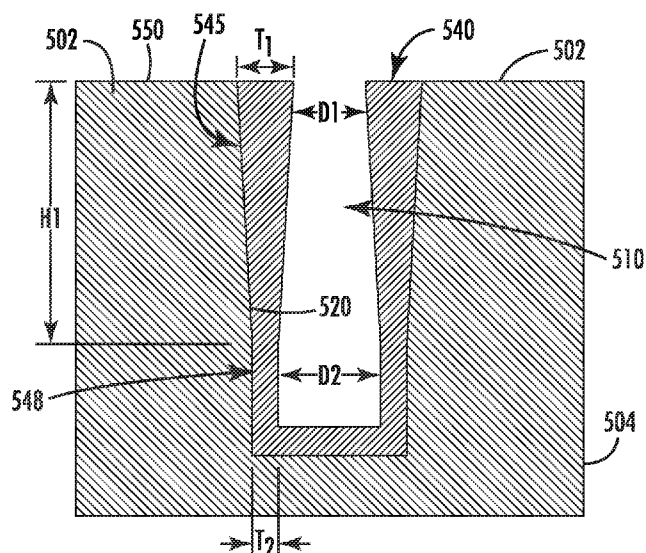


FIG 5

(57) Abstract: Provided herein are approaches for forming a gate oxide layer for a DRAM device, the method including providing a finned substrate having a recess formed therein, and performing an ion implant into a sidewall surface of the recess to form a gate oxide layer having a non-uniform thickness, wherein a thickness of the gate oxide layer at a top section of the sidewall surface is greater than a thickness of the gate oxide layer at a bottom section of the sidewall surface. In some approaches, the ion implant is provided as a series of ion implants at multiple different implant angles, varied along with an ion implantation energy and/or an ion dose to increase the thickness of the gate oxide of the top section of the sidewall surface. In some approaches, the finned substrate is also exposed to a plasma, either during or after, the ion implantation.

WO 2017/112276 A1



Published:

— *with international search report (Art. 21(3))*

NON-UNIFORM GATE OXIDE THICKNESS FOR DRAM DEVICE

Field of the Disclosure

[0001] The present embodiments relate to substrate patterning, and more particularly, to techniques for implanting a substrate with ions to form a gate oxide having a non-uniform thickness.

Background of the Disclosure

[0002] Plasma immersion ion implantation is performed by generating a plasma containing ions of species to be implanted in a semiconductor wafer or workpiece. The plasma may be generated using a plasma source, such as a toroidal plasma source, at the reactor chamber ceiling. Ion energy sufficient to achieve an intended ion implantation depth profile below the wafer surface is provided by coupling a very high RF bias voltage (e.g., 10 kV to 20 kV) to the semiconductor wafer through an insulated cathode electrode within the wafer support pedestal. High implant dose rate requires a high plasma ion density, achieved using a toroidal plasma source operating at a low chamber pressure. The requisite ion implant depth profile requires a very high ion energy, achieved by applying a very high RF bias voltage across the plasma sheath at the wafer surface. The process gas employed in plasma immersion ion implantation can be a fluoride or a hydride of the dopant species to be implanted.

[0003] In DRAM/flash memory fabrication, implanting a semiconductor dopant species into the polycrystalline silicon (polysilicon) gate electrodes beneficially increases conductivity. The gate electrodes are formed by depositing amorphous silicon on a thin gate oxide layer and then annealing the wafer sufficiently to transform the deposited silicon from the amorphous state to a polycrystalline state. The polycrystalline silicon gate layer

thus formed is about 50 nm to 80 nm thick. The implanted species is one promoting p-type conductivity in silicon, such as boron, or n-type conductivity, such as arsenic, phosphorous or antimony. The gate electrode can also be made by certain metals such as TiN or W.

[0004] Long refresh time in DRAM is influential for device function. Refresh time is directly proportional to the amount of time charge can be held in DRAM cells. Thus, minimizing the cell junction leakage increases the charge retention time. Gate induced drain leakage (GIDL) is the primary mechanism for junction leakage. Thickening the gate oxide layer at the location of maximum GIDL will reduce overall junction leakage and increase charge retention time.

[0005] On the other hand, the layer thickness of the gate oxide continues to be reduced in order to provide suitable gate control over the sub-threshold region. Also, increasing doping density in the channel and source/drain regions advantageously improves punch through characteristics and increase drives. Thus, difficulties exist in providing a scaled down semiconductor device having a suitable balance between high current driving capability and low GIDL current.

Summary of the Disclosure

[0006] In view of the foregoing, what is needed are methods for improving GIDL in DRAM access devices by providing a non-uniform gate oxide having an area of increased thickness. In one approach, a process for reducing GIDL includes providing a finned substrate having a recess formed therein, and performing an ion implant into a sidewall surface of the recess to form a gate oxide layer having a non-uniform thickness, wherein a thickness of the gate oxide layer at a top section of the sidewall surface is greater than a thickness of the gate oxide layer at a bottom section of the sidewall surface. In some

embodiments, approaches further include performing a series of ion implants at multiple different implant angles, varied during the series of ion implants along with an ion implantation energy and/or an ion dose, to increase the thickness of the gate oxide of the top section of the sidewall surface. In some embodiments, the finned substrate is also exposed to a plasma, either during or after, the ion implantation.

[0007] In some embodiments, a method of forming a dynamic random access memory (DRAM) device includes providing a finned substrate having a recess formed therein, and performing an ion implant into a sidewall surface of the recess to form a gate oxide layer having a non-uniform thickness, wherein a thickness of the gate oxide layer at a top section of the sidewall surface is greater than a thickness of the gate oxide layer at a bottom section of the sidewall surface.

[0008] In some embodiments, a method of forming a gate oxide layer for a dynamic random access memory (DRAM) device includes providing a finned substrate having a recess formed therein, and performing a series of ion implants into a sidewall surface of the recess to form a gate oxide layer having a non-uniform thickness. The series of ion implants impacts the sidewall surface at multiple different implant angles to form the gate oxide layer with a thickness at a top section of the sidewall surface greater than a thickness of the gate oxide layer at a bottom section of the sidewall surface.

[0009] In some embodiments, a dynamic random access memory (DRAM) device includes a set of fins defining a recess in a substrate, the recess having a sidewall surface and a bottom surface, and a gate oxide formed along the sidewall surface and the bottom surface of the recess. A thickness of the gate oxide along a top section of the sidewall surface is greater than a thickness of the gate oxide along a bottom section of the sidewall surface.

Brief Description of the Drawings

[0010] **FIG. 1** depicts a side cross-sectional view of an approach for treating a finned substrate in accordance with an embodiment of the present disclosure.

[0011] **FIG. 2** depicts a side cross-sectional view of an approach for implanting ions into a sidewall surface of a recess of a finned substrate in accordance with an embodiment of the present disclosure.

[0012] **FIG. 3** depicts a side cross-sectional view of an approach for forming a non-uniform gate oxide along a sidewall surface of a finned substrate in accordance with embodiments of the present disclosure.

[0013] **FIG. 4** depicts a side cross-sectional view of a series of sidewall implants performed at varying angles in accordance with an embodiment of the present disclosure.

[0014] **FIG. 5** depicts a side cross-sectional view of a non-uniform gate oxide formed along a sidewall surface of a finned substrate in accordance with embodiments of the present disclosure.

[0015] **FIG. 6** depicts a graph illustrating the sputter yield of Si under irradiation of an ion beam in accordance with an embodiment of the present disclosure.

[0016] **FIGS. 7A-B** depict growth of an oxide layer after an ion implant in accordance with an embodiment of the present disclosure.

[0017] **FIG. 8** is a flowchart illustrating an exemplary method according to the present disclosure.

[0018] The drawings are not necessarily to scale. The drawings are merely representations, not intended to portray specific parameters of the disclosure. The drawings

are intended to depict exemplary embodiments of the disclosure, and therefore are not be considered as limiting in scope. In the drawings, like numbering represents like elements.

[0019] Furthermore, certain elements in some of the figures may be omitted, or illustrated not-to-scale, for illustrative clarity. The cross-sectional views may be in the form of "slices", or "near-sighted" cross-sectional views, omitting certain background lines otherwise visible in a "true" cross-sectional view, for illustrative clarity. Furthermore, for clarity, some reference numbers may be omitted in certain drawings.

Detailed Description

[0020] Methods in accordance with the present disclosure will now be described more fully hereinafter with reference to the accompanying drawings, where embodiments of the methods are shown. The method may be embodied in many different forms and are not to be construed as being limited to the embodiments set forth herein. Instead, these embodiments are provided so this disclosure will be thorough and complete, and will fully convey the scope of the system and method to those skilled in the art.

[0021] For the sake of convenience and clarity, terms such as "top," "bottom," "upper," "lower," "vertical," "horizontal," "lateral," and "longitudinal" will be used herein to describe the relative placement and orientation of these components and their constituent parts with respect to the geometry and orientation of a component of a semiconductor manufacturing device as appearing in the figures. The terminology will include the words specifically mentioned, derivatives thereof, and words of similar import.

[0022] As used herein, an element or operation recited in the singular and proceeded with the word "a" or "an" is to be understood as including plural elements or operations, until such exclusion is explicitly recited. Furthermore, references to "one

embodiment" of the present disclosure are not intended as limiting. Additional embodiments may also incorporating the recited features.

[0023] As further described herein, provided are approaches for forming a gate oxide layer for a semiconductor device (e.g., DRAM), the method including providing a finned substrate having a recess formed therein, and performing an ion implant into a sidewall surface of the recess to form a gate oxide layer having a non-uniform thickness, wherein a thickness of the gate oxide layer at a top section of the sidewall surface is greater than a thickness of the gate oxide layer at a bottom section of the sidewall surface. In some embodiments, approaches further include performing a series of ion implants at multiple different implant angles, varied during the series of ion implants along with an ion implantation energy and/or an ion dose to increase the thickness of the gate oxide of the top section of the sidewall surface. In some embodiments, the finned substrate is also exposed to a plasma, either during or after, the ion implantation. As a result, unlike a prior art thermally based DRAM gate oxide process, requiring heating of wafers to $>800^{\circ}\text{C}$, ion-beam based implementations provided herein form an oxide with local variation in thickness, achieved at a lower temperature.

[0024] Turning now to **FIG. 1**, there is shown a cross-sectional view of an approach for forming a device 100 (e.g., a DRAM device) according to embodiments of the disclosure. The device 100 comprises a substrate 104 (e.g., bulk silicon) and a plurality of fins 102 patterned (e.g., etched) from the substrate 104. The fins 102 may be fabricated using any suitable process including one or more photolithography and etch processes. As further shown, the set of fins 102 define a recess 110 formed therebetween, the recess 110 including a bottom surface 112 and a set of sidewalls 120.

[0025] The photolithography process for forming the set of fins 102 may include forming a photoresist layer (not shown) overlying the substrate 104 (e.g., on a silicon layer), exposing the resist to a pattern, performing post-exposure bake processes, and developing the resist to form a masking element including the resist. The masking element may then be used to etch the fins 102 into the silicon layer, e.g., using reactive ion etch (RIE) and/or other suitable processes. In one embodiment, the fins 102 are formed using a sidewall image transfer technique. In another embodiment, the fins 102 are formed by a double-patterning lithography (DPL) process. DPL is a method of constructing a pattern on a substrate by dividing the pattern into two interleaved patterns. DPL allows enhanced feature (e.g., fin) density. Various DPL methodologies may be used including, but not limited to, double exposure (e.g., using two mask sets), forming spacers adjacent features and removing the features to provide a pattern of spacers, resist freezing, and/or other suitable processes.

[0026] The term "substrate" as used herein is intended to include a semiconductor substrate, a semiconductor epitaxial layer deposited or otherwise formed on a semiconductor substrate and/or any other type of semiconductor body, and all such structures are contemplated as falling within the scope of the present embodiments. For example, the semiconductor substrate may comprise a semiconductor wafer (e.g., silicon, SiGe, or an SOI wafer) or one or more die on a wafer, and any epitaxial layers or other type semiconductor layers formed there over or associated therewith. A portion or entire semiconductor substrate may be amorphous, polycrystalline, or single-crystalline. In addition to the aforementioned types of semiconductor substrates, the semiconductor substrate employed in the present embodiments may also comprise a hybrid oriented (HOT) semiconductor substrate having surface regions of different crystallographic orientation.

The semiconductor substrate may be doped, undoped, or contain doped regions and undoped regions therein. The semiconductor substrate may contain regions with strain and regions without strain therein, or contain regions of tensile strain and compressive strain.

[0027] In some embodiments, the set of fins 102 may have a uniform height 'H' across the wafer, as well as a uniform distance 'D' between adjacent fins. Because the geometries of the set of fins 102 are generally constant across the wafer, the set of fins 102 may be used to shadow the space between the fins 102. In one embodiment, an ion incidence implant angle ' α ' of an ion implantation 118 may be chosen in such a way so just an intended portion of the sidewall surface 120 of the fins 102 is implanted. Meanwhile, the bottom surface 112 of the recess 110 is generally unaffected.

[0028] As further shown in **FIG. 1**, the ion implantation 118 to the sidewall surface 120 of the set of fins 102 forms an oxide layer 124 (e.g., SiO₂). In exemplary embodiments, the ion implantation 118 is performed at an implant angle ' α ' nonparallel with the sidewall surface 120. For example, the ion implantation 118 may impart ions at approximately 30° incidence angle to the sidewall surface 120 (or approximately 60° relative to a plane normal to the sidewall surface 120) to form the oxide layer 124 along just a portion of the sidewall surface 120. The implantation angle may vary in other embodiments by +/- 15°.

[0029] During operation, the ion implantation 118 may be performed while the device 100 is in a first position, for example as shown in **FIG. 1**. Following formation of the oxide layer 124 along the sidewall surface 120, the device 100 is rotated (e.g., by 30, 45, 60, or 90 degrees), and another ion implantation may be applied to the device 100 to form the oxide layer 124 along one or more additional sidewall surfaces of the set of fins 102. In exemplary embodiments, the oxide layer 124 is again formed just along a

portion of the sidewall surface 120 of the fins 102. The ion implantation may similarly be performed at an implant approximately 60° incidence angle to the sidewall surface 120 (or approximately 30° relative to a plane normal to the sidewall surface 120).

[0030] In various embodiments, the ion implantation 118 may be performed before, or simultaneously with, a plasma exposure 130. For example, in the case of an Ar implantation for surface activation followed by O₂ plasma exposure, the wafer may cycle between an ion beam generator and an O₂ plasma source (not shown). In the case of simultaneous surface activation and plasma exposure, the growth process to form the oxide layer 124 is activated by a low energy (e.g., ~10-100eV) Ar ion-bombardment of the sidewall surface 120 whilst the surface is subjected to an O plasma. The Ar ion-irradiated implant reduces the activation energy of Si oxidation so oxidation readily occurs at a low temperature. Meanwhile, the Ar beam of the ion implantation 118 can be directed at an angle so oxidation occurs just where the Si surface is irradiated with the beam on certain parts of the sidewall surface 120, e.g., an area corresponding to the oxide layer 124 shown in **FIG. 1**.

[0031] In some embodiments, the ion energy is low enough to eliminate damage to the crystalline Si of the substrate 104 and to maintain good structural integrity of the oxide. For example, a high quality stoichiometric Si-oxide with no end-of-range of damage to the underlying Si may be formed at 450° C. In one non-limiting embodiment, ion implantation may be provided by a beamline ion-implanter, a beamline implanter with modified end-station containing a remote O plasma source, or a modified beamline implanter delivering a beam of multiple 10s of eV energy.

[0032] Referring now to **FIG. 2-3**, formation of a gate oxide layer within a recess 210 of a device 200 will be described in greater detail. As shown, formation of the

gate oxide layer 240 may include forming a base oxide layer 242 along the sidewall surface 220 and the bottom surface 212 within the recess 210. In various embodiments, the base oxide layer 242 may be conformally deposited within the recess 210, wherein "depositing" may include any now known or later developed techniques appropriate for the material to be deposited including but not limited to, for example: chemical vapor deposition (CVD), low-pressure CVD (LPCVD), plasma-enhanced CVD (PECVD), semi-atmosphere CVD (SACVD) and high density plasma CVD (HDPCVD), rapid thermal CVD (RTCVD), ultra-high vacuum CVD (UHVCVD), limited reaction processing CVD (LRPCVD), metal-organic CVD (MOCVD), sputtering deposition, ion beam deposition, electron beam deposition, laser assisted deposition, thermal oxidation, thermal nitridation, spin-on methods, physical vapor deposition (PVD), atomic layer deposition (ALD), chemical oxidation, molecular beam epitaxy (MBE), plating, evaporation.

[0033] As further shown, an ion implantation 218 may be performed to the sidewall surface 220 of the set of fins 202. In exemplary embodiments, the ion implantation 218 is performed at an implant angle ' α ' nonparallel with the sidewall surface 220 so as to impact just a portion of the sidewall surface 220. As shown in **FIG. 3**, this results in a gate oxide layer 340 having a non-uniform thickness in the areas of the sidewall surface 320 impacted by the ion implantation 318. For example, a thickness T_1 of the gate oxide layer 340 at a top section 345 of the recess 310 is greater than a thickness T_2 of the gate oxide layer 340 at a bottom section 348 of the recess 310. This localized, relatively thicker top section 345 of the gate oxide layer 340 advantageously reduces GIDL.

[0034] Referring now to **FIGS. 4-5**, an embodiment for performing a series of ion implants at varying implant angles will be described in greater detail. In this embodiment, ion implantation energy and/or ion dose may also be varied during performance of the series

of ion implantations 418A-C to the sidewall surface 420 to form an oxide layer 440 with a dose gradient varying along a height 'H1' of the top section 445 of the recess 410. As a result, a thermal oxide layer with variable thickness may be produced due to the difference in oxide growth rates. Furthermore, the energy of the series of ion implantations 418A-C may be chosen in such a way so all the damaged Si will be consumed during oxidation, thus minimizing leakage from end-of-range damage.

[0035] For example, as shown in **FIG. 4**, the series of ion implantations 418A-C may be performed to the sidewall surface 420 of the set of fins 402 at a variety of implant angles, α_{1-3} . In exemplary embodiments, the first ion implantation 418-A is performed at an implant angle α_1 and at a first implant energy/ion dose, the second ion implantation 418-B is performed at another implant angle α_2 and implant energy/ion dose, and the third ion implantation 418-C is performed at yet another implant angle α_3 and implant energy/ion dose. Each of the implant angles α_{1-3} is nonparallel with the sidewall surface 420 so as to impact various points along the top section 445 of the sidewall surface 420. As shown, the bottom section 448 of the sidewall surface 420 (other portions of text recite bottom portion of the recess – choose) remains generally unaffected by the series of ion implantations 418A-C.

[0036] As shown in **FIG. 5**, the varied ion implant results in a gate oxide layer 540 having a non-uniform thickness, wherein a thickness T1 of the gate oxide layer 540 at a top section 545 is greater than a thickness T2 of the gate oxide layer 540 at the bottom section 548. More specifically, the thickness of the oxide varies along the top section 545 so the gate oxide layer 540 is thickest proximate a top surface 550 of the fins 502. As shown, a diameter D1 of the recess 510 proximate the top section 545 is smaller than a diameter D2 of the recess 510 proximate the bottom section 548. To achieve this oxide

profile, the ion implantation energy and the ion dose may be increased as the implant angle (e.g., α_{1-3}) decreases over the series of ion implants 418A-C (**FIG. 4**). For example, the ion implantation energy and/or the ion dose of the ion implantation 418-C may be greater than the ion implantation energy and/or the ion dose of the ion implantation 418-A.

[0037] Referring now to **FIG. 6**, shown is a graph 658 illustrating the sputter yield of Si under irradiation of an O ion beam, such as an ion beam of the ion implantations shown in **FIGS. 1-5**. In this non-limiting embodiment, the maximum Si removal rate is set at 10keV. In addition, with the implantation of O, there may be a volume expansion due to the formation of SiO₂, for example, to counter the loss of Si due to sputtering. The transmission electron microscopy (TEM) images of **FIGS. 7A-B** demonstrate, after O implant at 1keV, the top surface 760 grows 3.5nm above the interface 762, e.g., instead of having a recess due to loss by sputtering.

[0038] Referring now to **FIG. 8**, a flow diagram illustrating an exemplary method 800 for patterning a semiconductor device in accordance with the present disclosure is shown. The method 800 will be described in conjunction with the representations shown in **FIGS. 1-7**.

[0039] Method 800 may include providing a finned substrate having a recess formed therein, as shown in block 801. In some embodiments, the finned substrate is silicon.

[0040] The method 800 may further include performing an ion implant into a sidewall surface of the recess to form a gate oxide layer having a non-uniform thickness, as shown in block 803. In some embodiments, a thickness of the gate oxide layer at a top section of the recess is greater than a thickness of the gate oxide layer at a bottom section

of the recess. In some embodiments, the ion implant is performed as a series of ion implants having multiple different implant angles. In some embodiments, the method 800 includes varying at least one of the following during performance of the series of ion implants: an ion implantation energy, and an ion dose. In some embodiments, the ion implantation energy and the ion dose is increased over the series of ion implants as the implant angle decreases, wherein the implant angle is measured relative to the sidewall surface.

[0041] The method 800 may further include exposing the finned substrate to a plasma, as shown at block 805. In some embodiments, the plasma exposure and ion implant may be simultaneous. In other embodiments, the ion implant is performed prior to the plasma exposure.

[0042] The method 800 may further include increasing the thickness of the gate oxide along the top section of sidewall surface of the sidewall surface to form a non-uniform thickness gate oxide layer, as shown in block 807. In some embodiments, the thickness of the gate oxide is greatest proximate a top surface of the finned substrate.

[0043] In view of the foregoing, at least the following advantages are achieved by the embodiments disclosed herein. A first advantage includes angling an ion implant directed to a sidewall surface of a fin to allow local growth of a gate oxide layer, thus decreasing GIDL. A second advantage includes implanting the device at an ion energy low enough to eliminate damage to the crystalline Si of the substrate, yet maintain good structural integrity of the oxide.

[0044] While certain embodiments of the disclosure have been described herein, the disclosure is not limited thereto, as the disclosure is as broad in scope as the art will allow and the specification may be read likewise. Therefore, the above description is not

to be construed as limiting. Instead, the above description is merely as exemplifications of particular embodiments. Those skilled in the art will envision other modifications within the scope and spirit of the claims appended hereto.

Claims

1. A method of forming a dynamic random access memory device (DRAM) device, the method comprising:

providing a finned substrate having a recess formed therein; and

performing an ion implant into a sidewall surface of the recess to form a gate oxide layer having a non-uniform thickness, wherein a thickness of the gate oxide layer at a top section of the sidewall surface is greater than a thickness of the gate oxide layer at a bottom section of the sidewall surface.

2. The method of claim 1, further comprising performing a series of ion implants at multiple different implant angles.

3. The method according to claim 2, further comprising varying at least one of the following during performance of the series of ion implants: an ion implantation energy, and an ion dose.

4. The method according to claim 3, further comprising increasing the ion implantation energy and the ion dose over the series of ion implants as an implant angle decreases, wherein the implant angle is measured relative to the sidewall surface.

5. The method according to claim 3, further comprising increasing the thickness of the gate oxide along the top section of the sidewall surface, wherein the thickness of the gate oxide is greatest proximate a top surface of the finned substrate.

6. The method according to claim 2, further comprising forming a base oxide layer within the recess prior to performing the series of ion implants to the sidewall surface of the recess.
7. The method according to claim 2, further comprising exposing the finned substrate to a plasma.
8. The method according to claim 7, further comprising simultaneously exposing the finned substrate to the plasma and performing the series of ion implants to the sidewall surface of the recess.
9. The method according to claim 7, further comprising performing at least one of the series of ion implants prior to exposing the finned substrate to the plasma.
10. A method of forming a gate oxide layer for a memory device, comprising:
providing a finned substrate having a recess formed therein; and
performing a series of ion implants into a sidewall surface of the recess to form a gate oxide layer having a non-uniform thickness, wherein the series of ion implants impact the sidewall surface at multiple different implant angles to form the gate oxide layer with a thickness at a top section of the sidewall surface greater than a thickness of the gate oxide layer at a bottom section of the sidewall surface.

11. The method according to claim 10, further comprising varying at least one of the following during performance of the series of ion implants: an ion implantation energy, and an ion dose.

12. The method according to claim 11, further comprising increasing the ion implantation energy and the ion dose over the series of ion implants as an implant angle decreases, wherein the implant angle is measured relative to the sidewall surface.

13. A dynamic random access memory (DRAM) device comprising:

a set of fins defining a recess in a substrate, the recess having a sidewall surface and a bottom surface; and

a gate oxide formed along the sidewall surface and the bottom surface of the recess, wherein a thickness of the gate oxide along a top section of the sidewall surface is greater than a thickness of the gate oxide along a bottom section of the sidewall surface.

14. The DRAM device of claim 13, wherein the finned substrate is Si and the gate oxide is SiO₂.

15. The DRAM device of claim 13, wherein the thickness of the gate oxide along the top section of the sidewall surface increases towards a top surface of the finned substrate.

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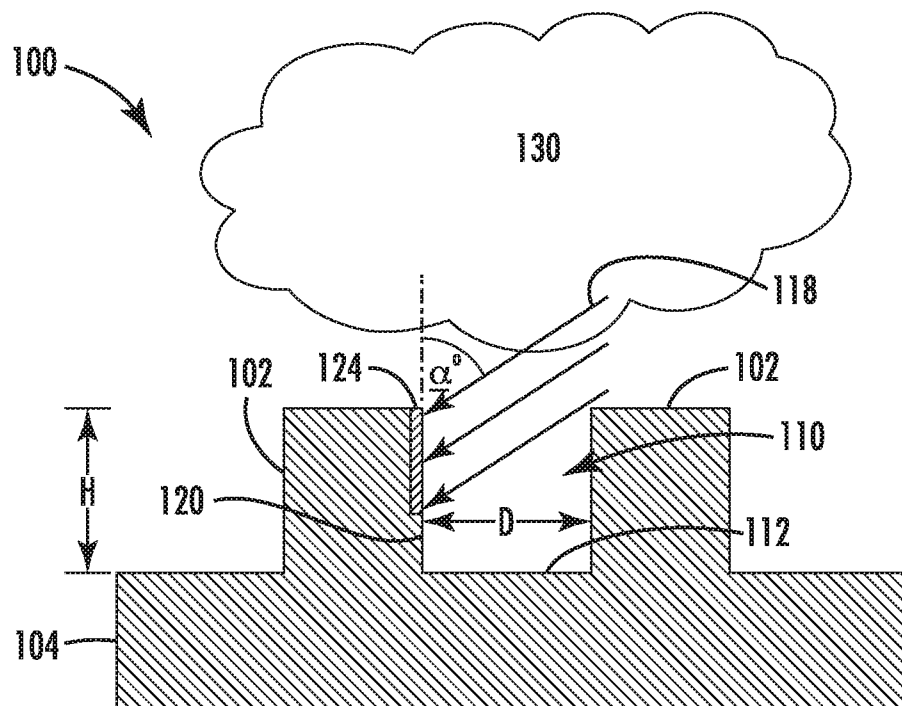


FIG 1

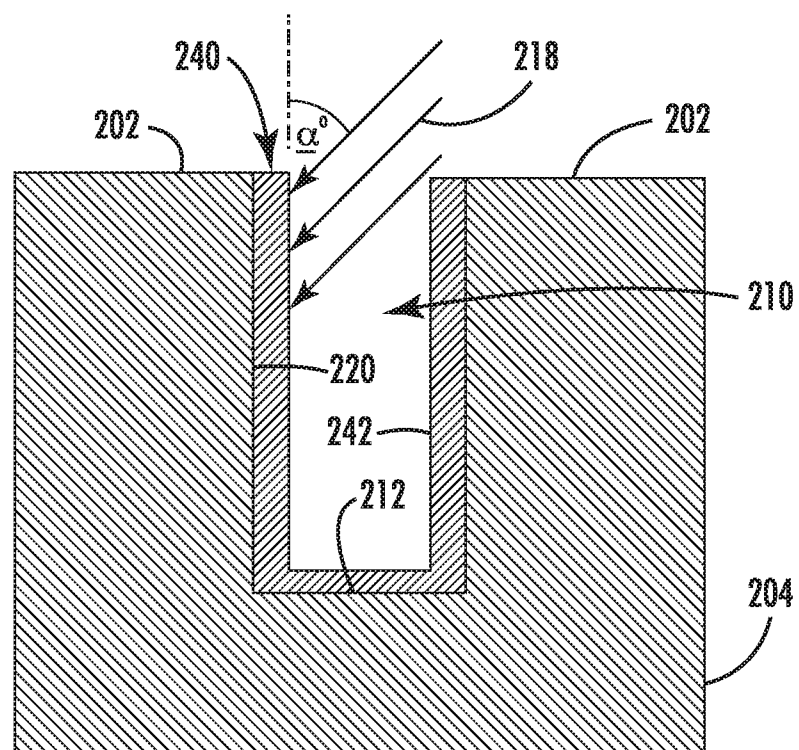


FIG 2

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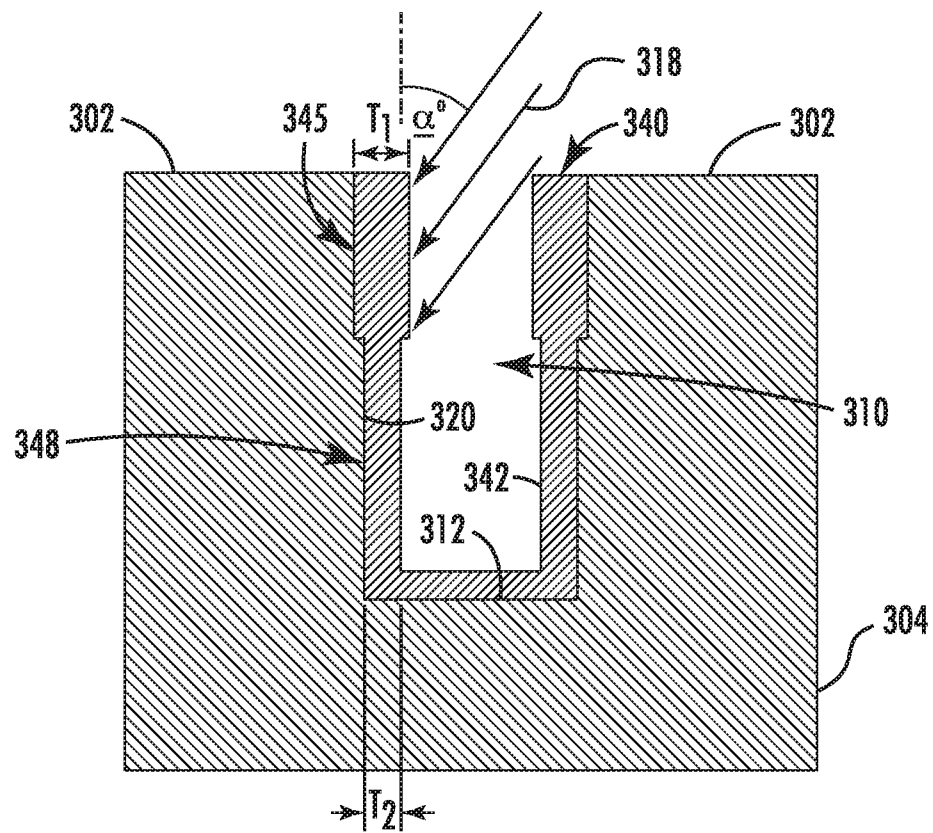


FIG. 3

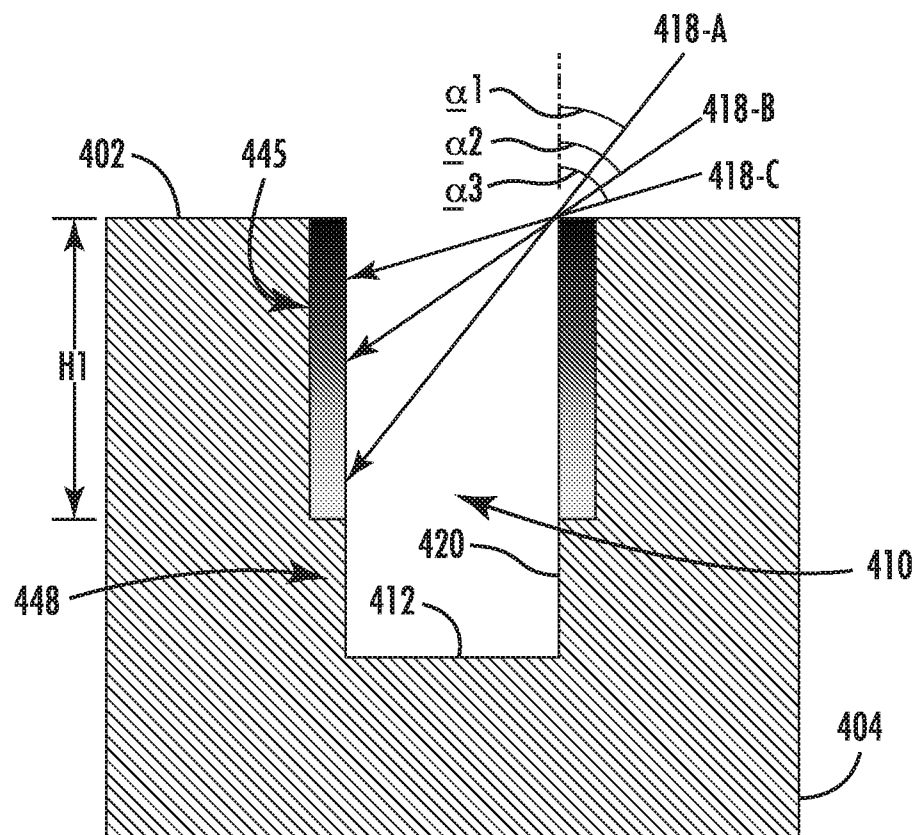


FIG 4

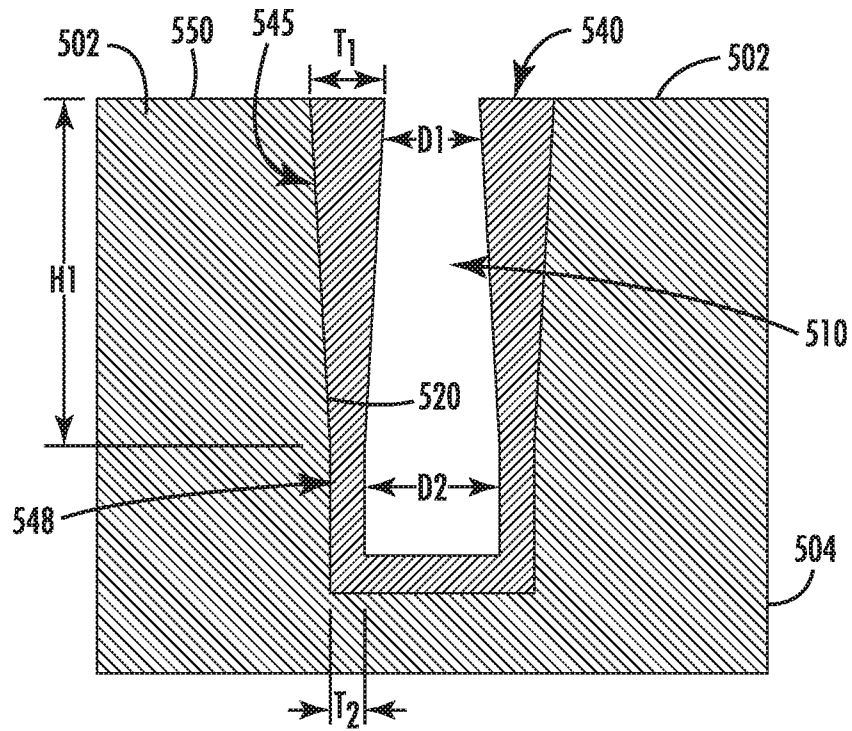


FIG. 5

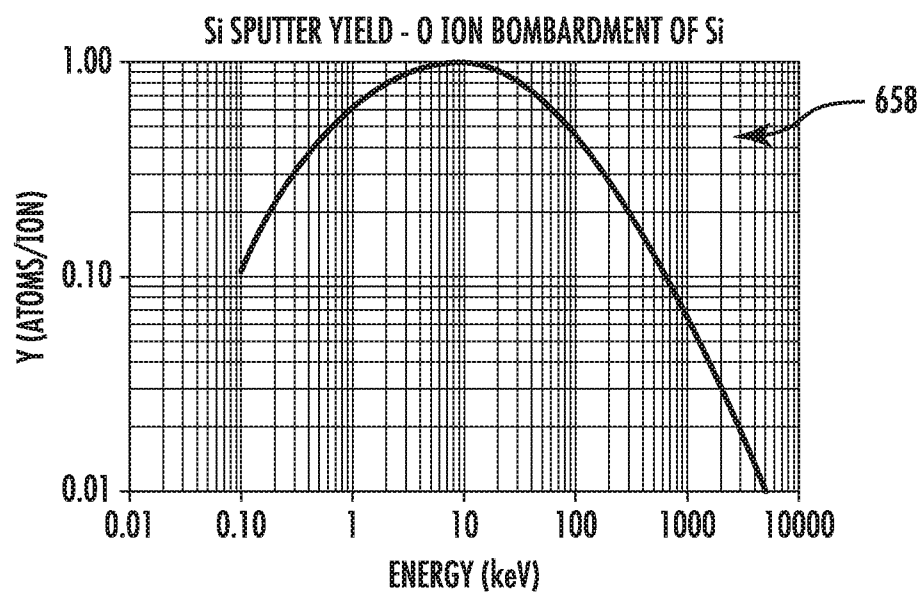


FIG. 6

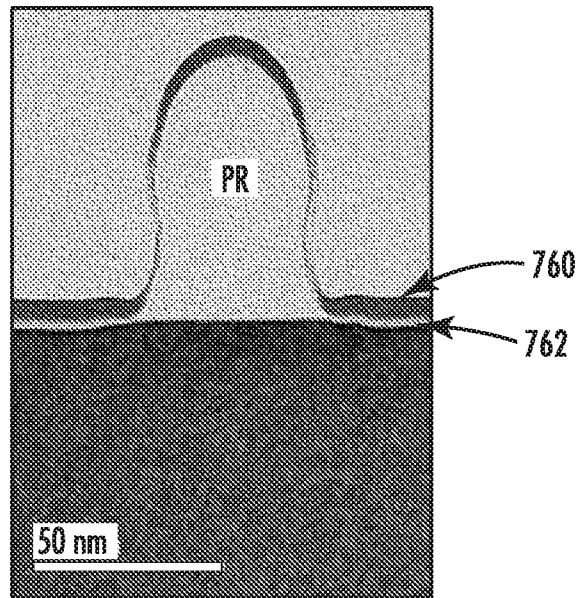


FIG. 7A

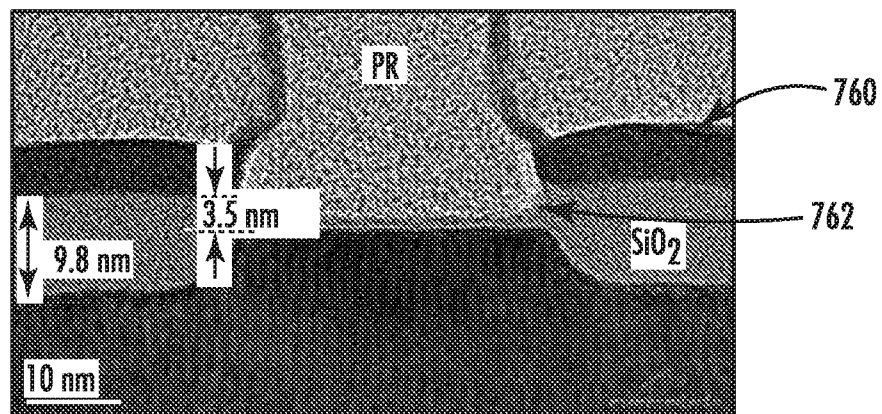
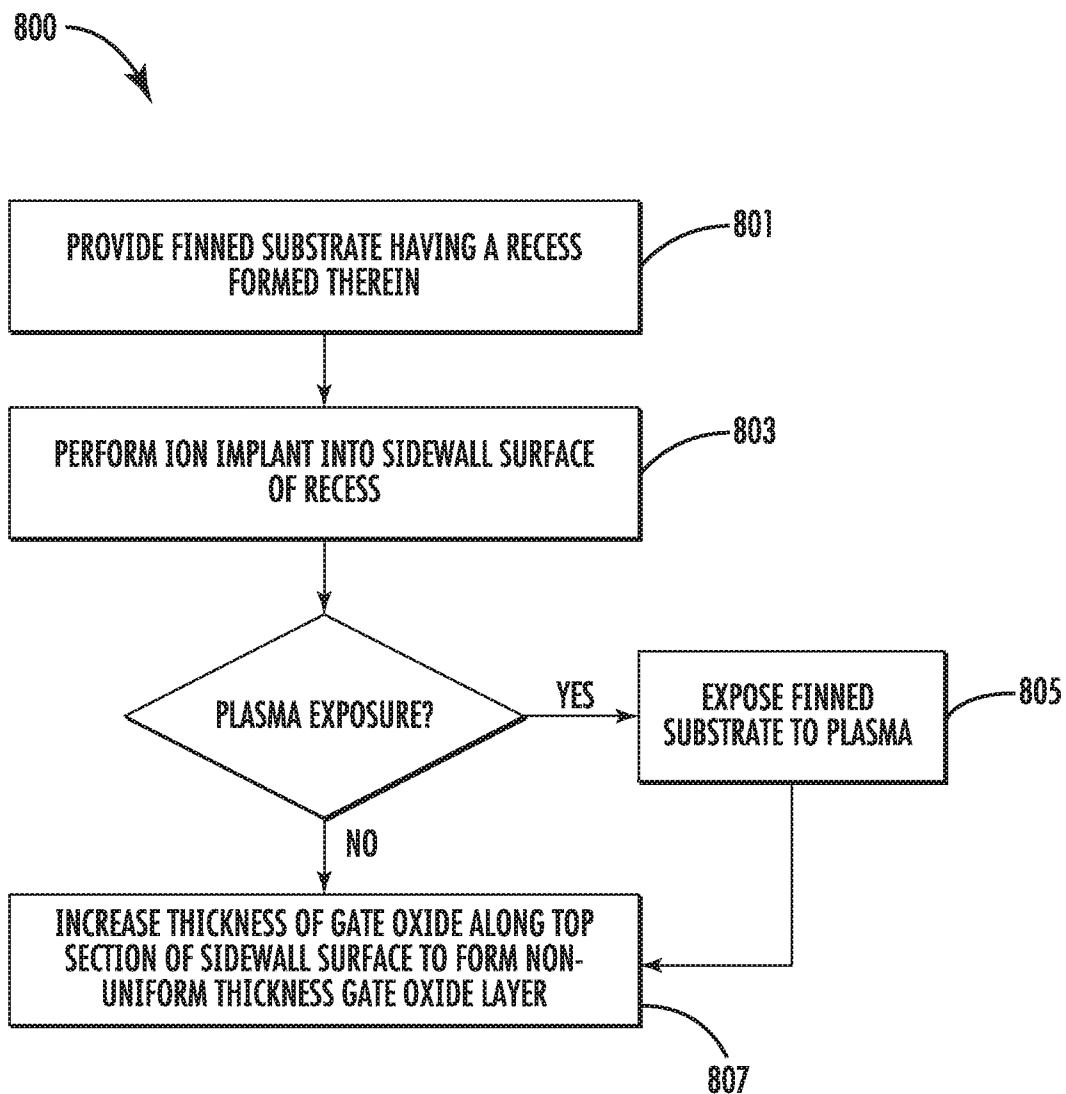


FIG. 7B

**FIG 8**

A. CLASSIFICATION OF SUBJECT MATTER**H01L 27/108(2006.01)i, H01L 21/768(2006.01)i, H01L 29/78(2006.01)i, H01L 29/66(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/108; H01L 21/3065; H01L 21/336; H01L 29/78; H01L 29/76; H01L 21/265; H01L 25/07; H01L 21/768; H01L 29/66

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: non-uniform, gate oxide, thickness, fin, implanting substrate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2012-0238046 A1 (SAN YU et al.) 20 September 2012 See paragraphs [0020]–[0036] and figures 1–9.	1–15
A	US 2014-0206197 A1 (CANON ANELVA CORPORATION) 24 July 2014 See paragraphs [0042]–[0052] and figures 2–5.	1–15
A	US 2009-0267161 A1 (RAVI PILLARISETTY et al.) 29 October 2009 See paragraphs [0014]–[0022] and figure 2.	1–15
A	US 2011-0024841 A1 (FRANK BIN YANG et al.) 03 February 2011 See paragraphs [0028]–[0034] and figures 2–3.	1–15
A	KR 10-2012-0020062 A (SEN CORPORATION) 07 March 2012 See paragraphs [0011]–[0069] and figures 1–4.	1–15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

20 March 2017 (20.03.2017)

Date of mailing of the international search report

20 March 2017 (20.03.2017)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/063458

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012-0238046 A1	20/09/2012	TW 201237920 A US 8664027 B2 WO 2012-109110 A1	16/09/2012 04/03/2014 16/08/2012
US 2014-0206197 A1	24/07/2014	JP 2014-160802 A KR 10-1652908 B1 KR 10-2014-0095446 A KR 10-2016-0040493 A TW 201448051 A TW I532103 B US 9190287 B2	04/09/2014 31/08/2016 01/08/2014 14/04/2016 16/12/2014 01/05/2016 17/11/2015
US 2009-0267161 A1	29/10/2009	US 2011-0291192 A1 US 8022487 B2	01/12/2011 20/09/2011
US 2011-0024841 A1	03/02/2011	US 2009-0283806 A1 US 7829401 B2 US 8193592 B2	19/11/2009 09/11/2010 05/06/2012
KR 10-2012-0020062 A	07/03/2012	EP 2423953 A1 JP 2012-049286 A US 2012-0052664 A1 US 9023720 B2	29/02/2012 08/03/2012 01/03/2012 05/05/2015