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(71) Applicants *(for all designated States except US)*: **UNIVERSITAT POLITECNICA DE CATALUNYA** [ES/ES]; C. Jordi Girona, 31, E-08034 Barcelona (ES). **UNIVERSITAT AUTONOMA DE BARCELONA** [ES/ES]; Edifici A - campus universitari s/n, 08193 Barcelona (ES).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **GARCIA ALMUDEVER, Carmen** [ES/ES]; Universitat Politecnica De Catalunya, C. Jordi Girona, 31, 08034 Barcelona (ES). **RUBIO SOLA, Antonio** [ES/ES]; Universitat Politecnica De Catalunya, C. Jordi Girona, 31, 08034 Barcelona (ES). **CRESPO YEPES, Albert** [ES/ES]; Universitat Autonoma De Barcelona, Edifici A - campus universitari s/n, 08193 Barcelona (ES). **MARTIN MARTINEZ, Javier** [ES/ES]; Universitat Autonoma De Barcelona, Edifici A - campus universitari s/n, 08193 Barcelona (ES). **NAFRIA MAQUEDA, Montserrat** [ES/ES]; Universitat Autonoma De Barcelona, Edifici A - campus universitari s/n, 08193 Barcelona (ES). **RODRIGUEZ MARTINEZ, Rosana** [ES/ES]; Universitat Autonoma De Barcelona, Edifici A - campus universitari s/n, 08193 Barcelona (ES).

(74) Agent: **TORNER LASALLE, Elisabet**; Gran Via de les Corts Catalanes, 669 bis, 1r. 2a, E-08013 Barcelona (ES).

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(54) Title: METHOD FOR OPERATING A TRANSISTOR, RECONFIGURABLE PROCESSING ARCHITECTURE AND USE OF A RESTORED BROKEN DOWN TRANSISTOR FOR A MULTIPLE MODE OPERATION

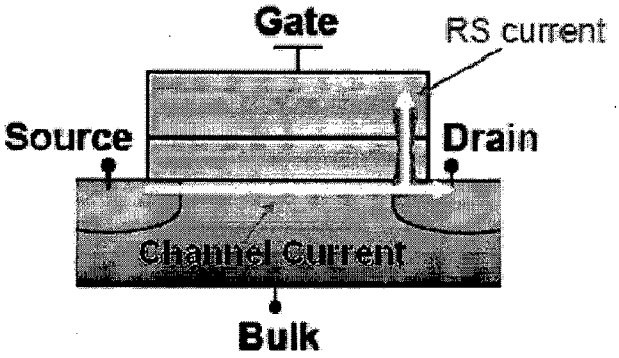

Fig. 5

(57) Abstract: The method comprises operating a transistor as per a conventional mode, after reversibly breaking the transistor dielectric, and according to a second mode based on the creation of a closable resistive switching path through the transistor dielectric and employed for using the transistor as a non volatile memory and/or as a multi-switch element. The reconfigurable processing architecture comprises a plurality of reconfigurable transistors and a control unit intended to reconfigure them to make them work according to said conventional mode and/or said second mode of operation. The architecture is flexible and not fixed as happen in conventional computers but adapts the size and composition dynamically. The use includes, simultaneously or selectively, using the transistor for implementing logic functions, non-volatile memory functions and/or for implementing a controlled multidirectional switch.

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Method for operating a transistor, reconfigurable processing architecture and use of a restored broken down transistor for a multiple mode operation

Field of the art

The present invention generally relates, in a first aspect, to a method for operating a transistor, and more particularly to a method allowing selectively operating a transistor as per a conventional mode, after reversibly breaking the transistor dielectric, and according to a second mode based on the creation of a closable resistive switching path through the transistor dielectric and employed for using the transistor as a non volatile memory.

A second aspect of the invention relates to a reconfigurable processing architecture, comprising a plurality of reconfigurable transistors, and intended to reconfigure them to make them work according to said conventional mode and/or said second mode of operation of the method of the first aspect.

A third aspect of the invention relates to a use of a restored broken down transistor for a multiple mode operation, including, simultaneously or selectively, using the transistor for implementing logic functions, for implementing non-volatile memory functions and/or for implementing a controlled multidirectional switch.

Prior State of the Art

Several kinds of transistors are usually operated according to conventional modes by applying different electrical signals at their terminals in order to create a conductive channel between a first and a second of said terminals, through a semiconductor substrate, and make a channel current to flow there through.

Depending on the type of FET transistor (MOSFET, etc.), the electrical signals applied to their terminals are current signals and/or voltage signals.

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a fundamental device in CMOS integrated circuits [4]. Fig. 3 shows the MOSFET structure. The main body of the device is a Metal-Oxide-Semiconductor capacitor. At each side of the MOS capacitor two highly doped regions are implanted (Drain and Source). Then, the MOSFET has four terminals and the current collected at the drain, that is called the drain current, is controlled by the voltage applied to the gate and drain contacts.

If a voltage with the adequate polarity is applied between gate and bulk, the electric field creates an inversion layer of carriers (channel) close to the interface between the semiconductor and the insulator. The inversion layer provides a channel through which current can flow if a voltage is applied between drain and source. Varying the voltage between the gate and bulk the conductivity of this layer is modulated and allows controlling the channel current.

On the other hand, the ultimate non-volatile memory devices (NVM) should present characteristics such as high-density and low cost, fast write and read access, low energy operation and high performance with respect to endurance (write cyclability) and retention. Until now, Si based Flash memory devices represent the most prominent NVM because of their high density and low fabrication costs. However, Flash devices suffer from low endurance, low write speed and high voltages required for the write operations. In addition, further scaling, i.e. a continuation in increasing the density of Flash is

expected to run into physical limits in the near future. On the other hand, ferroelectric random access memory (FeRAM) and magneto resistive random access memory (MRAM) are focused on special applications because, among different reasons, exhibit technological and inherent problems in the scalability, i. e. achieving the same density as Flash today. To overcome the problems of current NVM, a variety of alternative memory concepts is explored. Recently, the resistive switching (RS) based resistive random access memory (RRAM) is one of the most promising candidates for emerging NVM and crossbar logic concepts. Attractive properties of RRAMs are low fabrication costs, scalability into the nanometer range, fast write and read access, low power consumption and low threshold voltages.

The Resistive Switching effect:

The resistive switching (RS) phenomenon is observed in capacitor structures as Metal-Insulator-Metal (MIM) and Metal-Insulator-Semiconductor (MIS) structures [1,2,3]. The 'M' in MIM denotes any reasonable good electron conductor, often different for the two sides, and the 'I' stands for an insulator, typically rare earths materials with thicknesses around tens of nanometers (Fig. 1). These two terminal resistive switching devices (2-t RSD) can switch between a high conductivity state 'ON state' and a low conductivity state 'OFF state', by applying adequate voltages, and controlling the flow of the current between the two terminals of the structure (gate and bulk). In some materials, switching has a filamentary character, which means that the current mainly flows through a small area of the insulator (from now on we call to this area the RS path, and the current through it the RS current, Fig. 1).

The switching between both states can be achieved, for example, by applying ramp voltages to the device (Fig. 2), and limiting the maximum current through the device in the transition between the OFF and ON states. When the voltage reaches critical values, the dielectric changes the state from ON to OFF or OFF to ON. That is, the other state is 'written' in the device. If the voltage is kept below the 'writing' voltages, the conductive state remains stable, and it is possible to 'read' it without changing to the other state.

US2003112055A1 discloses an anti-fuse circuit, which uses a transistor to provide two detected states, an un-programmed state where the transistor operates as a normal transistor and a programmed state which is achieved by forcing a normal transistor to conduct current through its gate, i.e. by permanently breaking its dielectric. Due to the permanent nature of said dielectric breaking, once in the programmed state, the transistor is a degraded device that cannot go back to the un-programmed state. Said dielectric breaking is provided between gate and drain, gate and source or both at a time, and, obviously, its permanent nature does not allow using said transistor as a switch but as a fuse, as no return for the created dielectric conductive paths to a non-conductive state is possible once the dielectric is broken.

An application for said anti-fuse circuit relates to the implementation of a function such as redundancy in a memory, providing the anti-fuse circuit, not the memory storing entities, but interconnection paths (when in the broken dielectric state) between memory storing entities which are not disclosed by US2003112055A1.

US2003112055A1 further discloses the interconnection of several of the anti-fuse circuits to provide a kind of interconnection architecture.

US2003112055A1 does not disclose to use a transistor to implement logic functions, while the memory functions implemented by the proposed anti-fuse circuit are only related to the above mentioned interconnection functions, not related to storing functions.

Nor selection between two possible states is also possible for the anti-fuse circuit of US2003112055A1 once the dielectric has been broken.

Clearly said permanent dielectric breaking has nothing to do with the above mentioned resistive switching phenomenon.

US20100008132A1 discloses a resistance memory element formed by an alike MIM structure joined to a transistor. Said alike MIM structure is formed by a sandwich of three layers: a first conductive layer, or word line, a resistance switching layer and a second conductive layer, or bit line. Said bit line is placed onto a substrate channel region of the transistor, whether directly or through an intermediate isolating layer, depending on the embodiment, the conductive layer of said bit line acting also as the transistor electrode.

The RS phenomenon of said alike MIM structure is not local, as the resistive state of the intermediate resistive switching layer uniformly distributed there along.

No RS phenomenon appears in the transistor isolating layer, but in the alike MIM structure intermediate resistive switching layer, thus no current circulating through said intermediate switching layer goes to the source, drain or bulk of the transistor.

US20100008132A1 further discloses to implement a memory array structure by interconnecting several of the proposed memory elements, with their drains and/or sources interconnected, thus not allowing using individual drain and/or sources of each transistor independently from other transistor drains and/or sources.

No reconfigurable processing structure formed by elements which implement logic functions is disclosed in US20100008132A1, as the memory elements disclosed therein only provide memory functions.

US2008106926A1 relates to an integrated circuit memory cell which, for some embodiments, includes a FET transistor and a layer of a variable resistance material (VRM) directly above the FET channel or via an intermediate insulating layer.

The resistive phenomenon appearing in the VRM layer is not local, i.e. does not provide a local conduction path there through, but provides a uniformly distributed resistance there along, being thus the memory cell provided able to store only one bit.

For the embodiment for which said VRM is placed directly over a MESFET channel and an upper electrode is placed over the VRM layer (see US2008106926A1 Fig. 12), no local conduction channel is provided between said upper electrode, the VRM layer and one of the source, drain or substrate of the MESFET, the reading of the memory state of the VRM layer being performed by monitoring its effects on the transistor conduction channel between source and drain which, for a certain voltage applied at the upper electrode, will conduct a higher or lower current depending on the VRM resistance value.

No other use for the memory elements disclosed by US2008106926A1 regarding functions other

than those related to memory functions is disclosed therein.

US2008106926A1 further discloses to implement a memory circuit formed by an array of the proposed memory elements, constituting a two-terminal crossbar which only implements memory functions. No logic functions at all can be implemented by said crossbar, neither by the memory elements themselves nor by any other entity included therein.

The above described resistive switching phenomenon observed in capacitor structures has also been studied in transistor structures, where such phenomenon, or a similar one, has been caused in the transistor gate dielectric in a controlled manner in order to create a closable RS channel, by means of a reversible dielectric breaking.

[15] and [16] disclose some of said studies, particularly focused on the gate dielectric breakdown (BD) reversibility in MOSFETs with ultra-thin high-k dielectric. The dielectric is reversibly electrically broken by applying a current limited voltage stress, thus creating a kind of closable conductive path, or RS path, which can be `opened' and `closed' many times, the BD recovery partially restoring not only the current through the gate, but also the MOSFET channel related electrical characteristics.

Both [15] and [16] are focused on reliability issues referring to how the normal operation of the MOSFET is affected because of the deterioration of its channel electrical characteristics after the reversible dielectric breakdown.

In [15] is simply concluded that the restoration of the MOSFET performance could have an impact in the circuit functionality, which will have to be analysed to make accurate reliability predictions, while in [16] a step beyond is taken by testing circuit functionality implementing different circuits with MOSFETs with such a partially restored channel current characteristics, showing that for some circuits (ring oscillator) the functionality of the circuit is restored but damaged, while for others (logic gates) the obtained results are the same than before breaking their dielectrics.

Although [16] suggests operating the restored MOSFET for a normal transistor operation, i.e. that associated to the conduction through the restored channel, for at least some circuits, neither [16] nor [15] teach to further use the conduction through the closable RS path for any function, as said RS path is created, opened and closed only with the purpose of studying its impacts on the channel electrical characteristics, i.e. on reliability matters.

Particularly, neither [15] nor [16] disclose to use the created closable RS path to provide a memory state, nor to any method for writing/reading a memory bit in said RS path.

The present inventors don't know any proposal disclosing the operation of a transistor according to different modes, including the above referred as conventional mode and a further operation mode based on said resistive switching phenomenon, and the employment of the latter for using the transistor as a non volatile memory.

One of the main applications or uses of transistors is their inclusion, in a high number, in processing architectures.

Today the advanced and promising computing industry, at all levels, from laptops to supercomputers, is based on the existence of complex and sophisticated monolithic integrated circuits

implemented through circuits formed by billions of MOS [5] transistors. The architecture or organization of such devices, usually called microprocessors, is the result of years of research and experience. Microprocessors behave as general machines in such a way that through the use of programming languages they can be applied to unlimited number of data process applications. The fixed architecture of the microprocessor device is oriented to execute such programs with a high level of efficiency. For a given computer the flexibility in the application domain is based on the programming capability, and because of this the programs are also called software while the physical implementations of the integrated circuits are called hardware. The first electronic computers were developed in the mid-20th century (1940-45) while the invention of the integrated circuits corresponds to 1958. It is important to indicate that the adaptability, the flexibility of computers to specific applications is based on the software, while the hardware is fixed.

High performance microprocessors are based on specific and sophisticated architectures implemented on silicon integrated circuits [6]. Through the principles of semiconductor devices with a finely calculated and fixed size, distribution and interconnection of a complex network of MOS transistors the processor is configured at the design time. Consequently the high performance processors are based on a fixed hardware organization. As an alternative to integrated circuits with a fixed organization a new idea was developed under the name FPGA (Field Programmable Logic Arrays) devices, based on the use of fuse devices first and electrically erasable transistors. The first patents related with this new concept are dated in 1980 but most of the industry's foundational concepts and technologies for FPGAs are founded in patents awarded to David W. Page and LuVerne R. Peterson in 1985 [7]. The FPGAs contain a huge number of pre-defined logic blocks with a hierarchy of reconfigurable interconnects that allow the blocks to be wired among them following the indications of designers or CAD tools given as a result a specifically oriented final configuration. The 1990s were an explosive period of time for FPGAs, both in sophistication and volume of production. In the early 1990s, FPGAs were primarily used in telecommunication and networking. By the end of the decade, FPGA found their way into consumer, automotive, and industrial applications.

The appearance of new electronic devices has been always the motivation of new architectural solutions and paradigms. First, the invention of the Metal Oxide Semiconductor transistors together with the discovering of the integrated circuits by Jack Kilby from Texas Instruments concluded in the implementation of integrated circuits with fixed structure and function. Later the appearance of the new devices fuses and non-volatile electrically erasable transistors produced the flexible FPGAs.

New devices are nowadays being investigated, mainly oriented to what is called unified memory devices (non-volatile, highly dense). Among them the most promising are the based on the Resistive Switching (RS) effect [8]. The devices that exhibit this phenomenon (RS devices) could be used in huge crossbar structures. Overlaying two nanowire electrode arrays perpendicularly, a RS device is located at each crosspoint or junction. Furthermore, each crosspoint can be independently configured in a non-volatile low or high impedance state by applying appropriate voltages in the respective bar extremes. The device can be configured easily and can be read through any mechanism of resistance evaluation. So, it is a promising device for future memories. Perhaps the main exponent of these RS devices is the exposed in the recent works of Stanley Williams [9] from Hewlett Packard. One of the recognized drawbacks of these devices is that although they are the basis of a new promising type of non-volatile memories, it is not

possible to use them for computing purposes, because several fundamental logic functions, as just the logic inversion, cannot be implemented with only RS devices. In recent papers [13][14] the team from Hewlett Packard is showing the potential of implement logic functions by using hybrid structures of RS/CMOS devices, but always as separate elements.

Today's computational integrated circuits, both full-custom high performance or reconfigurable FPGA types, are based on a pre-defined and fixed organization of processing entities that collaborate in the computing tasks. These entities are physically distributed through the entire surface of the integrated circuit in a fixed manner. Hence, each one of the entities that form the integrated circuit is characterized by a specific and fixed characteristic (e.g. the number of stored words in a memory, the number of core units, the number of I/O sections...).

None of the above cited patent documents discloses a reconfiguration architecture formed by transistors which are capable of providing both, logic functions and memory functions, and are controllable to selectively implement at least one of said logic functions and/or memory functions.

Description of the Invention

It is necessary to offer an alternative to the state of the art which covers the gaps found therein, particularly those referring to the under-use of transistors when operating them only according to the above described conventional mode, and those referring to the lack of flexibility current reconfigurable processing architectures suffer from.

To that end, the present invention provides, in a first aspect, a method for operating a transistor, comprising:

- reversibly electrically breaking the dielectric of said transistor in a controlled manner for creating a closable resistive switching path to appear there through while at least partially restoring the channel electric properties of said transistor, at least when said resistive switching path is closed, and

- using said transistor according to a first mode of operation, once said transistor channel electric properties are at least partially restored, by applying a first set of electrical signals at at least part of the terminals of said transistor in order to create a conductive channel between a first and a second of said terminals, through a semiconductor substrate, and make a channel current to flow there through.;

On contrary to the conventional methods for operating a transistor, the method of the invention further comprises, in a characteristic manner:

- using said transistor according to a second mode of operation by applying a second set of electrical signals at at least part of the terminals of said transistor in order to open said created resistive switching path and make current to flow locally through said dielectric between a third terminal and said first, second or another of said terminals, and

- employing said second mode of operation for using said transistor as a non volatile memory, where said resistive switching path represents a memory bit having a value with a certain logic state (such as 1) or with a logic state (such as 0) complementary to said certain logic state, depending on at least the value of the current circulating there through.

Depending on the embodiment, the method comprises selecting using said transistor according to one of said first and second modes, or according to both of said first and second modes.

According to an embodiment, said resistive switching path is a first resistive switching path, and said second mode of operation further comprises applying at least a third set of electrical signals at at least part of the terminals of said transistor in order to create at least a second resistive switching path and make current to flow locally through said dielectric between said third terminal and another of said terminals not involved in said first resistive switching path.

For other embodiments the second mode of operation of the method comprises applying further sets of electrical signals at at least part of the terminals of the transistor in order to create further corresponding resistive switching paths and make current to flow locally through the dielectric between the third terminal and another of the terminals not involved in said first and second resistive switching paths.

The method of the first aspect of the invention comprises, for an embodiment, employing said second mode of operation for using said transistor as a non volatile multibit memory, where each of said resistive switching paths represents a memory bit having a value with a certain logic state or with a logic state complementary to said certain logic state, depending on at least the value of the current circulating there through.

The method of the first aspect of the invention comprises, as per an embodiment, controlling said sets of electrical signals in order to control the opening/closing of the resistive switching paths, their location and the values and directions of said current flows.

As per the reading of the transistor memory states, the method comprises, for an embodiment, carrying out said control such that said channel current flow is substantially null and reading each memory bit value by measuring the respective resistive switching path current value at a terminal of the transistor where said current flows.

For an alternative embodiment, the method comprises carrying out said control such that the channel current flow is not null and reading each memory bit value by measuring the combined current resulting from the combination (such as the subtraction or addition) of the respective resistive switching path current and the channel current, at a terminal of the transistor where said current combination is produced.

As per the control according to said alternative embodiment, the method comprises at least the next two manners of performing it:

- create a channel current with a value lower than the value of said resistive switching path current, such that the combined current values at said terminal of the transistor are of the same sign for both, an ON state representing a memory bit value with a certain logic state and an OFF state representing a memory bit value with a logic state complementary to said certain logic state, or

- create a channel current with a value higher than the value of said resistive switching path current when in an OFF state, and lower than the value of said resistive switching path current when in an ON state, such that the combined current values at said terminal of the transistor are of different signs for said ON state, representing a memory bit value with a certain logic state, and said OFF state, representing a memory bit value with a logic state complementary to said certain logic state.

As per another embodiment, the method of the first aspect of the invention comprises employing said second mode of operation for using the transistor, instead or complementarily to as a non volatile memory, as a controlled multidirectional switch between the third terminal and two or more of the other transistor terminals, where:

- at least a single connection of the third terminal and at least one of the other terminals being provided, the method comprising selectively controlling the switching ON/OFF and location of said single connection, or

- a first connection between the third terminal and one of the other terminals and at least a second connection between the third terminal and another one of the other terminals, i.e. several parallel connections being provided, the method comprising controlling the simultaneous switching ON/OFF of said first and second connections.

The method of the first aspect of the invention comprises, for an embodiment, selecting employing said second mode of operation for using the transistor as said non volatile memory and/or as said multidirectional switch.

Depending on the embodiment, the transistor is a Field Effect Transistor (FET) such as a MOSFET with a single gate, a multigate transistor (such as a FINFET) or a CNTFET, with a material with resistive switching properties.

For a preferred embodiment, the transistor operated according to the method of the first aspect of the invention is a MOSFET with a dielectric with resistive switching properties, said first, second and third terminals corresponding, respectively, to the source, drain and gate of said MOSFET, the above referred as electrical signals being voltage signals, and each of said one or more resistive switching paths passing only:

- through gate, dielectric and source, or
- through gate, dielectric and substrate, or
- through gate, dielectric and drain.

Contrarily to the memories based purely in the RS effect, where the fabrication process could not be compatible with the CMOS standard process due to the use of rare earths and thick oxides, the transistor used according to the method of the first aspect of the invention is, for an embodiment, a standard MOSFET with ultra-thin high-k material as gate dielectric. No especial characteristics of the transistor (gate electrode, oxide thickness, dimensions...) are required to observe the RS phenomenon in them. Therefore, the device can be fabricated using state of the art high-performance logic CMOS technology.

Although in the previous description of several embodiments, operation modes have been denominated as first mode for the conventional mode of operating a transistor, i.e. a transistor mode, and as second mode for referring individually to all the possible new operation modes, a different manner of referring to said new operation modes is that of calling the 1 bit non volatile memory as second operation mode, the multibit non volatile memory as third operation mode and the controlled multidirectional switch as fourth mode, the method comprising to use the transistor to make it operate according to part or all of said operation modes, individually or at a time.

A second aspect of the invention concerns to a reconfigurable processing architecture, comprising:

- a plurality of transistors for implementing required logic functions,
- a plurality of resistive switching elements for implementing memory functions, and
- a control unit for controlling said transistors and resistive switching elements.

On contrary to conventional reconfigurable processing architectures, and particularly to the above indicated HP hybrid structures of RS/CMOS devices, in the reconfigurable processing architecture of the second aspect of the invention said transistors are intended for implementing both, said required logic functions and said memory functions, said resistive switching elements being provided by said transistors, as the latter have respective reversibly electrically breakable dielectrics each providing, after being reversibly broken in a controlled manner, at least one closable resistive switching path to appear there through while at least partially restoring the channel electric properties of the respective transistor, at least when said at least one resistive switching path is closed, and said control unit is intended for, once said dielectric reversible breaking has been caused, selecting and controlling at least part of said transistors for making each of them work according to first and second modes of operation, at least one mode at a time, by means of:

- regarding said first mode of operation, once said transistor channel electric properties are at least partially restored, applying a first set of electrical signals at at least part of the terminals of each selected transistor in order to create a conductive channel between a first and a second of said terminals, through a semiconductor substrate, and make a channel current to flow there through, where said first mode of operation comprises using the transistors for said required logic functions implementing; and
- regarding said second mode of operation, applying a second set of electrical signals at at least part of the terminals of each selected transistor in order to open said at least one created resistive switching path and make current to flow locally through said dielectric between a third terminal and said first, second or another of said terminals, said control unit being intended for employing said second mode of operation for using each selected transistor as a non volatile memory, where said at least one resistive switching path represents a memory bit having a value with a certain logic state or with a logic state complementary to said certain logic state, depending on at least the value of the current circulating there through.

Depending on the embodiment said transistor dielectrics are already reversibly broken (each providing at least one of said closable resistive paths) when the architecture is built, or they are broken in an initial phase of use of the architecture or when required, individually, by groups or all of them at the same time.

According to an embodiment, said control unit is also intended for employing said second mode of operation for using each selected transistor as a controlled multidirectional switch between said third terminal and at least two of the other transistor terminals, by connections provided by respective closable resistive switching paths, the control unit being in charge of selecting if employing said second mode for using each selected transistor as a non volatile memory or as a controlled multidirectional switch.

For an embodiment, the control unit of the reconfigurable processing architecture implements the method of the first aspect to control and supply said sets of electrical signals to make each selected transistor work in said first and/or second modes of operation.

According to an embodiment, the control unit is intended for controlling said sets of electrical signals, to select transistors and dynamically modify the mode of operation they work between said first and second modes, as a function of instantaneous computing requirements and/or in order to correct possible malfunctioning of some parts of the processing architecture, the control unit being arranged for sensing the processing architecture performance in order to carry out said dynamic modification.

For another embodiment the control unit is intended for controlling the sets of electrical signals to select transistors and dynamically making them stop working, as a function of instantaneous computing requirements and/or in order to correct possible malfunctioning of some parts of the processing architecture, the control unit being arranged for sensing the processing architecture performance in order to carry out said working stop.

The reconfigurable processing architecture comprises, for an embodiment, a library registering several possible logic and memory entities to be mounted, and the control unit has access to said library and is intended:

- to replicate each of said entities, on an architecture board, by selecting corresponding transistors and making them work according to said first mode and/or second mode of operation; and
- to dismount each of said entities by selecting corresponding transistors and making them stop working.

Said logic entities include, for an embodiment, entities implementing negate Boolean functions.

By means of the invention as per its second aspect, a new architecture principle self-adaptive to the data requirements is presented, representing a new computing and organizational architecture paradigm or new operative computer organization oriented to execute computing tasks in a dynamic, flexible, efficient and adaptive way taking into account the processing needs that are being executed in each moment. The space distribution of the processing entities is not fixed but oriented to satisfy the instantaneous needs of computation, being modified dynamically and managed by a control unit through the selective supply of the transistors forming the architecture.

A third aspect of the invention concerns to a use of a restored broken down transistor for a multiple mode operation, where said restoration relates to the at least partially restoring of the transistor channel electric properties after reversibly electrically breaking the dielectric of said transistor in a controlled manner for creating a closable resistive switching path to appear there through, said multiple mode operation including, simultaneously or selectively:

- using the transistor for implementing logic functions based on the conduction state of a conductive channel created through a semiconductor substrate of the transistor, and
- using the transistor for implementing non-volatile memory functions based on the conduction state of said resistive switching path created in the transistor dielectric.

Said multiple mode operation further includes, for an embodiment of the use of the third aspect of the invention, selectively or simultaneously with said logic functions use and non-volatile memory functions use, using the transistor for implementing a controlled multidirectional switch also based on the conduction state of said resistive switching path created in the transistor dielectric.

Brief Description of the Drawings

The previous and other advantages and features will be more fully understood from the following detailed description of embodiments, with reference to the attached drawings (some of which have already been described in the Prior State of the Art section), which must be considered in an illustrative and non-limiting manner, in which:

Fig. 1 shows a MIM or MIS structure with the RS effect, for an ON state, left view, where the current flowing through the RS path is high, and for an OFF state, right view, where the RS current is low;

Fig. 2 is a graph showing ramp voltages applied to change the state of the device of Fig. 1, where the transition between the ON-OFF or OFF-ON states can be detected, respectively, as a high decrease or increase of the gate current;

Fig. 3 shows a MOSFET structure, which four terminals allow controlling the current that flows from source to drain, i.e. the channel current;

Fig. 4 shows, by means of a graph, the typical channel currents measured in a MOSFET as a function of the drain-source voltage for three different gate voltages;

Fig. 5 shows a MOSFET used according to the method of the first aspect of the invention, for an embodiment, in which the RS effect can be observed, so that two currents due to two different mechanisms are present in the transistor, the current due to the RS effect (RS current) and the channel current, both of said currents being controlled by the method of the invention by applying the adequate voltages to the MOSFET terminals;

Fig. 6 shows a MOSFET used according to the method of the first aspect of the invention, for another embodiment, where the transistor is used as a 1 bit memory element, and according to a first reading method, a null channel current is forced, and the memory state is read from the RS current;

Fig. 7 shows the reading window obtained using the first reading method of Fig. 6, said reading window being similar to the one corresponding to the MIM structure represented in Fig. 1;

Fig. 8 shows also a MOSFET used according to the method of the first aspect of the invention, for another embodiment, where the transistor is used as a 1 bit memory element, like in Fig. 6, but for a second reading method where a low channel current is forced, lower than the RS current at the OFF state, and the read operation is done in the drain terminal, where the difference of both currents difference is measured;

Fig. 9 shows the reading window obtained using the first and the second reading methods of Figs. 6 and 8 respectively, where it can be observed that in the second reading method, the forced channel current reduces the current measured at the OFF state respect the first reading method, whereas it has negligible effects in the ON state; therefore, an enlargement of the reading window is obtained;

Fig. 10 shows the reading window obtained using a third reading method, for which a channel current higher than the RS current at the OFF state but lower than the RS current at the ON state is forced,

which makes that the memory state is distinguished by the sign of the current at the drain terminal. In addition, at the OFF state the current is dominated by the channel current, that has lower dispersion;

Fig. 11 shows a MOSFET used according to the method of the first aspect of the invention, for an embodiment, in which the device is used as a multibit non-volatile memory by creating several RS paths through the dielectric thereof;

Fig. 12 is a graph which shows the channel current measured in a transistor in which, according to the method of the first aspect of the invention, two RS paths have been created, one close to the drain and another one close to the source. Four different drain current levels are possible (I1, I2, I3, I4) demonstrating its operation as a 2-bit memory cell;

Fig. 13 shows a MOSFET used according to the method of the first aspect of the invention, for an embodiment, in which several RS paths are created in the transistor (see left view), the current flowing between gate and the terminals where the paths are created, for an operating mode where controlling the state of the RS paths, the transistor is equivalent to a multidirectional/multiplexor switch between gate and the other terminals thereof, as shown schematically in the right view;

Fig. 14 is a graph which shows the electrical characteristics of a MOSFET used according to the method of the first aspect of the invention, but keeping the RS current at the OFF state, where similar curves than standard MOSFETs used according to conventional methods are obtained, which, therefore, if kept at the OFF state, makes the MOSFET able to be used as a standard transistor;

Fig. 15 shows schematically an electronic device including a MOSFET with a gate dielectric of a material with RS properties, and a control unit connected to its terminals to make it operate according to the method of the first aspect of the invention;

Fig. 16 schematically shows the structure of the reconfigurable processing architecture of the second aspect of the invention, for an embodiment;

Fig. 17 shows an example of adaptive computing for the mounting phases of a LIFO memory, implemented with the reconfigurable processing architecture of the second aspect of the invention, for an embodiment;

Fig. 18 shows an example of adaptive computing for the dismount phases of a LIFO memory, implemented with the reconfigurable processing architecture of the second aspect of the invention, for an embodiment; and

Fig. 19 shows, by means of four views, an example of sequential mounting and dismounting phases adapting the capability of the circuit to the data requirements, by means of the reconfigurable processing architecture of the second aspect of the invention, for an embodiment. The Figure shows how the architecture is not fixed as happen in conventional computers but adapts the size and composition dynamically.

Fig. 20 shows the electrical model of a RS path, at view A, and of a memFet, at view B;

Fig. 21 shows at view A a conventional crossbar architecture based purely on 2t-RSDs for memory applications, and at view B a crossbar implementing the reconfigurable architecture of the second aspect of the invention for an embodiment;

Fig. 22 shows several designs obtained by a crossbar implementing the reconfigurable architecture of the second aspect of the invention for several embodiments that exemplify how a crossbar based in memFETs works;

Fig. 23A schematically shows an EHW based on a FPGA, logic and memory entities change from one stage (left view) to other (right view);

Fig. 23B shows the Shapeshifting Evolvable Hardware concept based on a memFET crossbar architecture as per the second aspect of the invention, where different entities (logic gates in this case) are stored in a library, and the HOS is the responsible to mount, dismount or change the position of any block on the computing board in accordance with task requirements; and

Fig.24 shows different examples of application of the SEHW concept, particularly at view A an application of SEHW concept in a LIFO memory is shown, where the elemental blocks of both, the binary counter (1 bit counting unit) and the memory unit (register) are stored in the library, which are mounted or dismounted depending on the input/output data; and at view B an application of SEHW concept in a multi-core system, is shown for which a core and a memory unit are stored in the library.

Detailed Description of Several Embodiments

The method for operating a MOSFET according to multiple operation modes of the first aspect of the invention is represented, for different embodiments, in Figs. 1 to 14, and an electronic device implementing said method by means of a control unit connected to the terminals of the MOSFET is illustrated in Fig. 15.

The transistor used is a MOSFET in which the gate dielectric is a material with RS properties. For example, the RS effect can be observed in standard high-k dielectrics in MOSFETs after their dielectric breakdown (BD) [2]. Therefore, the RS path, which is equivalent to the BD path, is opened electrically controlling the BD event in these layers. As stated above, by properly biasing the transistor, according to the method of the invention, it can be used as a non-volatile memory cell, as a conventional transistor, as a multi-switch or as an electrically reconfigurable logic device.

Fig. 5 illustrates the MOSFET transistor after the resistive switching path has been created. This device will be called hereafter memFET. Two different currents can be distinguished:

1) the typical current between source and drain in a MOSFET (channel current)

2) the current through the RS path (RS current).

The channel and RS currents can be controlled by applying adequate voltages at the device terminals (gate, source, drain and bulk), as per the method of the first aspect of the invention.

The next operation modes can be obtained depending on the voltages applied to the terminals of the MOSFET according to the method of the invention.

- Single bit non-volatile memories operation mode:

Using the RS effect, the memFET can be used for memory applications, to store 1 bit, as in MIS/MIM capacitors. However, the presence of four terminals allows taking advantage of the channel current, which can be used to enlarge and improve the possibilities of reading, as it is explained later.

Writing the memFET acting as a memory element:

The information is written in the memFET as in conventional MIM/MIS capacitors (see Prior State of the Art section). The gate dielectric can be switched between the ON and OFF states applying voltages to the gate, with source, drain and bulk grounded. With this voltage configuration, the RS path is created in a random location of the dielectric of the memFET. For simplicity, in this first application, a unique RS path is considered located between drain and gate, as shown in Fig. 6, to explain the reading process of the memFET.

Reading the memFET:

Due to the availability of four terminals, that allows to force a channel current, the number of possibilities to read the memFET increases with respect to the case of MIM/MIS capacitors. A distinction will be made between three different reading methods depending on the channel current forced: null, low or high. The first one is also possible in MIM/MIS capacitors, whereas the second and the third ones are only possible due to the use of transistors.

Reading method 1: As a MIM/MIS capacitor (null channel current).

In this method for reading a null channel current is forced, setting the same voltage between drain and source. If a voltage V_{read} is set to the gate, there will be a current between drain and gate (a RS path is considered to be located between the drain and gate), as shown in Fig. 6. The current through the gate will be low or high depending on the RS dielectric state, OFF or ON, respectively.

Fig. 7 shows the read current after ten successive switching cycles (writing + erasing) between the ON and OFF states. At the ON state the current is around 1mA– 100uA; at the OFF state the maximum current is less than 1uA. Therefore, the reading window between both states (a key parameter for memory devices, which should be as large as possible) is around 2-3 orders of magnitude, which are typical values in conventional MIM structures based in the RS effect.

Reading method 2: Forcing a low channel current.

In this method, a small voltage difference between drain and source and a voltage at the gate are applied. Thus, the RS current and the channel current are flowing during the reading process, as shown in Fig. 8. In this case, a channel current lower than the RS current during the ON state and comparable to the RS current during the OFF state is forced. The memory-MOSFET state is read from the current at the drain terminal, where the difference between the two currents is measured. Note that the use of the drain current for reading is a different methodology as the used in conventional MIM structures, where the reading process is performed at the gate terminal.

Fig. 9 shows the drain current at the ON and OFF states when the second reading method is applied (crosses). For comparison, the current measured using reading method 1 is also plotted (circles). When using the second method, when at the ON state, the RS current is much higher than the channel current, so that no difference in the ON current measured is observed with respect to the one obtained in the previous method. However, when at the OFF state, with the second method the channel current is lower

but comparable to the RS current. Therefore a lower OFF current is measured when the second method is used for reading. Therefore, if the second method is used for reading, the reading window between the ON and OFF states increases, improving the memory performance.

Reading method 3: Forcing a high channel current.

The last method to read this memory-MOSFET consists in forcing a channel current higher than the RS current in the OFF state but lower than the RS current in the ON state. Under these conditions, the current in the drain terminal has opposite direction (changes its sign) when the device is in the ON or OFF state.

Fig 10 shows the drain current measured using this third reading method. At the ON state the current is around 300uA (same order of magnitude than the one measured using the two previous methods); however at the OFF state the measured channel current is -600nA. Therefore, both states are distinguished by the current sign. Then, with this new method a new technique for the reading process is allowed since typically the memories based on the RS effect discriminate the state from the difference in magnitude of the currents, and not from their sign. Moreover, when using method 1 or 2 the RS current at the OFF state has a high dispersion (200%-300%). With this new method the current at the OFF state is mainly due to the channel current, that has a low standard deviation (25%).

- Multi bit non-volatile memories operation mode.

The use of MOSFET transistors allows implementing a multi-bit non volatile memory cell. The advantage of reading through a high channel current, (change in the current sign and lower dispersion) can be obtained at different RS paths along the channel: between gate and source, gate and bulk or gate and drain (see Fig. 11). The appearance of the RS path in these different locations can be controlled applying the correct voltages to the transistor terminals, as per the method of the first aspect, and can be used to implement a multi-bit memory cell. This increases widely the possibilities of the memFET in front the MIM/MIS capacitors, where the RS path is created randomly and a determined location can not be selected.

Fig. 12 shows the channel current measured in a multi bit non-volatile memFET in which two RS paths have been created, one close to the drain and another one close to the source. Four different drain current levels are possible (I1, I2, I3, I4) and therefore, two bits can be stored in this device.

- Voltage controlled multidirectional switch/multiplexor operation mode.

The generation of different RS paths in a MOSFET transistor is used, for an embodiment of the method of the invention, to implement a multidirectional switch between gate and source, gate and bulk or gate and drain. The current flows through the gate and the terminals which have the RS path at the ON state, as Fig. 13 shows, providing several (in this case three) possible connections, to be established at a time, individually or in any possible combination of two connections. Again, the use of memFETs increases the possibilities respect the MIM/MIS capacitors where only one switch can be obtained.

- Transistor operation mode.

When all the RS paths are kept at the OFF state for an embodiment of the method of the first aspect of the invention or of the electronic device of the second aspect, the memFET used shows the behaviour of a typical MOSFET. Hence, if the RS paths remain at the OFF state it can be used as a standard MOSFET with the same applications. Fig. 14 shows the I_D-V_{DS} characteristics of the transistor of the electronic device when its RS paths are kept at the OFF state. In this case, similar I_D-V_{DS} dependences than in standard MOSFETs are measured.

The method of the first aspect of the invention has many applications, including those which require circuitry including elements operating as transistors, memory elements and/or multi-switches, and particularly for those which require the same elements to carry out, under control, at least two of the above mentioned operation modes, individually or at a time, which provides a new type of reconfigurable circuitry unknown up to now, which can transform in part the functions provided by an electronic circuit, or even transform completely the main functions of such a circuit just by applying different sets of voltages to the transistors it includes, as it could be for example the case of a memory board transformable into a switch board, or vice versa.

The reconfigurable processing architecture of the second aspect of the invention, described in a previous section, takes advantage of the use of transistors controlled as per the method of the first aspect, being therefore an application of particular interest.

For an embodiment, said architecture is a highly-scaled system, where the MOSFET transistors in which the RS effect takes place are used, according to the method of the first aspect, in adaptive computing architectures that use the crossbar logic concepts.

In that case, a memFET is located in each crosspoint and can be dynamically and electrically configured as memory cell, multidirectional switch or transistor, as per the method of the first aspect of the invention. Another advantage of using memFETs transistors instead of MIM/MIS capacitors in the crossbars is that the correct combination of nMOS and pMOS memFETs in the array allows obtaining the negative logic with CMOS technology completely integrated in the architecture. The integration of the memFETs in the crossbar makes possible to implement the logic inversion. Therefore, complex systems can be built by replicating the same kind of device and electrically configuring it as needed, which simplifies their fabrication process.

For circuit design applications, the RS path can be electrically modelled as a voltage controlled switch, with a control voltage equal to the voltage that drops at the RS-path, in the form of a RS path model as shown at Fig. 20A. The ON and OFF switch resistances and threshold voltages can be easily obtained from IGS-VGS characteristics.

A MOSFET transistor in which a RS path has been created can be electrically modelled by connecting the RS path model between the gate and the terminal/s where the RS path/s is/are located, as shown in Fig. 20B for a p-type MOSFET. This memFET model can accurately reproduce the memFET electrical characteristics at the OFF and ON states when introduced in a circuit simulator.

In Figs. 21 and 22 the memFET model of Fig. 20B is used to represent the memFETs included in

the crossbars there illustrated.

Fig. 21A shows a conventional crossbar architecture based purely on 2t-RSDs for memory applications, while Fig. 21B shows a crossbar implementing the reconfigurable architecture of the second aspect of the invention, including memFETs, which, as previously shown, offers additional operation modes compared to 2t-RSDs, and can thus be used to optimize the circuit design, including not only increasing its storage capacities, as multi-bi cells, but also due to their increased functionalities opening the possibility of extending the concept of RSDs based crossbar to more advanced architectures, since the inclusion of memFETs in a crossbar also adds computation and multi-switch capabilities to the structure.

For the embodiment of Fig. 21B, the memFETs are interconnected by voltage controlled switches, which will be opened or closed to define the operations performed by the structure. These switches can be fabricated with the same technology as that of the memFETs and would be activated or deactivated using an auxiliary crossbar (zoom in Fig. 21B). Each memFET can be used as a standard MOSFET transistor, when all the RS paths are in the OFF state, so that logic circuits can be implemented in the crossbar. The same device can be used as a n-bit memory cell or n-directional switch, if one or more RS paths are created.

A block of eight memFETs (four P type and four N type, with RS paths located at drain and source) arranged in a bi-dimensional crossbar structure (shaded in grey in Fig. 21B), allows to configure the basic logic operations (NAND, NOR and NOT). The connection of different blocks increases the capability of logic computation and information storage.

Fig. 22 shows several designs that exemplify how a crossbar based in memFETs works. In Fig. 22A the switches in the block are configured to build a NOR gate. The interconnected memFETS are used as MOSFETs (i.e., all the RS paths are OFF), whereas those memFETs that are not involved in the logic operation (enclosed in grey rectangles) can be used as memory cells.

Fig. 22B shows two blocks of eight memFETs designed to implement a AND operation. This is done by configuring the first and the second eight-memFETs blocks as NAND and NOT gates, respectively, and using the multidirectional switch function of one of the memFETs (enclosed in a grey oval) in which one RS path is at the ON state to connect the NAND output to the NOT input. In this case, 9 memFETs (enclosed in grey rectangles) can be used as memory cells.

In Figs. 22A and 22B the shaded lines show the memFET connections.

These two examples illustrate that a crossbar made of memFETs allows performing logic computation, with simultaneous storage capability, without changing the repetitive structure concept introduced by the 2t-RSDs crossbar. Since a unique device (same architecture, same fabrication technology) is used in the 4t-RSD crossbar structure, the fabrication process is considerably simplified.

The crossbar of Fig. 22 is a crossbar supplying the above mentioned sets of electrical signals at the source, drain gate and bulk of the selected memFETs from the crossbar terminals, in this case through the voltage controlled switches, although for another embodiment said supplying is performed by different means.

For other embodiments the crossbar has a number of terminals different from four.

The multiple operation modes of the memFETs also add reconfiguration properties to the crossbar. To show this point, the operation of a 8-memFET block (as that shaded in grey in Fig. 21B) has been simulated, whose configuration is sequentially changed to work as different logic gates. To describe the memFETs behaviour, an electrical model presented in Fig. 20B has been introduced in a circuit simulator. Fig. 22C shows the transient simulation of the block output. The configuration of the block has been sequentially modified at 2ms, 6ms, 12ms and 16ms to build a NOT, NAND, NOR logic gates and a connection stage, respectively. Additionally, the block can store information. After these times, a short time interval (marked with grey rectangles) is reserved to change the operation mode of the block (by opening/closing the adequate switches and selecting the memFETs operation modes) and for the writing or reading process of the memFETs acting as memory cells. The number of available bits that each 8-memFET block is store at any moment of the simulation is also indicated in Fig. 22C, and has been determined by multiplying the number of memFETs that are not involved in the logic gate by the number of bits that each memFET can store (n).

Fig. 16 shows the basis of the structure of the reconfigurable processing architecture of the second aspect of the invention, for an embodiment assuming a large planar bi-dimensional crossbar structure, indicated as architecture board AB, where in each cross point there is a hybrid RS/CMOS device (MOSFET with dielectric providing the RS phenomenon), which are non-volatile devices programmable through voltage excitation actions caused by an internal section, implemented in the circuit that is called HOS (Hardware Operating System), and which was called in a previous section as control unit.

The HOS is able to replicate or mount any specific logic entity from a set called LIBRARY (see Fig. 16) to any point of the architecture board (AB) thanks to the flexibility of the hybrid RS/CMOS device, indicated as basic device in Fig. 16, with no more limit that the dimension of the global circuit. The HOS configures the computing architecture in the AB through the dynamic "mounting" of entities, depending on the computing requirements. The HOS is able also to dismount or erase blocks in the dynamic reconfiguration sequences, adapting the computing architecture to the instantaneous data requirement. The ability of mounting or dismounting entities is based on the RS/CMOS electrical reconfiguration principles.

The HOS adapts the architecture to the computational requirements. One of the complementary advantages of the reconfigurable processing architecture of the second aspect of the invention is based on the capability to reconfigure the circuit in the AB in case of manufacturing defects in certain cross point. The new paradigm provided by the invention extends the flexibility of the software to the architecture level, allowing a higher efficiency of the circuit in case of different computing tasks or loads.

EXAMPLE OF APPLICATION (I)

Figs. 17 and 18 show an example of application, or embodiment, of the architecture of the second aspect of the invention, consisting of a simple LIFO (Last Input, First Output memory) represented by a register unit and a counter unit.

Fig. 17 shows the system at starting time where no information is registered and a cero is indicated in the counter module, and for different needs of storage, 1, 2, 3, 4 data, indicated in binary by the counter

module, respectively, as 01, 10, 11 and 100. Observe that the architecture adapts both the width of the counter and the memory map to the storage requirements.

The architecture is also able to erase or dismount entities when no required, as is shown in Fig. 18 for 4, 3, 2, 1, 0 data, i.e. 100, 11, 10, 01, 00 being indicated in the binary counter unit.

EXAMPLE OF APPLICATION (II)

Another example of application of the architecture of the second aspect of the invention, is shown in Fig. 19, where different blocks are illustrated representing different elements forming an architecture, such as the one of a microprocessor, corresponding to, for example, memory blocks, processing cores, arithmetic units and I/O banks.

Said and other elements form part of a set of blocks stored in the LIBRARY section of the architecture (see Fig. 16).

As shown by the different views of Fig. 19, the architecture is evolving, i.e. being reconfigured, by selectively adding or removing some of said elements, depending on the requirements, what is done, as described previously, by changing the functions of the hybrid RS/CMOS devices forming the architecture, i.e. by means of the HOS circuit replicating and erasing blocks of the LIBRARY on the Architecture Board through a sequence of signals and voltages to the hybrid RS/CMOS devices.

The reconfigurable memFETs based architecture opens new possibilities for the design of future large computation systems, where the function of all the elements could be adapted to the instantaneous needs. The strongly repetitive structure of this architecture suggests a reduction in the complexity of the fabrication process, when compared to the actual approaches. Making the most of versatility and easy reconfiguration of memFETs crossbar architecture, a novel computing hardware implementation principle called Shapeshifting Evolvable Hardware (SEHW) is herein reported, that could be considered as a new approach to implement Evolvable Hardware (EHW). EHW concept appeared early 90's and it refers to hardware that can change its own hardware structure and behaviour dynamically and autonomously adapting itself to changes in task requirements or in its environment. EHW approach has been usually built using Programmable Logic Devices such as FPGA (Field Programmable Gate Array) and uses a Genetic Algorithm (GA) to online architecture reconfiguration. So, EHW is able to perform different functions or show diverse behaviours at different stages by self-reconfiguring a pre-defined structure.

An illustrative example of EHW concept is shown in Fig. 23A. As can be observed the computing hardware, implemented on a FPGA structure, is evolving through the use of external configuration techniques. The chip is composed of a finite number of pre-defined entities (logic blocks and memory, I/O blocks and programmable interconnections) that are stationary distributed over the entire surface of the chip, and that can be reconfigured from configuration bits and evolve (find out better hardware structure) thanks to the use of genetic algorithms. Observe how the logic and memory (flat rectangles, in dark grey means not used, in light grey means used) change from one stage to other.

A new EHW operative computer organization oriented to execute computing tasks in a dynamic, flexible, efficient and adaptive way taking into account the processing requirements/needs that are being executed at each time is presented here. The SEHW mechanism implementing an embodiment of the

second aspect of the invention is able to transform the functionality and change the location of the hardware structure dynamically and autonomously, self-adapting resources to computation requirements. In other words, the hardware develops its own hardware structure depending on task requirements. To achieve this goal, SEHW is built on a large bi-dimensional memFET crossbar (Fig. 23B, left); it is called Computing Board (CB). Within this structure the Library is defined, where a set of specific elementary processing elements is stored (Fig. 23B, left). The CB is surrounded by a programmable interconnection ring that links up the CB with the above mentioned controller element called Hardware Operative System (HOS). The HOS is responsible for identifying the computing requirements and satisfy them. For that, the HOS is able to replicate any specific logic entity from the Library in the CB (mount) as well as erase (dismount) or modify the position of any logic entity within the CB (relocate). This is achieved applying a set of electrical signals through the ring connections that allows reconfiguring each non-volatile memFET device (crosspoint) of the CB. So, the HOS detects the processing requirements and satisfy them by copying, deleting or changing the position of the different logic blocks towards a new structure. It is worth noting that the interconnection ring allows the communication between the CB and the HOS for both configure the computing structure and sense the need of hardware evolution. The SEHW concept is shown in Fig. 23B. Observe that the space distribution of the processing entities is not fixed as in FPGAs but can be positioned in any free space of the CB. So SEHW, not having a predefined or predetermined structure, makes better use of available chip area and therefore higher performance. In addition, thanks to the mounting, dismounting and relocation of the blocks, SEHW could be a defect-tolerant and even fault-tolerant system.

In order to clarify the SEHW concept, some examples of application are shown in Fig. 24. A simple illustrative example of SEHW application in a LIFO (Last In, First Out) memory is shown in Fig. 24A. Note that both, the counter (light grey blocks) and the memory unit (dark grey blocks) expand or shrink dynamically depending on the input/output data. First two data are stored, and then a third one is stacked. A new register is "mounted" to the memory unit whereas the binary counter works keeping its size (2 counting units). Next, a fourth data enters, an in this case a counting unit is added to the counter. Finally, the last data is removed so the last register and counting unit are "dismounted". Another example of application is the use of SEHW in many-core systems. A many-core system, as its name suggest, is a single component with a high number (tens or hundreds) of independent cores that have been attached for enhanced performance, reduced power consumption, and more efficient simultaneous processing of multiple tasks (parallel processing). However, maximizing the utilization of the computing resources provided by these systems requires adjustments both to the operative system (OS), that must recognize multi-threading, and to existing application software that must be written using simultaneous multi-threading technology (SMT). In other words, both OS and software have to be adapted to take advantage of these systems. Again, in many-core systems the number of cores is fixed and not all of them are used at every time. So, the application of the SEHW concept in this kind of systems could improve their efficiency.

Fig. 24B shows an application of SEHW technique in a many-core structure. In this case, just to simplify, a core and a basic memory block form the library. The HOS starts with a basic computing architecture formed by a single core and a certain amount of memory. Evolving towards the computing

needs, the system modifies the number of cores and the amount of memory assigned to each core. In Fig. 24B the system first evolves from a single-core structure to a three-core architecture in which each core has a specific amount of memory to finally become a dual-core system.

By the reconfigurable processing architecture of the second aspect of the invention, a new computer organizational concept that autonomously configures the type, size and position of the elementary bock elements is provided. The configuration is highly dynamic adapting the architecture to the instantaneous data requirements.

The block elements that form part of the architecture are replicated or erased in the architecture depending of the data requirements.

Hence, the architecture is not fixed as happen in conventional computers but adapts the size and composition dynamically.

To conclude, the reconfigurable memFETs based architecture is a step toward the design of future large computation systems. The versatility and easy reconfiguration of memFETs crossbar architecture, leads to the Shapeshifting Evolvable Hardware principle, a technique that can change the location of the hardware structure dynamically and autonomously self-adapting resources to computation requirements.

A person skilled in the art could introduce changes and modifications in the embodiments described without departing from the scope of the invention as it is defined in the attached claims.

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[14] J. Borghetti, Z.Li, J. Straznicky, X. Li, D.A. Ohlberg, D.R. Stewart, R. Stanley Williams, "A hybrid nanomemristor/transistor logic circuit capable of self-programming", Proceedings of the National Academy of Sciences of the United States of America, on-line publication, www.pnas.org/cgi/doi/10.1073/pnas.0806642106.

[15] A. Crespo-Yepes, J. Martín-Martínez, R. Rodríguez, M. Nafria and X. Aymerich, "Resistive switching-like behaviour of the dielectric breakdown in ultra-thin Hf based gate stacks in MOSFETs", Solid-State Device Research Conference (ESSDERC), 2010 Proceedings of the European

[16] A. Crespo-Yepes, J. Martín-Martínez, A. Rothschild, R. Rodríguez, M. Nafria and X. Aymerich, "Recovery of the MOSFET and circuit functionality after the dielectric breakdown of ultrathin high-k gate stacks", IEEE Electron Device Letters, Vo. 31, No 6, June 2010.

Claims

1.- Method for operating a transistor, comprising:

- reversibly electrically breaking the dielectric of said transistor in a controlled manner for creating a closable resistive switching path to appear there through while at least partially restoring the channel electric properties of said transistor, at least when said resistive switching path is closed, and

- using said transistor according to a first mode of operation, once said transistor channel electric properties are at least partially restored, by applying a first set of electrical signals at at least part of the terminals of said transistor in order to create a conductive channel between a first and a second of said terminals, through a semiconductor substrate, and make a channel current to flow there through;

wherein the method is **characterised in that** it further comprises:

- using said transistor according to a second mode of operation by applying a second set of electrical signals at at least part of the terminals of said transistor in order to open said created resistive switching path and make current to flow locally through said dielectric between a third terminal and said first, second or another of said terminals, and

- employing said second mode of operation for using said transistor as a non volatile memory, where said resistive switching path represents a memory bit having a value with a certain logic state or with a logic state complementary to said certain logic state, depending on at least the value of the current circulating there through.

2.- Method as per claim 1, comprising selecting using said transistor according to one of said first and second modes.

3.- Method as per claim 1, comprising selecting using said transistor according to both of said first and second modes.

4.- Method as per claim 1, wherein said at least one resistive switching path is a first resistive switching path, and said second mode of operation further comprises applying at least a third set of electrical signals at at least part of the terminals of said transistor in order to create at least a second resistive switching path and make current to flow locally through said dielectric between said third terminal and another of said terminals not involved in said first resistive switching path.

5.- Method as per claim 4, comprising employing said second mode of operation for using said transistor as a non volatile multibit memory, where each of said resistive switching paths represents a memory bit having a value with a certain logic state or with a logic state complementary to said certain logic state, depending on at least the value of the current circulating there through.

6.- Method as per any of the previous claims, comprising controlling said sets of electrical signals in order to control the opening/closing of said one or more resistive switching paths, their location and the values and directions of said current flows.

7.- Method as per claim 6, comprising carrying out said control such that said channel current flow is substantially null and reading each memory bit value by measuring the respective resistive switching path current value at a terminal of the transistor where said current flows.

8.- Method as per claim 6, comprising carrying out said control such that said channel current flow is not null and reading each memory bit value by measuring the combined current resulting from the

combination of the respective resistive switching path current and the channel current, at a terminal of the transistor where said current combination is produced.

9.- Method as per claim 8, comprising carrying said control to create a channel current with a value lower than the value of said resistive switching path current, such that the combined current values at said terminal of the transistor are of the same sign for both, an ON state representing a memory bit value with a certain logic state and an OFF state representing a memory bit value with a logic state complementary to said certain logic state.

10.- Method as per claim 8, comprising carrying said control to create a channel current with a value higher than the value of said resistive switching path current when in an OFF state, and lower than the value of said resistive switching path current when in an ON state, such that the combined current values at said terminal of the transistor are of different signs for said ON state, representing a memory bit value with a certain logic state, and said OFF state, representing a memory bit value with a logic state complementary to said certain logic state.

11.- Method as per claim 4, comprising employing said second mode of operation for using said transistor as a controlled multidirectional switch between said third terminal and at least two of the other transistor terminals, at least a single connection of the third terminal and at least one of the other terminals being provided, the method comprising selectively controlling the switching ON/OFF and location of said single connection.

12.- Method as per claim 4, comprising employing said second mode of operation for using said transistor as a controlled multidirectional switch between said third terminal and at least two of the other transistor terminals, a first connection between the third terminal and one of the other terminals and at least a second connection between the third terminal and another one of the other terminals being provided, the method comprising controlling the simultaneous switching ON/OFF of said first and second connections.

13.- Method as per claim 11 or 12, comprising selecting employing said second mode of operation for using said transistor as said non volatile memory and/or as said multidirectional switch.

14.- Method as per any of the previous claims, wherein said transistor is a Field Effect Transistor, FET.

15.- Method as per claim 14, wherein said transistor is a MOSFET having a material with resistive switching properties, where said first, second and third terminals correspond, respectively, to the source, drain and gate of said MOSFET, and where said electrical signals are voltage signals, each of said one or more resistive switching paths passing only:

- through gate, dielectric and source, or
- through gate, dielectric and substrate, or
- through gate, dielectric and drain.

16.- Method as per claim 14, wherein said transistor is one of a multigate transistor and a CNTFET, with a material with resistive switching properties.

17.- Reconfigurable processing architecture, comprising:

- a plurality of transistors for implementing required logic functions,
- a plurality of resistive switching elements for implementing memory functions, and
- a control unit for controlling said transistors and resistive switching elements,

wherein said reconfigurable processing architecture is **characterised in that:**

said transistors are intended for implementing both, said required logic functions and said memory functions, said resistive switching elements being provided by said transistors, as the latter have respective reversibly electrically breakable dielectrics each providing, after being reversibly broken in a controlled manner, at least one closable resistive switching path to appear there through while at least partially restoring the channel electric properties of the respective transistor, at least when said at least one resistive switching path is closed, and

in that said control unit is intended for, once said dielectric reversible breaking has been caused, selecting and controlling at least part of said transistors for making each of them work according to first and second modes of operation, at least one mode at a time, by means of:

- regarding said first mode of operation, once said transistor channel electric properties are at least partially restored, applying a first set of electrical signals at at least part of the terminals of each selected transistor in order to create a conductive channel between a first and a second of said terminals, through a semiconductor substrate, and make a channel current to flow there through, where said first mode of operation comprises using the transistors for said required logic functions implementing; and

- regarding said second mode of operation, applying a second set of electrical signals at at least part of the terminals of each selected transistor in order to open said at least one created resistive switching path and make current to flow locally through said dielectric between a third terminal and said first, second or another of said terminals, said control unit being intended for employing said second mode of operation for using each selected transistor as a non volatile memory, where said at least one resistive switching path represents a memory bit having a value with a certain logic state or with a logic state complementary to said certain logic state, depending on at least the value of the current circulating there through.

18.- Reconfigurable processing architecture as per claim 17, wherein said transistor dielectrics are already reversibly broken, each providing at least one of said closable resistive paths.

19.- Reconfigurable processing architecture as per claim 17 or 18, wherein said control unit is also intended for employing said second mode of operation for using each selected transistor as a controlled multidirectional switch between said third terminal and at least two of the other transistor terminals, by connections provided by respective closable resistive switching paths, the control unit being in charge of selecting if employing said second mode for using each selected transistor as a non volatile memory or as a controlled multidirectional switch.

20.- Reconfigurable processing architecture as per claim 17, 18 or 19, wherein said control unit implements the method as per any of claims 1 to 16 to control and supply said sets of electrical signals to make each selected transistor work in said first and/or second modes of operation.

21.- Reconfigurable processing architecture as per any of claims 17 to 20, wherein said control unit is intended for controlling said sets of electrical signals to select transistors and dynamically modify the mode of operation they work, between said first and second modes, as a function of instantaneous computing requirements and/or in order to correct possible malfunctioning of some parts of the processing

architecture, the control unit being arranged for sensing the processing architecture performance in order to carry out said dynamic modification.

22.- Reconfigurable processing architecture as per any of claims 17 to 21, wherein said control unit is intended for controlling said sets of electrical signals to select transistors and dynamically making them stop working, as a function of instantaneous computing requirements and/or in order to correct possible malfunctioning of some parts of the processing architecture, the control unit being arranged for sensing the processing architecture performance in order to carry out said working stop.

23.- Reconfigurable processing architecture as per claim 21 or 22, comprising a library registering several possible logic and memory entities to be mounted, and in that the control unit has access to said library and is intended:

- to replicate each of said entities, on an architecture board, by selecting corresponding transistors and making them work according to said first mode and/or second mode of operation; and

- to dismount or erase each of said entities by selecting corresponding transistors and making them stop working.

24.- Reconfigurable processing architecture as per claim 23, wherein said logic entities include entities implementing negate Boolean functions.

25.- Reconfigurable processing architecture as per any of claims 17 to 24, constituting a crossbar interconnecting the transistors through voltage controlled switches.

26.- Reconfigurable processing architecture as per claim 25, wherein said transistors are MOSFETs with at least one created RS path, said first, second and third terminals correspond, respectively, to the source, drain and gate of each MOSFET, and wherein said crossbar is a crossbar supplying said sets of electrical signals at the source, drain gate and bulk of the selected MOSFETs from the crossbar terminals.

27.- Reconfigurable processing architecture as per claim 26, wherein said crossbar is arranged for supplying said sets of electrical signals at the source, drain gate and bulk of the selected MOSFETs from the crossbar terminals, through said voltage controlled switches.

28.- Reconfigurable processing architecture as per any of claims 24 to 27, where said transistors and said voltage controlled switches are CMOS compatible.

29.- Use of a restored broken down transistor for a multiple mode operation, where said restoration relates to the at least partially restoring of the transistor channel electric properties after reversibly electrically breaking the dielectric of said transistor in a controlled manner for creating at least one closable resistive switching path to appear there through, said multiple mode operation including, simultaneously or selectively:

- using the transistor for implementing logic functions based on the conduction state of a conductive channel created through a semiconductor substrate of the transistor, and

- using the transistor for implementing non-volatile memory functions based on the conduction state of said at least one resistive switching path created in the transistor dielectric.

30.- Use as per claim 29, where said multiple mode operation further includes, selectively or simultaneously with said logic functions use and non-volatile memory functions use, using the transistor

for implementing a controlled multidirectional switch also based on the conduction state of said resistive switching path created in the transistor dielectric.

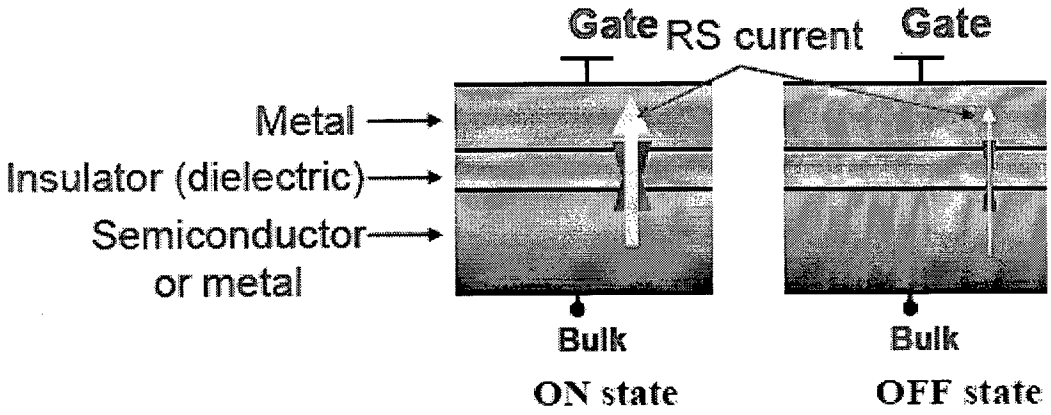

Fig. 1

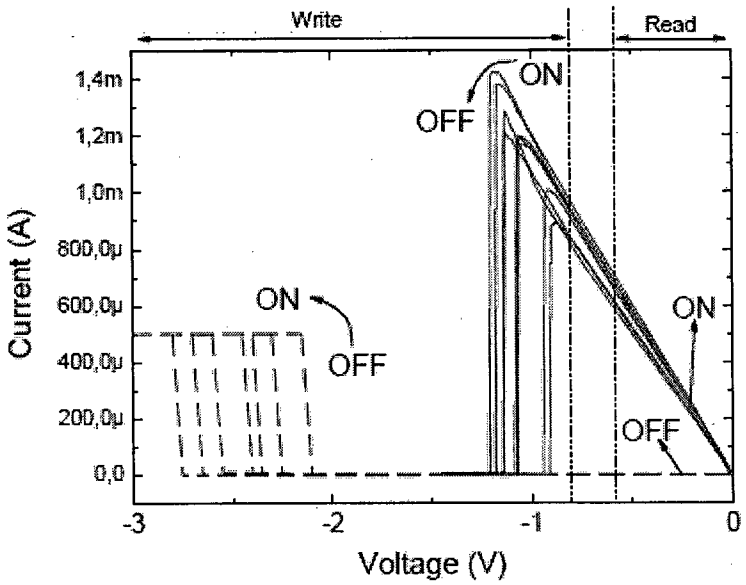

Fig. 2

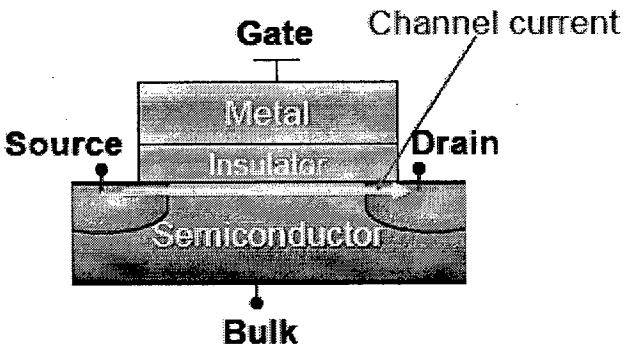

Fig. 3

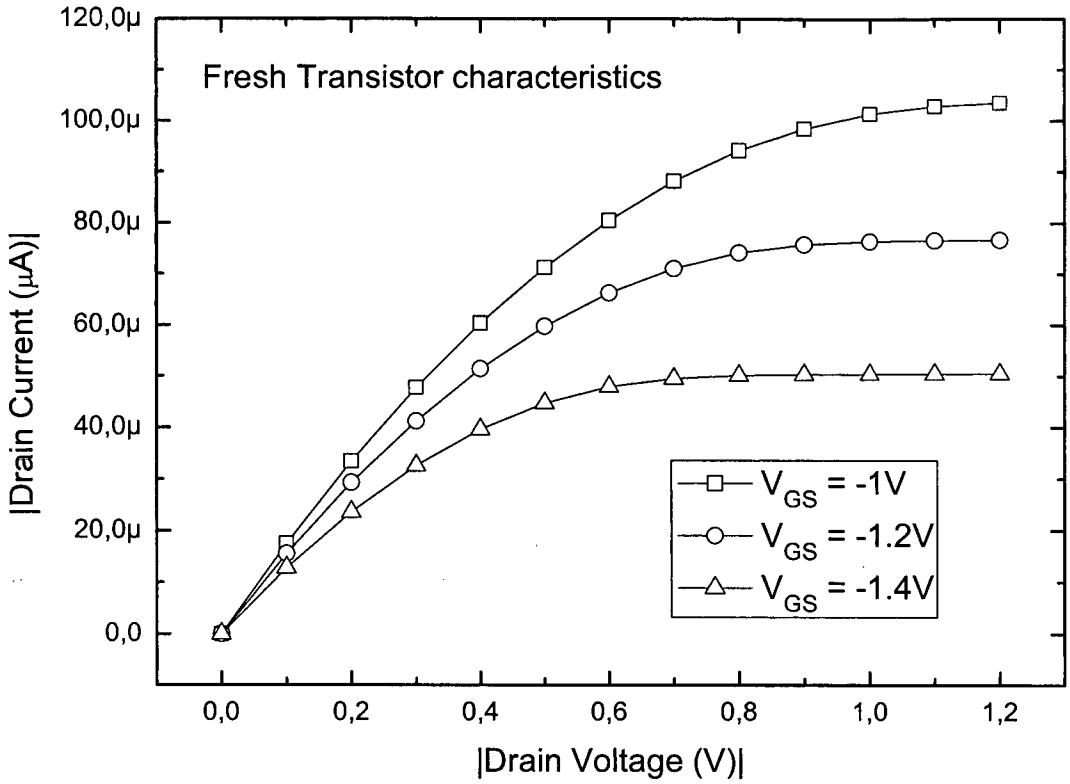
Fresh Transistor characteristics
120,0µ
100,0µ
80,0µ
60,0µ
40,0µ
20,0µ
0,0
|Drain Current (µA)|
0,0
0,2
0,4
0,6
0,8
1,0
1,2
|Drain Voltage (V)|
V_GS = -1V
V_GS = -1.2V
V_GS = -1.4V

Fig. 4

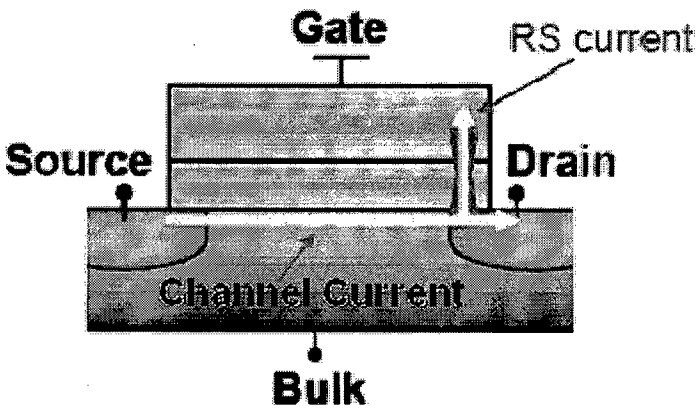
Gate
RS current
Source
Drain
Channel Current
Bulk

Fig. 5

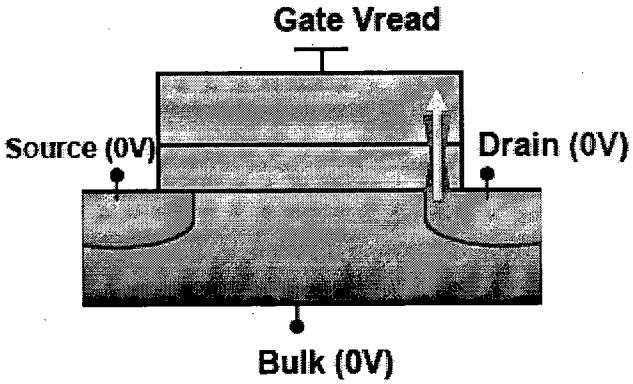

Fig. 6

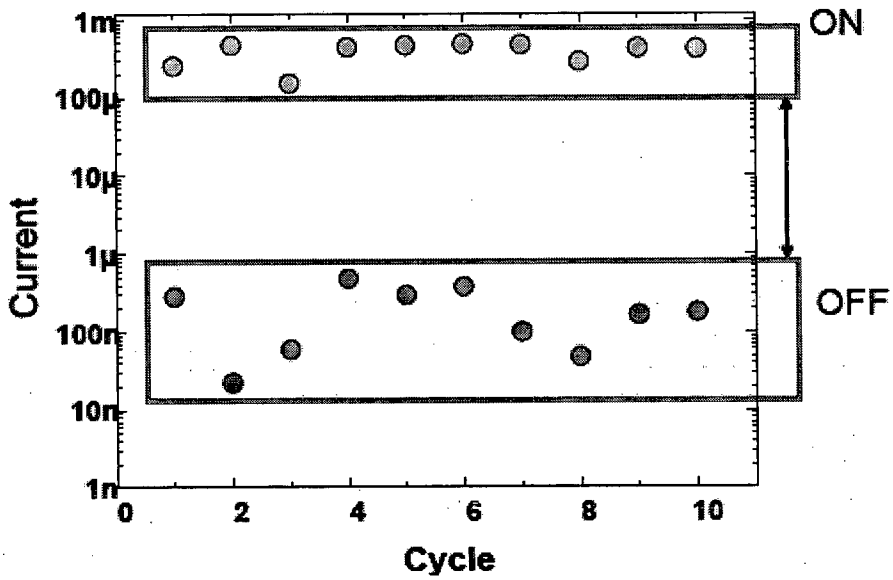

Fig. 7

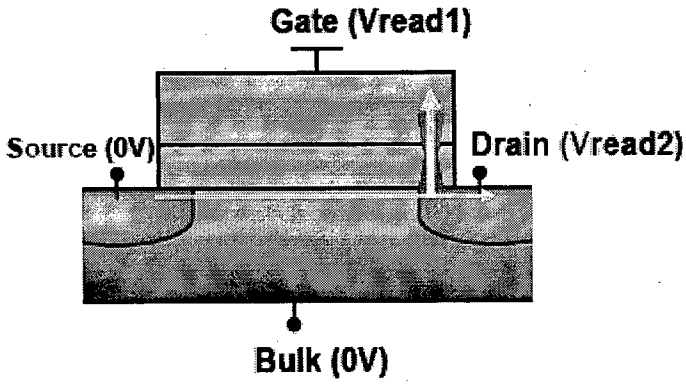

Fig. 8

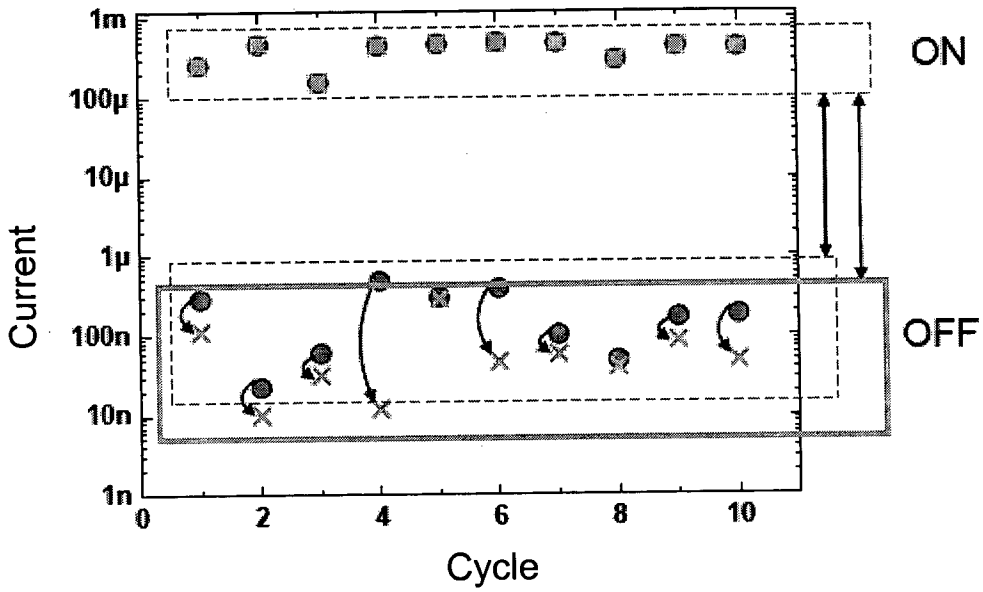

Fig. 9

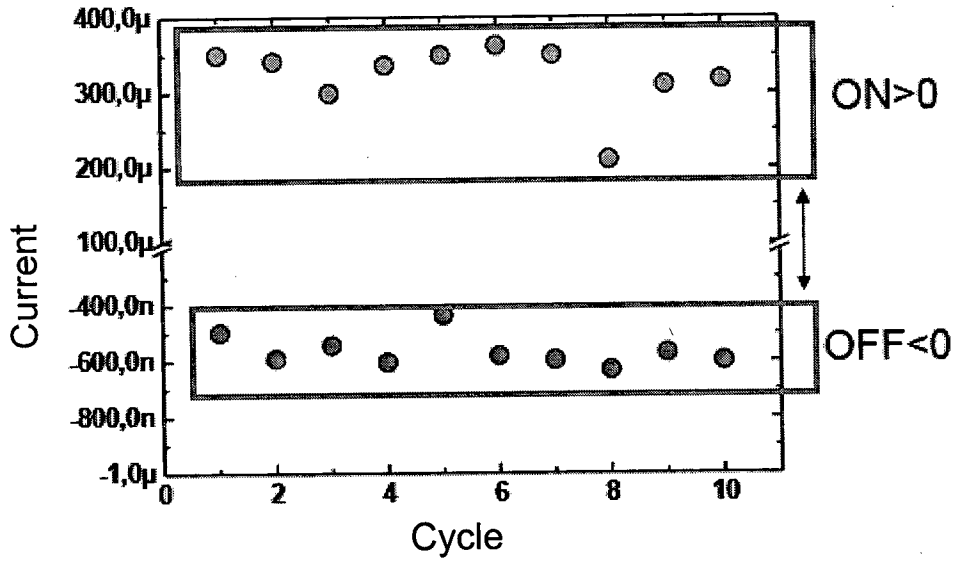

Fig. 10

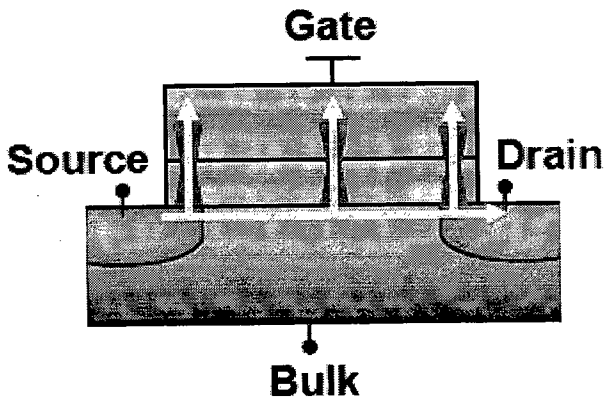

Fig. 11

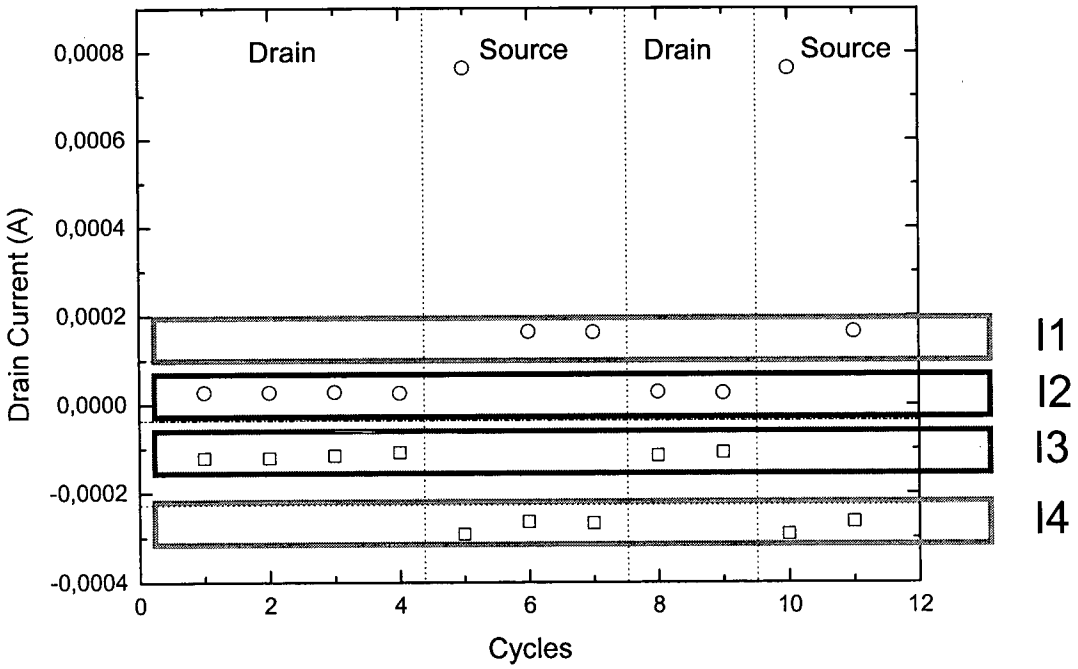
Drain
Source
Drain
Source
0,0008
0,0006
0,0004
0,0002
0,0000
-0,0002
-0,0004
Drain Current (A)
0
2
4
6
8
10
12
Cycles
I1
I2
I3
I4

Fig. 12

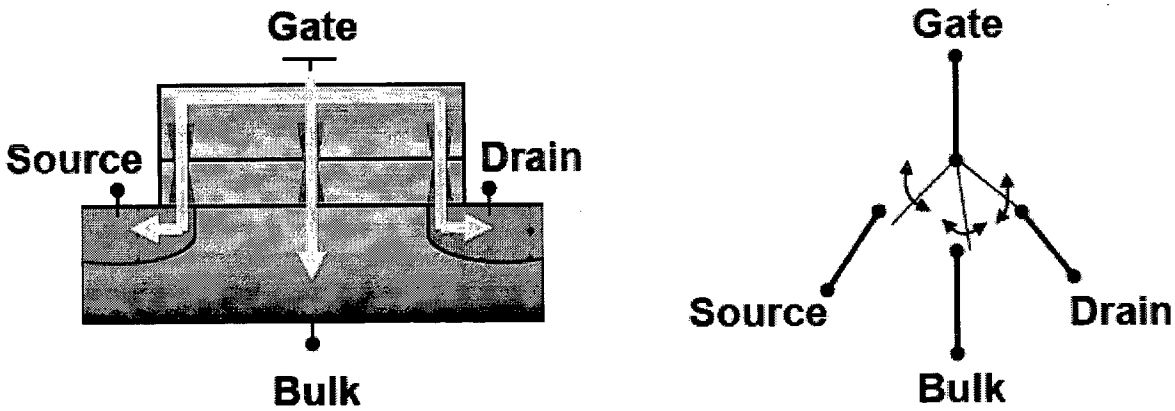
Gate
Source
Drain
Bulk
Gate
Source
Drain
Bulk

Fig. 13

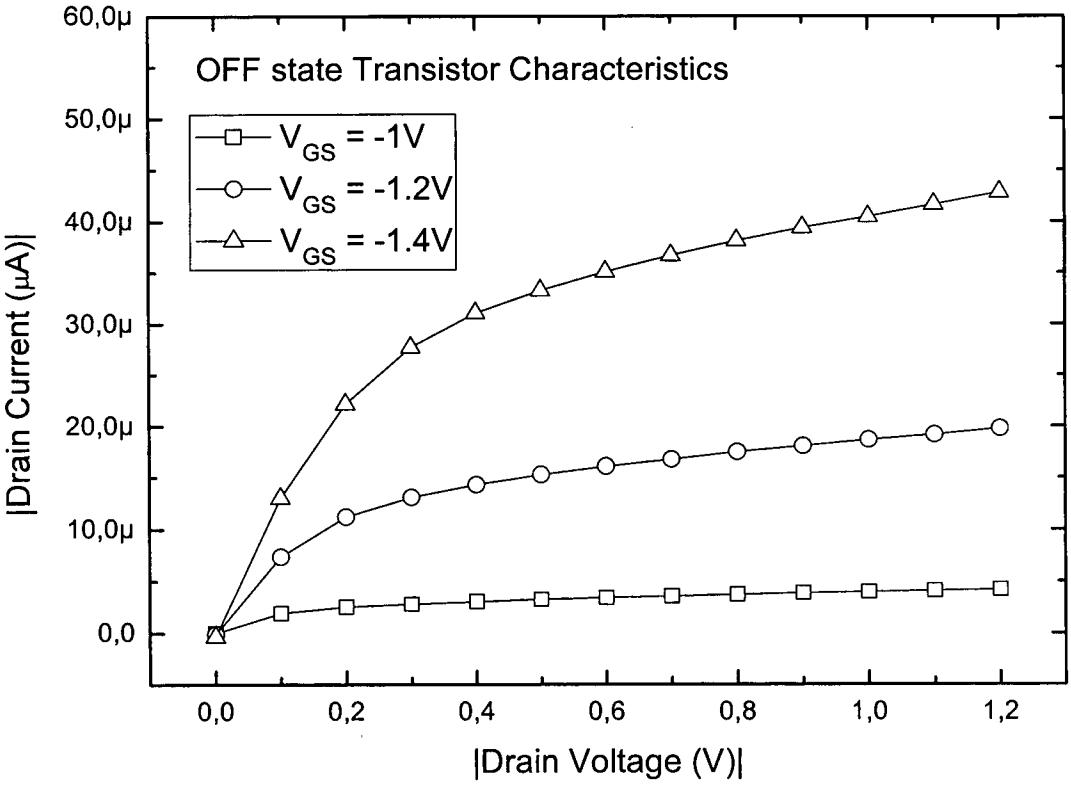
OFF state Transistor Characteristics
V_{GS} = -1V
V_{GS} = -1.2V
V_{GS} = -1.4V
|Drain Current (μA)|
60,0μ
50,0μ
40,0μ
30,0μ
20,0μ
10,0μ
0,0
0,0
0,2
0,4
0,6
0,8
1,0
1,2
|Drain Voltage (V)|

Fig. 14

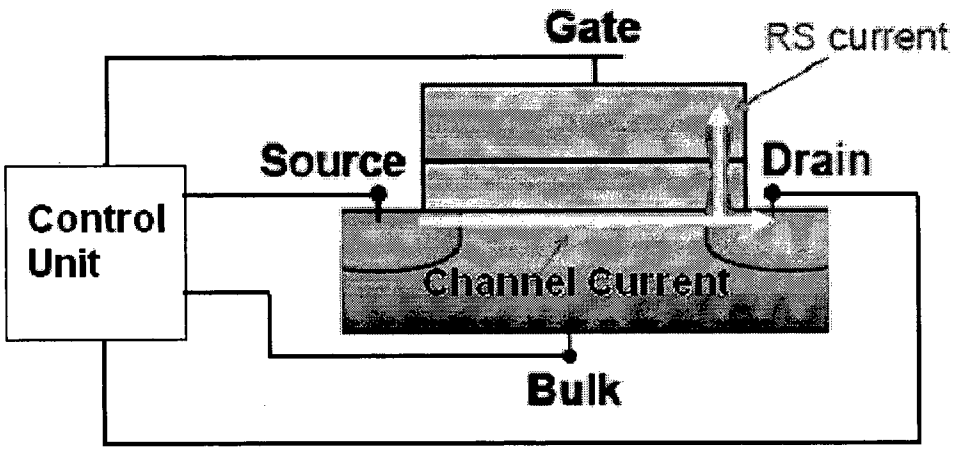
Gate
RS current
Source
Drain
Control Unit
Channel Current
Bulk

Fig. 15

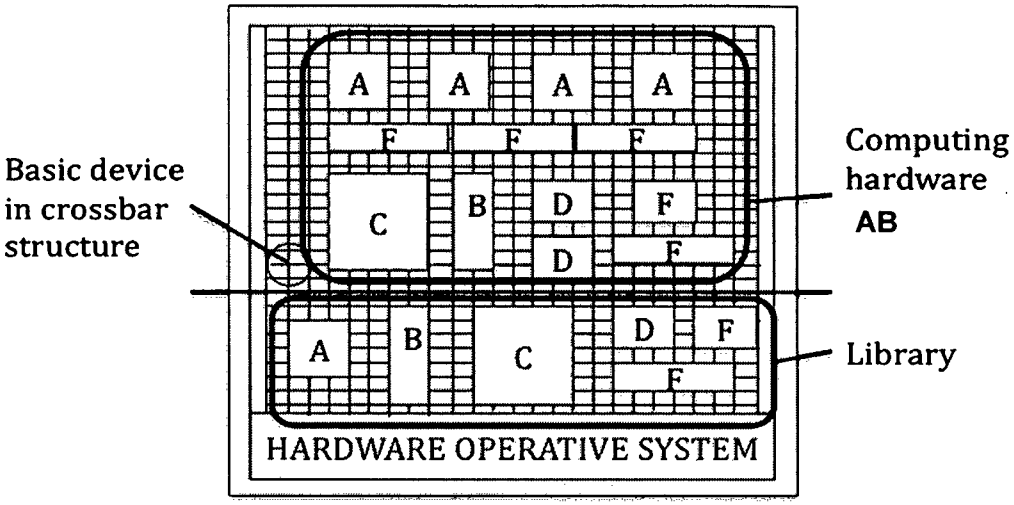
Basic device in crossbar structure
Computing hardware AB
Library
HARDWARE OPERATIVE SYSTEM

Fig. 16

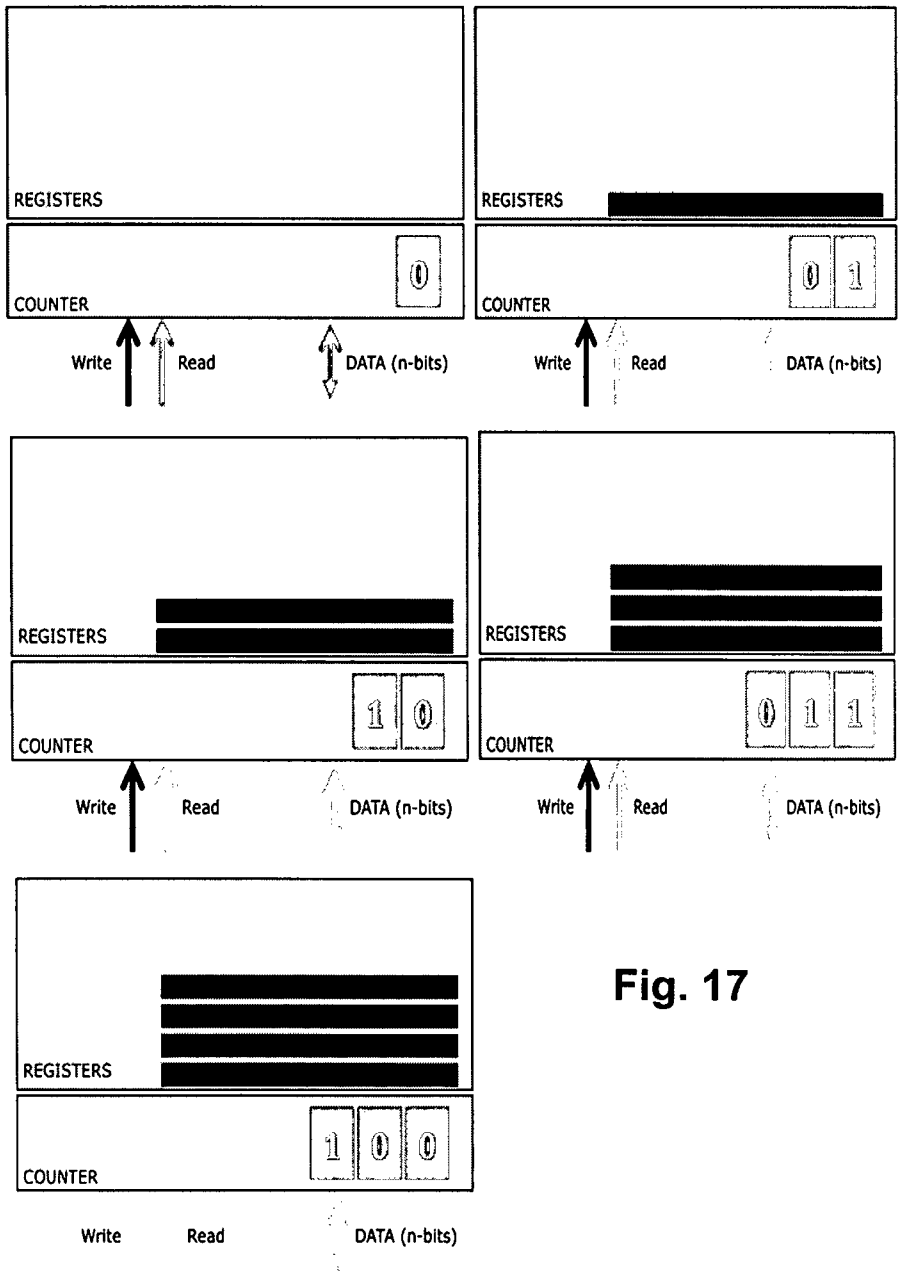
REGISTERS
COUNTER
Write
Read
DATA (n-bits)

Fig. 17

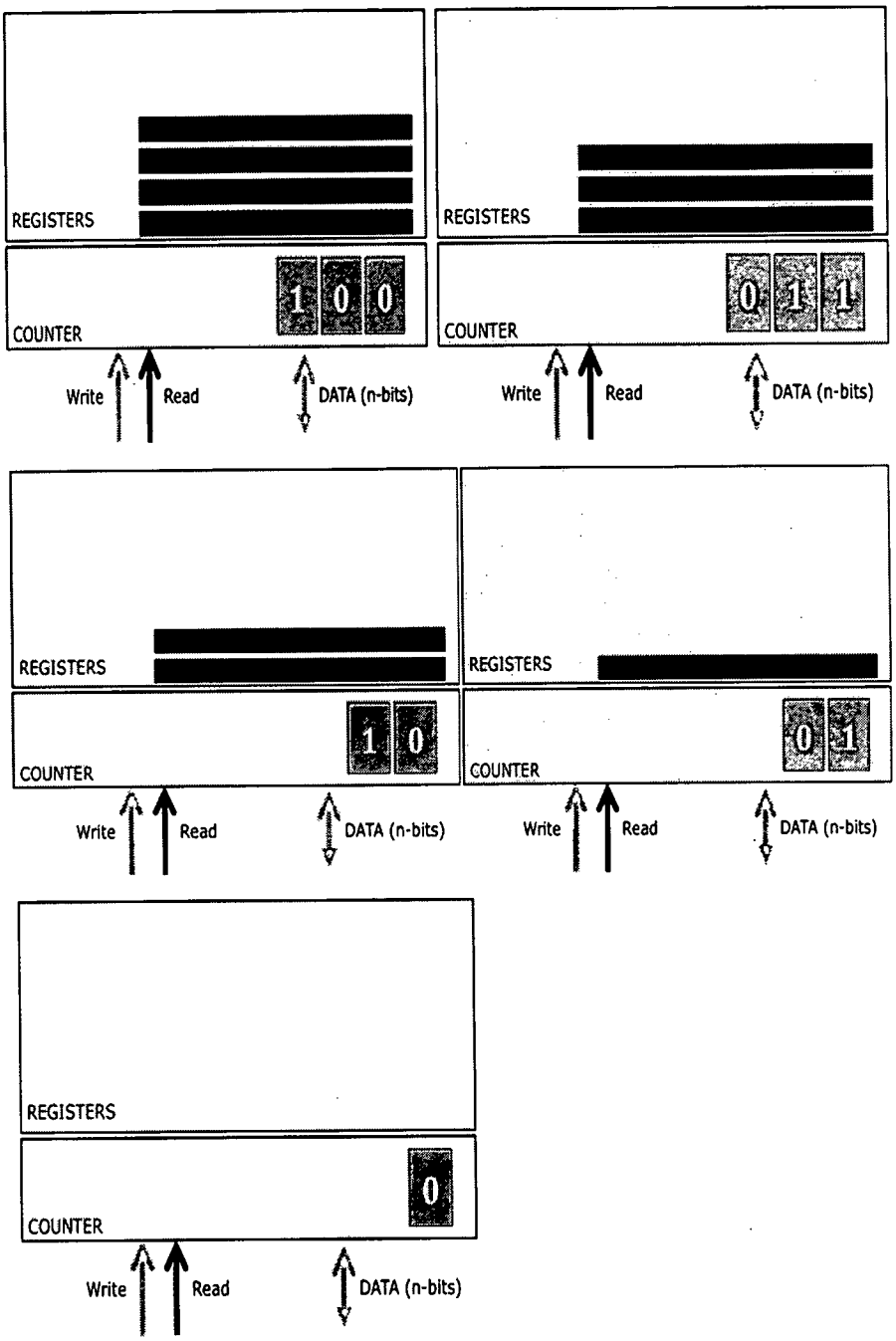
REGISTERS
COUNTER
1 0 0
Write
Read
DATA (n-bits)
REGISTERS
COUNTER
0 1 1
Write
Read
DATA (n-bits)
REGISTERS
COUNTER
1 0
Write
Read
DATA (n-bits)
REGISTERS
COUNTER
0 1
Write
Read
DATA (n-bits)
REGISTERS
COUNTER
0
Write
Read
DATA (n-bits)

Fig. 18

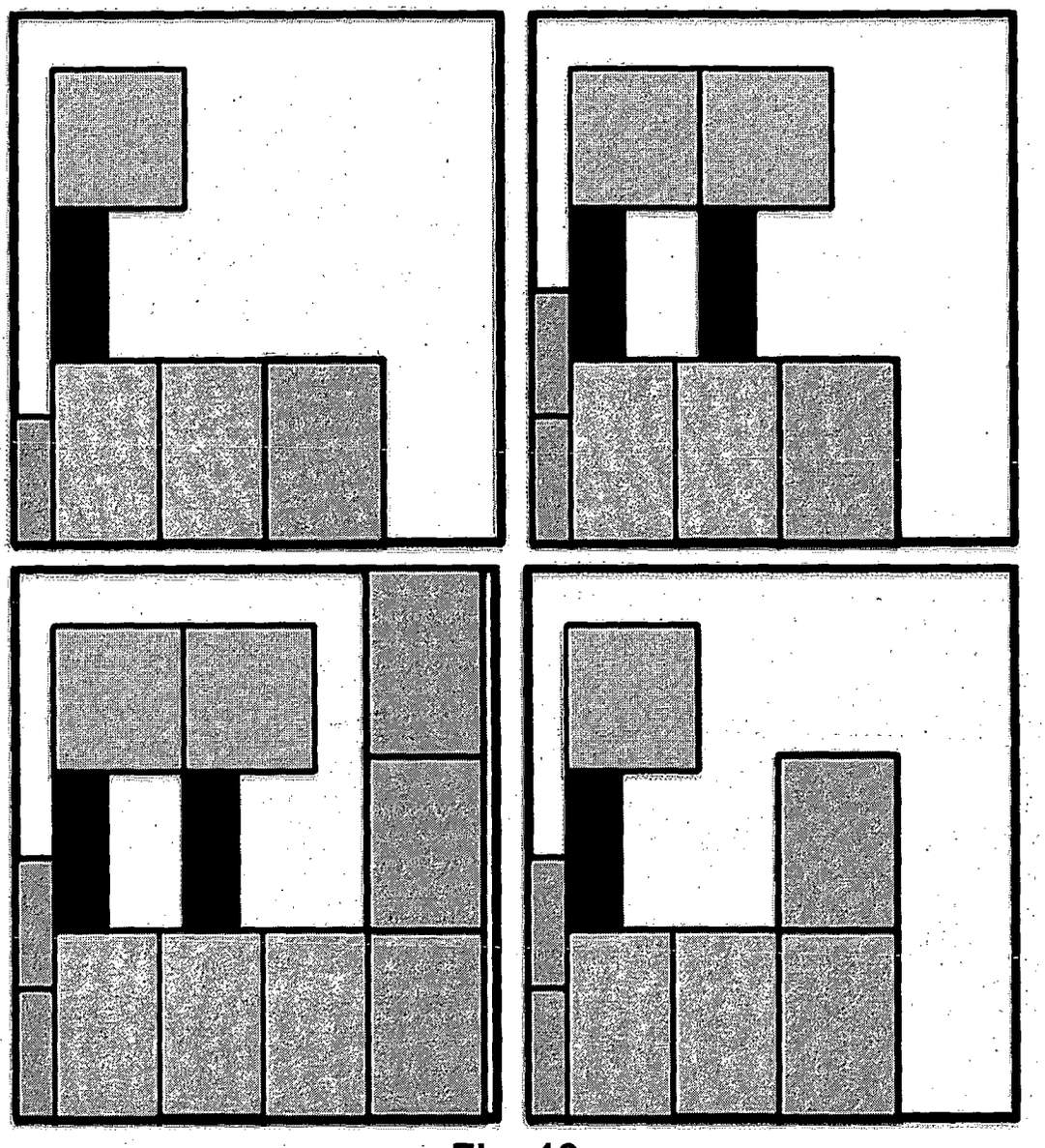

Fig. 19

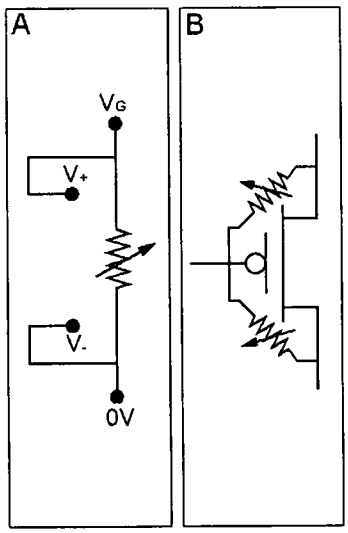

Fig. 20

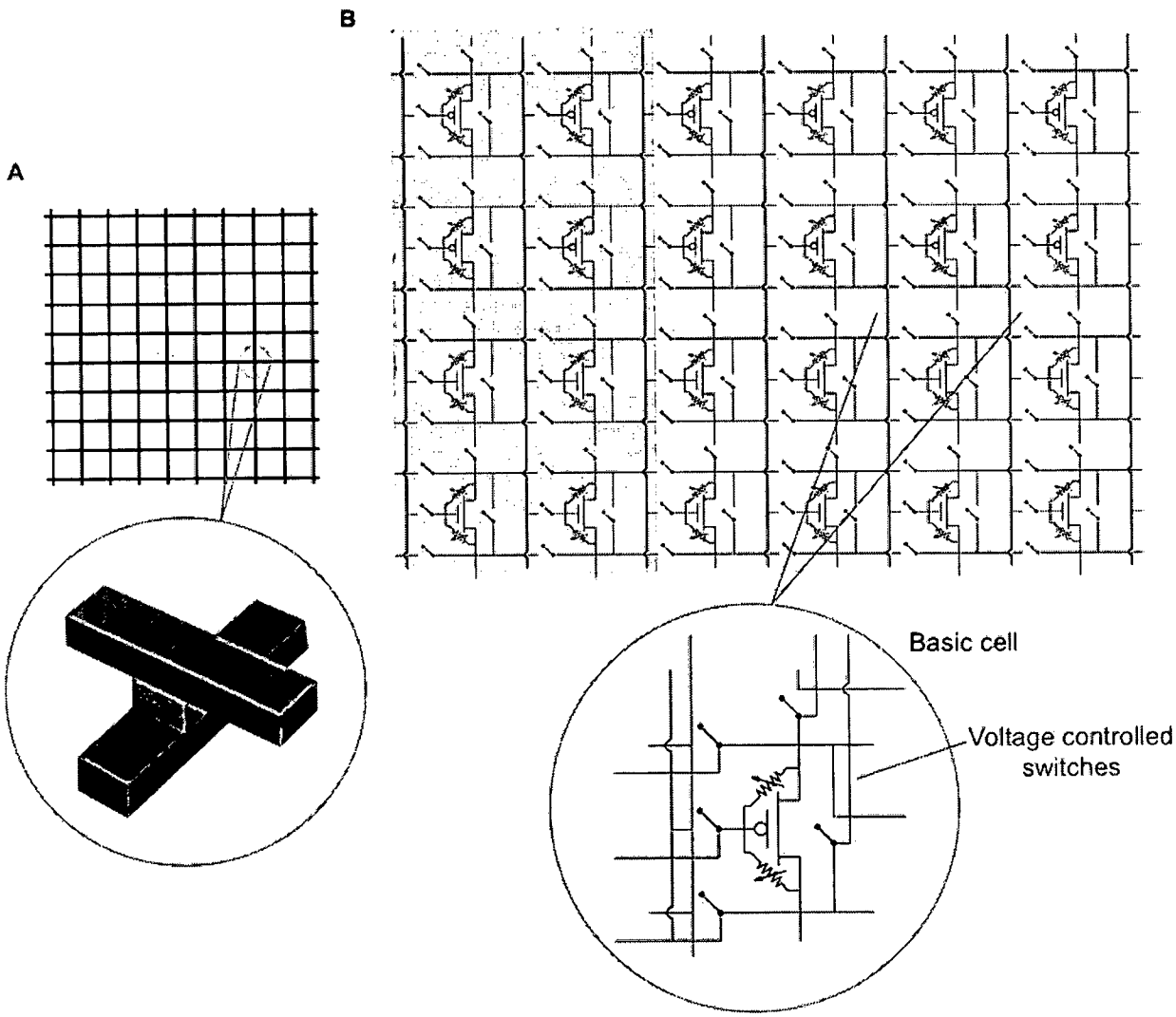

Fig. 21

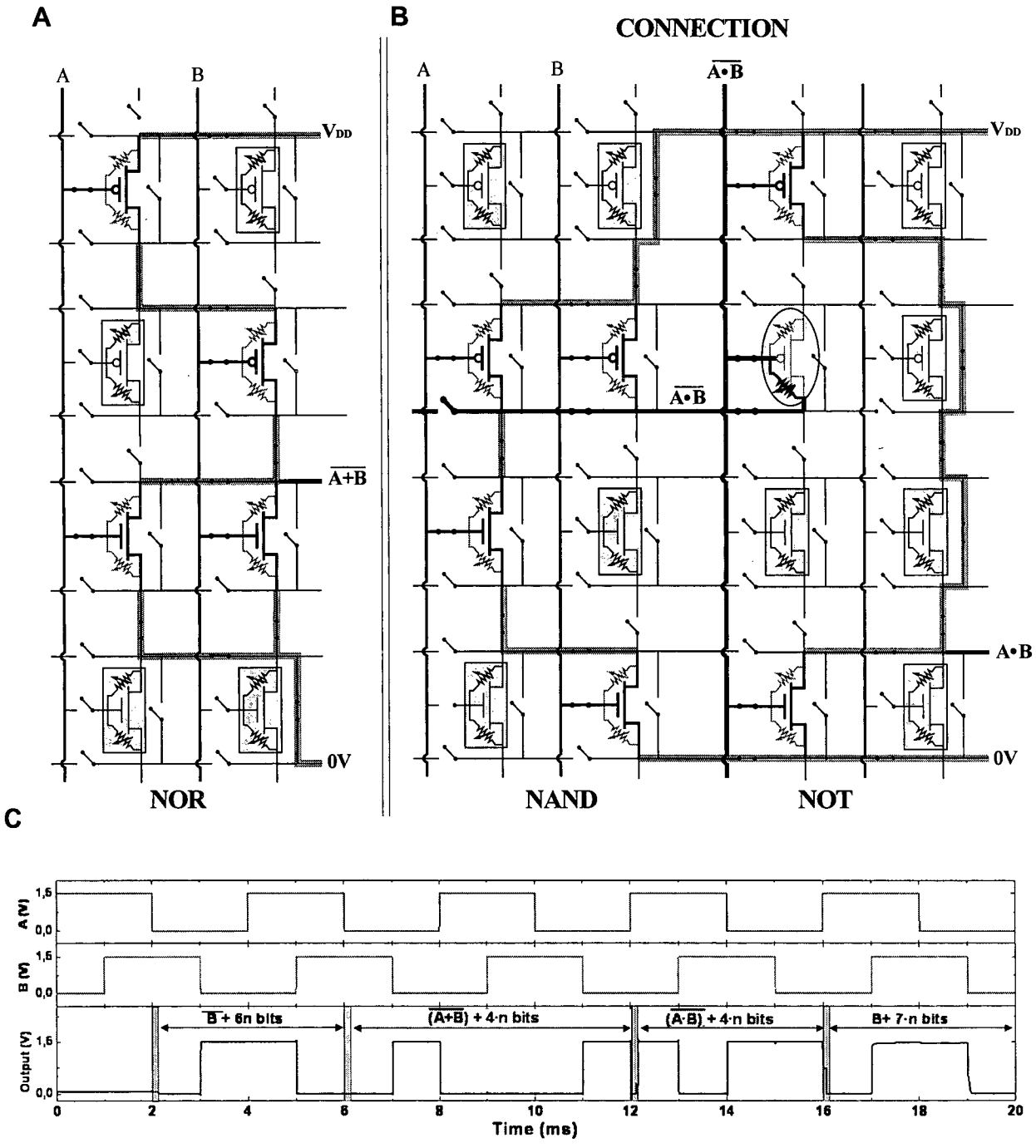
A
B
CONNECTION
A
B
$\overline{A \cdot B}$
V_{DD}
$\overline{A+B}$
0V
$\overline{A \cdot B}$
A•B
0V
NOR
NAND
NOT
C
A (V)
B (V)
Output (V)
1,5
0,0
$\overline{B}$ + 6n bits
$\overline{(A+B)}$ + 4·n bits
$\overline{(A \cdot B)}$ + 4·n bits
B+ 7·n bits
0
2
4
6
8
10
12
14
16
18
20
Time (ms)

Fig. 22

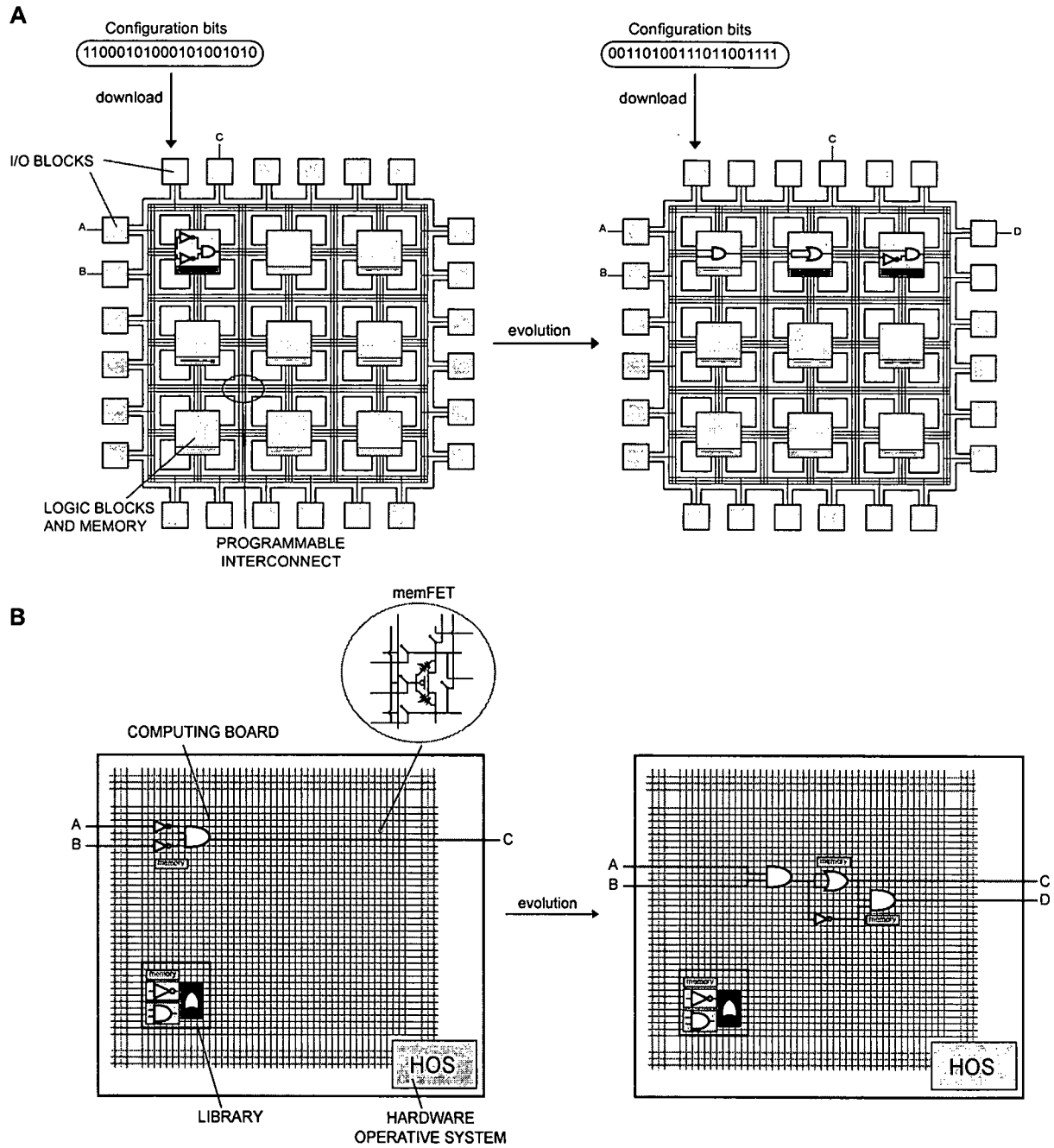
A
Configuration bits
1100010100010100101O
download
I/O BLOCKS
C
A
B
LOGIC BLOCKS
AND MEMORY
PROGRAMMABLE
INTERCONNECT
evolution
Configuration bits
0011010011101100111 1
download
C
A
B
D
B
memFET
COMPUTING BOARD
A
B
C
HOS
LIBRARY
HARDWARE
OPERATIVE SYSTEM
evolution
A
B
C
D
HOS

Fig. 23

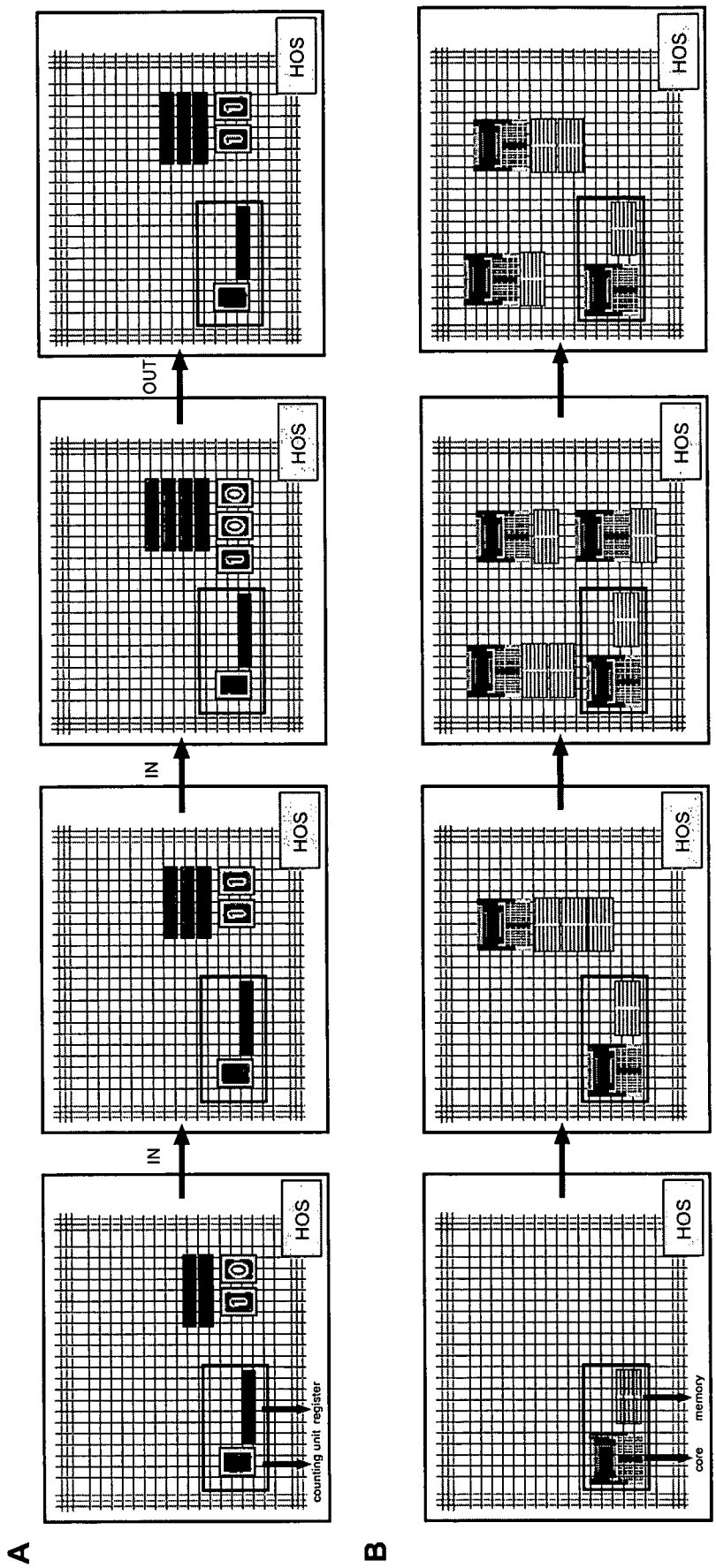

Fig. 24

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2011/001257

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C11/56 G11C13/00 G11C11/40 H03K19/177
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C H01L H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, COMPENDEX, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CRESPO-YEPES A ET AL: "Resistive switching-like behaviour of the dielectric breakdown in ultra-thin Hf based gate stacks in mosfets", SOLID-STATE DEVICE RESEARCH CONFERENCE (ESSDERC), 2010 PROCEEDINGS OF THE EUROPEAN, IEEE, PISCATAWAY, NJ, USA, 14 September 2010 (2010-09-14), pages 138-141, XP031787645, ISBN: 978-1-4244-6658-0	1-3,14, 15,17, 18, 20-24, 28,29
Y	the whole document	4-13,16, 19, 25-27,30

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 August 2011	17/08/2011

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Havard, Corinne

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2011/001257

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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