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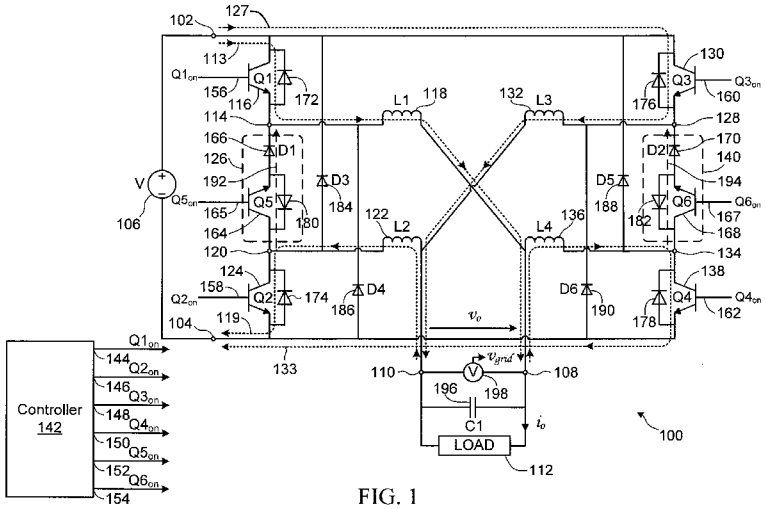


FIG. 1

(57) **Abstract**: A method and apparatus for converting a direct current into an alternating current is disclosed. The load is connected between a first and a second load nodes and a source is connected between a first and a second source nodes. The method involves producing a positive and negative half cycle of alternating current through the load. The positive half cycle is produced by causing a first and a second switching control signals to effect a plurality of sub-cycles each comprising a first time period during which the first and second switching signals are asserted and a second time period during which the first and second switching signals are not asserted. During each first time period of each sub-cycle, direct current flows from the first source node then through a first switch that conducts current from the first source node to a first intermediate node in response to the first switching signal, then through a first inductor connected between the first intermediate node and the first load node, then through the load, then through a second inductance connected between the second load node and a second intermediate node, and then through a second switch that conducts current from the second intermediate node to the second source node in response to the second switching signal. During each second time period of each sub-cycle, a first shunt control signal is asserted to cause current to flow through a first unidirectional shunt from the second intermediate node to

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the first intermediate node, then through the first inductor, then through the load node and then through the second inductor back to the second intermediate node. The negative half cycle is produced by causing a third and a fourth switching control signals to effect a plurality of sub-cycles each comprising a third time period during which the third and fourth switching signals are asserted and a fourth time period during which the third and fourth switching signals are not asserted. During the third time period in each sub-cycle, direct current flows from the first source node, then through a third switch that conducts current from the first source node to a third intermediate node in response to the third switching signal, then through a third inductor connected between the third intermediate node and the second load node, then through the load, then through a fourth inductance connected between the first load node and a fourth intermediate node, and then through a fourth switch that conducts current from the fourth intermediate node to the second source node in response to the fourth switching signal. During each fourth time period of each sub-cycle, a second shunt control signal is asserted to cause current to flow through a second unidirectional shunt from the fourth intermediate node to the third intermediate node, then through the third inductor, then through the load, then through the fourth inductor back to the fourth intermediate load node.

METHOD AND APPARATUS FOR CONVERTING DIRECT CURRENT INTO AN ALTERNATING CURRENT

BACKGROUND OF THE INVENTION

1. Field of Invention

This invention relates generally to direct current to alternating current converters.

2. Description of Related Art

Direct current to alternating current (DC/AC) converters generally receive electrical energy from a direct current (DC) source and employ switches to convert the DC into alternating current (AC) waveform for powering a load. The DC source may be a photovoltaic panel or a fuel cell, for example. The load may include common loads such as motors, lighting components, or other electrical appliances. Alternatively the DC/AC converter may be connected to provide power to an AC power grid.

In DC/AC converters, average power flow is generally from the DC source to the AC load, which is known as inverter mode operation. However, if the load includes capacitive or inductive components, the DC/AC converter is required to also receive reactive power back from the load, in which case the converter must also be able to operate in a rectifier mode of operation.

Various converter circuit configurations may be used to implement DC/AC converters. In one circuit configuration pairs of series-connected semiconductor switches are connected in parallel with a DC source to form a bridge circuit. An AC load is connected between respective common nodes of the series-connected switch pairs. The semiconductor switches may be switched in response to high-frequency pulse width modulated control signals received at respective control inputs of the switches. The control signals

generally cause the semiconductor switches to conduct current in a time sequence that produces a substantially sinusoidal AC waveform at the load.

It is generally desirable to configure DC/AC converter circuits to provide good electromagnetic compatibility (EMC), good conversion efficiency, and good fault tolerance. As described in US Patent **7,046,534** to Schmidt et al. EMC performance may be improved by configuring the converter circuit to prevent common mode voltages at the switching frequency from appearing at the DC source, while conversion efficiency may be improved by preventing current flow back to the source when the semiconductor switches are not conducting.

However DC/AC converter circuits, such as the bridge circuit described above and the circuit described in US Patent **7,046,534**, generally include series-connected switch pairs across the DC source. Such circuits may be susceptible to failure caused by timing errors in the control signals. For example, in the event that both of a pair of series-connected switches are both in a conducting state even for a short period of time, a short circuit appears across the DC source and can cause a fault current to flow through the switches. The fault current may damage or destroy the switches and/or the DC source, possibly resulting in a catastrophic failure of the converter. Series-connected switches may become simultaneously conducting under a variety of conditions, such as timing jitter in the control signals, failure of one or more components in a controller, and/or failure of a power supply for powering control signal generation circuitry, for example.

Circuits employing series-connected switch pairs thus have little or no inherent fault tolerance and consequently in such circuits the control signals for controlling the switches should be generated such that simultaneous conduction of series-connected switches can never occur. Commonly, control signals are generated such that both the first and the second switches of the series-connected pair are not conducting during a dead-time period when

commutation of the current between the first switch and the second switch occurs. The dead-time period must thus be of sufficient duration to ensure that a fault current condition cannot occur under worst case conditions. However operating the AC/DC converter with a sufficient time margin may reduce conversion efficiency and/or increase the total harmonic distortion (THD) of the AC waveform. Control signal generation should also take into account all conditions that could result in a fault current flowing. For this reason, many microprocessor based controllers utilize a digital signal processor (DSP) having sufficient processing power to implement control algorithms in real-time, at the cost of increased complexity of control circuitry.

There remains a need for DC/AC converter circuits that are less susceptible to failure.

SUMMARY OF THE INVENTION

In accordance with one aspect of the invention there is provided a method for converting a direct current received from a direct current source into an alternating current at first and second load nodes, the first and second load nodes for connecting a load, the source being connected to first and second source nodes, the first source node for receiving direct current from the source and the second source node for providing a return path for the direct current to the source. The method involves producing positive and negative half cycles of alternating current at the first and second load nodes, the positive half cycle being produced by causing first and second switching control signals to effect a plurality of positive half cycle switching sub-cycles by causing the first and second switching control signals to be asserted for a first time period of the positive half cycle switching sub-cycle and not asserted for a second time period of the positive half cycle switching sub-cycle. During each positive half cycle switching sub-cycle direct current flows from the source through a first supply current path into the first load node for the first time period. The first supply current path includes a first intermediate node, a

first switch operable to selectively conduct current from the first source node to the first intermediate node in response to the first switching control signal, and a first inductor connected between the first intermediate node and the first load node. A first return current flows from the second load node through a first return current path for the first time period. The first return current path includes a second intermediate node, a second inductor connected between the second load node and the second intermediate node, and a second switch operable to selectively conduct current from the second intermediate node to the second source node in response to the second switching control signal. During the second time period, a first shunt control signal is asserted to cause the first return current to flow through a first shunt from the second intermediate node to the first intermediate node and through the first inductor back to the first load node, the first shunt being operably configured to prevent current from flowing from the first intermediate node to the second intermediate node and to selectively conduct current between the second intermediate node and the first intermediate node in response to the first shunt control signal. The negative half cycle is produced by causing third and fourth switching control signals to effect a plurality of negative half cycle switching sub-cycles by causing the third and fourth switching control signals to be asserted for a third time period of the negative half cycle switching sub-cycle and to be not asserted for a fourth time period of the negative half cycle switching sub-cycle. During each negative half cycle switching sub-cycle direct current flows from the source through a second supply current path into the second load node for the third time period. The second supply current path includes a third intermediate node, a third switch operable to selectively conduct current from the first source node to the third intermediate node in response to the third switching control signal, and a third inductor connected between the third intermediate node and the second load node. A second return current flows from the first load node through a second return current path for the third time period. The second return current path includes a fourth intermediate node, a fourth inductor connected between the first load

node and the fourth intermediate node, and a fourth switch operable to selectively conduct current from the fourth intermediate node to the second source node in response to the fourth switching control signal. During the fourth time period, a second shunt control signal is asserted to cause the second return current to flow through a second shunt from the fourth intermediate node to the third intermediate node and through the third inductor back to the second load node, the second shunt being operably configured to prevent current from flowing from the third intermediate node to the fourth intermediate node and to selectively conduct current between the fourth intermediate node and the third intermediate node in response to the second shunt control signal.

The first shunt may include a fifth current switch and a first diode connected in series between the second intermediate node and the first intermediate node, the fifth current switch being operable to conduct current in response to the first shunt control signal, and the first diode being operable to block current flow between the first intermediate node and the second intermediate node.

The second shunt may include a sixth current switch and a second diode connected in series between the fourth intermediate node and the third intermediate node, the sixth current switch being operable to conduct current in response to the second shunt control signal, and the second diode being operable to block current flow between the third intermediate node and the fourth intermediate node.

The method may involve producing the first, second, third, and fourth switching control signals and the first and second shunt control signals.

Producing the first, second, third, and fourth switching control signals may involve producing first, second, third, and fourth pulse width modulated switching control signals.

Producing the first shunt control signal may involve causing the first shunt control signal to be asserted for substantially all of the positive half cycle, thereby causing the first shunt to permit current flow during substantially all of the positive half cycle, and producing the second shunt control signal may involve causing the second shunt control signal to be asserted for substantially all of the negative half cycle, thereby causing the second shunt to permit current flow during substantially all of the negative half cycle.

Producing the first shunt control signal may involve causing the first shunt control signal to be asserted during the second time periods of the positive half cycle, thereby causing the first shunt to selectively permit current flow during the second time periods, and producing the second shunt control signal may involve causing the second shunt control signal to be asserted during the fourth time periods of the negative half cycle, thereby causing the second shunt to selectively permit current flow during the fourth time periods.

Producing the first shunt control signal may involve inverting the first switching control signal and producing the second shunt control signal may involve inverting the third switching control signal.

Producing the first shunt control signal may involve causing the first shunt control signal to be asserted for a first portion of the positive half cycle and causing the first shunt control signal to be not asserted for a second portion of the positive half cycle, thereby causing the first shunt to selectively permit current flow during the first portion of the positive half cycle, and the first return current flows from the second intermediate node through a third diode to the first source node and from the second source node through a fourth diode to the first intermediate node during the second portion of the positive half cycle, and producing the second shunt control signal may involve causing the second shunt control signal to be asserted for a first portion of the

negative half cycle and causing the second shunt control signal to be not asserted for a second portion of the negative half cycle, thereby causing the second shunt to selectively permit current flow during the first portion of the negative half cycle, and the second return current flows from the second intermediate node through a fifth diode to the first source node and from the second source node through a sixth diode to the first intermediate node during the second portion of the negative half cycle.

Producing the first and second switching control signals may involve causing each of the first and second switching control signals to be asserted to cause both the first switch and the second switch to permit current flow during the first time period, and producing the third and fourth switching control signals may involve causing each of the third and fourth switching control signals to be asserted to cause both the third switch and the fourth switch to permit current flow during the third time period.

The method may involve receiving a reference signal representing a desired output voltage waveform and producing the first, second, third, and fourth switching control signals and the first and second shunt control signals may involve producing first, second, third, and fourth switching control signals and the first and second shunt control signals in response to the reference signal.

The method may involve producing the reference signal.

Producing the reference signal may involve producing a sinusoidal reference signal having a frequency defining a desired frequency of an output voltage waveform across the first and second load nodes.

The load may include a power grid load and the method may further involve receiving a reference signal representing a grid voltage waveform of the power grid across the first and second load nodes and producing the first,

second, third, and fourth switching control signals and the first and second shunt control signals may involve producing first, second, third, and fourth switching control signals and the first and second shunt control signals in response to the reference signal to cause an output current to be supplied to the power grid substantially in phase with the grid voltage waveform.

The load may involve a power grid load and the method may further involve receiving a signal representing a grid voltage waveform of the power grid across the first and second load nodes and producing a phase shifted reference signal in response to receiving the signal representing the grid voltage waveform, and producing the first, second, third, and fourth switching control signals and the first and second shunt control signals may involve producing first, second, third, and fourth switching control signals and the first and second shunt control signals in response to the phase shifted reference signal to cause an output current to be supplied to the power grid out of phase with the grid voltage waveform.

The method may involve, during a portion of the positive half cycle when the phase shifted reference signal is positive and the signal representing the grid voltage waveform is negative, causing the first and second switching control signals to be in a non-asserted state, and causing the first shunt control signal to effect a plurality of half cycle switching sub-cycles by causing the first shunt control signal to be asserted for a fifth time period of the positive half cycle switching sub-cycle and not asserted for a sixth time period of the positive half cycle switching sub-cycle. During the fifth time period the first return current flows through the first shunt from the second intermediate node to the first intermediate node and through the first inductor back to the first load node. During the sixth time period the first return current flows from the second intermediate node through a third diode to the first source node and from the second source node through a fourth diode to the first intermediate node and through the first inductor back to the first load node. The method also

involves, during a portion of the negative half cycle when the phase shifted reference signal is negative and the signal representing the grid voltage waveform is positive, causing the third and fourth switching control signals to be in a non-asserted state, and causing the second shunt control signal to effect a plurality of half cycle switching sub-cycles by causing the second shunt control signal to be asserted for a seventh time period of the negative half cycle switching sub-cycle and not asserted for an eighth time period of the negative half cycle switching sub-cycle. During the seventh time period the second return current flows through the second shunt from the fourth intermediate node to the third intermediate node and through the third inductor back to the second load node. During the eighth time period the second return current flows from the fourth intermediate node through a fifth diode to the first source node and from the second source node through a sixth diode to the third intermediate node and through the third inductor back to the second load node.

In accordance with another aspect of the invention there is provided an apparatus for converting a direct current into an alternating current. The apparatus includes first and second source nodes, the first source node being operably configured to receive direct current from a direct current source and the second source node being operably configured to provide a return path for the direct current from the apparatus to the source. The apparatus also includes first and second load nodes for supplying alternating current produced by the apparatus to a load. The apparatus also includes a first supply current path including a first intermediate node, a first switch operable to selectively conduct current from the first source node to the first intermediate node in response to a first switching control signal, and a first inductor connected between the first intermediate node and the first load node. The apparatus also includes a first return current path including a second intermediate node, a second inductor connected between the second load node and the second intermediate node, and a second switch operable

to selectively conduct current from the second intermediate node to the second source node in response to a second switching control signal. The apparatus further includes a first shunt operably configured to prevent current from flowing from the first intermediate node to the second intermediate node and to selectively conduct current between the second intermediate node and the first intermediate node in response to a first shunt control signal. The apparatus also includes a second supply current path including a third intermediate node, a third switch operable to selectively conduct current from the first source node to the third intermediate node in response to a third switching control signal, and a third inductor connected between the third intermediate node and the first load node. The apparatus also includes a second return current path including a fourth intermediate node, a fourth inductor connected between the second load node and the fourth intermediate node, and a fourth current switch operable to selectively conduct current from the fourth intermediate node to the second source node in response to a fourth switching control signal. The apparatus further includes a second shunt operably configured to prevent current from flowing from the third intermediate node to the fourth intermediate node and to selectively conduct current between the fourth intermediate node and the third intermediate node in response to a second shunt control signal. The apparatus also includes a controller operably configured to generate the first, second, third, and fourth switching control signals and the first and second shunt control signals to control the first, second, third, and fourth switches and the first and second shunts to produce positive and negative half cycles of the alternating current, the positive half cycle being produced by causing the first and second switching control signals to effect a plurality of positive half cycle switching sub-cycles by causing the first and second switching control signals to be asserted for a first time period of the positive half cycle switching sub-cycle and not asserted for a second time period of the positive half cycle switching sub-cycle. During each positive half cycle switching sub-cycle direct current flows from the source through the first supply current path into the first load

node for the first time period and a first return current flows from the second load node through the first return current path for the first time period. During the second time period, the first shunt control signal is asserted to cause the first return current to flow through the first shunt from the second intermediate node to the first intermediate node and through the first inductor back to the first load node. The negative half cycle is produced by causing the switching control signals to effect a plurality of negative half cycle switching sub-cycles by causing the third and fourth switching control signals to be asserted for a third time period of the negative half cycle switching sub-cycle and to be not asserted for a fourth time period of the negative half cycle switching sub-cycle. During each negative half cycle switching sub-cycle direct current flows from the source through the second supply current path into the second load node for the third time period, and a second return current flows from the first load node through the second return current path for the third time period. During the fourth time period, the second shunt control signal is asserted to cause the second return current to flow through the second shunt from the fourth intermediate node to the third intermediate node and through the third inductor back to the second load node.

The second shunt may include a sixth current switch and a second diode connected in series between the fourth intermediate node and the third intermediate node, the sixth current switch being operable to conduct current in response to the second shunt control signal, and the second diode being operable to block current flow between the third intermediate node and the fourth intermediate node.

The apparatus may include a capacitor connected between the first and second load nodes, the capacitor being operable, in combination with the first, second, third, and fourth inductors, to attenuate alternating current frequency components at frequencies other than a fundamental frequency associated with the alternating current waveform.

The apparatus may include a controller operably configured to produce the first, second, third, and fourth switching control signals and the first and second shunt control signals.

The controller may be operably configured to produce first, second, third, and fourth pulse width modulated switching control signals.

The controller may be operably configured to produce the first shunt control signal by causing the first shunt control signal to be asserted for substantially all of the positive half cycle, thereby causing the first shunt to permit current flow during substantially all of the positive half cycle, and the controller is operably configured to produce the second shunt control signal by causing the second shunt control signal to be asserted for substantially all of the negative half cycle, thereby causing the second shunt to permit current flow during substantially all of the negative half cycle.

The controller may be operably configured to produce the first shunt control signal by causing the first shunt control signal to be asserted during the second time periods of the positive half cycle, thereby causing the first shunt to selectively permit current flow during the second time periods, and the controller is operably configured to produce the second shunt control signal by causing the second shunt control signal to be asserted during the fourth time periods of the negative half cycle, thereby causing the second shunt to selectively permit current flow during the fourth time periods.

The controller may be operably configured to produce the first shunt control signal by inverting the first switching control signal and to produce the second shunt control signal by inverting the third switching control signal.

The apparatus may include a third diode connected to conduct current between the second intermediate node and the first source node, a fourth diode connected to conduct current between the second source node and the first intermediate node, a fifth diode connected to conduct current between the fourth intermediate node and the first source node, and a sixth diode connected to conduct current between the second source node and the third intermediate node, and the controller may be operably configured to produce the first shunt control signal by causing the first shunt control signal to be asserted for a first portion of the positive half cycle and causing the first shunt control signal to be not asserted for a second portion of the positive half cycle, thereby causing the first shunt to selectively permit current flow during the first portion of the positive half cycle, and the first return current flows from the second intermediate node through the third diode to the first source node and from the second source node through the fourth diode to the first intermediate node during the second portion of the positive half cycle, and produce the second shunt control signal by causing the second shunt control signal to be asserted for a first portion of the negative half cycle and causing the second shunt control signal to be not asserted for a second portion of the negative half cycle, thereby causing the second shunt to selectively permit current flow during the first portion of the negative half cycle, and the second return current flows from the second intermediate node through the fifth diode to the first source node and from the second source node through the sixth diode to the first intermediate node during the second portion of the negative half cycle.

The controller may be operably configured to produce the first and second switching control signals by causing each of the first and second switching control signals to be asserted to cause both the first switch and the second switch to permit current flow during the first time period, and produce the third and fourth switching control signals by causing each of the third and fourth

switching control signals to be asserted to cause both the third switch and the fourth switch to permit current flow during the third time period.

The controller may be operably configured to receive a reference signal representing a desired output voltage waveform and to produce the first, second, third, and fourth switching control signals and the first and second shunt control signals in response to the reference signal.

The controller may be operably configured to produce the reference signal.

The controller may be operably configured to produce a sinusoidal reference signal having a frequency defining a desired frequency of an output voltage waveform across the first and second load nodes.

The load may include a power grid load and the controller may be operably configured to receive a reference signal representing a grid voltage waveform of the power grid across the first and second load nodes and to produce the first, second, third, and fourth switching control signals and the first and second shunt control signals in response to the reference signal to cause an output current to be supplied to the power grid substantially in phase with the grid voltage waveform.

The load may include a power grid load and the controller may be operably configured to receive a signal representing a grid voltage waveform of the power grid across the first and second load nodes, produce a phase shifted reference signal in response to receiving the signal representing the grid voltage waveform, and produce the first, second, third, and fourth switching control signals and the first and second shunt control signals in response to the phase shifted reference signal to cause an output current to be supplied to the power grid out of phase with the grid voltage waveform.

The controller may be operably configured to cause the first and second switching control signals to be in a non-asserted state during a portion of the positive half cycle when the phase shifted reference signal is positive and the signal representing the grid voltage waveform is negative and to cause the first shunt control signal to effect a plurality of half cycle switching sub-cycles by causing the first shunt control signal to be asserted for a fifth time period of the positive half cycle switching sub-cycle and not asserted for a sixth time period of the positive half cycle switching sub-cycle during the portion of the positive half cycle. During the fifth time period the first return current flows through the first shunt from the second intermediate node to the first intermediate node and through the first inductor back to the first load node, and during the sixth time period the first return current flows from the second intermediate node through a third diode to the first source node and from the second source node through a fourth diode to the first intermediate node and through the first inductor back to the first load node. The controller may also be operably configured to cause the third and fourth switching control signals to be in a non-asserted state during a portion of the negative half cycle when the phase shifted reference signal is negative and the signal representing the grid voltage waveform is positive to cause the second shunt control signal to effect a plurality of half cycle switching sub-cycles by causing the second shunt control signal to be asserted for a seventh time period of the negative half cycle switching sub-cycle and not asserted for an eighth time period of the negative half cycle switching sub-cycle during the portion of the negative half cycle. During the seventh time period the second return current flows through the second shunt from the fourth intermediate node to the third intermediate node and through the third inductor back to the second load node, and during the eighth time period the second return current flows from the fourth intermediate node through a fifth diode to the first source node and from the second source node through a sixth diode to the third intermediate node and through the third inductor back to the second load node.

The first shunt may include a fifth current switch and a first diode connected in series between the second intermediate node and the first intermediate node, the fifth current switch being operable to conduct current in response to the first shunt control signal, and the first diode being operable to block current flow between the first intermediate node and the second intermediate node.

The first and second load nodes may include respective first and second load terminals operably configured to facilitate connecting the load to the first and second load nodes.

The first and second source nodes may include respective first and second source terminals operably configured to facilitate connecting the source to the first and second source nodes.

In accordance with another aspect of the invention there is provided an apparatus for converting a direct current into an alternating current. The apparatus includes first and second source nodes, the first source node being operably configured to receive direct current from a direct current source and the second source node being operably configured to provide a return path for the direct current from the apparatus to the source. The apparatus also includes first and second load nodes for supplying alternating current produced by the apparatus to a load. The apparatus also includes a first supply current path including a first intermediate node, a first switch operable to selectively conduct current from the first source node to the first intermediate node in response to a first switching control signal, and a first inductor connected between the first intermediate node and the first load node. The apparatus also includes a first return current path including a second intermediate node, a second inductor connected between the second load node and the second intermediate node, and a second switch operable to selectively conduct current from the second intermediate node to the second source node in response to a second switching control signal. The

apparatus further includes a first shunt operably configured to prevent current from flowing from the first intermediate node to the second intermediate node and to selectively conduct current between the second intermediate node and the first intermediate node in response to a first shunt control signal. The apparatus also includes a second supply current path including a third intermediate node, a third switch operable to selectively conduct current from the first source node to the third intermediate node in response to a third switching control signal, and a third inductor connected between the third intermediate node and the first load node. The apparatus also includes a second return current path including a fourth intermediate node, a fourth inductor connected between the second load node and the fourth intermediate node, and a fourth current switch operable to selectively conduct current from the fourth intermediate node to the second source node in response to a fourth switching control signal. The apparatus further includes a second shunt operably configured to prevent current from flowing from the third intermediate node to the fourth intermediate node and to selectively conduct current between the fourth intermediate node and the third intermediate node in response to a second shunt control signal. The apparatus also includes controlling provisions for generating the first, second, third, and fourth switching control signals and the first and second shunt control signals to control the first, second, third, and fourth switches and the first and second shunts to produce positive and negative half cycles of the alternating current, the positive half cycle being produced by causing the first and second switching control signals to effect a plurality of positive half cycle switching sub-cycles by causing the first and second switching control signals to be asserted for a first time period of the positive half cycle switching sub-cycle and not asserted for a second time period of the positive half cycle switching sub-cycle. During each positive half cycle switching sub-cycle direct current flows from the source through the first supply current path into the first load node for the first time period, and a first return current flows from the second load node through the first return current path for the first time period. During

the second time period, the first shunt control signal is asserted to cause the first return current to flow through the first shunt from the second intermediate node to the first intermediate node and through the first inductor back to the first load node. The negative half cycle is produced by causing the switching control signals to effect a plurality of negative half cycle switching sub-cycles by causing the third and fourth switching control signals to be asserted for a third time period of the negative half cycle switching sub-cycle and to be not asserted for a fourth time period of the negative half cycle switching sub-cycle. During each negative half cycle switching sub-cycle direct current flows from the source through the second supply current path into the second load node for the third time period, and a second return current flows from the first load node through the second return current path for the third time period. During the fourth time period, the second shunt control signal is asserted to cause the second return current to flow through the second shunt from the fourth intermediate node to the third intermediate node and through the third inductor back to the second load node.

The controller provisions may include provisions for producing first, second, third, and fourth pulse width modulated switching control signals.

The controller provisions may include provisions for producing the first shunt control signal by causing the first shunt control signal to be asserted for substantially all of the positive half cycle, thereby causing the first shunt to permit current flow during substantially all of the positive half cycle, and the controller provisions may include provisions for producing the second shunt control signal by causing the second shunt control signal to be asserted for substantially all of the negative half cycle, thereby causing the second shunt to permit current flow during substantially all of the negative half cycle.

The controller provisions may include provisions for producing the first shunt control signal by causing the first shunt control signal to be asserted during

the second time periods of the positive half cycle, thereby causing the first shunt to selectively permit current flow during the second time periods, and the controller provisions may include provisions for producing the second shunt control signal by causing the second shunt control signal to be asserted during the fourth time periods of the negative half cycle, thereby causing the second shunt to selectively permit current flow during the fourth time periods.

The controller provisions may include provisions for inverting the first switching control signal and the third switching control signal to respectively produce the second switching control signal and the fourth switching control signal.

The apparatus may include a third diode connected to conduct current between the second intermediate node and the first source node, a fourth diode connected to conduct current between the second source node and the first intermediate node, a fifth diode connected to conduct current between the fourth intermediate node and the first source node, and a sixth diode connected to conduct current between the second source node and the third intermediate node, and the controller provisions may include provisions for producing the first shunt control signal by causing the first shunt control signal to be asserted for a first portion of the positive half cycle and causing the first shunt control signal to be not asserted for a second portion of the positive half cycle, thereby causing the first shunt to selectively permit current flow during the first portion of the positive half cycle, and the first return current flows from the second intermediate node through the third diode to the first source node and from the second source node through the fourth diode to the first intermediate node during the second portion of the positive half cycle, and provisions for producing the second shunt control signal by causing the second shunt control signal to be asserted for a first portion of the negative half cycle and causing the second shunt control signal to be not asserted for a second portion of the negative half cycle, thereby causing the second shunt to

selectively permit current flow during the first portion of the negative half cycle, and the second return current flows from the second intermediate node through the fifth diode to the first source node and from the second source node through the sixth diode to the first intermediate node during the second portion of the negative half cycle.

The controller provisions may include provisions for producing the first and second switching control signals by causing each of the first and second switching control signals to be asserted to cause both the first switch and the second switch to permit current flow during the first time period, and provisions for producing the third and fourth switching control signals by causing each of the third and fourth switching control signals to be asserted to cause both the third switch and the fourth switch to permit current flow during the third time period.

The controller provisions may include provisions for receiving a reference signal representing a desired output voltage waveform and provisions for producing the first, second, third, and fourth switching control signals and the first and second shunt control signals in response to the reference signal.

The controller provisions may include provisions for producing the reference signal.

The controller provisions may include provisions for producing a sinusoidal reference signal having a frequency defining a desired frequency of an output voltage waveform across the first and second load nodes.

The load may include a power grid load and the controller provisions may include provisions for receiving a reference signal representing a grid voltage waveform of the power grid across the first and second load nodes and provisions for producing the first, second, third, and fourth switching control

signals and the first and second shunt control signals in response to the reference signal to cause an output current to be supplied to the power grid substantially in phase with the grid voltage waveform.

The load may include a power grid load and the controller provisions may include provisions for receiving a signal representing a grid voltage waveform of the power grid across the first and second load nodes, provisions for producing a phase shifted reference signal in response to receiving the signal representing the grid voltage waveform, and provisions for producing the first, second, third, and fourth switching control signals and the first and second shunt control signals in response to the phase shifted reference signal to cause an output current to be supplied to the power grid out of phase with the grid voltage waveform.

The controller provisions may include provisions for causing the first and second switching control signals to be in a non-asserted state during a portion of the positive half cycle when the phase shifted reference signal is positive and the signal representing the grid voltage waveform is negative, provisions for causing the first shunt control signal to effect a plurality of half cycle switching sub-cycles by causing the first shunt control signal to be asserted for a fifth time period of the positive half cycle switching sub-cycle and not asserted for a sixth time period of the positive half cycle switching sub-cycle during the portion of the positive half cycle. During the fifth time period the first return current flows through the first shunt from the second intermediate node to the first intermediate node and through the first inductor back to the first load node, and during the sixth time period the first return current flows from the second intermediate node through a third diode to the first source node and from the second source node through a fourth diode to the first intermediate node and through the first inductor back to the first load node. The controller provisions may also include provisions for causing the third and fourth switching control signals to be in a non-asserted state during a portion

of the negative half cycle when the phase shifted reference signal is negative and the signal representing the grid voltage waveform is positive, and provisions for causing the second shunt control signal to effect a plurality of half cycle switching sub-cycles by causing the second shunt control signal to be asserted for a seventh time period of the negative half cycle switching sub-cycle and not asserted for an eighth time period of the negative half cycle switching sub-cycle during the portion of the negative half cycle. During the seventh time period the second return current flows through the second shunt from the fourth intermediate node to the third intermediate node and through the third inductor back to the second load node, and during the eighth time period the second return current flows from the fourth intermediate node through a fifth diode to the first source node and from the second source node through a sixth diode to the third intermediate node and through the third inductor back to the second load node.

Other aspects and features of the present invention will become apparent to those ordinarily skilled in the art upon review of the following description of specific embodiments of the invention in conjunction with the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

In drawings which illustrate embodiments of the invention,

Figure **1** is a schematic diagram of an apparatus for converting a direct current into an alternating current according to a first embodiment of the invention;

Figure **2** is a block diagram of a processor circuit used to implement a controller for controlling the apparatus shown in Figure **1**;

Figure **3** is a graphical depiction of control signals produced by the controller shown in Figure **2** when operating in accordance with one embodiment if the invention;

Figure **4** is a graphical depiction of control signals produced by the controller shown in Figure **2** when operating in accordance with an alternative embodiment if the invention; and

Figure **5** is a graphical depiction of control signals produced by the controller shown in Figure **2** when operating to supply power to a power grid load in accordance with an alternative embodiment if the invention.

DETAILED DESCRIPTION

Referring to Figure **1**, an apparatus for converting a direct current into an alternating current in accordance with a first embodiment of the invention is shown generally at **100**. The apparatus **100** includes first and second source nodes **102** and **104**. The first source node **102** is operably configured to receive direct current from a DC source **106** and the second source node **104** is operably configured to provide a return path for the direct current from the apparatus **100** to the DC source **106**. The apparatus **100** also includes first and second load nodes **108** and **110** for supplying alternating current produced by the apparatus **100** to a load **112**. The source nodes **102** and **104** and the load nodes **108** and **110** may comprise electrical terminals such as screw terminals, spade lugs, or socket terminals, for example.

A first supply current path **113** through the apparatus **100** includes a first intermediate node **114** and a first switch (Q1) **116** connected between the first source node **102** and the first intermediate node **114**. The first switch **116** is operable to selectively conduct current from the first source node **102** to the

first intermediate node **114** in response to a first switching control signal $Q1_{on}$. The apparatus **100** also includes a first inductor (L1) **118** connected between the first intermediate node **114** and the first load node **108**.

A first return current path **119** through the apparatus **100** includes a second intermediate node **120** and a second inductor (L2) **122** connected between the second load node **110** and the second intermediate node. The first return current path **119** also includes a second switch (Q2) **124** connected between the second intermediate node **120** and the second source node **104**. The second switch **124** is operable to selectively conduct current from the second intermediate node **120** to the second source node **104** in response to a second switching control signal $Q2_{on}$.

The apparatus **100** further includes a first shunt **126** connected between the first and second intermediate nodes **114** and **120**. The first shunt **126** is operably configured to prevent current from flowing from the first intermediate node **114** to the second intermediate node **120** and to selectively conduct current between the second intermediate node and the first intermediate node in response to a first shunt control signal $Q5_{on}$.

A second supply current path **127** through the apparatus **100** includes a third intermediate node **128** and a third switch (Q3) **130** connected between the first source node **102** and the third intermediate node. The third switch **130** is operable to selectively conduct current from the first source node **102** to the third intermediate node **128** in response to a third switching control signal $Q3_{on}$. The apparatus **100** also includes a third inductor (L3) **132** connected between the third intermediate node **128** and the second load node **110**.

A second return current path **133** through the apparatus **100** includes a fourth intermediate node **134** and a fourth inductor (L4) **136** connected between the first load node **108** and the fourth intermediate node. The second return

current path **133** also includes a fourth current switch (Q**4**) **138** connected between the fourth intermediate node **134** and the second source node **104**. The fourth current switch **138** is operable to selectively conduct current from the fourth intermediate node **134** to the second source node **104** in response to a fourth switching control signal $Q4_{on}$.

The apparatus **100** further includes a second shunt **140** connected between the third and fourth intermediate nodes **128** and **134**. The second shunt **140** is operably configured to prevent current from flowing from the third intermediate node **128** to the fourth intermediate node **134** and to selectively conduct current between the fourth intermediate node and the third intermediate node in response to a second shunt control signal $Q6_{on}$.

In the embodiment shown, the first shunt **126** includes a fifth switch (Q**5**) **164** and a first diode (D**1**) **166** connected in series between the first intermediate node **114** and the second intermediate node **120**. The first diode **166** blocks current from flowing from the first intermediate node **114** to the second intermediate node **120**, and permits current flow from the second intermediate node to the first intermediate node when the fifth switch **164** is switched on. Similarly, in this embodiment, the second shunt **140** includes a sixth switch (Q**6**) **168** and a second diode (D**2**) **170** connected in series between the third intermediate node **128** and the fourth intermediate node **134**. The second diode **170** blocks current flowing from the third intermediate node **128** to the fourth intermediate node **134**, and permits current flow from the fourth intermediate node to the third intermediate node when the sixth switch **168** is switched on.

In embodiment shown, Q**1** to Q**6** are semiconductor switches such as an insulated gate bipolar transistor (IGBT), a metal–oxide–semiconductor field-effect transistor (MOSFET), a bipolar junction transistor (BJT), or a junction field-effect transistor (JFET). The first switch **116** includes a control signal

input **156** for receiving the first switching control signal $Q1_{on}$ for controlling the conduction state of the first switch between an "on" state, where the switch conducts current, and an "off" state, where the switch conducts no more than a small leakage current. Similarly the switches Q**2** to Q**6** each include respective control signal inputs **158, 160, 162, 165**, and **167** for receiving respective control signals $Q2_{on}$, $Q3_{on}$, $Q4_{on}$, $Q5_{on}$, and $Q6_{on}$ for controlling the conduction state of the respective switches.

In the embodiment shown in Figure **1**, the apparatus **100** also includes a third diode (D**3**) **184** connected to conduct current between the second intermediate node **120** and the first source node **102**, and a fourth diode (D**4**) **186** connected to conduct current between the second source node **104** and the first intermediate node **114**. The apparatus **100** also optionally includes a fifth diode (D**5**) **188** connected to conduct current between the fourth intermediate node **134** and the first source node **102**, and a sixth diode (D**6**) **190** connected to conduct current between the second source node **104** and the third intermediate node **128**. If included, the third, fourth, fifth and sixth diodes **184**, **186**, **188**, and **190** provide a current path back to the DC source **106** when none of the first, second, third or fourth switches **116**, **124**, **130** and **138**, or the shunts **126** and **140** are conducting, as described later herein.

In the embodiment shown in Figure **1**, the apparatus **100** also includes a capacitor **196** (C**1**). The capacitor **196**, together with the inductors **118**, **122**, **132**, and **136** provide low pass filtering of the alternating current by attenuating alternating current frequency components at frequencies other than a fundamental frequency associated with the alternating current waveform. For example, a capacitance value of the capacitor **196** and inductance values of the inductors **118**, **122**, **132**, and **136** may be selected to provide negligible attenuation at power grid frequencies (e.g. **50**Hz or **60**Hz) and high attenuation of higher harmonics of the power grid frequency that would otherwise cause distortion of the output alternating current waveform.

In the circuit configuration shown in Figure **1**, additional circuit components may also be included (not shown) to provide further filtering of DC source current and/or AC output current. For example, such circuit components may include a capacitor across the source nodes **102** and **104** for filtering the DC source current.

In one embodiment the apparatus **100** may be configured as a grid-tied inverter that provides AC current to a power grid load, in which case the load **112** is the power grid, and the load nodes **108** and **110** are connected to the power grid. In other embodiments the apparatus **100** may be configured for islanded operation in which the apparatus provides AC current to a local load **112**, which is not connected to a power grid.

Controller

The apparatus **100** further includes a controller **142**, which includes a plurality of outputs **144, 146, 148** and **150** for generating the first, second, third, and fourth switching control signals $Q1_{on}$, $Q2_{on}$, $Q3_{on}$, and $Q4_{on}$ and outputs **152** and **154** for producing the first and second shunt control signals $Q5_{on}$ and $Q6_{on}$. The outputs **144, 146, 148** and **150** of the controller **142** are coupled to respective control signal inputs **156**, **158**, **160**, and **162** of Q1 – Q4 and the outputs **152** and **154** are coupled to the control signal inputs **165** and **167** of Q5 and Q6 respectively. The switching control signals $Q1_{on}$ - $Q4_{on}$ are operable to control the first, second, third, and fourth switches **116**, **124**, **130**, and **138** and the shunt control signals $Q5_{on}$ and $Q6_{on}$ are operable to control respective first and second shunts **126** and **140** to produce positive and negative half cycles of an AC output waveform at the first and second load nodes **108** and **110**. In one embodiment the controller produces control signals $Q1_{on}$ - $Q6_{on}$ with voltage and current levels suitable for driving the switches Q1 – Q6 directly, and may be coupled directly to the respective control signal inputs **156, 158, 160, 162**, **165**, and **167**. In other embodiments the control signals $Q1_{on}$ - $Q6_{on}$ may be logic level signals and the apparatus

100 may further include driver circuitry (not shown) for converting the logic level signals into suitable control signals for driving the respective switches Q**1** – Q**6**.

Referring to Figure **2**, in one embodiment the controller **142** may be implemented using a processor circuit as shown generally at **200**. In this embodiment, the processor circuit **200** includes a microprocessor **202**, a program memory **204**, a random access memory (RAM) **206**, and an input output port (I/O) **208**, all of which are in communication with the microprocessor **202**.

Program codes for directing the microprocessor **202** to carry out various functions are stored in the program memory **204**, which may be implemented as a flash memory, for example.

The I/O port **208** includes an interface **210** having a first input **212** for receiving a voltage reference signal v_{ref} or a grid voltage signal v_{grid} representing a voltage waveform of a power grid. The I/O port **208** further includes the outputs **144, 146, 148, 150, 152,** and **154** for producing the control signals $Q1_{on}$ - $Q6_{on}$.

The RAM **206** may include volatile and/or non-volatile memory and provides storage for operating parameters and local storage for variables used during operation in accordance with the program codes.

In general, the program codes in the program memory **204** direct the microprocessor **202** to receive the reference signal v_{ref} or the grid voltage signal v_{grid} at the input **212** of the I/O port **208** and to produce the first, second, third, and fourth switching control signals ($Q1_{on}$ - $Q4_{on}$) at the outputs **144, 146, 148,** and **150**, and the first and second shunt control signals $Q5_{on}$ and $Q6_{on}$ at the outputs **152** and **154** to cause an alternating current to be supplied

to the load **112**. The reference signal v_{ref} may be generated externally to the processor circuit **200**, for example by an external signal generator (not shown). Alternatively, the program codes in the program memory **204** may direct the microprocessor **202** to generate the reference signal v_{ref} internally by producing a set of digital values representing voltages defining a reference signal waveform. Such values may be generated using processor circuit timing functions that use a microprocessor clock signal as a timing reference, for example.

The processor circuit **200** may be implemented using a general purpose microprocessor, or alternatively may be implemented using a digital signal processing (DSP) processor such as the TMS**320**LF**2407**APGE processor produced by Texas Instruments of Dallas, Texas, for example. The TMS**320**LF**2407**APGE processor is optimized for digital motor control and power conversion applications and thus generally works well in this application. In other embodiments (not shown), the controller processor circuit **200** may be partly or fully implemented using a hardware circuit including analog electronic components, and/or discrete logic circuits, for example. Various other analog electronic components, and/or discrete logic circuits may be used to provide interfacing between the apparatus **100** and the processor circuit **200**.

A positive half cycle of the alternating current waveform is produced by causing the first and second switching control signals $Q1_{on}$ and $Q2_{on}$ and the first and second shunt control signal $Q5_{on}$ to be asserted to effect a plurality of positive half cycle switching sub-cycles. During a first time period of each positive half cycle switching sub-cycle when the first and second switching control signals $Q1_{on}$ and $Q2_{on}$ are asserted, direct current flows from the DC source **106** through the first supply current path **113** into the first load node **108**, and a first return current flows from the second load node **110** through the first return current path **119** to the second source node **104**. During a

second time period of each positive half cycle switching sub-cycle when the first and second switching control signals $Q1_{on}$ and $Q2_{on}$ are not asserted, the first shunt control signal $Q5_{on}$ is asserted and the return current flows through the first shunt **126** along a first shunt current path **192** from the second intermediate node **120** to the first intermediate node **114**.

The negative half cycle of the alternating current waveform is produced by causing the third and fourth switching control signals $Q3_{on}$ and $Q4_{on}$ and the second shunt control signal $Q6_{on}$ to be asserted to effect a plurality of negative half cycle switching sub-cycles. During a third time period of each negative half cycle switching sub-cycle when the third and fourth switching control signals $Q3_{on}$ and $Q4_{on}$ are asserted, direct current flows from the DC source **106** through the second supply current path **127** into the second load node **110**, and a second return current flows from the first load node **108** through the second return current path **133**. During a fourth time period of each negative half cycle switching sub-cycle when the third and fourth switching control signals $Q3_{on}$ and $Q4_{on}$ are not asserted, the second shunt control signal $Q6_{on}$ is asserted and the second return current flows through the second shunt **140** along a second shunt current path **194** from the fourth intermediate node **134** to the third intermediate node **128**.

In this embodiment, each of the switches **Q1** to **Q6** also includes a respective anti-parallel diode **172, 174, 176, 178, 180,** and **182** connected across the switch. Semiconductor switches are generally available with an anti-parallel diode co-packaged together with the switch. Most semiconductor switches generally only permit current flow in one direction, and the inclusion of an anti-parallel diode facilitates bi-directional current flow through the combination of switch and anti-parallel diode.

In the circuit configuration shown in Figure **1**, the first shunt **126** conducts current during the positive half cycle when the first and second switches **116**

and **124** are not conducting and the second shunt **140** conducts current during the positive half cycle when the third and fourth switches **130** and **138** are not conducting. Advantageously, shunting the current through respective shunts **126** and **140** provides a path for current flow when the first and second switches **116** and **124** or the third and fourth switches **130** and **138** are not conducting, without returning current through the anti-parallel diodes **172, 174, 176, 178, 180,** and **182** to the DC source **106**. Returning current through anti-parallel diodes to the DC source is generally associated with higher conversion losses. Accordingly in the apparatus **100**, the anti-parallel diodes **172, 174, 176, 178, 180,** and **182** are only included for transient protection and are not required to conduct supply or return currents. Consequently, in the circuit configuration shown in Figure **1**, anti-parallel diodes that have a lower current rating than required in conventional inverter circuits may be used.

Grid-tied Operation

The operation of the apparatus **100** shown in Figure **1** to supply AC current to a power grid load **112** is described with reference to Figure **1** and Figure **3**. Referring to Figure **1**, in grid-tied operation, the load nodes **108** and **110** of the apparatus **100** are connected to a power grid. Generally, the power grid acts as a low impedance voltage source, and the apparatus **100** is controlled to act as a current source for supplying an output current to the power grid at the first and second load nodes **108** and **110**. In grid-tied operation, the apparatus **100** further includes a voltage sensor **198** connected between the first and second load nodes **108** and **110** for sensing the voltage v_o appearing across the first and second load nodes. In this embodiment, the voltage v_o is the power grid voltage. The voltage sensor **198** produces a grid voltage signal v_{grid} representing the power grid voltage and having a suitable amplitude for coupling to the input **212** of the I/O port **208** shown in Figure **2** and having a frequency and phase corresponding to the frequency and phase of a waveform of the power grid voltage at the load nodes **108** and **110**. The

interface **210** (shown in Figure **2**) may include an analog-to-digital converter for converting an analog grid voltage signal v_{grid} into a digital representation thereof.

Referring to Figure **3**, a waveform of the reference signal v_{ref} is shown generally at **240**. The reference signal v_{ref} has a waveform that generally corresponds to the grid voltage signal v_{grid} produced by the voltage sensor **198**, and this embodiment the waveforms of the reference signal v_{ref} and the grid voltage signal v_{grid} are in phase. In other embodiments the reference signal v_{ref} may be shifted in phase with respect to the grid voltage signal v_{grid} to cause an output AC current waveform to be produced that is out of phase with the grid voltage waveform. The waveform of the reference signal v_{ref} includes periodically repeating positive and negative half-cycles **242** and **244**.

A waveform of the first and second switching control signals $Q1_{on}$ and $Q2_{on}$ is shown at **246**. The first and second switching control signals $Q1_{on}$ and $Q2_{on}$ control the respective conduction states of the first and second switches **116** and **124** during the positive half cycle **242**. In this embodiment the first and second switching control signals $Q1_{on}$ and $Q2_{on}$ have substantially the same waveforms and accordingly the first and second switches **116** and **124** are switched substantially simultaneously. However, it should be understood that actual signals for driving respective control inputs **156** and **158** of first and second switches **116** and **124** may be level shifted as required for driving the particular switching devices Q1 and Q2 that are used in the apparatus **100**. The first and second switching control signals $Q1_{on}$ and $Q2_{on}$ include a plurality of positive half cycle switching sub-cycles **250**. During each sub-cycle **250**, the first and second switching control signals $Q1_{on}$ and $Q2_{on}$ are in an asserted state for a first time period **252** and in a non-asserted state for a second time period **254**. In this embodiment, a duty cycle of the switching first and second control signals $Q1_{on}$ and $Q2_{on}$ is pulse width modulated such that the first time periods **252** of the switching sub-cycles **250** occupy

progressively greater proportions of the sub-cycle than the second time periods **254**, towards a peak **243** of the positive half-cycle **242**. The first time periods **252** also occupy progressively lesser proportions of the sub-cycle than the second time periods **254** as the output current waveform approaches zero crossings (as shown at **245** and **247** in Figure **3**).

Referring back to Figure **1**, when the first switching control signal $Q1_{on}$ is asserted, the first switch **116** is switched on to conduct current from the DC source **106** to the power grid load **112** along the first supply current path **113** and accordingly, current flows from the first source node **102**, to the first intermediate node **114**, through the first inductor **118**, and to the first load node **108**. When the second switching control signal $Q2_{on}$ is asserted, the second switch **124** is switched on to conduct current along the first return current path **119** to the DC source **106** and accordingly, current flows back from the power grid load **112**, from the second load node **110**, through the second inductor **122**, to the second intermediate node **120**, and back to the second source node **104**. During respective first time periods **252** (shown in Figure **3**), when current flows along the first supply current path **113** and the first return current path **119**, the first diode **166** is reverse biased, thus blocking current from flowing between the first intermediate node **114** and the second intermediate node **120**. During the positive half cycles **242** the third and fourth switches **130** and **138** are switched off.

Referring back to Figure **3**, a waveform of the first shunt control signal $Q5_{on}$ for controlling the conduction state of the fifth switch **164** is shown at **248**. In this embodiment the first shunt control signal $Q5_{on}$ is asserted for substantially the entire positive half cycle **242**, thereby causing the fifth switch **164** to be on for substantially the entire positive half cycle. In an alternative embodiment, the first switching control signal $Q1_{on}$ (or the second switching control signal $Q2_{on}$) may be inverted to produce the first shunt control signal $Q5_{on}$, such that the first shunt control signal is asserted when the first and second switching

control signals $Q1_{on}$ and $Q2_{on}$ are not asserted. In this alternative embodiment, during the positive half cycle the fifth switch **164** is switched on to permit current flow through the shunt **126** when the first and second switches **116** and **124** are switched off.

When the first and second switching control signals $Q1_{on}$ and $Q2_{on}$ are not asserted, the first and second switches **116** and **124** are switched off thus interrupting the flow of current from the DC source **106** (except for a small leakage current through the first and second switches). However, the inductors **118** and **122** act to oppose changes in current flow, and current continues to flow into the first load node **108** and back from the second load node **110**, and is shunted through the first shunt current path **192** between the second intermediate node **120** and the first intermediate node **114**. The first shunt current path **192** thus provides a path through the fifth switch **164** and the first diode **166** for the first return current during the second time periods **254**, and consequently the first return current does not flow back to the DC source **106** through the third and fourth diodes **184** and **186** or the anti-parallel diodes **176** and **178**.

The AC output current waveform i_0 is shown at **266** in Figure **3**. An instantaneous amplitude of the positive half cycle of the output current i_0 is proportional to the time for which the first and second switching control signals $Q1_{on}$ and $Q2_{on}$ are asserted. At a peak **268** of the output current waveform i_o, the first and second switching control signals $Q1_{on}$ and $Q2_{on}$ are predominantly in an asserted state, while proximate zero crossings of the output current waveform at **270**, the first and second switching control signals are predominantly in a non-asserted state. The inductors **118** and **122** resist changes in current flow and thus produce a generally smooth sinusoidal positive half cycle of the output current waveform i_o at the load nodes **108** and **110**.

Still referring to Figure **3**, a waveform of the third and fourth switching control signals $Q3_{on}$ and $Q4_{on}$ is shown at **262**. The third and fourth switching control signals $Q3_{on}$ and $Q4_{on}$ control the respective conduction states of the third and fourth switches **130** and **138** during the negative half cycle **244**. The third and fourth switching control signals $Q3_{on}$ and $Q4_{on}$ include a plurality of negative half cycle switching sub-cycles **256**. During each sub-cycle **256**, the third and fourth switching control signals $Q3_{on}$ and $Q4_{on}$ are in an asserted state for a third time period **258** and in a non-asserted state for a fourth time period **260**. As in the case of the first and second switching control signals $Q1_{on}$ and $Q2_{on}$, the third and fourth switching control signals $Q3_{on}$ and $Q4_{on}$ are pulse width modulated and have the same waveform timing, and thus in this embodiment, the third and fourth switches **130** and **138** are switched substantially simultaneously.

Referring back to Figure **1**, when the third switching control signal $Q3_{on}$ is asserted, the third switch **130** is switched on to conduct current from the DC source **106** to the power grid load **112** along the second supply current path **127**, and accordingly current flows from the first source node **102**, to the third intermediate node **128**, through the third inductor **132**, and to the second load node **110**. When the fourth switching control signal $Q4_{on}$ is asserted, the fourth switch **138** is switched on to conduct current from the power grid load **112** to the DC source **106** along the second return current path **133**, and accordingly current flows from the first load node **108**, through the fourth inductor **136**, to the fourth intermediate node **134**, and back to the second source node **104**. During respective third time periods **258** (shown in Figure **3**) when current flows along the second supply current path **127** and the second return current path **133**, the second diode **170** is reverse biased, thus blocking current from flowing between the third intermediate node **128** and the fourth intermediate node **134**. During the negative half cycles **244** the first and second switches **116** and **124** are switched off.

Referring back to Figure **3**, a waveform of the second shunt control signal $Q6_{on}$ for controlling the conduction state of the sixth switch **168** is shown at **264**. In this embodiment the second shunt control signal $Q6_{on}$ is asserted for substantially the entire negative half cycle **244**, thereby causing the sixth switch **168** to be on for substantially all of the negative half cycle. As described earlier, in an alternative embodiment the third switching control signal $Q3_{on}$ (or the fourth switching control signal $Q4_{on}$) may be inverted to produce the second shunt control signal $Q6_{on}$, such that the second shunt control signal $Q6_{on}$ is asserted when the third and fourth switching control signals $Q3_{on}$ and $Q3_{on}$ are not asserted. In this alternative embodiment, during the negative half cycle, the sixth switch **168** is switched on to permit current flow through the shunt **140** when the third and fourth switches **130** and **138** are switched off.

When the third and fourth switching control signals $Q3_{on}$ and $Q4_{on}$ are not asserted, the third and fourth switches **130** and **138** are switched off thus interrupting the flow of current from the DC source **106** (except for a small leakage current through the switches). However, the inductors **132** and **136** act to oppose changes in current flow and current continues to flow into the second load node **110** and back from the first load node **108**, and is shunted through the second shunt current path **194** between the fourth intermediate node **134** and the third intermediate node **128**. The second shunt current path **194** thus provides a path through the sixth switch **168** and the second diode **170** when the third and fourth switches **130** and **138** are switched off, and thus the second return current does not flow back to the DC source **106** through the fifth and sixth diodes **188** and **190** or the anti-parallel diodes **172** and **174**.

An instantaneous amplitude of the negative half cycle of the output current i_o shown at **266** is thus proportional to the time for which the third and fourth switching control signals $Q3_{on}$ and $Q4_{on}$ are asserted. At a negative peak **274**

of the output current waveform i_o, the third and fourth switching control signals $Q3_{on}$ and $Q4_{on}$ are predominantly in an asserted state, while proximate a zero crossing point **272**, the third and fourth switching control signals are predominantly in a non-asserted state. The inductors **132** and **136** resist changes in current flow and thus produce a generally smooth sinusoidal negative half cycle of the output current waveform i_o at the load nodes **108** and **110**.

In this embodiment, since the reference signal v_{ref} is in phase with the grid voltage signal v_{grid}, the output current i_o is supplied to the power grid load **112** substantially in phase with the grid voltage (i.e. the voltage v_o shown at **266**).

Advantageously, in the circuit configuration shown in Figure **1**, should the fourth switch **138** be unintentionally switched on while the first and second switches **116** and **124** are conducting current, the inductors **118** and **136** (L**1** and L**4**) are effectively connected in series with the first and second switches across the DC source **106** and limit current flow, thus reducing the possibility of damage to the first, second and fourth switches. Such a conduction state is generally referred to as a cross-conduction condition, and similar cross conduction conditions may occur between when the third and fourth switches **130** and **138** are conducting and the second switch **124** is unintentionally switched on. Under a cross conduction condition, for example when the first, second, and fourth switches **116**, **124**, and **138** are all simultaneously conducting, a short circuit does not appear across the source nodes **102** and **104**, as is the case with many prior-art circuit configurations. Furthermore the first diode **166** blocks current flow between the first and second intermediate nodes **114** and **120**, and the second diode **170** blocks current flow between the third and fourth intermediate nodes **128** and **134**, irrespective of the respective conduction states of the fifth and sixth switches **164** and **168**. Consequently, the circuit configuration shown in Figure **1** provides some

inherent fault tolerance irrespective of where the switching and shunt control signals $Q1_{on}$ - $Q6_{on}$ are asserted or not.

The inductors **118**, **122**, **132** and **136** may comprise a high flux core material to keep the size of the inductors to a minimum. Conventional prior-art circuit configurations generally include only two inductors, while the circuit configuration shown in Figure **1** includes four inductors **118**, **122**, **132** and **136**. However, while each of the inductors **118**, **122**, **132** and **136** is required to handle the same peak current as in prior art configurations, advantageously, each of the inductors is only required to handle half of the RMS (route-mean-square) current compared to prior art circuit configurations. Consequently while two additional inductors are required in the circuit configuration shown in Figure **1**, lower RMS current requirements per inductor lead to a generally similar total inductor volumetric size when compared to prior art circuit configurations that include only two inductors.

As shown in Figure **3**, the first shunt control signal $Q5_{on}$ is asserted for substantially the entire positive half cycle **242**. At the end of the positive half cycles **242**, the current flowing through the inductors **118** and **122** is reduced to a small residual current. However at this time, the grid voltage is also relatively low and thus the rate of change of current through the inductors **118** and **122** is also low and may cause a waveform of the output current i_o to be distorted in the region of the zero crossing points **270** and **272**. In an alternative embodiment, such distortions may be reduced by modifying the first and second shunt control signals $Q5_{on}$, and $Q6_{on}$ such that the fifth and sixth switches **164** and **168** switch off just before the respective zero crossing points **245** and **247**. Referring to Figure **4**, a modified waveform of the first shunt control signal $Q5_{on}$ is shown at **330** and a modified waveform of the second shunt control signal $Q6_{on}$ is shown at **336**. The first shunt control signal $Q5_{on}$ is in an asserted state for a first portion **332** of the positive half cycle **242** and in a non-asserted state during a second portion **334** of the

positive half cycle. Referring back to Figure **1**, when the first and second switches **116** and **124** are switched off and when the first shunt control signal $Q5_{on}$ is not asserted during the second portion **334** of the positive half cycle, the fifth switch **164** is also switched off. Accordingly, residual current through the inductors **118** and **122** is conducted back to the DC source **106** through the third and fourth diodes **184** and **186**, and is quickly reduced. Similarly, the second shunt control signal $Q6_{on}$ is in an asserted state for a first portion **338** of the negative half cycle **244** and in a non-asserted state during a second portion **340** of the negative half cycle, thereby causing residual current through the inductors **132** and **136** to be conducted back to the DC source **106** through the fifth and sixth diodes **188** and **190**. Advantageously, in such embodiments the sinusoidal output current i_o produced at the load nodes **108** and **110** may have lower total harmonic distortion (THD) than in embodiments where the first and second shunt control signals $Q5_{on}$ and $Q6_{on}$ are asserted for substantially all of the respective positive and negative half-cycles **242** and **244**.

Referring to Figure **5**, in an alternative embodiment of the invention, the apparatus **100** shown in Figure **1** may be operated to produce an output current waveform that is out of phase with the grid voltage in order to compensate for other loads on the power grid that have a non-unity power factor. The grid voltage signal v_{grid} is shown at **340** in Figure **5**. The I/O port **208** of the processor circuit **200** (shown in Figure **2**) receives the grid voltage signal v_{grid} at the input **212** and produces a reference signal v_{ref} (also shown at **340** in Figure **5**) that is phase shifted with respect to the grid voltage signal v_{grid} by a phase angle of φ degrees, as shown at **342**. In Figure **5**, the phase angle φ is shown as being positive, but in general the phase angle φ may be positive or negative, depending on whether it is required to provide power factor compensation for a load with a leading or a lagging power factor.

In grid–tied operation, the reference signal waveform v_{ref} represents a desired output current waveform rather than a desired output voltage waveform, and the switching control signals $Q1_{on}$ to $Q4_{on}$ and the first and second shunt control signals $Q5_{on}$ and $Q6_{on}$ are respectively asserted to produce a desired out of phase output current i_o as shown at **364**. A waveform of the first and second switching control signals $Q1_{on}$ and $Q2_{on}$ is shown at **344** and a waveform of the first shunt control signal $Q5_{on}$ is shown at **352**.

During a portion **380** of the positive half cycle the first and second switching control signals $Q1_{on}$ and $Q2_{on}$ and the first shunt control signal $Q5_{on}$ are asserted as described above in connection with Figure **3** and current flows along the first supply current path **113** and first return current path **119**, thereby supplying power to the power grid load **112** from the DC source **106**. During a portion **382** of the positive half cycle when the phase shifted reference signal v_{ref} is positive and the signal representing the grid voltage waveform v_{grid} is negative, reactive power is received from the power grid load **112**. During the portion **382** the first and second switching control signals $Q1_{on}$ and $Q2_{on}$ are in a non-asserted state, thereby preventing reactive currents from flowing back to the DC source **106**.

The first shunt control signal $Q5_{on}$ includes a plurality of positive half cycle switching sub-cycles **346**. During each sub-cycle **346**, the shunt control signal $Q5_{on}$ is an asserted state for fifth time periods, such as shown at **348**, and in a non-asserted state for sixth time periods, such as shown at **350**. During the fifth time period **348** the first return current flows through the first shunt **126** from the second intermediate node **120** to the first intermediate node **114** and through the first inductor **118** back to the first load node **108**. During the sixth time period **350** the first return current flows from the second intermediate node **120** through the third diode **184** to the first source node **102** and from the second source node **104** through the fourth diode **186** to the first

intermediate node **114** and through the first inductor **118** back to the first load node**108**.

A waveform of the third and fourth switching control signals $Q3_{on}$ and $Q4_{on}$ is shown at **354** and a waveform of the second shunt control signal $Q6_{on}$ is shown at **362**.

During a portion **384** of the negative half cycle the third and fourth switching control signals $Q3_{on}$ and $Q4_{on}$ and the second shunt control signal $Q6_{on}$ are asserted as described above in connection with Figure **3** and current flows along the second supply current path **127** and the second return current path **133**, thereby supplying power to the power grid load **112** from the DC source **106**. During a portion **386** of the negative half cycle when the phase shifted reference signal v_{ref} is negative and the signal representing the grid voltage waveform v_{grid} is positive, reactive power is received from the power grid load **112**. During the portion **386** the third and fourth switching control signals $Q3_{on}$ and $Q4_{on}$ are in a non-asserted state, thereby preventing reactive currents from flowing back to the DC source **106**.

The second shunt control signal $Q6_{on}$ includes a plurality of negative half cycle switching sub-cycles **356**. During each sub-cycle **356**, the shunt control signal $Q6_{on}$ is an asserted state for seventh time periods, such as shown at **358**, and in a non-asserted state for eighth time periods, such as shown at **360**. During the seventh time period **358** the second return current flows through the second shunt **140** from the fourth intermediate node **134** to the third intermediate node **128** and through the third inductor **132** back to the second load node **110**. During the eighth time period **360** the second return current flows from the fourth intermediate node **134** through the fifth diode **188** to the first source node **102** and from the second source node **104** through the sixth diode **190** to the third intermediate node **128** and through the third inductor **132** back to the second load node **110**.

Advantageously, when the apparatus **100** is controlled in accordance with the control signals shown in Figure **5**, reactive power received back from the power grid load **112** during the fifth and seventh time periods **348** and **358** is shunted through the first and second current shunts **126** and **140** respectively and is not returned to the DC source **106** during the fifth and seventh time periods.

Islanded Load Operation

The operation of the apparatus **100** shown in Figure **1** to supply AC current to an islanded load **112** is described with reference to Figure **1** and Figure **3**. In islanded load operation of the apparatus **100**, the controller **142** of Figure **1** receives or generates a reference signal v_{ref} having a frequency and amplitude defining a desired frequency and amplitude of an AC output voltage waveform v_o (shown at **266**), and the apparatus **100** is controlled to act as a low impedance voltage source for powering the load **112**.

Referring to Figure **3** the reference signal v_{ref} shown at **240** and as described above, may be generated externally to the controller **142** shown in Figure **1** or processor circuit **200** shown in Figure **2**. Alternatively the reference signal v_{ref} may be generated internally by the processor circuit **200**.

In islanded load operation, the controller **142** produces the first, second, third, and fourth switching control signal waveforms as shown at **246** and **262** and the shunt control signal waveforms shown at **248** and **264** in response to the reference signal v_{ref} to cause the apparatus **100** to produce the desired AC output voltage v_o across the load nodes **108** and **110**. The output voltage v_o has a waveform having positive and negative half cycles that generally correspond to the positive and negative half cycles **242** and **244** of the reference signal v_{ref} shown at **240**. Current flow through the apparatus **100** in

islanded load operation remains as described above in connection with grid-tied operation of the apparatus.

Whether operating the apparatus to power an islanded load or the a power grid load, in the circuit configuration shown in Figure **1** when the first, second, third, and fourth switches **116**, **124**, **130** and **138** are switched off, the DC source **106** is effectively isolated from the load **112** and current flows through the first and second shunts **126** and **140** during respective positive and negative half-cycles. Advantageously, isolation of the DC source **106** from the load **112** prevents common mode signals at the switching frequency from appearing at the DC source, thereby providing improved EMC performance and improved electrical safety at the DC source. The first and second shunts **126** and **140** also prevent current flow back to the DC source **106**, which would otherwise cause a reduction in conversion efficiency. Furthermore, the circuit configuration shown in Figure **1** has a further advantage over prior-art configurations in that the first, second, third, and fourth switches **116**, **124**, **130** and **138** and the DC source **106** are inherently protected from damage due to short circuit currents that may be caused in the event of control signal errors.

While specific embodiments of the invention have been described and illustrated, such embodiments should be considered illustrative of the invention only and not as limiting the invention as construed in accordance with the accompanying claims.

What is claimed is:

1. A method for converting a direct current received from a direct current source into an alternating current at first and second load nodes, the first and second load nodes for connecting a load, the source being connected to first and second source nodes, the first source node for receiving direct current from the source and the second source node for providing a return path for the direct current to the source, the method comprising:

producing positive and negative half cycles of alternating current at the first and second load nodes;

said positive half cycle being produced by causing first and second switching control signals to effect a plurality of positive half cycle switching sub-cycles by causing said first and second switching control signals to be asserted for a first time period of said positive half cycle switching sub-cycle and not asserted for a second time period of said positive half cycle switching sub-cycle, and wherein during each positive half cycle switching sub-cycle:

direct current flows from the source through a first supply current path into the first load node for said first time period, said first supply current path comprising a first intermediate node, a first switch operable to selectively conduct current from the first source node to said first intermediate node in response to said first switching control signal, and a first inductor connected between said first intermediate node and the first load node;

a first return current flows from the second load node through a first return current path for said first time period, said first return current path comprising a second intermediate node, a second inductor connected between the second load node and said second intermediate node, and a second switch operable to selectively conduct current from said second intermediate node to the second source node in response to said second switching control signal; and

during said second time period, a first shunt control signal is asserted to cause said first return current to flow through a first shunt from said second intermediate node to said first intermediate node and through said first inductor back to the first load node, said first shunt being operably configured to prevent current from flowing from said first intermediate node to said second intermediate node and to selectively conduct current between said second intermediate node and said first intermediate node in response to said first shunt control signal;

said negative half cycle being produced by causing third and fourth switching control signals to effect a plurality of negative half cycle switching sub-cycles by causing said third and fourth switching control signals to be asserted for a third time period of said negative half cycle switching sub-cycle and to be not asserted for a fourth time period of said negative half cycle switching sub-cycle, and wherein during each negative half cycle switching sub-cycle:

direct current flows from the source through a second supply current path into the second load node for said third time period, said second supply current path comprising a third intermediate node, a third switch operable to selectively conduct current from the first source node to said third intermediate node in response to said third switching control signal, and a third inductor connected between said third intermediate node and the second load node;

a second return current flows from the first load node through a second return current path for said third time period, said second return current path comprising a fourth intermediate node, a fourth inductor connected between the first load node and said fourth intermediate node, and a fourth switch operable to selectively conduct current from said fourth intermediate node to the second source node in response to said fourth switching control signal; and

during said fourth time period, a second shunt control signal is asserted to cause said second return current to flow through a second shunt from said fourth intermediate node to said third intermediate node and through said third inductor back to the second load node, said second shunt being operably configured to prevent current from flowing from said third intermediate node to said fourth intermediate node and to selectively conduct current between said fourth intermediate node and said third intermediate node in response to said second shunt control signal.

2. The method of claim **1** wherein said first shunt comprises a fifth current switch and a first diode connected in series between said second intermediate node and said first intermediate node, said fifth current switch being operable to conduct current in response to said first shunt control signal, and said first diode being operable to block current flow between said first intermediate node and said second intermediate node.

3. The method of claim **1** wherein said second shunt comprises a sixth current switch and a second diode connected in series between said fourth intermediate node and said third intermediate node, said sixth current switch being operable to conduct current in response to said second shunt control signal, and said second diode being operable to block current flow between said third intermediate node and said fourth intermediate node.

4. The method of claim **1** further comprising producing said first, second, third, and fourth switching control signals and said first and second shunt control signals.

5. The method of claim **4** wherein producing said first, second, third, and fourth switching control signals comprises producing first, second, third, and fourth pulse width modulated switching control signals.

6. The method of claim **4** wherein producing said first shunt control signal comprises causing said first shunt control signal to be asserted for substantially all of said positive half cycle, thereby causing said first shunt to permit current flow during substantially all of said positive half cycle, and wherein producing said second shunt control signal comprises causing said second shunt control signal to be asserted for substantially all of said negative half cycle, thereby causing said

second shunt to permit current flow during substantially all of said negative half cycle.

7. The method of claim **4** wherein producing said first shunt control signal comprises causing said first shunt control signal to be asserted during said second time periods of said positive half cycle, thereby causing said first shunt to selectively permit current flow during said second time periods, and wherein producing said second shunt control signal comprises causing said second shunt control signal to be asserted during said fourth time periods of said negative half cycle, thereby causing said second shunt to selectively permit current flow during said fourth time periods.

8. The method of claim **7** wherein producing said first shunt control signal comprises inverting said first switching control signal and wherein producing said second shunt control signal comprises inverting said third switching control signal.

9. The method of claim **4** wherein:

producing said first shunt control signal comprises causing said first shunt control signal to be asserted for a first portion of said positive half cycle and causing said first shunt control signal to be not asserted for a second portion of said positive half cycle, thereby causing said first shunt to selectively permit current flow during said first portion of said positive half cycle, and wherein said first return current flows from said second intermediate node through a third diode to the first source node and from the second source node through a fourth diode to said first intermediate node during said second portion of said positive half cycle; and

producing said second shunt control signal comprises causing said second shunt control signal to be asserted for a first portion of said negative half cycle and causing said second shunt control signal to be not asserted for a second portion of said negative half cycle, thereby causing said second shunt to selectively permit current flow during said first portion of said negative half cycle, and wherein said second return current flows from said second intermediate node through a fifth diode to the first source node and from the second source node through a sixth diode to said first intermediate node during said second portion of said negative half cycle.

10. The method of claim **4** wherein producing said first and second switching control signals comprises causing each of said first and second switching control signals to be asserted to cause both said first switch and said second switch to permit current flow during said first time period, and wherein producing said third and fourth switching control signals comprises causing each of said third and fourth switching control signals to be asserted to cause both said third switch and said fourth switch to permit current flow during said third time period.

11. The method of claim **4** further comprising receiving a reference signal representing a desired output voltage waveform and wherein producing said first, second, third, and fourth switching control signals and said first and second shunt control signals comprises producing first, second, third, and fourth switching control signals and said first and second shunt control signals in response to said reference signal.

12. The method of claim **11** further comprising producing said reference signal.

13. The method of claim **12** wherein producing said reference signal comprises producing a sinusoidal reference signal having a frequency defining a desired frequency of an output voltage waveform across the first and second load nodes.

14. The method of claim **4** wherein the load comprises a power grid load and further comprising receiving a reference signal representing a grid voltage waveform of the power grid across the first and second load nodes and wherein producing said first, second, third, and fourth switching control signals and said first and second shunt control signals comprises producing first, second, third, and fourth switching control signals and said first and second shunt control signals in response to said reference signal to cause an output current to be supplied to the power grid substantially in phase with the grid voltage waveform.

15. The method of claim **4** wherein the load comprises a power grid load and further comprising receiving a signal representing a grid voltage waveform of the power grid across the first and second load nodes and producing a phase shifted reference signal in response to receiving said signal representing said grid voltage waveform, and wherein producing said first, second, third, and fourth switching control signals and said first and second shunt control signals comprises producing first, second, third, and fourth switching control signals and said first and second shunt control signals in response to said phase shifted reference signal to cause an output current to be supplied to the power grid out of phase with the grid voltage waveform.

16. The method of claim **15** further comprising:

during a portion of said positive half cycle when said phase shifted reference signal is positive and said signal representing said grid voltage waveform is negative:

causing said first and second switching control signals to be in a non-asserted state; and

causing said first shunt control signal to effect a plurality of half cycle switching sub-cycles by causing said first shunt control signal to be asserted for a fifth time period of said positive half cycle switching sub-cycle and not asserted for a sixth time period of said positive half cycle switching sub-cycle, and wherein:

during said fifth time period said first return current flows through said first shunt from said second intermediate node to said first intermediate node and through said first inductor back to said first load node; and

during said sixth time period said first return current flows from said second intermediate node through a third diode to the first source node and from the second source node through a fourth diode to said first intermediate node and through said first inductor back to said first load node;

during a portion of said negative half cycle when said phase shifted reference signal is negative and said signal representing said grid voltage waveform is positive:

causing said third and fourth switching control signals to be in a non-asserted state; and

causing said second shunt control signal to effect a plurality of half cycle switching sub-cycles by causing said second shunt control signal to be asserted for a seventh time period of said negative half cycle switching sub-cycle and not asserted for an eighth time period of said negative half cycle switching sub-cycle, and wherein:

during said seventh time period said second return current flows through said second shunt from said fourth intermediate node to said third intermediate node and through said third inductor back to said second load node;

during said eighth time period said second return current flows from said fourth intermediate node through a fifth diode to the first source node and from the second source node through a sixth diode to said third intermediate node and through said third inductor back to said second load node.

17. An apparatus for converting a direct current into an alternating current, the apparatus comprising:

first and second source nodes, said first source node being operably configured to receive direct current from a direct current source and said second source node being operably configured to provide a return path for said direct current from the apparatus to the source;

first and second load nodes for supplying alternating current produced by the apparatus to a load;

a first supply current path comprising:

a first intermediate node;

a first switch operable to selectively conduct current from said first source node to said first intermediate node in response to a first switching control signal; and

a first inductor connected between said first intermediate node and said first load node;

a first return current path comprising:

a second intermediate node;

a second inductor connected between said second load node and said second intermediate node; and

a second switch operable to selectively conduct current from said second intermediate node to said second source node in response to a second switching control signal;

a first shunt operably configured to prevent current from flowing from said first intermediate node to said second intermediate node and to selectively conduct current between said second intermediate node and said first intermediate node in response to a first shunt control signal;

a second supply current path comprising:

a third intermediate node;

a third switch operable to selectively conduct current from said first source node to said third intermediate node in response to a third switching control signal; and

a third inductor connected between said third intermediate node and said first load node;

a second return current path comprising:

a fourth intermediate node;

a fourth inductor connected between said second load node and said fourth intermediate node; and

a fourth current switch operable to selectively conduct current from said fourth intermediate node to said second source node in response to a fourth switching control signal;

a second shunt operably configured to prevent current from flowing from said third intermediate node to said fourth intermediate node and to selectively conduct current between said fourth intermediate node and said third intermediate node in response to a second shunt control signal; and

a controller operably configured to generate said first, second, third and fourth switching control signals and said first and second shunt control signals to control said first, second, third,

and fourth switches and said first and second shunts to produce positive and negative half cycles of the alternating current;

said positive half cycle being produced by causing said first and second switching control signals to effect a plurality of positive half cycle switching sub-cycles by causing said first and second switching control signals to be asserted for a first time period of said positive half cycle switching sub-cycle and not asserted for a second time period of said positive half cycle switching sub-cycle, and wherein during each positive half cycle switching sub-cycle:

direct current flows from the source through said first supply current path into said first load node for said first time period;

a first return current flows from said second load node through said first return current path for said first time period; and

during said second time period, said first shunt control signal is asserted to cause said first return current to flow through said first shunt from said second intermediate node to said first intermediate node and through said first inductor back to the first load node;

said negative half cycle being produced by causing said switching control signals to effect a plurality of negative half cycle switching sub-cycles by causing said third and fourth switching control signals to be asserted for a third time period of said negative half cycle switching sub-cycle and to be not asserted for a fourth time period of said negative half cycle

switching sub-cycle, and wherein during each negative half cycle switching sub-cycle:

direct current flows from the source through said second supply current path into said second load node for said third time period;

a second return current flows from said first load node through said second return current path for said third time period; and

during said fourth time period, said second shunt control signal is asserted to cause said second return current to flow through said second shunt from said fourth intermediate node to said third intermediate node and through said third inductor back to the second load node.

18. The apparatus of claim **17** wherein said second shunt comprises a sixth current switch and a second diode connected in series between said fourth intermediate node and said third intermediate node, said sixth current switch being operable to conduct current in response to said second shunt control signal, and said second diode being operable to block current flow between said third intermediate node and said fourth intermediate node.

19. The apparatus of claim **17** further comprising a capacitor connected between said first and second load nodes, said capacitor being operable, in combination with said first, second, third, and fourth inductors, to attenuate alternating current frequency components at frequencies other than a fundamental frequency associated with the alternating current waveform.

20. The apparatus of claim **17** further comprising a controller operably configured to produce said first, second, third, and fourth switching control signals and said first and second shunt control signals.

21. The apparatus of claim **20** wherein said controller is operably configured to produce first, second, third, and fourth pulse width modulated switching control signals.

22. The apparatus of claim **20** wherein said controller is operably configured to produce said first shunt control signal by causing said first shunt control signal to be asserted for substantially all of said positive half cycle, thereby causing said first shunt to permit current flow during substantially all of said positive half cycle, and wherein said controller is operably configured to produce said second shunt control signal by causing said second shunt control signal to be asserted for substantially all of said negative half cycle, thereby causing said second shunt to permit current flow during substantially all of said negative half cycle.

23. The apparatus of claim **20** wherein said controller is operably configured to produce said first shunt control signal by causing said first shunt control signal to be asserted during said second time periods of said positive half cycle, thereby causing said first shunt to selectively permit current flow during said second time periods, and wherein said controller is operably configured to produce said second shunt control signal by causing said second shunt control signal to be asserted during said fourth time periods of said negative half cycle, thereby causing said second shunt to selectively permit current flow during said fourth time periods.

24. The apparatus of claim **23** wherein said controller is operably configured to produce said first shunt control signal by inverting said first switching control signal and to produce said second shunt control signal by inverting said third switching control signal.

25. The apparatus of claim **20** further comprising:

a third diode connected to conduct current between said second intermediate node and said first source node;

a fourth diode connected to conduct current between said second source node and said first intermediate node;

a fifth diode connected to conduct current between said fourth intermediate node and said first source node; and

a sixth diode connected to conduct current between said second source node and said third intermediate node;

and wherein said controller is operably configured to:

produce said first shunt control signal by causing said first shunt control signal to be asserted for a first portion of said positive half cycle and causing said first shunt control signal to be not asserted for a second portion of said positive half cycle, thereby causing said first shunt to selectively permit current flow during said first portion of said positive half cycle, and wherein said first return current flows from said second intermediate node through said third diode to the first source node and from the second source node through said fourth diode to said first

intermediate node during said second portion of said positive half cycle; and

produce said second shunt control signal by causing said second shunt control signal to be asserted for a first portion of said negative half cycle and causing said second shunt control signal to be not asserted for a second portion of said negative half cycle, thereby causing said second shunt to selectively permit current flow during said first portion of said negative half cycle, and wherein said second return current flows from said second intermediate node through said fifth diode to the first source node and from the second source node through said sixth diode to said first intermediate node during said second portion of said negative half cycle.

26. The apparatus of claim **20** wherein said controller is operably configured to:

produce said first and second switching control signals by causing each of said first and second switching control signals to be asserted to cause both said first switch and said second switch to permit current flow during said first time period; and

produce said third and fourth switching control signals by causing each of said third and fourth switching control signals to be asserted to cause both said third switch and said fourth switch to permit current flow during said third time period.

27. The apparatus of claim **20** wherein said controller is operably configured to receive a reference signal representing a desired output voltage waveform and to produce said first, second, third, and fourth

switching control signals and said first and second shunt control signals in response to said reference signal.

28. The apparatus of claim **27** wherein said controller is operably configured to produce said reference signal.

29. The apparatus of claim **28** wherein said controller is operably configured to produce a sinusoidal reference signal having a frequency defining a desired frequency of an output voltage waveform across the first and second load nodes.

30. The apparatus of claim **20** wherein the load comprises a power grid load and wherein said controller is operably configured to receive a reference signal representing a grid voltage waveform of the power grid across said first and second load nodes and to produce said first, second, third, and fourth switching control signals and said first and second shunt control signals in response to said reference signal to cause an output current to be supplied to the power grid substantially in phase with the grid voltage waveform.

31. The apparatus of claim **20** wherein the load comprises a power grid load and wherein said controller is operably configured to:

receive a signal representing a grid voltage waveform of the power grid across said first and second load nodes;

produce a phase shifted reference signal in response to receiving said signal representing said grid voltage waveform; and

produce said first, second, third, and fourth switching control signals and said first and second shunt control signals in

response to said phase shifted reference signal to cause an output current to be supplied to the power grid out of phase with the grid voltage waveform.

32. The apparatus of claim **31** wherein said controller is operably configured to:

cause said first and second switching control signals to be in a non-asserted state during a portion of said positive half cycle when said phase shifted reference signal is positive and said signal representing said grid voltage waveform is negative :

cause said first shunt control signal to effect a plurality of half cycle switching sub-cycles by causing said first shunt control signal to be asserted for a fifth time period of said positive half cycle switching sub-cycle and not asserted for a sixth time period of said positive half cycle switching sub-cycle during said portion of said positive half cycle , and wherein:

during said fifth time period said first return current flows through said first shunt from said second intermediate node to said first intermediate node and through said first inductor back to said first load node;

during said sixth time period said first return current flows from said second intermediate node through a third diode to the first source node and from the second source node through a fourth diode to said first intermediate node and through said first inductor back to said first load node; and

cause said third and fourth switching control signals to be in a non-asserted state during a portion of said negative half cycle when said phase shifted reference signal is negative and said signal representing said grid voltage waveform is positive;

cause said second shunt control signal to effect a plurality of half cycle switching sub-cycles by causing said second shunt control signal to be asserted for a seventh time period of said negative half cycle switching sub-cycle and not asserted for an eighth time period of said negative half cycle switching sub-cycle during said portion of said negative half cycle, and wherein:

during said seventh time period said second return current flows through said second shunt from said fourth intermediate node to said third intermediate node and through said third inductor back to said second load node; and

during said eighth time period said second return current flows from said fourth intermediate node through a fifth diode to the first source node and from the second source node through a sixth diode to said third intermediate node and through said third inductor back to said second load node.

33. The apparatus of claim **17** wherein said first shunt comprises a fifth current switch and a first diode connected in series between said second intermediate node and said first intermediate node, said fifth current switch being operable to conduct current in response to said first shunt control signal, and said first diode being operable to block

current flow between said first intermediate node and said second intermediate node.

34. The apparatus of claim **17** wherein said first and second load nodes comprise respective first and second load terminals operably configured to facilitate connecting the load to said first and second load nodes.

35. The apparatus of claim **17** wherein said first and second source nodes comprise respective first and second source terminals operably configured to facilitate connecting the source to said first and second source nodes.

36. An apparatus for converting a direct current into an alternating current, the apparatus comprising:

first and second source nodes, said first source node being operably configured to receive direct current from a direct current source and said second source node being operably configured to provide a return path for said direct current from the apparatus to the source;

first and second load nodes for supplying alternating current produced by the apparatus to a load;

a first supply current path comprising:

a first intermediate node;

a first switch operable to selectively conduct current from said first source node to said first intermediate node in response to a first switching control signal; and

a first inductor connected between said first intermediate node and said first load node;

a first return current path comprising:

a second intermediate node;

a second inductor connected between said second load node and said second intermediate node; and

a second switch operable to selectively conduct current from said second intermediate node to said second source node in response to a second switching control signal;

a first shunt operably configured to prevent current from flowing from said first intermediate node to said second intermediate node and to selectively conduct current between said second intermediate node and said first intermediate node in response to a first shunt control signal;

a second supply current path comprising:

a third intermediate node;

a third switch operable to selectively conduct current from said first source node to said third intermediate node in response to a third switching control signal; and

a third inductor connected between said third intermediate node and said first load node;

a second return current path comprising:

a fourth intermediate node;

a fourth inductor connected between said second load node and said fourth intermediate node; and

a fourth current switch operable to selectively conduct current from said fourth intermediate node to said second source node in response to a fourth switching control signal;

a second shunt operably configured to prevent current from flowing from said third intermediate node to said fourth intermediate node and to selectively conduct current between said fourth intermediate node and said third intermediate node in response to a second shunt control signal; and

controlling means for generating said first, second, third, and fourth switching control signals and said first and second shunt control signals to control said first, second, third, and fourth switches and said first and second shunts to produce positive and negative half cycles of the alternating current;

said positive half cycle being produced by causing said first and second switching control signals to effect a plurality of positive half cycle switching sub-cycles by causing said first and second switching control signals to be asserted for a first time period of said positive half cycle switching sub-cycle and not asserted for a second time period of said positive half cycle switching sub-cycle, and wherein during each positive half cycle switching sub-cycle:

direct current flows from the source through said first supply current path into said first load node for said first time period;

a first return current flows from said second load node through said first return current path for said first time period; and

during said second time period, said first shunt control signal is asserted to cause said first return current to flow through said first shunt from said second intermediate node to said first intermediate node and through said first inductor back to the first load node;

said negative half cycle being produced by causing said switching control signals to effect a plurality of negative half cycle switching sub-cycles by causing said third and fourth switching control signals to be asserted for a third time period of said negative half cycle switching sub-cycle and to be not asserted for a fourth time period of said negative half cycle switching sub-cycle, and wherein during each negative half cycle switching sub-cycle:

direct current flows from the source through said second supply current path into said second load node for said third time period;

a second return current flows from said first load node through said second return current path for said third time period; and

during said fourth time period, said second shunt control signal is asserted to cause said second return current to flow through said second shunt from said fourth intermediate node to said third intermediate node and through said third inductor back to the second load node.

37. The apparatus of claim **36** wherein said controller means comprises means for producing first, second, third, and fourth pulse width modulated switching control signals.

38. The apparatus of claim **36** wherein said controller means comprises means for producing said first shunt control signal by causing said first shunt control signal to be asserted for substantially all of said positive half cycle, thereby causing said first shunt to permit current flow during substantially all of said positive half cycle, and wherein said controller means comprises means for producing said second shunt control signal by causing said second shunt control signal to be asserted for substantially all of said negative half cycle, thereby causing said second shunt to permit current flow during substantially all of said negative half cycle.

39. The apparatus of claim **36** wherein said controller means comprises means for producing said first shunt control signal by causing said first shunt control signal to be asserted during said second time periods of said positive half cycle, thereby causing said first shunt to selectively permit current flow during said second time periods, and wherein said controller means comprises means for producing said second shunt control signal by causing said second shunt control signal to be asserted during said fourth time periods of said negative half cycle, thereby causing said second shunt to selectively permit current flow during said fourth time periods.

40. The apparatus of claim **36** wherein said controller means comprises means for inverting said first switching control signal and said third switching control signal to respectively produce said second switching control signal and said fourth switching control signal.

41. The apparatus of claim **36** further comprising:

a third diode connected to conduct current between said second intermediate node and said first source node;

a fourth diode connected to conduct current between said second source node and said first intermediate node;

a fifth diode connected to conduct current between said fourth intermediate node and said first source node; and

a sixth diode connected to conduct current between said second source node and said third intermediate node;

and wherein said controller means comprises:

means for producing said first shunt control signal by causing said first shunt control signal to be asserted for a first portion of said positive half cycle and causing said first shunt control signal to be not asserted for a second portion of said positive half cycle, thereby causing said first shunt to selectively permit current flow during said first portion of said positive half cycle, and wherein said first return current flows from said second intermediate node through said third diode to the first source node and from the second source node through said fourth diode to

said first intermediate node during said second portion of said positive half cycle; and

means for producing said second shunt control signal by causing said second shunt control signal to be asserted for a first portion of said negative half cycle and causing said second shunt control signal to be not asserted for a second portion of said negative half cycle, thereby causing said second shunt to selectively permit current flow during said first portion of said negative half cycle, and wherein said second return current flows from said second intermediate node through said fifth diode to the first source node and from the second source node through said sixth diode to said first intermediate node during said second portion of said negative half cycle.

42. The apparatus of claim **36** wherein said controller means comprises:

means for producing said first and second switching control signals by causing each of said first and second switching control signals to be asserted to cause both said first switch and said second switch to permit current flow during said first time period; and

means for producing said third and fourth switching control signals by causing each of said third and fourth switching control signals to be asserted to cause both said third switch and said fourth switch to permit current flow during said third time period.

43. The apparatus of claim **36** wherein said controller means comprises means for receiving a reference signal representing a desired output voltage waveform and means for producing said first, second, third,

and fourth switching control signals and said first and second shunt control signals in response to said reference signal.

44. The apparatus of claim **43** wherein said controller means comprises means for producing said reference signal.

45. The apparatus of claim **44** wherein said controller means comprises means for producing a sinusoidal reference signal having a frequency defining a desired frequency of an output voltage waveform across the first and second load nodes.

46. The apparatus of claim **36** wherein the load comprises a power grid load and wherein said controller means comprises means for receiving a reference signal representing a grid voltage waveform of the power grid across said first and second load nodes and means for producing said first, second, third, and fourth switching control signals and said first and second shunt control signals in response to said reference signal to cause an output current to be supplied to the power grid substantially in phase with the grid voltage waveform.

47. The apparatus of claim **36** wherein the load comprises a power grid load and wherein said controller means comprises:

means for receiving a signal representing a grid voltage waveform of the power grid across said first and second load nodes;

means for producing a phase shifted reference signal in response to receiving said signal representing said grid voltage waveform; and

means for producing said first, second, third, and fourth switching control signals and said first and second shunt control signals in response to said phase shifted reference signal to cause an output current to be supplied to the power grid out of phase with the grid voltage waveform.

48. The apparatus of claim **46** wherein said controller means comprises:

means for causing said first and second switching control signals to be in a non-asserted state during a portion of said positive half cycle when said phase shifted reference signal is positive and said signal representing said grid voltage waveform is negative;

means for causing said first shunt control signal to effect a plurality of half cycle switching sub-cycles by causing said first shunt control signal to be asserted for a fifth time period of said positive half cycle switching sub-cycle and not asserted for a sixth time period of said positive half cycle switching sub-cycle during said portion of said positive half cycle, and wherein:

during said fifth time period said first return current flows through said first shunt from said second intermediate node to said first intermediate node and through said first inductor back to said first load node;

during said sixth time period said first return current flows from said second intermediate node through a third diode to the first source node and from the second source node through a fourth diode to said first intermediate node and through said first inductor back to said first load node; and

means for causing said third and fourth switching control signals to be in a non-asserted state during a portion of said negative half cycle when said phase shifted reference signal is negative and said signal representing said grid voltage waveform is positive;

means for causing said second shunt control signal to effect a plurality of half cycle switching sub-cycles by causing said second shunt control signal to be asserted for a seventh time period of said negative half cycle switching sub-cycle and not asserted for an eighth time period of said negative half cycle switching sub-cycle during said portion of said negative half cycle, and wherein:

during said seventh time period said second return current flows through said second shunt from said fourth intermediate node to said third intermediate node and through said third inductor back to said second load node;

during said eighth time period said second return current flows from said fourth intermediate node through a fifth diode to the first source node and from the second source node through a sixth diode to said third intermediate node and through said third inductor back to said second load node.

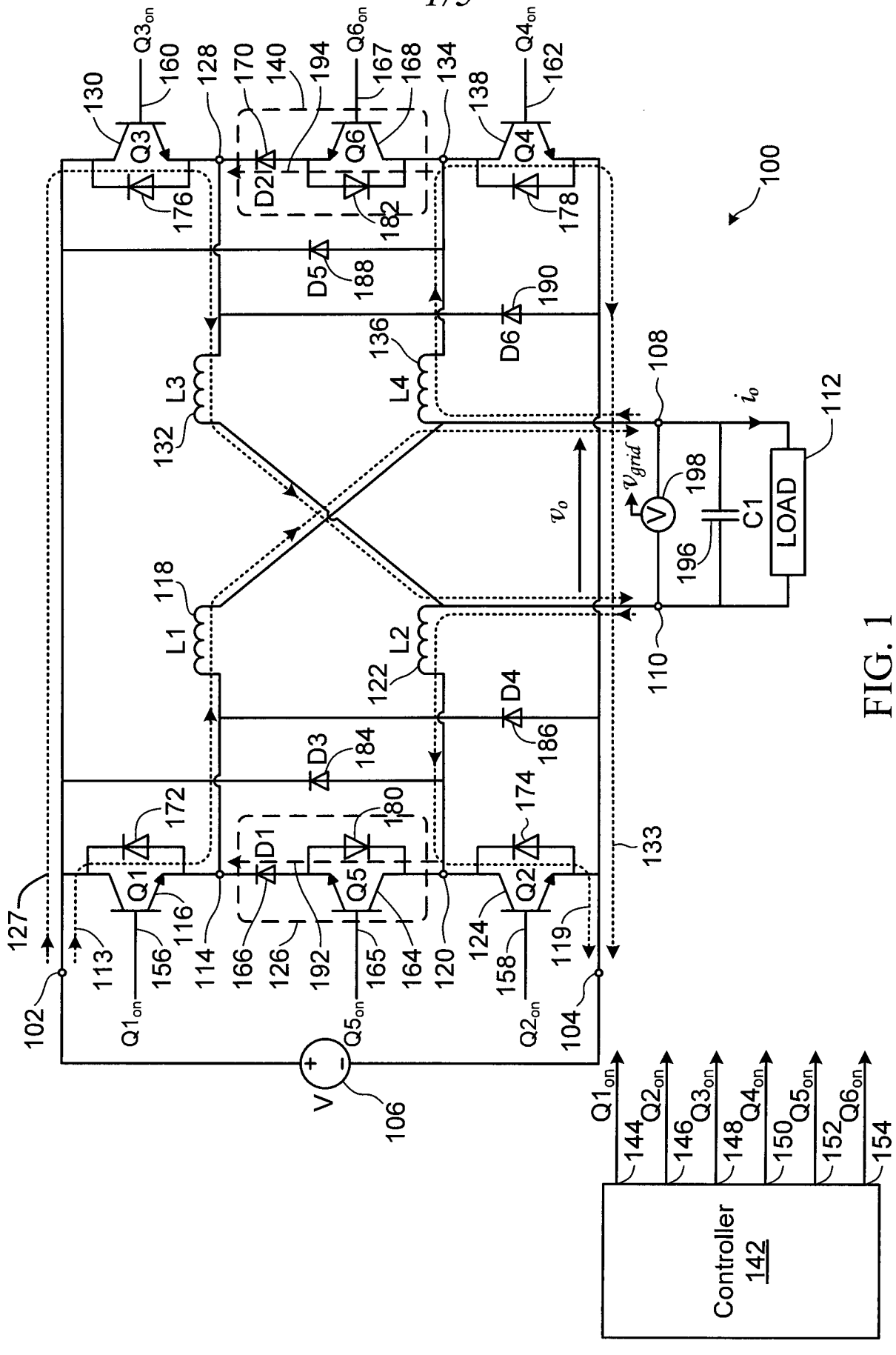

Q3on
Q6on
Q4on
130
160
128
170
140
194
167
168
134
138
162
Q3
Q6
Q4
D2
176
182
178
100
D5
188
190
D6
136
L4
L3
132
108
112
io
vo
vgrid
198
C1
LOAD
196
118
L1
L2
122
110
D4
D3
184
186
172
174
180
D1
Q1
Q5
Q2
133
127
113
156
116
114
166
126
192
165
164
120
124
158
119
102
104
Q1on
Q5on
Q2on
V
106
Q1on
Q2on
Q3on
Q4on
Q5on
Q6on
144
146
148
150
152
154
Controller
142

FIG. 1

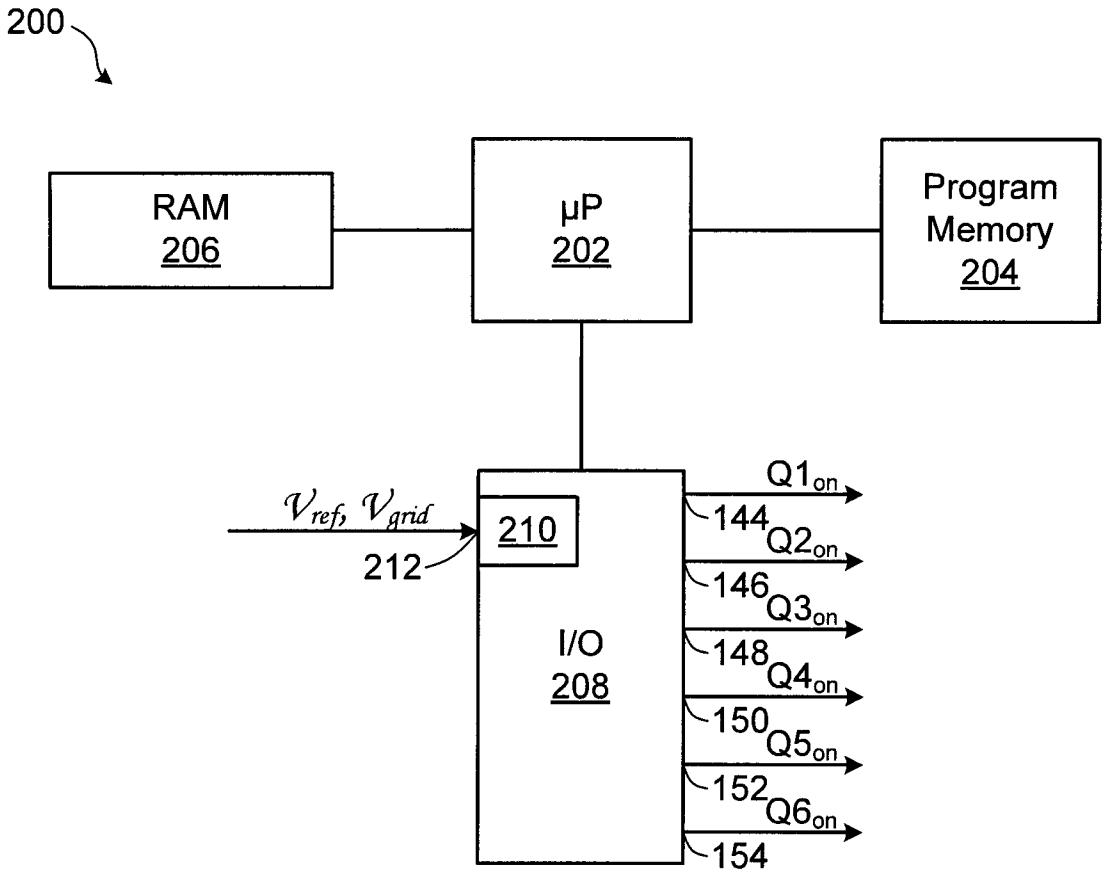

200
RAM
206
µP
202
Program
Memory
204
V_{ref}, V_{grid}
212
210
I/O
208
Q1on
144
Q2on
146
Q3on
148
Q4on
150
Q5on
152
Q6on
154

FIG. 2

Power Grid Load or Islanded Load: Unity power factor operation

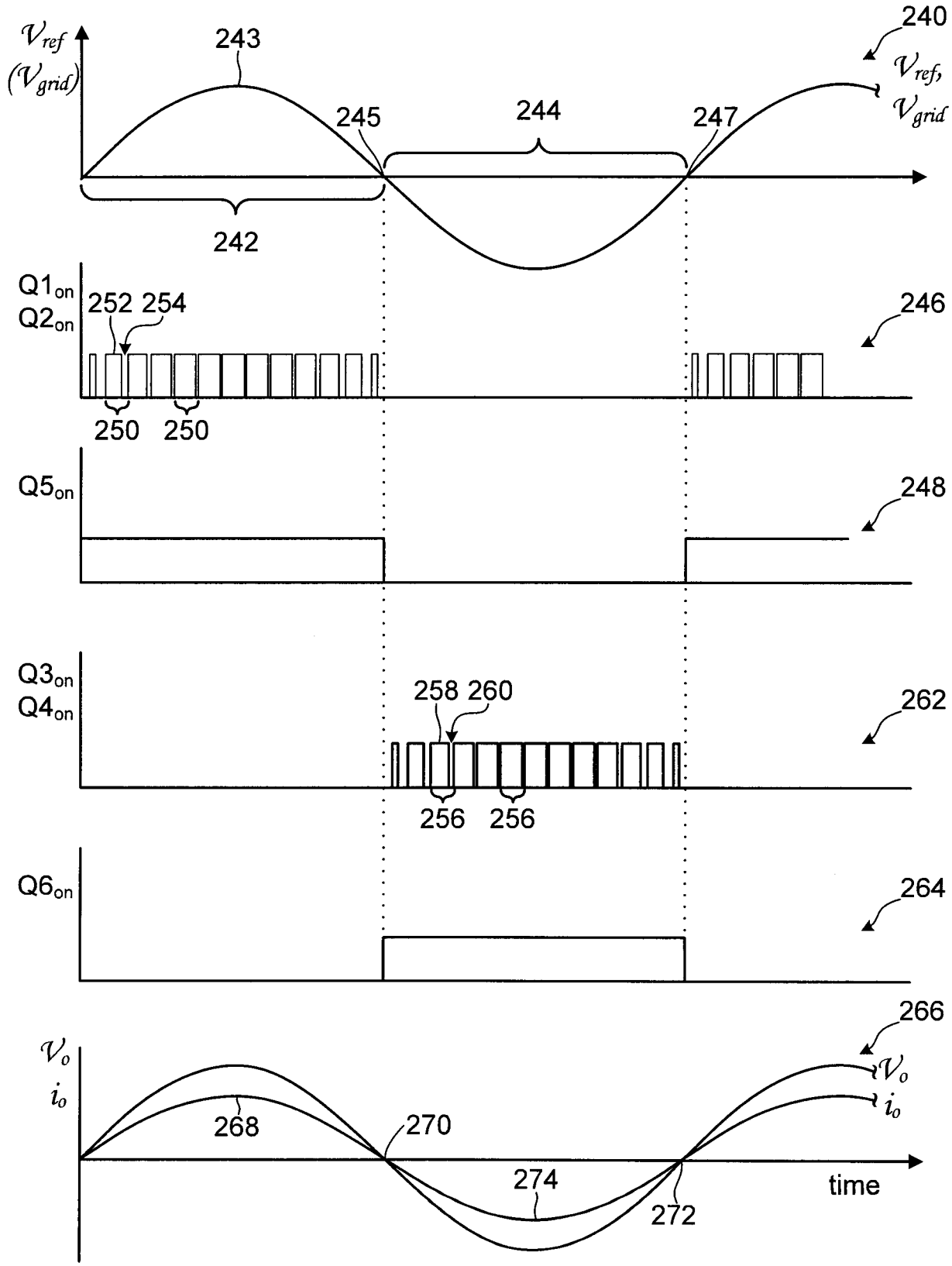


FIG. 3

Power Grid Load or Islanded Load: Unity power factor operation

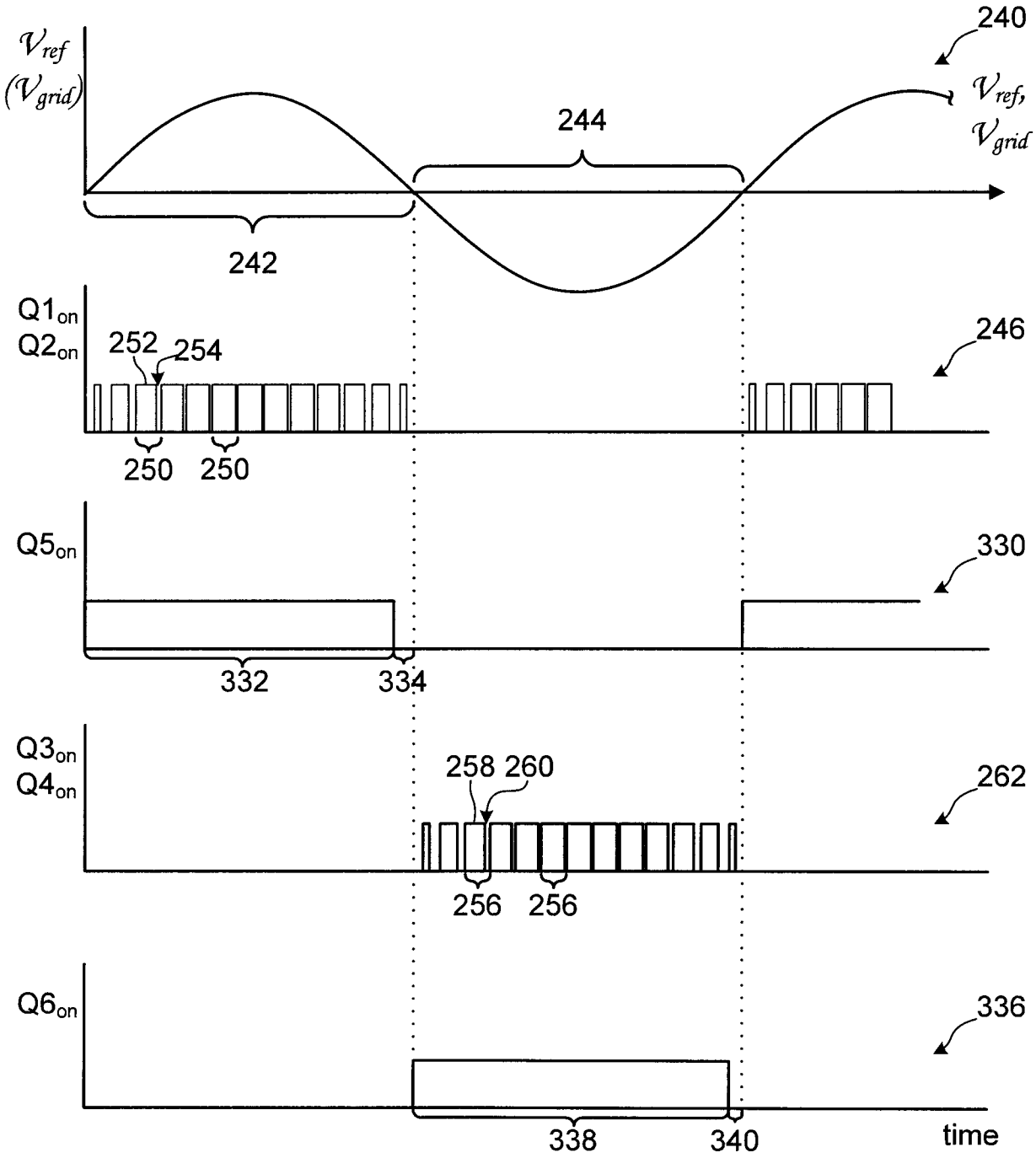


FIG. 4

Power Grid Load:
Non- unity power factor operation

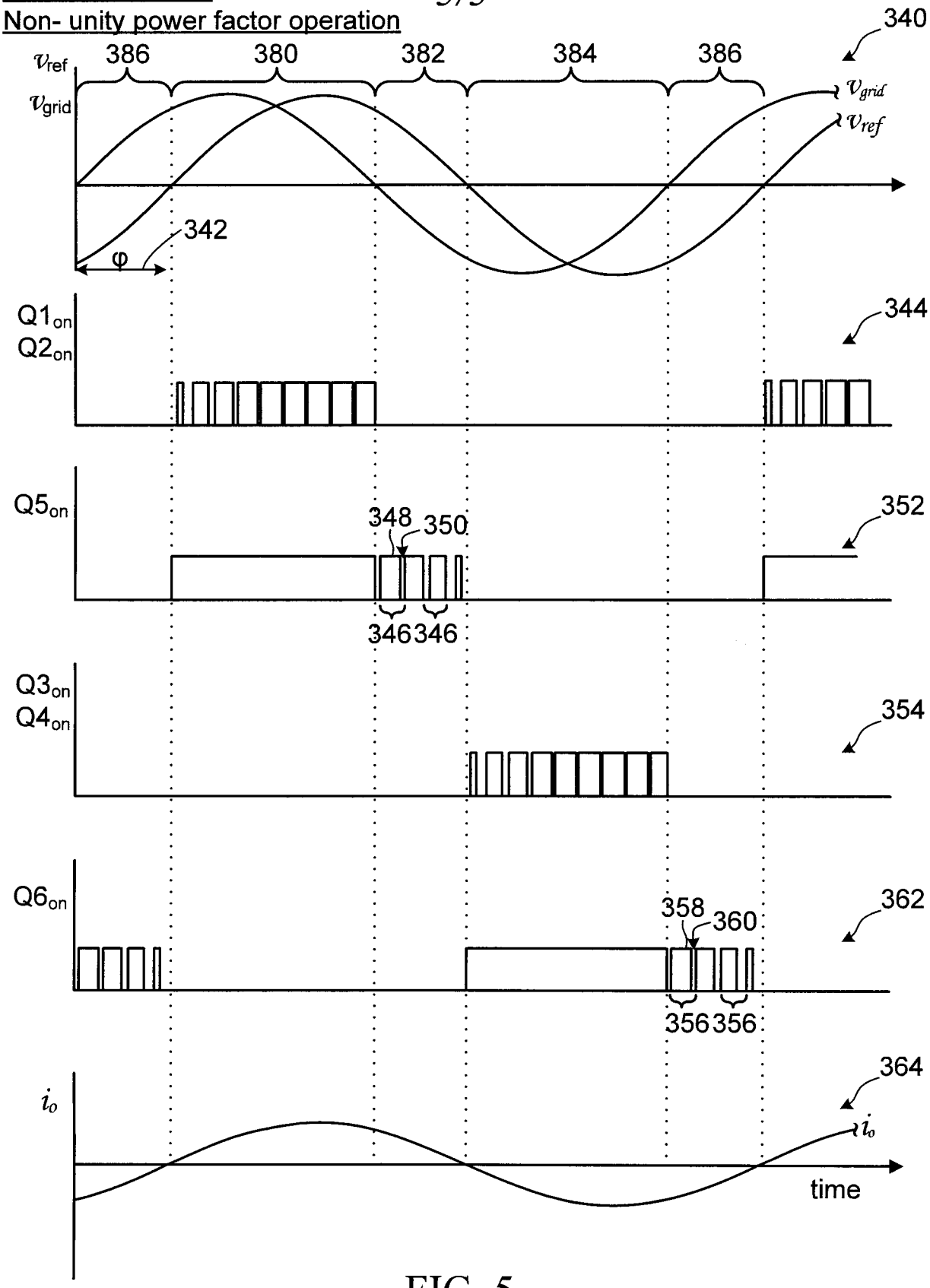


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2008/001155

A. CLASSIFICATION OF SUBJECT MATTER
IPC: ***H02M 7/48*** (2007.01) , ***H02M 1/08*** (2006.01)
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M (2006.01) and H02M (2007.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)
WEST, DELPHION, IEEE explore (inverter, DC/AC, DC-AC, bridge, inductor, single phase)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US - 7,046,534; 16 May 2006 (16-05-2006); Schmidt et al.	1-46

[ ] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 January 2009 (26-01-2009)	28 January 2009 (28-01-2009)

Name and mailing address of the ISA/CA	Authorized officer
Canadian Intellectual Property Office Place du Portage I, C114 - 1st Floor, Box PCT 50 Victoria Street Gatineau, Quebec K1A 0C9 Facsimile No.: 001-819-953-2476	Guillaume Murere 819- 934-6750

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CA2008/001155

Patent Document Cited in Search Report	Publication Date	Patent Family Member(s)	Publication Date
US 7046534B2	16-05-2006	US 2005174817A1	11-08-2005