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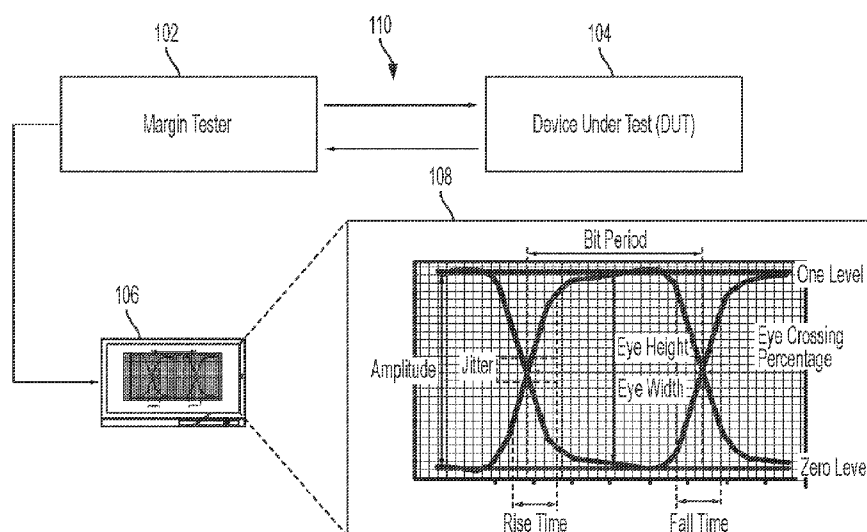


Fig. 1

(57) Abstract: Systems, devices and methods for high-speed I/O margin testing can screen high volumes of pre-production and production parts and identify cases where the electrical characteristics have changed enough to impact operation. The margin tester disclosed is lower cost, easier to use and faster than traditional BERT and scopes and can operate on the full multi-lane I/O links in their standard operating states with full loading and cross-talk. The margin tester assesses the electrical receiver margin of an operation multi-lane high speed I/O link of a device under test simultaneously in either or both directions. In a technology-specific form, an embodiment of the margin tester can be implemented as an add-in card margin tester to test motherboard slots of a mother board under test, or as a motherboard with slots to test add-in cards.

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SYSTEMS, METHODS AND DEVICES FOR HIGH-SPEED INPUT/OUTPUT MARGIN TESTING

TECHNICAL FIELD

[0001] This disclosure relates to test and measurement systems, and more particularly to systems and methods for performing high-speed electrical margin tests on an electrical device-under-test (DUT).

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0002] The components in the drawings are not necessarily to scale relative to each other. Like reference numerals designate corresponding parts throughout the several views.

[0003] Figure 1 is an overview block diagram illustrating an example environment in which embodiments of systems, devices and methods for high-speed input/output (I/O) margin testing may be implemented, according to an example embodiment.

[0004] Figure 2 is a block diagram illustrating an example technology-specific add-in card margin tester compliant with the Peripheral Component Interconnect (PCI) Express high-speed serial computer expansion bus standard to margin test PCI Express motherboard slots, according to an example embodiment.

[0005] Figure 3 is a block diagram illustrating a motherboard with slots compliant with the PCI Express high-speed serial computer expansion bus standard to margin test PCI Express add-in cards, according to an example embodiment.

[0006] Figure 4 is a chart showing results of an example margin test of a device under test (DUT) performed by a high-speed I/O margin tester and identification of potential DUT assembly or production issues based on the results of the margin test, according to an example embodiment.

[0007] Figure 5 is a chart showing results of another example margin test of a device under test (DUT) performed by a high-speed I/O margin tester and identification of potential DUT assembly or production issues based on the results of the margin test, according to an example embodiment.

[0008] Figure 6 is a block diagram illustrating a general purpose margin tester with a plurality of interfaces configured to be cabled to at least one test fixture to assess the electrical margin of the multi-lane high speed I/O link of the DUT in both transmit (Tx) and receive (Rx) directions, according to an example embodiment.

[0009] Figure 7 is a lower level block diagram of a margin tester for testing the electrical margin of a multi-lane high speed I/O link of a DUT in both Tx and Rx directions, according to an example embodiment.

[0010] Figure 8 is a block diagram of an example of a configured field programmable gate array (FPGA) that may be used in a controller of a margin tester for testing the electrical margin of a multi-lane high speed I/O link of a DUT in both Tx and Rx directions, according to an example embodiment.

[0011] Figure 9 is a block diagram of example output drive options of an FPGA that may be used in a controller of a margin tester for testing the electrical margin of a multi-lane high speed I/O link of a DUT in the Tx direction, according to an example embodiment.

[0012] Figure 10 is a flow diagram of an example method for margin testing a DUT, according to one example embodiment.

[0013] Figure 11 is a flow diagram of an example method for identifying potential DUT assembly or production issues based on margin testing electrical margin of a multi-lane high speed I/O link of a DUT in both Tx and Rx directions, according to one example embodiment.

[0014] Figure 12 is a flow diagram of an example method for initiating performance by the margin tester of the assessment of the electrical margin based on user-selectable options, according to one example embodiment.

[0015] Figure 13 is a flow diagram of an example method for providing a calibrated margin tester, according to one example embodiment.

[0016] Figure 14 is a flow diagram of an example method for configuring the DUT for running margin tests, according to one example embodiment.

DETAILED DESCRIPTION

[0017] Designers and manufacturers of electrical devices require test and measurement instruments and appropriate test procedures to ensure that the devices function properly. Such testing may be done during an engineering characterization stage of designing a new device in order to, for example, compare actual electrical performance of the device to simulated performance to ensure that the device is performing as designed. Such testing may also be done in a production manufacturing environment after an engineering design is finalized in order to find any manufacturing defects in each device produced.

[0018] Many electrical devices are designed to include high-speed I/O signal paths or busses. For example, modern personal computer (PC) motherboards, as well as other types of electrical devices, often include high-speed serial PCI Express (also abbreviated as PCIe, or PCI-e) busses, which are busses that are compliant with and perform according to the PCI Express high-speed serial computer expansion bus standard. Format specifications for the PCI Express standard are maintained and developed by the PCI Special Interest Group (PCI-SIG). These busses are typically used for communication between the motherboard and add-in/daughter cards that plug into PCIe connector slots or ports on the motherboard. Many other electrical devices besides motherboards also employ PCIe busses and connectors for high-speed I/O. PCIe Generation 4 (Gen 4 or version 4) devices can achieve bandwidths up to 16 gigatransfers per second (GT/s). PCIe Generation 5 (Gen 5 or version 5) devices can achieve bandwidths up to 32 GT/s.

[0019] PCIe devices communicate via a logical connection called an interconnect or link. A link is a point-to-point communication channel between

two PCIe ports allowing simultaneous bi-directional traffic. At the physical level, a link is composed of one or more lanes. Low-speed PCIe devices use a single-lane (x1) link, while a high-speed PCIe device, such as a graphics adapter, typically uses a much wider and faster 16-lane (x16) link. A lane is composed of two differential signaling pairs, with one pair for receiving data and the other for transmitting. Thus, each lane is composed of four wires or signal traces. Conventionally, performance of the lanes of a PCIe device is tested using a Bit Error Rate Tester (BERT) and/or a high-speed signal generator and oscilloscope (scope).

[0020] At an engineering bench test and/or engineering characterization stage of development of a printed circuit board (PCB), board design high speed routes (e.g. PCIe interconnects) are simulated, or design “recipes” or reference designs are followed. Pre-production board samples are then often built and tested. However, testing each board sample and each lane for all high speed I/Os with Bit Error Rate Test instruments (BERTs) and scopes is typically not feasible due to cost, time, and complexity constraints. In particular, traditional BERTs and scopes for testing high speed I/O standards such as PCIe continue to increase in cost and complexity as data rates increase. A single Tx and Rx test station for testing a single PCIe lane at a time can cost over one million dollars. The instruments are also difficult to use for traditional Tx and Rx tests and calibrations and expert (often PhD level) users and significant amounts of time are required to ensure measurements are taken correctly and instruments remain in good working order. As a result of these constraints, traditional BERTs and scopes are used infrequently in volume electrical testing of pre-production silicon, boards, PCBs and cables, and are usually not used at all in production testing.

[0021] However, as data rates of I/O links like PCI Express 5.0 at 32.0 GT/s increase, the risk of even small or subtle issues significantly impacting the performance of these I/O links increases, and the importance of doing some testing to flag electrical performance issues on every pre-production sample,

port and lane to prevent issues before production and to test electrical performance on every unit on production lines to catch production related issues (bad parts, etc.) before they lead to customers' issues and returns increases. Furthermore, traditional BERTs and scopes only allow testing on a single lane at a time, so the testing occurs in an environment different from the real operation of these I/O links, which usually form multi-lane links and can suffer significant cross-talk and loading issues during real operation, which can be missed by traditional BERT and scope testing even when that testing does/can occur. Likewise, in a manufacturing test environment, when assembling and testing multiple PCBs of a given design, production lines also do not typically use BERTs and scopes for high speed I/O tests due to cost, time, and complexity constraints.

[0022] Thus, there is a growing need for a new type of instrument that can screen high volumes of pre-production and production parts and identify cases where the electrical characteristics have changed enough to impact operation. This instrument has the most value if it is low cost, very easy to use and very fast compared to traditional BERT and scopes and can operate on the full multi-lane I/O links in their standard operating states with full loading and cross-talk. Overall, knowing the electrical margin (statistically valid operating margins) for each high speed I/O lane in each direction has value in increasing the likelihood of finding both design (e.g., per lane across all production samples) and assembly (e.g., specific board/lane instances) issues across all production samples.

[0023] Some conventional solutions rely only on functional tests as the best approximation (e.g., simply plugging in a "golden" or reference device and testing the link will come up at full speed). Other companies use on-die electrical margining in the silicon for their board, but that gives them only information in one direction and is not calibrated/characterized like a test instrument and leaves significant work to deal with and understand unit to unit variation in the add-in card they have selected for the purpose.

[0024] Disclosed herein are systems, devices and methods for high-speed input/output (I/O) margin testing that solve the technical problems above.

[0025] Figure 1 is an overview block diagram illustrating an example environment in which embodiments of systems, devices and methods for high-speed I/O margin testing may be implemented, according to an example embodiment. In one embodiment, shown is a margin tester 102 that assesses the electrical receiver margin of an operation multi-lane high speed I/O link 110 of an example DUT 104 in either or both Tx and Rx directions. The margin tester 102 of Figure 1 represents one or more of the embodiments of the margin tester disclosed herein.

[0026] The margin tester 102 may be coupled to a test station, PC, terminal or other display device 106 that may process, replicate and/or present an eye pattern display or data eye diagram 108 representing various aspects of the multi-lane high speed I/O link 110. In some embodiments, the test station, PC, terminal or other display device 106 may be integrated with or as part of the margin tester 102. The eye pattern display or data eye diagram 108 is a representation of a high speed digital signal that allows key parameters of the electrical quality of a signal to be quickly visualized and determined, and thus data therefrom may be used to determine statistically valid operating margins of a DUT. The eye pattern display or data eye diagram 108 is constructed from a digital waveform by folding the parts of the waveform corresponding to each individual bit into a single graph with signal amplitude on the vertical axis and time on horizontal axis. By repeating this construction over many samples of the waveform, the resultant graph will represent the average statistics of the signal and will resemble an eye. The eye opening corresponds to one bit period and is typically called the Unit Interval (UI) width of the eye pattern display or data eye diagram 108. The bit period is a measure of the horizontal opening of an eye diagram at the crossing points of the eye and is usually measured in picoseconds for a high speed digital signal (i.e., 200 ps is used for a 5 Gbps signal). The data rate is the inverse of bit period (1/bit period). The

bit period is commonly called the Unit Interval (UI) when describing an eye diagram. The advantage of using UI instead of actual time on the horizontal axis is that it is normalized and eye diagrams with different data rates can be easily compared. Eye width is a measure of the horizontal opening of an eye diagram. It is calculated by measuring the difference between the statistical mean of the crossing points of the eye. Rise time is a measure of the mean transition time of the data on the upward slope of an eye diagram. The measurement is typically made at the 20 and 80 percent or 10 and 90% levels of the slope. Fall time is a measure of the mean transition time of the data on the downward slope of an eye diagram. The measurement is typically made at the 20 and 80 percent or 10 and 90 percent levels of the slope. Jitter is the time deviation from the ideal timing of a data-bit event and an important characteristic of a high speed digital data signal. To compute jitter, the time deviations of the transitions of the rising and falling edges of an eye diagram at the crossing point are measured. Fluctuations can be random and/or deterministic. The time histogram of the deviations may be analyzed to determine the amount of jitter. The peak-to-peak (p-p) jitter is defined as the full width of the histogram, meaning all data points present. Root mean square (RMS) jitter is defined as the standard deviation of the histogram. The units for a jitter measurement on a high speed digital signal are normally in picoseconds.

[0027] Embodiments of the margin tester 102 can take at least two forms: technology-specific and general purpose. The margin tester 102 can be used with any high speed I/O protocol link of any link width (number of lanes) and use any form of high speed differential signaling including, but not limited to, non-return to zero (NRZ), pulse amplitude modulation-3 (PAM-3), and pulse amplitude modulation-4 (PAM-4). For the sake of a specific example embodiment for testing, PCI Express will be used. However, different high-speed serial bus standards, hardware and protocols may be used.

[0028] Figure 2 is a block diagram illustrating an example technology-specific add-in card margin tester 202 compliant with the PCI Express high-

speed serial computer expansion bus standard to margin test PCI Express motherboard slots 206, according to an example embodiment.

[0029] In a technology-specific form, an embodiment of the margin tester can be implemented as a PCI Express add-in card margin tester 202 to test PCI Express motherboard slots 206 of a mother board under test 204. For example, the PCI Express add-in card margin tester 202 may be a PCI Express x16 card electromechanical specification (CEM) form factor add-in card. In another embodiment of the technology-specific form, an embodiment of the margin tester can be implemented as a motherboard with PCI Express slot(s) to test PCI Express add-in cards (which is shown in Figure 3).

[0030] The PCI Express add-in card margin tester 202 may be in the form factor of a standard PCI Express compliant add-in card for a specific PCI Express form factor (for example, CEM or M.2 (formerly known as the Next Generation Form Factor (NGFF) or U.2 (formerly known as SFF-8639), etc.). The PCI Express add-in card margin tester 202 may comprise one or more printed circuit boards (PCBs), such as PCB 212 and one or more components that implement compliant PCI Express physical and logical link layers for each lane. The PCI Express add-in card margin tester 202 may comprise a plurality of interfaces (such as connectors 208) coupled to the PCB 212 and a controller 210. For example, such interfaces may comprise a plurality of connectors 208 that connect to the motherboard slots 206 and margin tester transmitters, which, under control of the controller 210, optionally include the ability to inject controlled noise, for example, through voltage swing and sinusoidal jitter, such that the eye margin expected at the receiver of motherboard under test 204 can be varied to specific targets for timing or voltage margin without the need for software running on the motherboard under test 204. The controller 210 may also be coupled to memory 214, which may store instructions and other data the controller 210 may read, use and/or execute to perform the functions described herein.

[0031] Various embodiments of the margin tester 102 (including the technology-specific PCI Express add-in card margin tester 202, the technology-specific motherboard margin tester 302 and the general purpose margin tester 602) may be with or without the noise injection. For cost-conscious production tests, the embodiment without noise injection may be more appealing. The margin tester receivers in the compliant physical layer implementation may include the ability to margin the link as defined in the PCI Express 4.0/5.0 lane margining specifications, but may also include additional and more sophisticated on-die margining capabilities. In one embodiment, the margin tester receivers may measure eye margin by moving the independent error detector and comparing for mismatches with the data sampler. In one implementation, the controller 210, which causes the margin tester 102 (including technology-specific PCI Express add-in card margin tester 202, technology-specific motherboard margin tester 302 and the general purpose margin tester 602) to perform the functions described herein, may be implemented with a field programmable gate array (FPGA) and the FPGA I/Os, which is shown in further detail in Figure 7 through Figure 9. However, other combinations of configurable controller hardware, firmware and/or software may be used.

[0032] Figure 3 is a block diagram illustrating an example technology-specific motherboard margin tester 302 with slots compliant with the PCI Express high-speed serial computer expansion bus standard to margin test PCI Express add-in cards, according to an example embodiment.

[0033] The motherboard margin tester 302 is another example of a technology-specific embodiment of the margin tester 102 disclosed herein, implemented as a motherboard margin tester 302 with one or more PCI Express slots 306 to test PCI Express add-in cards, such as the PCIe x16 add-in card DUT 304 shown in Figure 3. The motherboard margin tester 302 may comprise a plurality of interfaces (e.g., one or more PCI Express slots 306) coupled to the PCB 312 and the controller 210. For example, such interfaces

may comprise a plurality of one or more PCI Express slots 306 into which the PCIe x16 add-in card DUT 304 may be inserted for testing. Margin tester transmitters, which, under control of the controller 210, optionally include the ability to inject controlled noise, for example, through voltage swing and sinusoidal jitter (described further below and with respect to Figure 8 and Figure 9), such that the eye margin expected at the receiver of PCIe x16 add-in card DUT 304 can be varied to specific targets for timing or voltage margin without the need for software running on the PCIe x16 Add-in card DUT 304. For example, the controller 210 may be configured to assess the electrical margin of the single-lane or multi-lane high speed I/O link by at least being configured to inject reduction of eye width opening by injecting jitter on margin test transmitters (or implementing other eye width opening reduction methods), the injection of jitter being selectable to be applied on all lanes of the single-lane or multi-lane high speed I/O link simultaneously or applied independently per lane of the of the single-lane or multi-lane high speed I/O link. Also, the controller 210 may be configured to assess the electrical margin of the single-lane or multi-lane high speed I/O link by at least being configured to inject reduction of eye height opening by injecting noise on margin test transmitters (or implementing other eye height opening reduction methods), the injection of noise being selectable to be applied on all lanes of the single-lane or multi-lane high speed I/O link simultaneously or applied independently per lane of the of the single-lane or multi-lane high speed I/O link.

[0034] The controller 210 may also be coupled to memory 214, which may store instructions and other data the controller 210 may read, use and/or execute to perform the functions described herein.

[0035] Durability and insertion count are significant issues for the technology-specific embodiments of the margin tester 102 (including technology-specific PCI Express add-in card margin tester 202 and technology-specific motherboard margin tester 302). Thus, the PCB 212 and PCB 312 may be implemented and the margins characterized using an adaptor which is

configured to be replaced at low cost when it wears out without replacing the rest of the margin test unit. For example, a replaceable adapter may be coupled to the one or more PCI Express slots 306 and/or connectors 208 and be configured to wear out after a particular amount of use. The adaptor may then be replaced once it wears without replacing the rest of the PCI Express add-in card margin tester 202 or motherboard margin tester 302, as applicable.

[0036] Figure 4 is a chart 402 showing results of an example margin test of several DUTs performed by the high-speed I/O margin tester 102 and identification of potential DUT assembly or production issues based on the results of the margin test, according to an example embodiment.

[0037] In an example embodiment, the margin test may include assessing, by the margin tester 102, for each DUT of a plurality of devices under test (DUTs), timing eye width margin, in either or both Tx and Rx directions, for each high-speed input/output (I/O) lane of a multi-lane high speed I/O link of the DUT. The margin tester 102 may then detect timing eye width margin measurements for multiple DUTs of the plurality of DUTs that are each below a predetermined threshold for different lanes across the multiple DUTs. A potential DUT assembly or production issue may then be detected (visually or automatically by the margin tester 102) based on the detection of the timing eye width margin measurements for the multiple DUTs that are each below the predetermined threshold for different lanes across the multiple DUTs.

[0038] As an example, in one embodiment, the add-in card margin tester, such as add-in card margin tester 202 shown in Figure 2, may be used for bench testing / characterization of pre-production samples of a motherboard with one PCIe x8 slot. The following example test process may be performed using the add-in card margin tester 202 with an E-6 timing eye width margin (Left + right) measured for the slot over several millisecond test on each lane simultaneously. The present example includes timing only for simplicity, but other embodiments may include other measurements. Each measurement in the present example is done 3 times. However, this may be user

programmable in various embodiments. The measurements shown in the chart 402 are done at the margin tester receivers as well as the at motherboard DUT receivers. The measurements done at the at motherboard DUT receivers and may be performed in two ways. The first way may be using margin tester jitter (Sj) and voltage swing sweeps. The second way may be using on-die margin testing at the motherboard receiver. For example, the on-die margin testing at the motherboard receiver may, under control of the controller 210 of the add-in card margin tester 202, be run through software on a bootable drive connected to motherboard DUT or basic input/output system (BIOS) software on the motherboard DUT, for supported speeds. In the present example, the measurements are done at 16 GT/s, but may vary and may be user configurable.

[0039] The above example test procedure may yield the example results shown in chart 402 for the average margin at the test receiver. As shown in the chart 402, the consistently low margin on Lane 2 across all five DUTs, DUT #1 to DUT #5, may be an indicator of a potential design issue. In contrast, the low margin on DUT #1 Lane 4, DUT #3 on Lane 0, and DUT #4 on Lane 6 may be indicators of potential assembly or production issues with those specific lanes on those specific DUTs.

[0040] Figure 5 is a chart showing results of another example margin test of a device under test (DUT) performed by a high-speed I/O margin tester and identification of potential DUT assembly or production issues based on the results of the margin test, according to an example embodiment.

[0041] Similar indicators of potential design issues and/or potential assembly issues may also be seen in the example results shown in the chart 502 of Figure 5 for voltage swing and Sj average margin at the DUT receiver: As shown in the chart 502, the consistently low margin on Lane 1 across all five DUTs, DUT #1 to DUT #5, may be an indicator of a potential design issue. In contrast, the low margin on DUT #1 Lane 0, DUT #1 on Lane 5, and DUT #2 on

Lane 7 may be indicators of potential assembly or production issues with those specific lanes on those specific DUTs.

[0042] Additional features of embodiments of the disclosed technology may include the following functionality that may be performed under control of the controller 210 (for example, executing instructions according to a configured FPGA and/or read from another non-transitory computer-readable storage medium): choosing one or more different high-speed I/O protocols with which to perform margin testing test based on the multi-lane high speed I/O link of the DUT; testing multiple ports of the DUT with mixed protocols simultaneously; outputting run-to-run variation in margin over any number of margin test runs of the margin tester on the multi-lane high speed I/O link; implementing fixed Tx Equalization (EQ) on the DUT to test how much of margin variation is due to Tx EQ training variation; using fixed continuous time linear equalization (CTLE) in receivers of the margin tester to test impact of receiver equalization on margin of the multi-lane high speed I/O link of the DUT; using decision feedback equalization (DFE) in the receivers of the margin tester to test impact of receiver equalization on margin of the multi-lane high speed I/O link of the DUT; calculating expected margins for the margin tester based on target channels; automatically producing debug information when low margins are detected as a result of the assessment of the electrical margin of the multi-lane high speed I/O link; switching to using variable Inter Symbol Interference (ISI) source to find how much ISI causes lanes of the multi-lane high speed I/O link to fail; testing each lane individually to identify an amount of margin loss to due to cross-talk of the multi-lane high speed I/O link of the DUT; turning off DFE in the receivers of the margin tester to assess margin with and without DFE and an amount of non-linear discontinuities in each channel associated with the multi-lane high speed I/O link; showing expected margins with reference receivers and typical channels which allows lower than expected margin to be flagged even when the lower than expected margin is consistent across all lanes of the multi-lane high speed I/O link of the DUT and of multiple DUTs; selecting from multiple speeds

of the multi-lane high speed I/O link on which the assessment of the electrical margin is performed; inferring when errors have happened at the receivers of the DUT based on traffic traveling in an opposite direction on the multi-lane high speed I/O link by the margin tester using protocol specific knowledge to enable the margin tester to perform margin tests on production lines without software on the DUT; automatically capturing time-domain reflectometry readings (TDRs) of low margin channels detected as a result of the assessment of the electrical margin of the multi-lane high speed I/O link; performing an automated connection to an oscilloscope to automatically capture digitized waveforms when low margins are detected as a result of the assessment of the electrical margin of the multi-lane high speed I/O link; and providing a software plug in to configure the one or more of the user-selectable options for the DUT by configuring DUT silicon to implement the one or more of the user-selectable options. Under control of the controller 210, some of all of the above functionality may also be provided as user-selectable options for operating the margin tester 102.

[0043] Figure 6 is a block diagram illustrating a general purpose margin tester 602 with a plurality of interfaces 604 configured to be connected, e.g., via one or more cables, to at least one test fixture to assess the electrical margin of the multi-lane high speed I/O link of the DUT in either or both Tx and Rx directions, according to an example embodiment.

[0044] The general purpose margin tester 602 includes a controller 210 and associated memory 214, which may store instructions and other data the controller 210 may read, use and/or execute to perform the functions described herein. The general purpose margin tester 602 may include some number of lanes that can be connected, e.g., cabled, to standard test fixtures via interfaces 604, such as the standard PCI Express Compliance Load Board (CLB), to carry out, under control of the controller 210, the same testing as the technology-specific embodiments of the margin tester (e.g., add-in card margin tester 202 and motherboard margin tester 302). In addition, the general

purpose margin tester 602 supports multiple protocols and the configuration software of the general purpose margin tester 602 includes options to configure the lanes for different protocols and host/device roles. The general purpose margin tester 602 may also be used to test add-in cards by cabling to test fixtures, including the standard PCI Express Compliance Base Board (CBB) for testing add-in cards. The interfaces 604 of the general purpose margin tester 602 may include standard co-axial connectors and cables for each high speed differential signal or, in various other embodiments, include custom high density connectors and fixtures to minimize the cable count and make switching from one DUT to another DUT more efficient.

[0045] Figure 7 is a lower level block diagram of a margin tester 102 for testing the electrical margin of a multi-lane high speed I/O link of a DUT in either or both Tx and Rx directions, according to an example embodiment.

[0046] Shown is an FPGA 714 operably coupled to a support unit 710 (which may include Ethernet and other communication functionality), a timebase unit 708 for providing a system reference clock, a high-speed I/O (HSIO) outputs unit 702 and a HSIO inputs unit 704. The margin tester 102 may also be powered via an AC/DC power unit 716. The HSIO outputs unit 702 and HSIO inputs unit 704 are also operably coupled to I/O connectors 706. The FPGA 714 is a semiconductor device that is based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. In various embodiments, the margin tester 102 may have fewer or more components than shown and some components or functionality of components shown, although in operable communication with the margin tester 102, may be located outside or separate from the margin tester 102, or located or integrated in the FPGA 714.

[0047] The FPGA 714 can be reprogrammed to desired application or functionality requirements after manufacturing, such as to perform the functionality of the margin tester 102 described herein. For example, firmware on the FPGA 714 may act as a standard PCI Express upstream port (for testing

motherboards, as in the embodiment of the add-in card margin tester 202) or standard PCI Express root port (for testing add-in cards, such as in the embodiment of the motherboard margin tester 302), including some link layer logic for the margin tester 102 to infer when errors start at the DUT receiver based on traffic in the opposite direction and to quickly reduce margin stress once errors occur to prevent catastrophic link failure. In some embodiments, the FPGA 714 may be implemented using or may otherwise include a systems-on-modules (SoM) architecture that may incorporate memory, interface, etc. in the FPGA 714. The SoM may be implemented, for example, with an Advanced Reduced Instruction Set (RISC) Machine, originally Acorn RISC Machine (ARM) architecture.

[0048] A configuration application and/or script may be implemented via the FPGA 714 or stored on another accessible memory device or other non-transitory computer-readable storage media that enables an end user to easily configure margin tester options of the margin tester 102, including multiple runs with one or more of the following options. In some embodiments, an option for a bit error rate (BER) target may be set for margin scans (milliseconds for E-6 type margins and minutes for E-12 type margins). For example, such targets may include, but are not limited to targets related to: number of times to margin, margin timing and/or voltage; fixing Tx equalization for the margin tester or DUT transmitters; and fixing Rx CTLE and DFE for margin tester receivers. In some embodiments, an optional application and/or script is provided that removes data from the margin tester 102 and provides visualization tools for users to view large sets of margin data across multiple products/samples and view averages, run-to-run variations and trends over time and compare margins across multiple runs on the same DUT with different configuration options (fixed Tx equalization, etc.). In some embodiments, an optional application, which may be implemented on a bootable drive to install on the motherboard under test, is provided that unlocks additional options for motherboard testing including, but not limited to: running in loopback instead of L0 and using specific

patterns; using on the on-die margining features in the DUT silicon instead of the voltage swing and S_j margining from the DUT transmitters, and running both ways and comparing results.

[0049] In some embodiments, an optional plug-in model is provided that would allow the margin tester configuration application to also configure RX equalization settings on the DUT silicon if a plug-in is provided for that particular DUT silicon. In some embodiments, an optional IBIS-AMI (or similar) software model is provided for each individual margin test unit that may be used by designers and system integrators to include in their simulations to help establish test limits/methodology for specific customer setups. IBIS-AMI is a modeling standard for Serializer/Deserializer (SerDes) physical layers (PHYs) that enables fast, accurate, statistically significant simulation of multi-gigabit serial links. In some embodiments, an optional IBIS-AMI model is provided for the margin test unit, along with customer models (IBIS-AMI or scattering (S) parameters) and can also be utilized by follow-on efforts to include some level of system de-embed for increased accuracy and repeatability.

[0050] Figure 8 is a block diagram of an example of a configured field programmable gate array (FPGA) 714 that may be used in a controller 210 of a margin tester 102 for testing the electrical margin of a multi-lane high speed I/O link of a DUT in either or both Tx and Rx directions, according to an example embodiment.

[0051] In various embodiments, the FPGA 714 may have fewer or more components than shown and some components shown, and/ or functionality of those components, which are in operable communication with the FPGA 714, may be located outside or separate from the FPGA 714. Shown is a register interface 804 operably coupled to a local area network (LAN) connection 802, which may include a SerDes. The register interface 804 is also operably coupled to a Link Training and Status State Machine (LTSSM), Rx controller 806. One of the processes at the physical layer of the operation of the margin tester 102 is the link initialization and training process. In PCI Express devices,

this process establishes many important tasks such as link width negotiation, link data rate negotiation, bit lock per lane, symbol lock/block alignment per lane, etc. All these functions are accomplished by the LTSSM devices, which observe the stimulus from remote link partners as well as the current state of the link, and responds accordingly. The register interface 804 is also operably coupled to one or more additional LTSSM controller units, such as a LTSSM Universal Serial Bus (USB) controller 808 and an additional LTSSM USB controller 810. In the example embodiment shown, the LTSSM Rx controller 806 is operably coupled to a PCIe physical layer (PHY) 16x SerDes 812 and the LTSSM USB controller 808 is operably coupled to a USB/Thunderbolt/Displayport (USB/TBT/DP) PHY x4 unit 814. A jitter control unit 816 is also present as part of, or operably coupled to, the FPGA 714 for controlling a jitter insertion unit such that the eye margin expected at the DUT receiver can be varied to specific targets for timing or voltage margin without the need for software running on the DUT.

[0052] Figure 9 is a block diagram of example output drive options of an FPGA, such as FPGA 714, that may be used in a controller, such as controller 210, of a margin tester for testing the electrical margin of a multi-lane high speed I/O link of a DUT in either or both Tx and Rx directions, according to an example embodiment.

[0053] The first output drive option is an FPGA direct drive option 818, which is not buffered and does not include any varactor delay injection or jitter injection. The second output drive option is a buffered drive option 820 which includes a linear buffer or limiting amp 826 with differential output voltage (V_{od}) which does not include any varactor delay injection or jitter injection. The third output drive option is a varactor delay injection option 822, which includes a linear buffer 826 and a varactor component 828, which results in intersymbol interference (ISI) plus some delay, which, for example, may be ~3-5ps. The fourth output drive option is a jitter injection option 824, which, in one embodiment, may include a linear buffer 826, which may or may not be

included, and a delay application specific integrated circuit (ASIC) 830 (~100ps at 32 GBd), which is also available from ADSANTEC. In some embodiments, the linear buffer 826 is not included. For example, in such embodiments where the linear buffer 826 is not included, the jitter injection may be performed by differential noise injection.

[0054] In various embodiments, different kinds of stresses may be used by the margin tester 102 to identify various different corresponding failure modes including, but not limited to, failure modes related to: assembly; interconnects (surface-mount technology (SMT), packages, connectors, through-holes, vias, etc.); defects; impacts series resistance; failure modes that cause ISI and baseline wander; eye closure impact; failure modes that cause other than width closure; functional test escape; operator configuration error; incoming material; process variation; receiver bandwidth, which is similar to interconnect changes; power supply rejection ratio (PSRR); vertical/horizontal eye closure; PLL stability; design; deltas between lanes. The varactor-based method for jitter insertion may be more effective for exacerbating assembly-related defects.

[0055] Figure 10 is a flow diagram of an example method 1000 for margin testing a DUT, according to one example embodiment.

[0056] At 1002, the margin tester 102 establishes a multi-lane high speed I/O link of the device under test (DUT).

[0057] At 1004, the margin tester 102 assesses an electrical margin, in either or both transmit (Tx) and receive (Rx) directions, for each high-speed input/output (I/O) lane of the multi-lane high speed I/O link. For example, the assessing the electrical margin may include injecting adjustable stress on margin test transmitters of the multi-lane high speed I/O link. The adjustable stress may include injection of jitter applied on all lanes of the multi-lane high speed I/O link simultaneously and applying voltage swing. The assessing the electrical margin may also include assessing the electrical margin, in both

transmit (Tx) and receive (Rx) directions, simultaneously for each high-speed input/output (I/O) lane of the multi-lane high speed I/O link.

[0058] Figure 11 is a flow diagram of an example method 1100 for identifying potential DUT assembly or production issues based on margin testing electrical margin of a multi-lane high speed I/O link of a DUT in either or both Tx and Rx directions, according to one example embodiment.

[0059] At 1102, the margin tester 102 assesses, for each DUT of a plurality of DUTs, timing eye width margin, in either or both Tx and receive Rx directions, for each high-speed input/output (I/O) lane of a multi-lane high speed I/O link of the DUT.

[0060] At 1104, the margin tester 102 detects, based on the assessing, timing eye width margin measurements for each DUT of the plurality of DUTs that are consistently below a predetermined threshold for a same lane across the plurality of DUTs.

[0061] At 1106, the margin tester 102 identifies a potential DUT design issue based on the detection of the timing eye width margin measurements for each DUT of the plurality of DUTs that are consistently below the predetermined threshold for the same lane across the plurality of DUTs. The detecting may also or instead include, detecting, based on the assessing, timing eye width margin measurements for multiple DUTs of the plurality of DUTs that are each below a predetermined threshold for different lanes across the multiple DUTs.

[0062] Figure 12 is a flow diagram of an example method 1200 for initiating performance by the margin tester 102 of the assessment of the electrical margin based on user-selectable options, according to one example embodiment.

[0063] At 1202, the margin tester 102 provides user-selectable options for a margin tester that is configured to establish a multi-lane high speed input/output (I/O) link of a device under test (DUT) and to assess an electrical margin of the multi-lane high speed I/O link in either or both transmit (Tx) and

receive (Rx) directions. The user-selectable options may include customizations for the assessment of the electrical margin of the multi-lane high speed I/O link.

[0064] At 1204, the margin tester 102 receives an indication of selection of one or more of the user-selectable options for the margin tester 102.

[0065] At 1206, the margin tester 102 initiates performance by the margin tester 102 of the assessment of the electrical margin of the multi-lane high speed I/O link based on the indication of the selection of the one or more of the user-selectable options for the margin tester 102. The user-selectable options may include, but are not limited to, one or more of: a selectable option to choose one or more different high-speed I/O protocols with which to perform margin testing test based on the multi-lane high speed I/O link of the DUT; a selectable option to test multiple ports of the DUT with mixed protocols simultaneously; a selectable option to output run-to-run variation in margin over any number of margin test runs of the margin tester on the multi-lane high speed I/O link; a selectable option to implement fixed Tx Equalization (EQ) on the DUT to test how much of margin variation is due to Tx EQ training variation; a selectable option to use Fixed CTLE in receivers of the margin tester to test impact of receiver equalization on margin of the multi-lane high speed I/O link of the DUT; a selectable option to use Decision Feedback Equalization (DFE) in the receivers of the margin tester to test impact of receiver equalization on margin of the multi-lane high speed I/O link of the DUT; a selectable option to calculate expected margins for the margin tester based on target channels; a selectable option to automatically produce debug information when low margins are detected as a result of the assessment of the electrical margin of the multi-lane high speed I/O link; a selectable option for the margin tester to switch to using variable Inter Symbol Interference (ISI) source to find how much ISI causes lanes of the multi-lane high speed I/O link to fail; a selectable option for the margin tester to test each lane individually to identify an amount of margin loss to due to cross-talk of the multi-lane high speed I/O link of the DUT; a

selectable option to turn off DFE in the receivers of the margin tester to assess margin with and without DFE and an amount of non-linear discontinuities in each channel associated with the multi-lane high speed I/O link; a selectable option for characterization data for the margin tester that shows expected margins with reference receivers and typical channels and allows lower than expected margin to be flagged even when the lower than expected margin is consistent across all lanes of the multi-lane high speed I/O link of the DUT and of multiple DUTs; a selectable option to select from multiple speeds of the multi-lane high speed I/O link on which the assessment of the electrical margin is performed; a selectable option for the margin tester to infer when errors have happened at the receivers of the DUT based on traffic traveling in an opposite direction on the multi-lane high speed I/O link by the margin tester using protocol specific knowledge to enable the margin tester to perform margin tests on production lines without software on the DUT; a selectable option to automatically capture Time-Domain Reflectometry readings (TDRs) of low margin channels detected as a result of the assessment of the electrical margin of the multi-lane high speed I/O link; a selectable option to perform an automated connection to an oscilloscope to automatically capture digitized waveforms when low margins are detected as a result of the assessment of the electrical margin of the multi-lane high speed I/O link; and a selectable option to configure the one or more of the user-selectable options for the DUT by configuring DUT silicon to implement the one or more of the user-selectable options.

[0066] Figure 13 is a flow diagram of an example method 1300 for providing a calibrated margin tester, according to one example embodiment.

[0067] At 1302, the margin tester 102 may provide options to perform or may perform calibration of the margin tester 102, enabling a user to receive a set of expected margins with a series of reference channels.

[0068] At 1304, the calibrated margin tester is provided that is configured to measure electrical eye margin in either or both transmit (Tx) and receive (Rx)

directions of a device under test (DUT) with a fully running operation link of the DUT without special test modes and to capture full loading and cross-talk effects. An individually calibrated model for the margin tester may also be provided, enabling computation of expected margins with one or more of: individualized system channels, receiver models and transmitter models. Also, a feature in DUT silicon is provided that enables the margin tester to use vendor defined messages or another protocol mechanism to indicate that a margin test is about to take place by the margin tester, causing the DUT silicon to be able to disable logic that would degrade link width or speed of the link due to errors for a duration of the margin test.

[0069] A software application of the margin tester is also provided, that enables performance of testing by the margin tester of a channel component under test (e.g., bare printed circuit board (PCB) or a cable) in a testing configuration where a margin tester is used on either or both sides of the channel component under test. In some embodiments, hardware of the margin tester is provided to a company that manufactures a printed circuit board (PCB) and data associated with use of the margin tester is provided to silicon companies which provide silicon used in production of the PCB.

[0070] Figure 14 is a flow diagram of an example method 1400 for configuring the DUT for running margin tests, according to one example embodiment.

[0071] At 1402 the margin tester 102 receives configuration settings for a device under test (DUT);

[0072] At 1404, the margin tester 102 configures the DUT for running margin tests by the margin tester 102 under different conditions for silicon of the DUT. The margin tester 102 may receive a software plug-in that enables configuration and DUT silicon parameters for running the margin tests by the margin tester 102 under the different conditions for the silicon of the DUT. The DUT silicon parameters may include, but are not limited to, one or more of:

parameters related to receiver continuous time CTLE and parameters related to DFE.

[0073] Benefits, advantages and improvements of the disclosed embodiments include, but are not limited to the following features. Some embodiments can be implemented almost entirely with off-the shelf components including standard FPGAs and sinusoidal jitter injection chips or delay lines and have very low cost compared to traditional BERTs and scopes. An example embodiment can run on full multi-lane links operating in the normal operating state without the need for special software and capturing any effects due to the all lanes operating at once. Another advantage is that embodiments of the present disclosure can test in either or both directions (Tx and Rx) in a single self-contained unit. Various embodiments can also be run in a production environment (for example, in a motherboard production test environment) without the need for any software or modifications on the DUT. Test specific logic, which varies by protocol, may be provided in the margin tester 102 silicon/firmware to recognize very quickly when errors are occurring at the DUT receiver based on the data that is being transmitted back to the margin tester by the device under test. Some example embodiments include features implemented in the DUT silicon to recognize through PCI Express vendor specific messages or other standard protocol features that margin testing is going to take place and place the DUT silicon in a state where it would not degrade the link width and/or speed normally due to errors. This helps to ensure that the margining process to the DUT receivers using noise injection or voltage swing adjustments could occur without risk of degrading the link width or speed through normal protocol mechanisms. This is an alternative to special logic to quickly infer when errors start and reduce stress before link or speed degradation can occur.

[0074] Another improvement provided by an example embodiment described herein is that each margin tester unit of a plurality of margin testers units are individually calibrated and characterized so the users know expected

margin values with each specific unit and can flag even the smallest discrepancies from expectation across their pre-production and production units. As part of this individual characterization and calibration a model such as an IBIS-AMI model may be provided for each individual margin tester 102 that enables end users to compute expected margins for their specific channel models based on simulated or measured S parameters.

[0075] The disclosure describes ingenious margin testers that are are very fast and very simple to use. Convenient and efficient configuration software is provided for the length margin measurements and various options that are configurable by the user. Once configured, the margin tester 102 brings up the link as any standard device and then automatically performs the measurements on the operating link. The testing takes place on all lanes simultaneously and for quick electrical margin scans can take place in milliseconds. This enables volume testing, including full testing of all high speed I/O ports and lanes. Various embodiments provide different margin test modes to enable some level of problem characterization without the need for traditional instruments including, but not limited to: a repeat count and analysis of run-to-run variability in margin and selected Tx equalization (for both DUT and margin tester) and selected RX equalization (for margin test receivers) and likelihood of training issues in the DUT under test Tx or Rx training algorithms; fixing Transmitter Equalization in either direction and observing the impact on margins; fixing receiver equalization (CTLE) and number of DFE taps (including zero) in the margin tester receiver and looking at the impact on margin values. For example, significant margin changes if DFE may be turned off indicate a significant discontinuity in a specific channel.

[0076] Another advantage provided by various embodiments of the margin tester 102 is that every high speed I/O port and lane of a particular DUT can be tested for electrical margin across all pre-production units and in actual production and create an unprecedented ability to flag issues and potential issues before they ever make it to production or before they make it to

customers. Various embodiments also enable margin to be analyzed before and after a variety of link events like power state transitions (in some cases, using software on the DUT).

[0077] Prior solutions have very general purpose and highly-featured jitter and noise insertion methods. Various embodiments of the disclosure have an advantage over those solutions by significantly simplifying, but not eliminating, jitter/amplitude stress to accomplish this needed task. This simplicity translates into lower operating cost, faster results, and increased product confidence (through large data set collection) over what would be required using existing methods.

[0078] Aspects of the disclosure may operate on a particularly created hardware, on firmware, digital signal processors, or on a specially programmed general purpose computer including a processor operating according to programmed instructions. The terms controller or processor as used herein are intended to include microprocessors, microcomputers, Application Specific Integrated Circuits (ASICs), and dedicated hardware controllers. One or more aspects of the disclosure may be embodied in computer-usable data and computer-executable instructions, such as in one or more program modules, executed by one or more computers (including monitoring modules and controllers), or other devices. Generally, program modules include routines, programs, objects, components, data structures, etc. that perform particular tasks or implement particular abstract data types when executed by a processor in a computer or other device. The computer executable instructions may be stored on a non-transitory computer readable storage medium such as a hard disk, optical disk, removable storage media, solid state memory, DDR memory, Random Access Memory (RAM), etc. As will be appreciated by one of skill in the art, the functionality of the program modules may be combined or distributed as desired in various aspects. In addition, the functionality may be embodied in whole or in part in firmware or hardware equivalents such as integrated circuits, FPGA, and the like. Particular data structures may be used

to more effectively implement one or more aspects of the disclosure, and such data structures are contemplated within the scope of computer executable instructions and computer-usable data described herein.

[0079] The disclosed aspects may be implemented, in some cases, in hardware, firmware, software, or any combination thereof. The disclosed aspects may also be implemented as instructions carried by or stored on one or more or non-transitory computer-readable media, which may be read and executed by one or more processors. Such instructions may be referred to as a computer program product. Computer-readable media, as discussed herein, means any media that can be accessed by a computing device. By way of example, and not limitation, computer-readable media may comprise computer storage media and communication media.

[0080] Computer storage media means any medium that can be used to store computer-readable information. By way of example, and not limitation, computer storage media may include RAM, ROM, Electrically Erasable Programmable Read-Only Memory (EEPROM), flash memory or other memory technology, Compact Disc Read Only Memory (CD-ROM), Digital Video Disc (DVD), or other optical disk storage, magnetic cassettes, magnetic tape, magnetic disk storage or other magnetic storage devices, and any other volatile or nonvolatile, removable or non-removable media implemented in any technology. Computer storage media excludes signals per se and transitory forms of signal transmission.

[0081] Communication media means any media that can be used for the communication of computer-readable information. By way of example, and not limitation, communication media may include coaxial cables, fiber-optic cables, air, or any other media suitable for the communication of electrical, optical, Radio Frequency (RF), infrared, acoustic or other types of signals.

[0082] Additionally, this written description makes reference to particular features. It is to be understood that the disclosure in this specification includes all possible combinations of those particular features. For example, where a

particular feature is disclosed in the context of a particular aspect, that feature can also be used, to the extent possible, in the context of other aspects.

[0083] Also, when reference is made in this application to a method having two or more defined steps or operations, the defined steps or operations can be carried out in any order or simultaneously, unless the context excludes those possibilities.

[0084] Although specific aspects of the disclosure have been illustrated and described for purposes of illustration, it will be understood that various modifications may be made without departing from the spirit and scope of the disclosure. Accordingly, the disclosure should not be limited except as by the appended claims.

CLAIMS

1. A test device, comprising:
one or more printed circuit boards (PCBs);
at least one interface coupled to the one or more PCBs; and
a controller coupled to the at least one interface, the controller configured to establish a single-lane or multi-lane high speed input/output (I/O) link of a device under test (DUT) and to cause the test device to assess an electrical margin of the single-lane or multi-lane high speed I/O link in either or both transmit (Tx) and receive (Rx) directions.
2. The test device of claim 1 wherein the at least one interface comprises at least one lane configured to be connected to at least one test fixture to assess the electrical margin of the single-lane or multi-lane high speed I/O link of the DUT in either or both Tx and Rx directions.
3. The test device of claim 2 wherein the at least one lane comprises a plurality of lanes, and wherein the controller is configured to support multiple different protocols for the test device to test multiple different devices that each operate according to a different protocol, and to provide options to configure the plurality of lanes for different device roles and the multiple different protocols.
4. The test device of claim 3 wherein the plurality of lanes is configured to be connected to at least one test fixture to assess an electrical margin of a multi-lane high speed I/O link of one or more of: a motherboard and an add-in card.
5. The test device of claim 3 wherein the plurality of lanes is configured to be connected to test fixtures to assess electrical margins of multi-

lane high speed I/O links of at least one motherboard and of at least one add-in card.

6. The test device of claim 4 wherein the at least one test fixture includes one or more of: a Peripheral Component Interconnect Express (PCI Express) Compliance Load Board (CLB) and a PCI Express Compliance Base Board (CBB).

7. The test device of claim 1 wherein the single-lane or multi-lane high speed I/O link of the DUT is a fully running operational link without a special test mode.

8. The test device of claim 1 wherein the one or more PCBs includes a PCB of an add-in card and the DUT is a motherboard, the add-in card configured to be plugged into a connector on the motherboard to implement physical and link logical layers for each lane of the single-lane or multi-lane high speed I/O link.

9. The test device of claim 8 wherein the add-in card is a PCI Express add-in card.

10. The test device of claim 1 wherein the controller is configured to assess the electrical margin of the single-lane or multi-lane high speed I/O link by at least being configured to inject adjustable stress on margin test transmitters, the adjustable stress including one or more of: reduction of eye width opening and reduction of eye height opening.

11. The test device of claim 10 wherein the controller is configured to assess the electrical margin of the single-lane or multi-lane high speed I/O link by at least being configured to inject reduction of eye width

opening by injecting jitter on margin test transmitters, the injection of jitter being selectable to be applied on all lanes of the single-lane or multi-lane high speed I/O link simultaneously or applied independently per lane of the of the single-lane or multi-lane high speed I/O link.

12. The test device of claim 10 wherein the controller is configured to assess the electrical margin of the single-lane or multi-lane high speed I/O link by at least being configured to inject reduction of eye height opening by injecting noise on margin test transmitters, the injection of noise being selectable to be applied on all lanes of the single-lane or multi-lane high speed I/O link simultaneously or applied independently per lane of the of the single-lane or multi-lane high speed I/O link.

13. The test device of claim 10 wherein the controller is configured to assess the electrical margin of the single-lane or multi-lane high speed I/O link by at least being configured to inject reduction of eye width and eye height opening by injecting differential noise on margin test transmitters, the injection of differential noise being selectable to be applied on all lanes of the single-lane or multi-lane high speed I/O link simultaneously or applied independently per lane of the of the single-lane or multi-lane high speed I/O link.

14. A method for electrical margin testing a device under test (DUT), the method comprising:

establishing, by a test device, a multi-lane high speed I/O link of the DUT; and

assessing, by the test device, an electrical margin, in either or both transmit (Tx) and receive (Rx) directions, for each high-speed input/output (I/O) lane of the multi-lane high speed I/O link.

15. The method of claim 14 wherein the assessing the electrical margin includes injecting adjustable stress on margin test transmitters of the multi-lane high speed I/O link, the adjustable stress including injection of jitter or other method of eye width closing applied on all lanes of the multi-lane high speed I/O link simultaneously or applied independently per lane and applying noise or other method of eye height reduction.

16. The method of claim 15 wherein the assessing the electrical margin includes assessing the electrical margin, in either or both Tx and Rx directions, simultaneously for each high-speed I/O lane of the multi-lane high speed I/O link.

17. The method of claim 14 wherein the assessing the electrical margin includes:

assessing, by the test device, for each DUT of a plurality of devices under test (DUTs), timing eye width margin, in either or both Tx and receive Rx directions, for each high-speed I/O lane of a multi-lane high speed I/O link of the DUT;

detecting, based on the assessing, timing eye width margin measurements for each DUT of the plurality of DUTs that are consistently below a predetermined threshold for a same lane across the plurality of DUTs; and

identifying a potential DUT design issue based on the detection of the eye width and/or eye height margin measurements for each DUT of the plurality of DUTs that are consistently below the predetermined threshold for the same lane across the plurality of DUTs.

18. The method of claim 14 wherein the assessing the electrical margin includes:

assessing, by the test device, for each DUT of a plurality of DUTs, eye width and/or eye height margin, in either or both Tx and Rx directions, for each high-speed I/O lane of a multi-lane high speed I/O link of the DUT;

detecting, based on the assessing, timing eye width margin measurements for multiple DUTs of the plurality of DUTs that are each below a predetermined threshold for different lanes across the multiple DUTs; and

identifying a potential DUT assembly or production issue based on the detection of the timing eye width margin measurements for the multiple DUTs that are each below the predetermined threshold for different lanes across the multiple DUTs.

19. A non-transitory computer-readable storage medium having computer-executable instructions stored thereon that, when executed, cause at least one processor to:

provide user-selectable options for a test device that is configured to establish a multi-lane high speed input/output (I/O) link of a device under test (DUT) and to assess an electrical margin of the multi-lane high speed I/O link in either or both transmit (Tx) and receive (Rx) directions, the user-selectable options including customizations for assessment of the electrical margin of the multi-lane high speed I/O link;

receive an indication of selection of one or more of the user-selectable options for the test device; and

initiate performance by the test device of the assessment of the electrical margin of the multi-lane high speed I/O link based on the indication of the selection of the one or more of the user-selectable options for the test device.

20. The non-transitory computer-readable storage medium of claim 19 wherein the user-selectable options include one or more of:

- a selectable option to choose one or more different high-speed I/O protocols with which to perform margin testing test based on the multi-lane high speed I/O link of the DUT;

- a selectable option to test multiple ports of the DUT with mixed protocols simultaneously;

- a selectable option to output run-to-run variation in margin over any number of margin test runs of the test device on the multi-lane high speed I/O link;

- a selectable option to implement fixed Tx Equalization (EQ) on the DUT to test how much of margin variation is due to Tx EQ training variation;

- a selectable option to use Fixed Continuous Time Linear Equalization (CTLE) in receivers of the test device to test impact of receiver equalization on margin of the multi-lane high speed I/O link of the DUT;

- a selectable option to use Decision Feedback Equalization (DFE) in the receivers of the test device to test impact of receiver equalization on margin of the multi-lane high speed I/O link of the DUT;

- a selectable option to calculate expected margins for the test device based on target channels;

- a selectable option to automatically produce debug information when low margins are detected as a result of the assessment of the electrical margin of the multi-lane high speed I/O link;

- a selectable option for the test device to switch to using variable Inter Symbol Interference (ISI) source to find how much ISI causes lanes of the multi-lane high speed I/O link to fail;

- a selectable option for the test device to test each lane individually to identify an amount of margin loss to due to cross-talk of the multi-lane high speed I/O link of the DUT;

a selectable option to turn off DFE in the receivers of the test device to assess margin with and without DFE and an amount of non-linear discontinuities in each channel associated with the multi-lane high speed I/O link;

a selectable option for characterization data for the test device that shows expected margins with reference receivers and typical channels and allows lower than expected margin to be flagged even when the lower than expected margin is consistent across all lanes of the multi-lane high speed I/O link of the DUT and of multiple DUTs;

a selectable option to select from multiple speeds of the multi-lane high speed I/O link on which the assessment of the electrical margin is performed;

a selectable option for the test device to infer when errors have happened at the receivers of the DUT based on traffic traveling in an opposite direction on the multi-lane high speed I/O link by the test device using protocol specific knowledge to enable the test device to perform margin tests on production lines without software on the DUT;

a selectable option to automatically capture Time-Domain Reflectometry readings (TDRs) of low margin channels detected as a result of the assessment of the electrical margin of the multi-lane high speed I/O link;

a selectable option to perform an automated connection to an oscilloscope to automatically capture digitized waveforms when low margins are detected as a result of the assessment of the electrical margin of the multi-lane high speed I/O link; and

a selectable option to configure the one or more of the user-selectable options for the DUT by configuring DUT silicon to implement the one or more of the user-selectable options.

21. The non-transitory computer-readable storage medium of claim 19 wherein the computer-executable instructions, when executed, cause the at least one processor to cause the test device to do one or more of:

- choose one or more different high-speed I/O protocols with which to perform margin testing test based on the multi-lane high speed I/O link of the DUT;

- test multiple ports of the DUT with mixed protocols simultaneously;

- output run-to-run variation in margin over any number of margin test runs of the test device on the multi-lane high speed I/O link;

- implement fixed Tx Equalization (EQ) on the DUT to test how much of margin variation is due to Tx EQ training variation;

- use fixed continuous time linear equalization (CTLE) in receivers of the test device to test impact of receiver equalization on margin of the multi-lane high speed I/O link of the DUT;

- use decision feedback equalization (DFE) in the receivers of the test device to test impact of receiver equalization on margin of the multi-lane high speed I/O link of the DUT;

- calculate expected margins for the test device based on target channels;

- automatically produce debug information when low margins are detected as a result of the assessment of the electrical margin of the multi-lane high speed I/O link;

- switch to using variable Inter Symbol Interference (ISI) source to find how much ISI causes lanes of the multi-lane high speed I/O link to fail;

- test each lane individually to identify an amount of margin loss to due to cross-talk of the multi-lane high speed I/O link of the DUT;

- turn off DFE in the receivers of the test device to assess margin with and without DFE and an amount of non-linear discontinuities in each channel associated with the multi-lane high speed I/O link;

show expected margins with reference receivers and typical channels and allows lower than expected margin to be flagged even when the lower than expected margin is consistent across all lanes of the multi-lane high speed I/O link of the DUT and of multiple DUTs;

select from multiple speeds of the multi-lane high speed I/O link on which the assessment of the electrical margin is performed;

infer when errors have happened at the receivers of the DUT based on traffic traveling in an opposite direction on the multi-lane high speed I/O link by the test device using protocol specific knowledge to enable the test device to perform margin tests on production lines without software on the DUT;

automatically capture Time-Domain Reflectometry readings (TDRs) of low margin channels detected as a result of the assessment of the electrical margin of the multi-lane high speed I/O link;

perform an automated connection to an oscilloscope to automatically capture digitized waveforms when low margins are detected as a result of the assessment of the electrical margin of the multi-lane high speed I/O link; and

provide a software plug in to configure the one or more of the user-selectable options for the DUT by configuring DUT silicon to implement the one or more of the user-selectable options.

22. A margin tester, comprising:

a motherboard; and

at least one slot coupled to the motherboard to margin test at least one add-in card, wherein the motherboard is configured to assess an electrical margin of a multi-lane high speed input/output (I/O) link of the add-in card in either or both transmit (Tx) and receive (Rx) directions after the add-in card is inserted into the at least one slot.

23. The margin tester of claim 22 wherein the multi-lane high speed I/O link of the add-in card is a fully running operational link without a special test mode.

24. The margin tester of claim 22 wherein the motherboard is configured to assess the electrical margin of the multi-lane high speed I/O link by at least being configured to:

inject controlled noise on margin test transmitters; and
vary an eye margin expected at a receiver of the motherboard to specific targets for timing or voltage margin.

25. The margin tester of claim 22 wherein the motherboard is configured to assess the electrical margin of the multi-lane high speed I/O link by at least being configured to:

inject jitter on margin test transmitters; and
vary an eye margin expected at a receiver of the motherboard to specific targets for timing or voltage margin.

26. The margin tester of claim 22 wherein the motherboard is configured to assess the electrical margin of the multi-lane high speed I/O link by at least being configured to cause margin test receivers to measure eye margin by moving an independent error detector and comparing for mismatches with a data sampler.

27. The margin tester of claim 22 wherein the motherboard is configured to provide different margin test modes to enable problem characterization of the add-in card based on margin test measurements.

28. The margin tester of claim 22 wherein the motherboard is configured to assess the electrical margin of the multi-lane high speed I/O link

by at least being configured to inject reduction of eye width and eye height opening by injecting differential noise on margin test transmitters, the injection of differential noise being selectable to be applied on all lanes of the multi-lane high speed I/O link simultaneously or applied independently per lane of the of the multi-lane high speed I/O link.

29. The margin tester of claim 22 wherein the motherboard is configured to assess the electrical margin of the multi-lane high speed I/O link by at least being configured to inject jitter on margin test transmitters, the injection of jitter being selectable to be applied on all lanes of the multi-lane high speed I/O link simultaneously or applied independently per lane of the of the multi-lane high speed I/O link.

30. The margin tester of claim 29 wherein the injection of jitter is selectable to be applied on all lanes of the multi-lane high speed I/O link simultaneously or applied independently per lane of the of the multi-lane high speed I/O link.

31. The margin tester of claim 29 wherein the motherboard is configured to inject jitter on margin test transmitters by at least being configured to modulate an electrical length of a signal path to effect a jitter characteristic relative to an assumed ideal constant timing fiducial.

32. The margin tester of claim 29 wherein the motherboard is configured to inject jitter on margin test transmitters using a varactor-based method.

33. A method, comprising:
calibrating a margin tester, enabling a user to receive a set of expected margins with a series of reference channels; and

providing the calibrated margin tester configured to measure electrical eye margin in either or both transmit (Tx) and receive (Rx) directions of a device under test (DUT) with a fully running operation link of the DUT without special test modes and to capture full loading and cross-talk effects.

34. The method of claim 33, further comprising:

providing an individually calibrated model for the margin tester, enabling computation of expected margins with one or more of: individualized system channels, receiver models and transmitter models.

35. The method of claim 33, further comprising:

providing a software plug-in model in a configuration software application for the margin tester, enabling silicon vendors to provide software plug-ins that enable configuration and DUT silicon parameters for running margin tests by the margin tester under different conditions for the DUT silicon.

36. The method of claim 33, further comprising:

providing a feature in DUT silicon, enabling the margin tester to use vendor defined messages or another protocol mechanism to indicate that a margin test is about to take place by the margin tester, causing the DUT silicon to be able to disable logic that would degrade link width or speed of the link due to errors for a duration of the margin test.

37. The method of claim 33, further comprising:

providing a software applications of the margin tester, enabling performance of testing by the margin tester of a channel component under test in a testing configuration where a margin tester is used on both sides of the channel component under test.

38. The method of claim 37 wherein the channel component under test is a bare printed circuit board (PCB) or a cable.

39. The method of claim 33, further comprising:
providing hardware of the margin tester to a company that manufactures a printed circuit board (PCB); and
providing data associated with use of the margin tester to silicon companies which provide silicon used in production of the PCB.

40. A non-transitory computer-readable storage medium having computer-executable instructions stored thereon that, when executed, cause at least one processor to:
receive configuration settings for a device under test (DUT); and
configure the DUT for running margin tests by a margin tester under different conditions for silicon of the DUT.

41. The non-transitory computer-readable storage medium of claim 39 wherein the computer-executable instructions, when executed, cause the at least one processor to cause the margin tester to do one or more of:
receive a software plug-in that enables configuration and DUT silicon parameters for running the margin tests by the margin tester under the different conditions for the silicon of the DUT.

42. The non-transitory computer-readable storage medium of claim 41 wherein the DUT silicon parameters include one or more of:
parameters related to receiver continuous time linear equalization (CTLE) and
parameters related to decision feedback equalization (DFE).

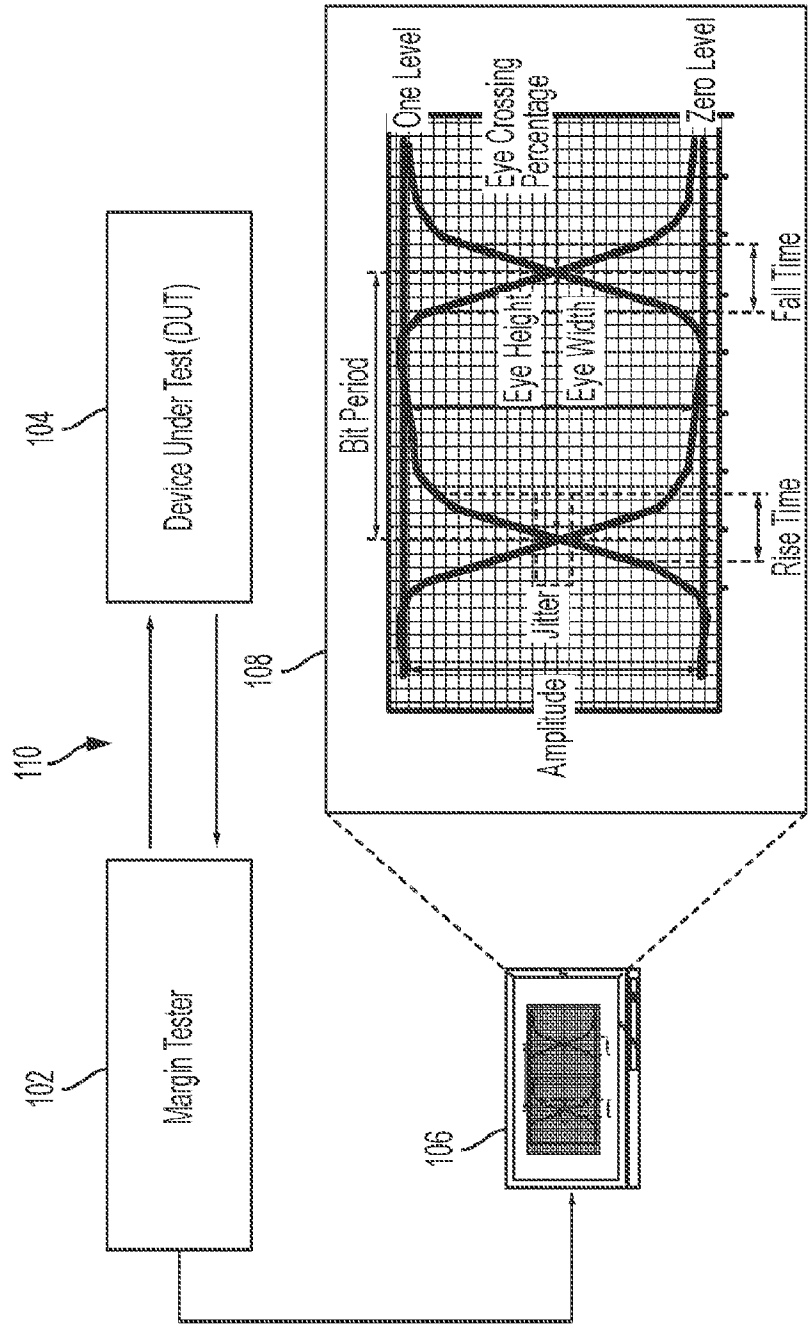
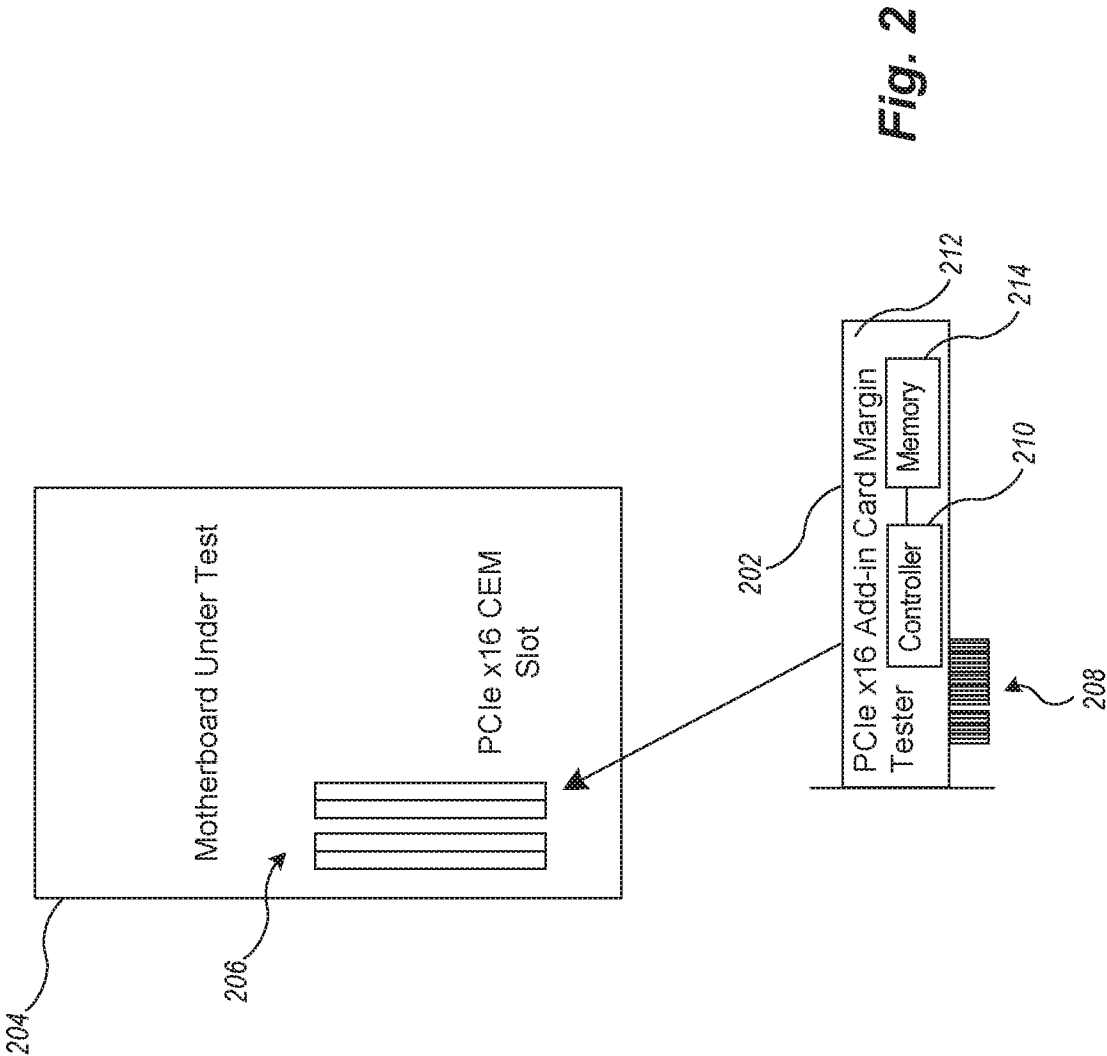


Fig. 1



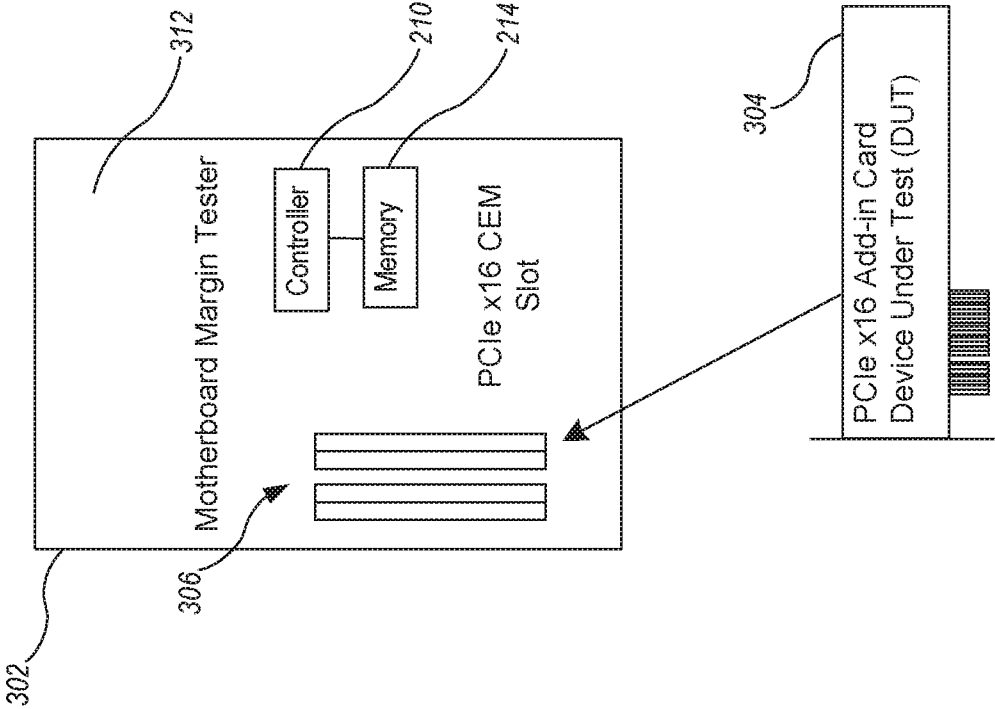


Fig. 3

402 ↗

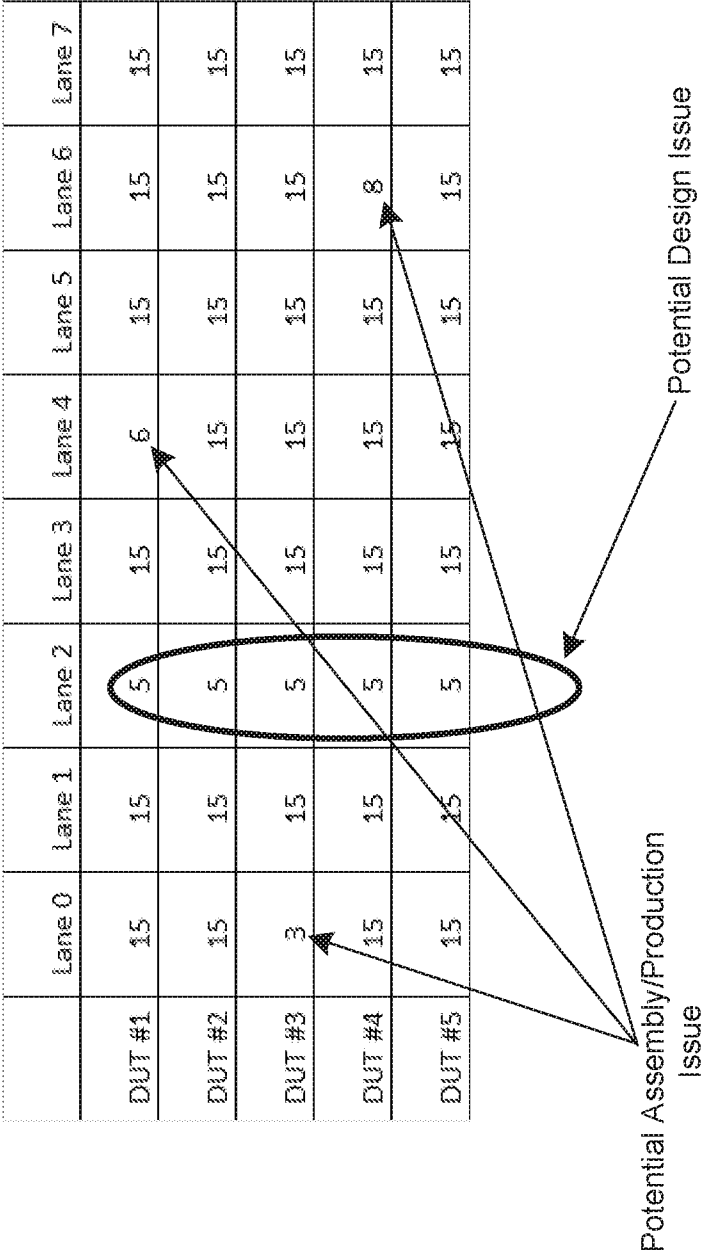


Fig. 4

502

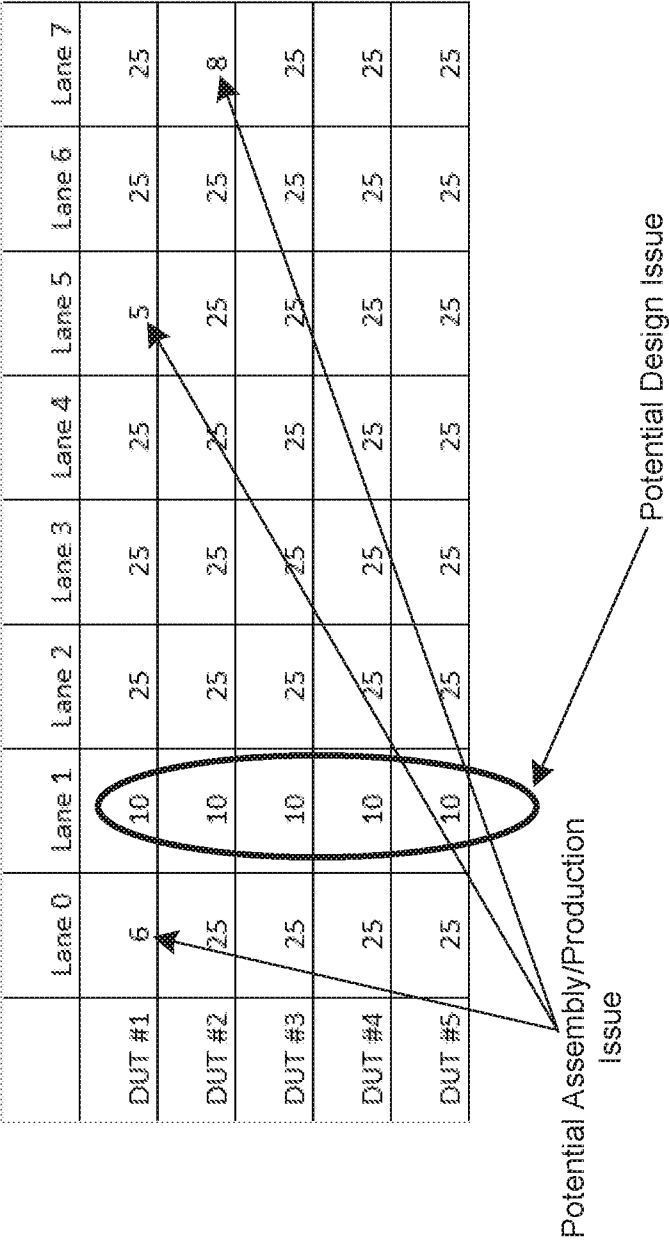


Fig. 5

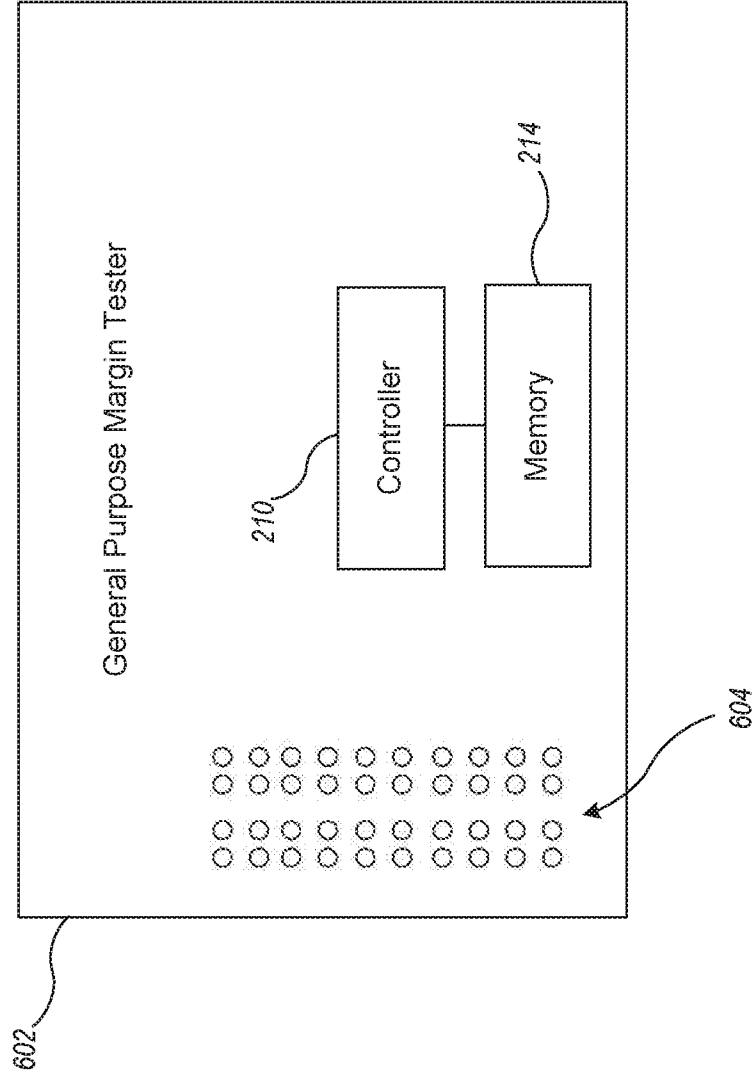


Fig. 6

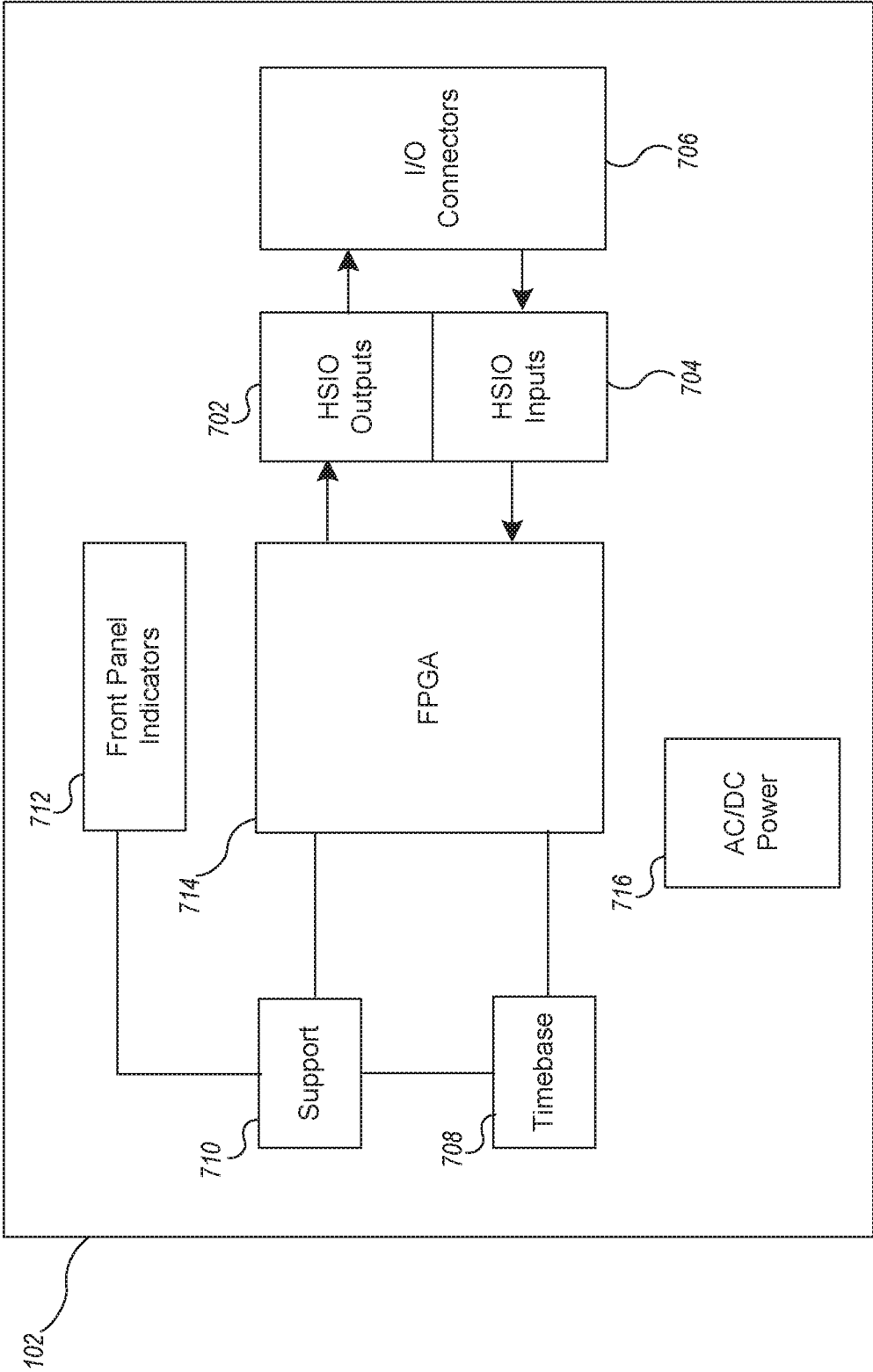


Fig. 7

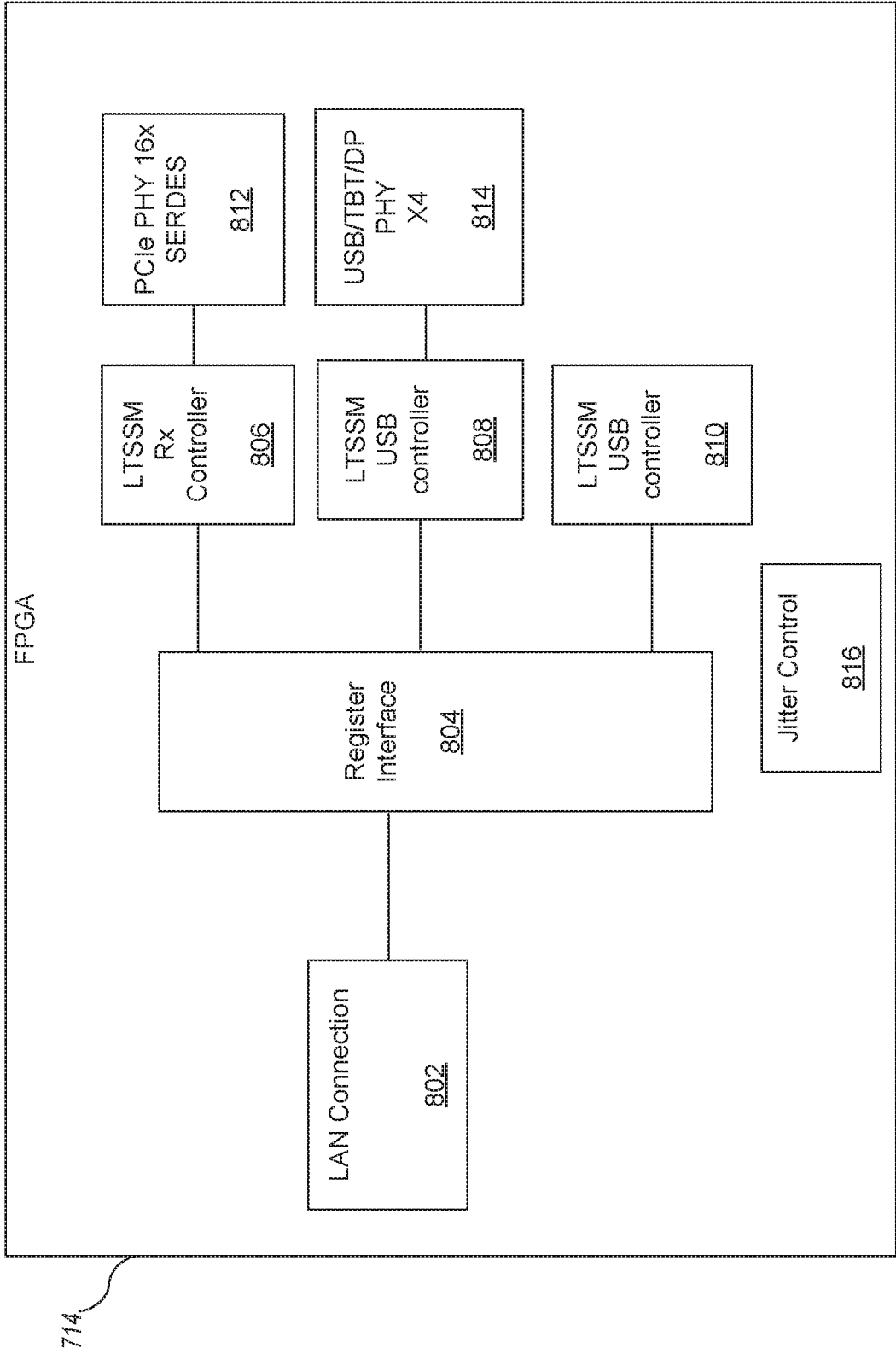
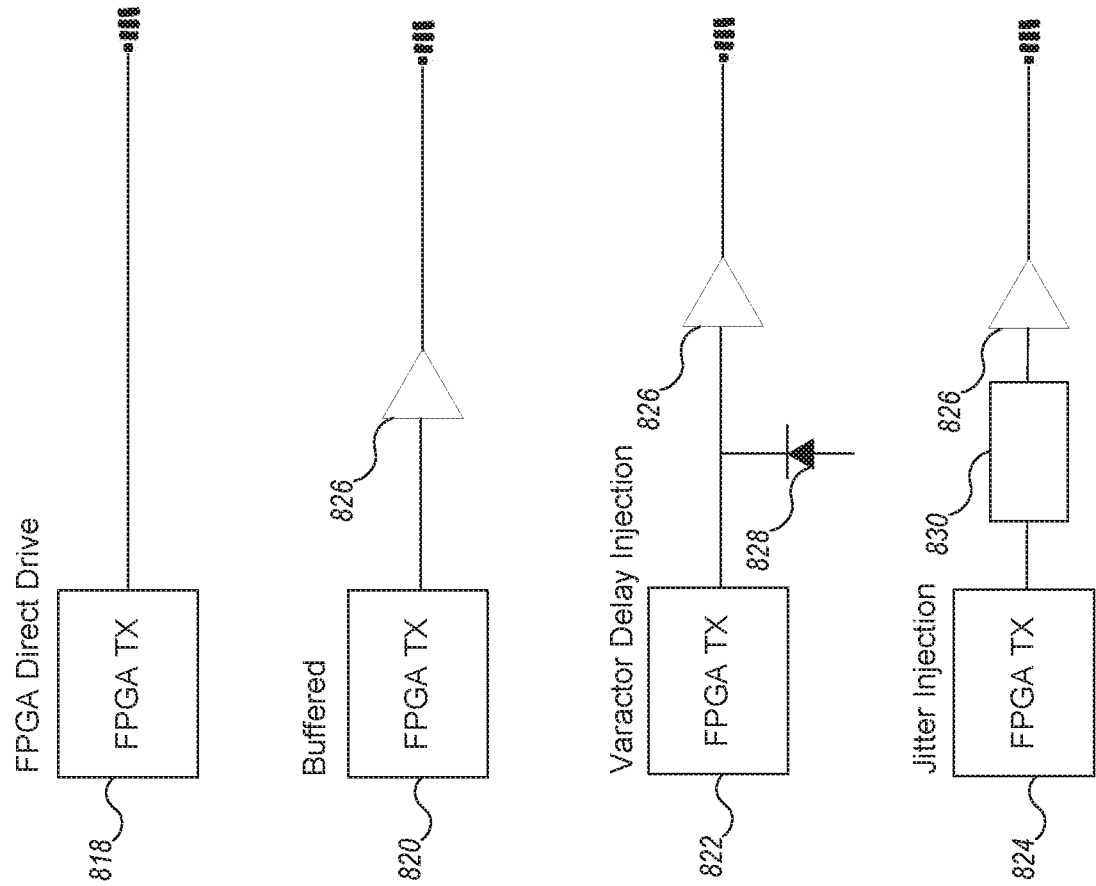


Fig. 8

Fig. 9



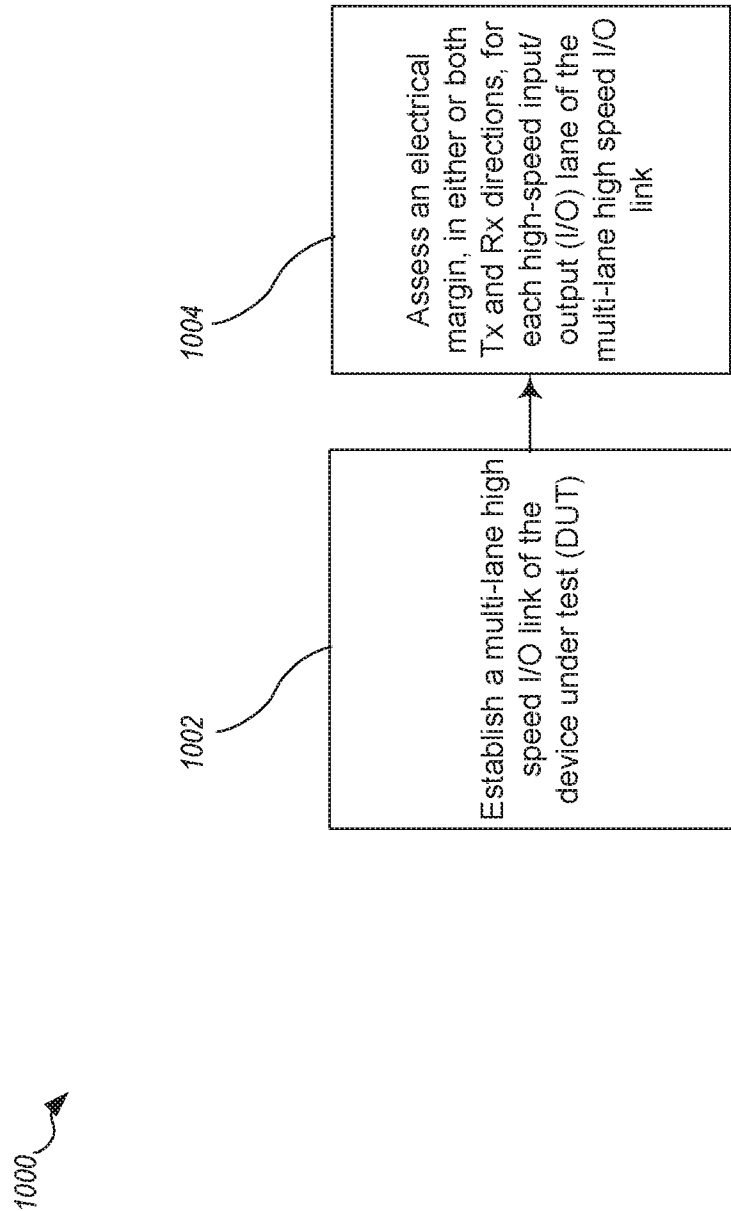


Fig. 10

1100 ↗

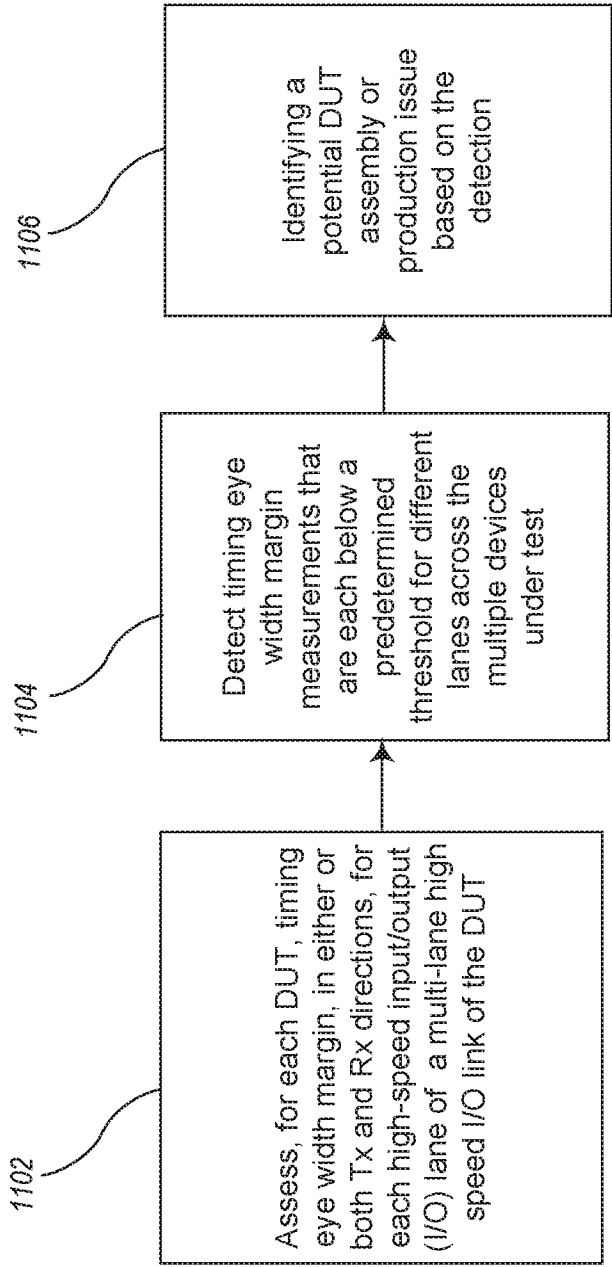


Fig. 11

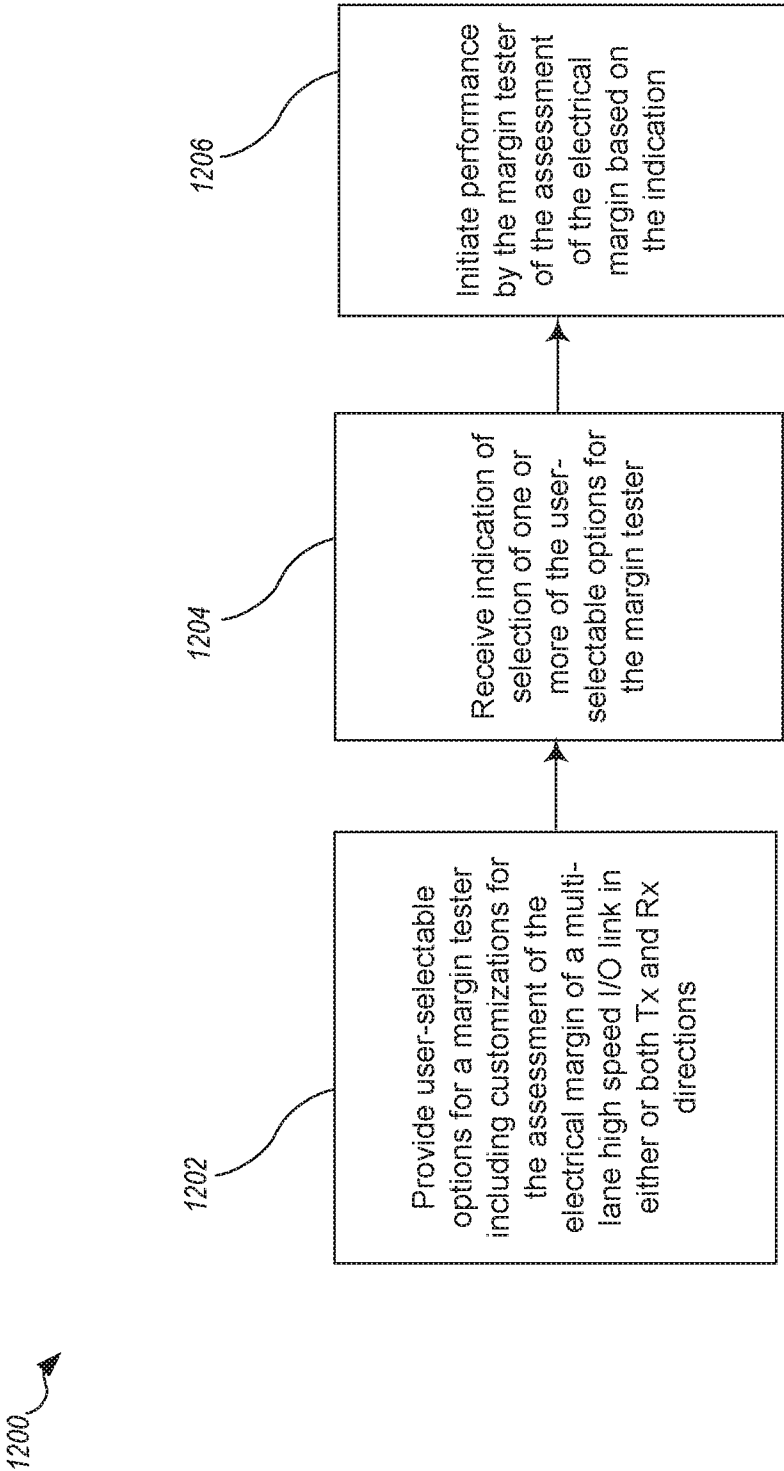


Fig. 12

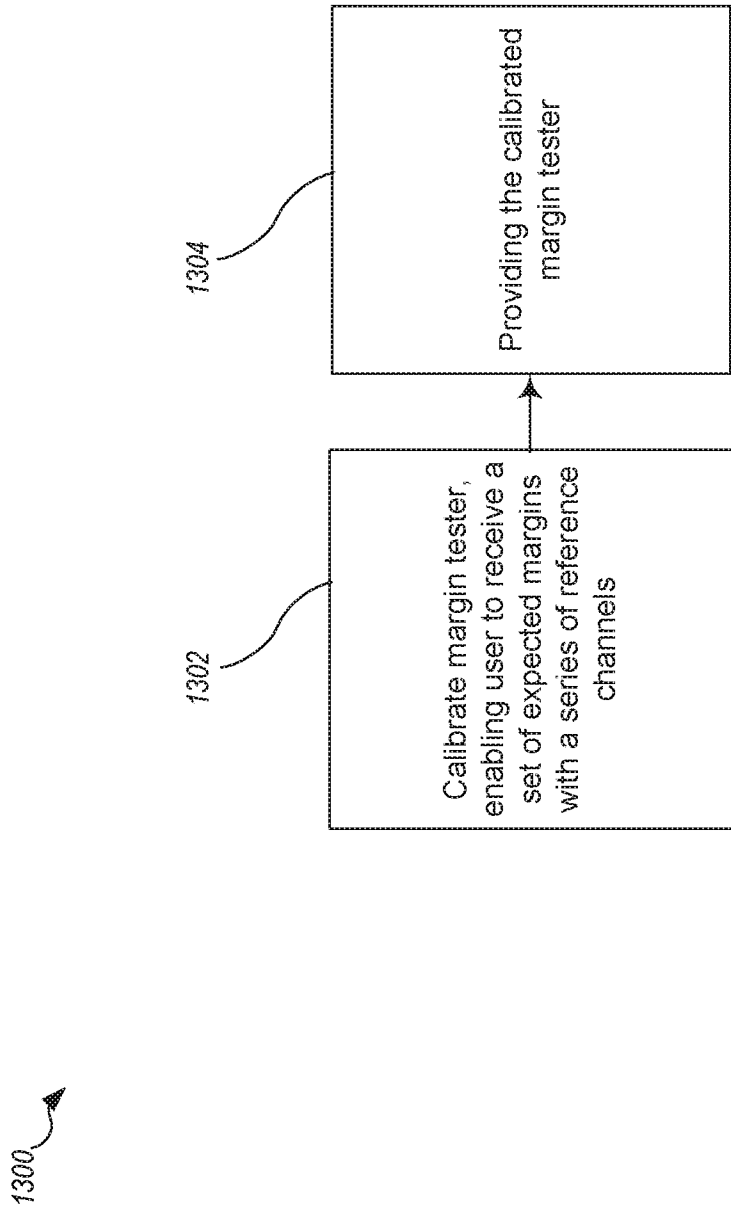


Fig. 13

1400

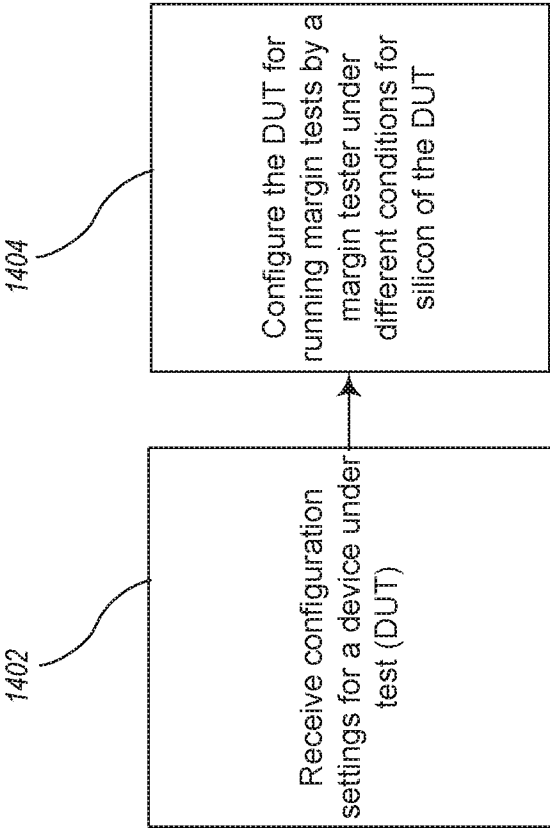


Fig. 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2020/016220

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☒ Claims Nos.: 22-42
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of Item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2020/016220

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F11/273 G01R31/317 H04L12/26
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G01R H04L G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/192814 A1 (HAFED MOHAMED M [CA] ET AL) 14 August 2008 (2008-08-14) figures 1,4-7,10-16 paragraph [0027] - paragraph [0029] paragraph [0034] - paragraph [0040] paragraph [0044] - paragraph [0045] paragraph [0052] - paragraph [0060] ----- -/--	1-21



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

26 May 2020

Date of mailing of the international search report

08/06/2020

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
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Authorized officer

Alonso Nogueiro, L

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2020/016220

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	LYONS TIMOTHY ET AL: "The implementation and application of a protocol aware architecture", 2013 IEEE INTERNATIONAL TEST CONFERENCE (ITC), IEEE, 6 September 2013 (2013-09-06), pages 1-10, XP032520877, ISSN: 1089-3539, DOI: 10.1109/TEST.2013.6651911 [retrieved on 2013-11-01] page 1 - page 9 figures 1-16	1-21
A	----- US 2013/145212 A1 (HSU LINDEN [US] ET AL) 6 June 2013 (2013-06-06) paragraph [0013] - paragraph [0016] paragraph [0040] - paragraph [0041] paragraph [0044] - paragraph [0049] paragraph [0086] figures 1-4	1-21
A	----- ABDENNADHER SALEM ET AL: "Practices in High-Speed IO testing", 2016 21TH IEEE EUROPEAN TEST SYMPOSIUM (ETS), IEEE, 23 May 2016 (2016-05-23), pages 1-8, XP032928443, DOI: 10.1109/ETS.2016.7519317 [retrieved on 2016-07-22] page 4 - page 8 figures 6-9	1-21
A	----- "PCI Express Base Specification Revision 3.0; Introduction and Physical Layer Specification", 10 November 2010 (2010-11-10), pages 37-412, XP055096393, Retrieved from the Internet: URL:http://komposter.com.ua/documents/PCI_Express_Base_Specification_Revision_3.0.pdf [retrieved on 2014-01-14] page 366 - page 375 -----	1-21

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2020/016220

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008192814 A1	14-08-2008	EP 2115940 A2	11-11-2009
		JP 2010518760 A	27-05-2010
		TW 200935781 A	16-08-2009
		US 2008192814 A1	14-08-2008
		WO 2008098202 A2	14-08-2008

US 2013145212 A1	06-06-2013	NONE	

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box II.2

Claims Nos.: 22-42

Although claims 1, 14, 19, 22, 33 and 40 have been drafted as separate independent claims, they relate partially to the same shared subject-matter and differ from each other by some features contained only in individual claims. These claims differ in respect of the terminology used for the features of that shared subject-matter. The aforementioned claims therefore lack conciseness and as such do not meet the requirements of Article 6 PCT.

Claims 1, 14 and 19 are directed to a tester device and method for testing electrical margin of multi-lane high-speed serial links. Claim 22 seems to be directed basically also to this subject-matter but using a different wording and leaves out some features. A search covering claims 1 to 21 roughly covers all subject-matter of claims 22 to 32. Claim 33 is not directed at testing high-speed serial links and covers calibration and capturing full-load and cross-talk effects. Claim 40 does not cover the type of device being tested, but comprises receiving configuration settings and testing under different conditions.

The independent claims are drafted in such a way that the claims as a whole are not in compliance with the provisions of clarity and conciseness of Article 6 PCT. The non-compliance with the substantive provisions is to such an extent, that the search was performed taking into consideration the non-compliance in determining the extent of the search (PCT Guidelines 9.19). The extent of the search was consequently limited to claims 1 to 21, which appears to comprise a reasonable definition of what is understood to be the invention for which protection is sought.

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guidelines C-IV, 7.2), should the problems which led to the Article 17(2) declaration be overcome.