United States Patent

[11] **3,543,929**

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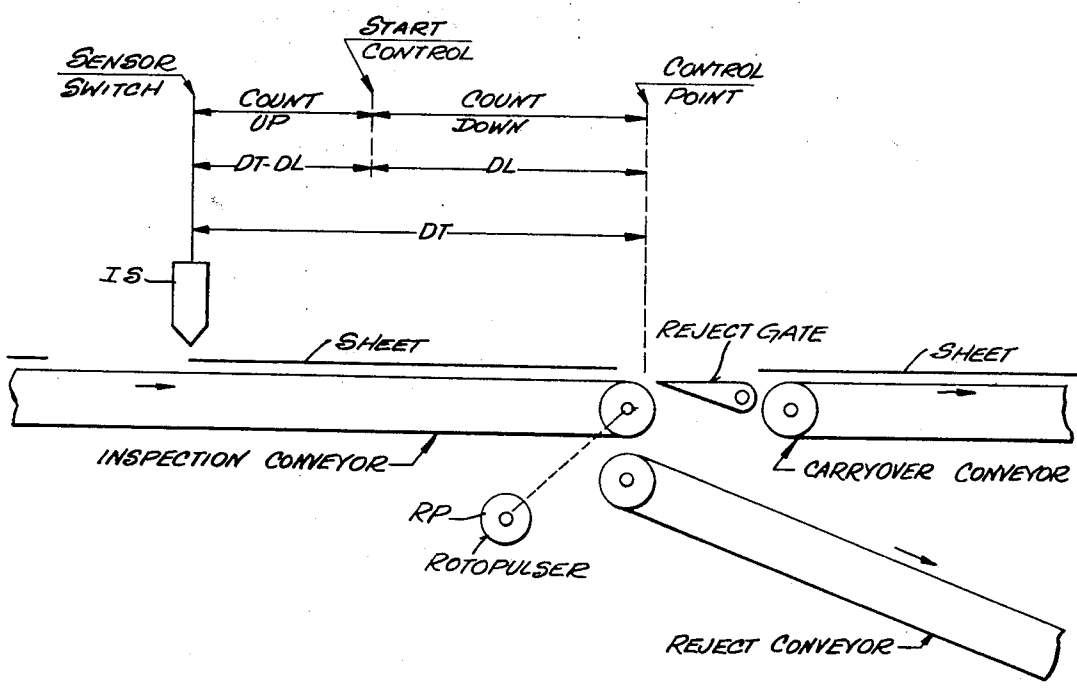   a corporation of Delaware

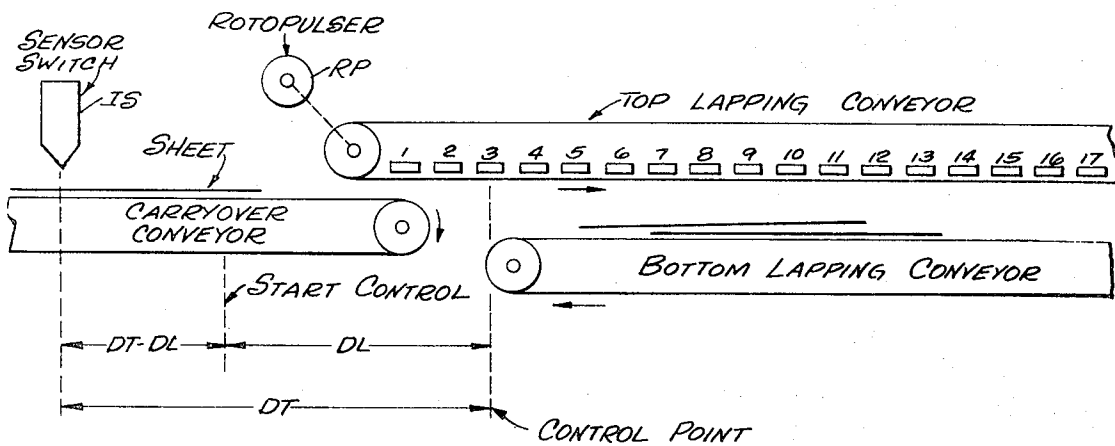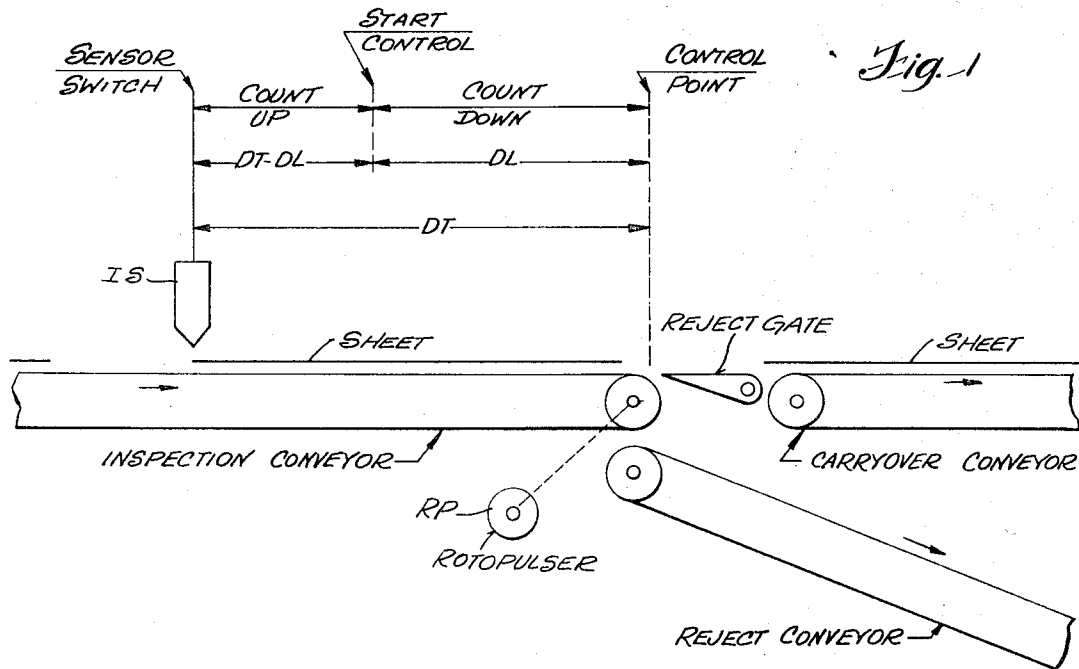[54] **LEAD DISTANCE COMPENSATION AND MAGNET SEQUENCING CONTROL SYSTEM FOR ARTICLE CONVEYORS**
11 Claims, 5 Drawing Figs.

[52] U.S. Cl.. **209/74,**
                                                          83/79
[51] Int. Cl.. **B07c 5/36**
[50] Field of Search..209/74, Cut
                        & Sort(Digest); 271/64; 83/79; 93/93

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ABSTRACT: A lead distance compensator that sets the time, relative to conveyor travel, at which an operation is initiated to allow for the operating time delay of the apparatus and automatically adjusts this time when the conveyor speed varies or is changed. The total distance from the article detector to the operation point (reject gate opening or magnet deenergization) includes the lead distance and the compute time, that is, the time it takes to compute the lead distance in terms of distance of conveyor travel. To provide for maximum lead distance variation, the compute time is scaled for very fast operation, thereby allowing greater variation in the lead distance within a given fixed time period. When used for reject gate operation, the system effects opening of the gate just ahead of the leading edge of a sheet and reclosing of the gate just ahead of the leading edge of the next sheet of closely spaced sheets. When used for magnet control, the system effects deenergization of magnets to drop metal sheets trailing end first onto a pile or in overlapping arrangement. Additionally, in the latter case, pulse frequency division apparatus provides for reenergization of the magnets in sequence just ahead of the leading edge of the next sheet.

Fig. 1

SENSOR SWITCH

START CONTROL

CONTROL POINT

COUNT UP

COUNT DOWN

DT-DL

DL

DT

IS

SHEET

REJECT GATE

SHEET

INSPECTION CONVEYOR

CARRYOVER CONVEYOR

RP

ROTOPULSER

REJECT CONVEYOR

SENSOR SWITCH

ROTOPULSER

RP

IS

TOP LAPPING CONVEYOR

SHEET

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17

CARRYOVER CONVEYOR

BOTTOM LAPPING CONVEYOR

START CONTROL

DT-DL

DL

DT

CONTROL POINT

Fig. 3

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Fig. 2
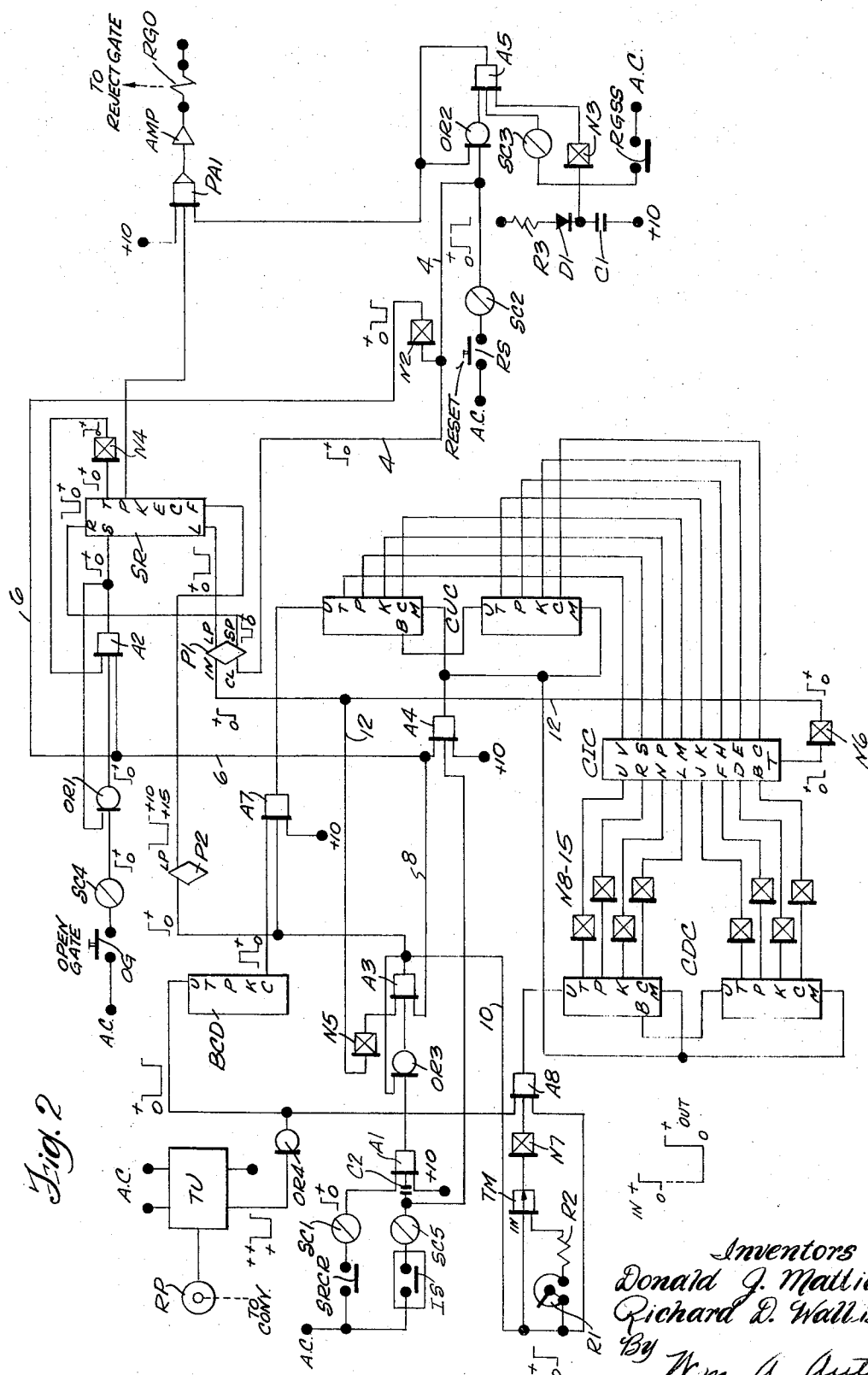
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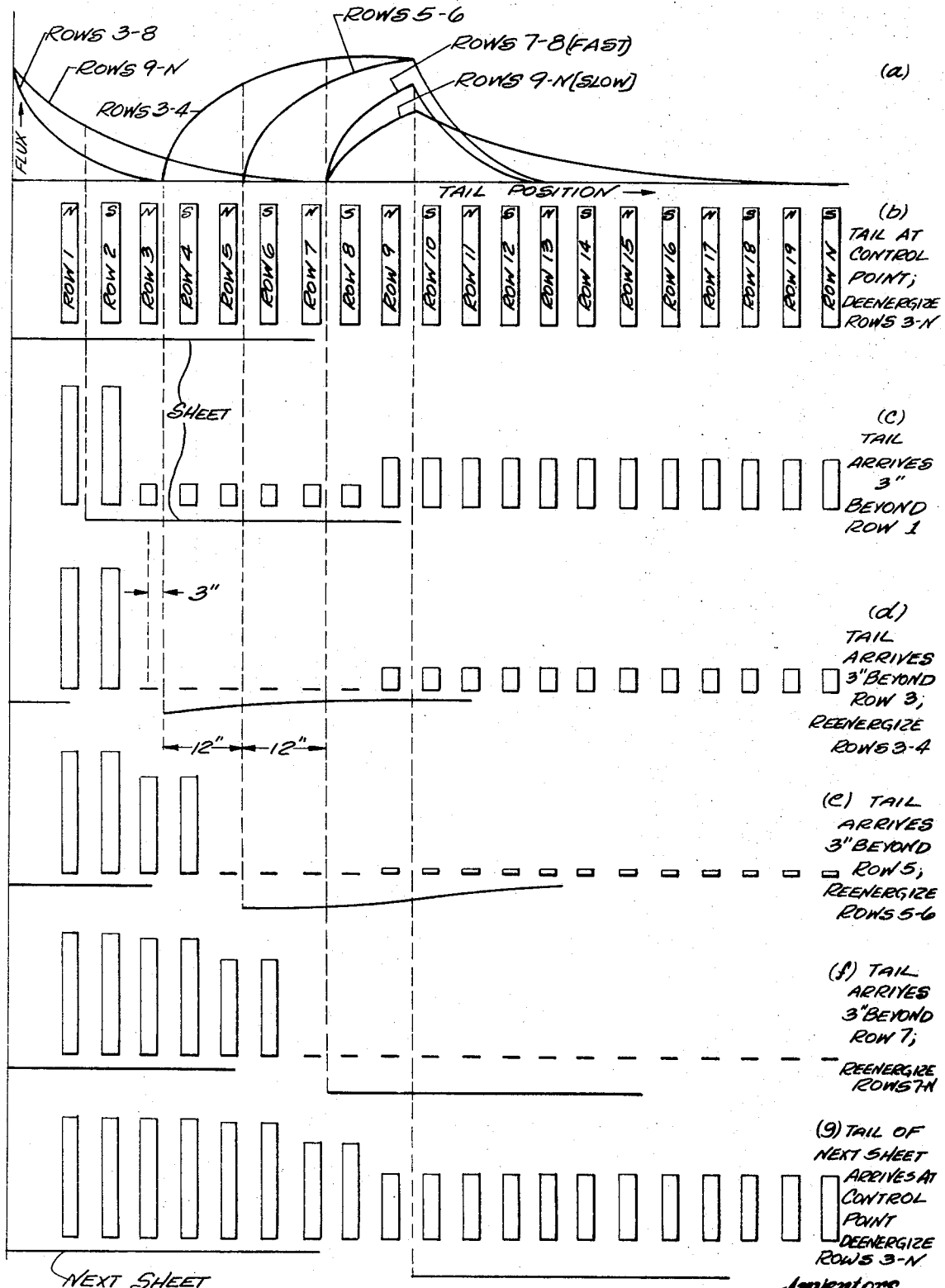Richard D. Wallis
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Fig. 4

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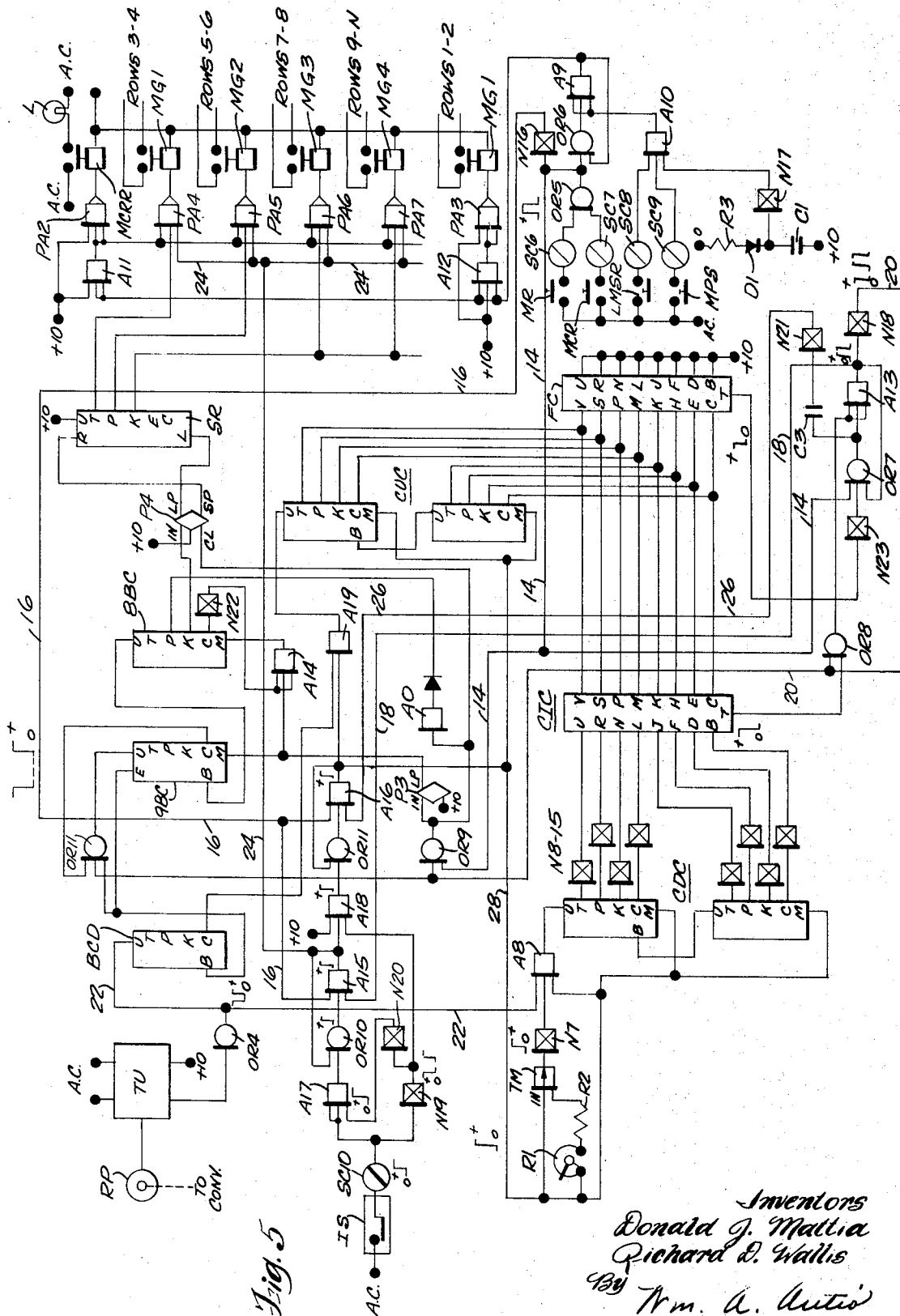Donald J. Mallia
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Fig. 5

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LEAD DISTANCE COMPENSATION AND MAGNET SEQUENCING CONTROL SYSTEM FOR ARTICLE CONVEYORS

BACKGROUND OF THE INVENTION

Lead distance compensators have been known heretofore such as that disclosed in J. W. Loeffler U.S. Pat. No. 3,027,817, dated April 3, 1962. In this patent, a pulse counter is arranged to count out in response to a number of conveyor-speed generated main positive pulses corresponding to the distance from a newspaper count detector to an intercept blade. In order to provide a delay time for intercept blade operation, additional positive pulses are generated for a fixed time interval equal to the delay time at the beginning of the count period and applied to the pulse counter. This will cause the counter to count out and initiate intercept blade operation one delay time before the first newspaper to be intercepted arrives thereat. In order to compensate for varying conveyor speed, the additional pulses are generated under conveyor drive control whereby the delay distance is adjusted in proportion to change in conveyor speed. In this patent, these additional positive pulses are conveniently obtained by inverting the negative half-cycles of an alternating current whereas the positive half-cycles provide the main positive pulses. This affords a double rate or frequency of pulses for the compute period.

While these prior lead distance compensator systems have been satisfactory for their intended purposes, the present invention is an improvement thereon.

SUMMARY OF THE INVENTION

This invention relates to improved lead distance compensation control systems and to such systems combined with magnet sequencing control systems for article conveyors.

An object of the invention is to provide an improved lead distance compensation control system.

A more specific object of the invention is to provide a lead distance compensation control system for an article conveyor with improved means affording faster computation of the delay time to allow greater variation in the lead distance within a given fixed time period.

Another specific object of the invention is to provide such lead distance compensation control system with improved means affording sequential operation of control devices following the lead distance controlled operation.

Another specific object of the invention is to provide such lead distance compensation control system including such improved means that is simple in construction and reliable in operation.

Other objects and advantages of the invention will hereinafter appear.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic illustration of an inspection conveyor system including a reject gate to control of which the invention may be applied;

FIG. 2 is a schematic circuit diagram of a lead distance compensation control system for controlling the reject gate in FIG. 1;

FIG. 3 is a schematic illustration of a lapping conveyor system including rows of magnets to control of which the invention may be applied;

FIG. 4 is a graphic illustration of certain operating characteristics of the rows of magnets of FIG. 3; and

FIG. 5 is a schematic circuit diagram of a lead distance compensation control system combined with magnet sequencing means for controlling deenergization and sequential reenergization of the rows of magnets of FIG. 3 in the manner graphically depicted in FIG. 4.

DESCRIPTION OF PREFERRED EMBODIMENTS

Referring to FIG. 1, there is shown an inspection conveyor system to which the invention is applied. This system comprises an inspection conveyor that delivers metal sheets in spaced apart relation from a shear or the like where the sheets are cut from a continuous strip. These sheets normally pass over a reject gate to a carryover conveyor when the gate is closed. When the gate is opened, the next sheet is rejected onto a reject conveyor. For exemplary purposes, it may be assumed that an inspector, upon seeing a defective sheet, presses a button to cause such defective sheet to be selected for, and diverted onto, the reject conveyor. Or an optical or electronic device may be used for automatic selection.

To control operation of the reject gate for diverting of defective sheets, there is shown in FIG. 1 a sensor switch such as an inductoswitch IS or the like that detects the leading edge of a sheet and puts out an electrical signal to be used in the lead distance compensation control system of FIG. 2. There is also provided a pulse generator such as a rotopulser RP driven by the inspection conveyor for providing electrical pulses to be used in the system of FIG. 2 as hereinafter described.

FIG. 1 also shows certain functional distances during which the above signal and pulses control the system of FIG. 2. These distances include the total distance DT between inductoswitch IS and the reject gate that is made up of the lead distance DL and the difference between the total distance and the lead distance DT-DL during which counting takes place.

The lead distance is the distance between the leading edge of the sheet and the reject gate (control point) when reject gate operation is initiated, marked in FIG. 1 as START CONTROL. This lead distance in terms of sheet travel is equal to the time it takes for the reject gate to open following initiation of gate opening. This time remains substantially constant although the lead distance will vary in direct proportion to conveyor speed.

This lead distance DL in FIG. 1 is also marked COUNTDOWN that refers to the count put in at high frequency into countdown counter CDC in FIG. 2. The difference between the total distance and the lead distance DT-DL in FIG. 1 is also marked COUNTUP that refers to the countup counter CUC in FIG. 2. The purpose of the countdown and the countup will become more meaningful in connection with the description of FIG. 2. Briefly stated, each counter has a capacity equal to the total distance DT and counter CDC is counted down from maximum count at high speed equal to the lead distance DL so that when counter CUC has counted up to the difference count for coincidence with counter CDC, a start control is initiated for opening the gate. Both counters are controlled by the inspection conveyor automatically to adjust the lead distance for variation is in speed.

The operation of the system in FIG. 2 will now be described with reference to opening and reclosing the reject gate in FIG. 1.

To prepare the system for operation, shear run control relay contact SRCR at the left portion of FIG. 2 closes when the shear is started running to cut sheets. As a result, a.c. voltage of 115 volts or the like is applied through this contact to 115 volts or the like is applied through this contact to signal converter SC1. As shown in FIG. 2, the output of this a.c. signal converter is normally at 0 volts and goes to +10 volts d.c. when a.c. supply voltage is connected thereto.

Signal converters of this type are well known and therefore are shown schematically to avoid complicating the drawing. One type usable herein is the Cutler-Hammer 115 Volt a.c. Signal Converter comprising generally a step-transformer, transformer, a full-wave rectifier, a filter capacitor and a voltage divider output having a diode connection to a 10 volt bus to clamp the output as 10 volts.

This +10 volts output of signal converter SC1 is applied to a first one of the three inputs of AND logic circuit A1.

This AND logic circuit A1 provides a +10 volts output only when all three inputs are at +10 volts. Circuits of this type are

well known and are not shown in detail to avoid complicating the drawing. A suitable AND circuit that may be used herein is the Cutler-Hammer DSL THREE INPUT FAIL-SAFE "AND" BOARD NO. 30. If any input is at 0 volts, the output will be at 0 volts.

The third input of AND logic A1 receives +10 volts from a supply.

Variable resistor R1 that is connected through a fixed value "minimum" resistor R2 to timer circuit TM is assumed to be set at a value giving the timer an interval proportional to the time required for the reject gate to operate. Timers of this type are will known and the details have not been shown to avoid complicating the drawing. A suitable timer for use herein is a Cutler-Hammer DELAY AFTER ENERGIZATION TIMER BOARD NO. 7A. Its input and output signals will be described in detail as the description proceeds.

Since the logic circuits herein contain transistor flip-flops and the like that have a tendency to assume either one or the other operating condition when power is initially applied, means is provided for resetting the system prior to initial operation. This means comprises a reset pushbutton switch RS shown at the right portion of FIG. 2.

To reset the system, this switch momentarily is pressed. This connects alternating current supply voltage to an a.c. signal converter SC2 that applies +10 volts through conductor 4 to clear terminal CL of a pulser circuit P1. As a result, a short (5 microsecond) negative pulse is applied from short pulse output SP to reset terminal R of shift register SR. This causes all five outputs T, P, K, E and C of the shift register to be turned off, that is, reset to 0 voltage. A known pulser such as Cutler-Hammer DSL DYNAMIC PULSER BOARD NO. 28 may be used herein. Also, a known shift register such as Cutler-Hammer DSL FIVE BIT SHIFT REGISTER BOARD NO. 13 may be used herein.

This +10 volts is also applied from conductor 4 to NOT logic circuit N2 that inverts it to 0 volts which is applied through conductor 6 to the third input of AND logic circuit A2 to release any lockup between this AND logic and its preceding OR logic circuit OR1. A suitable NOT logic usable herein is the Cutler-Hammer NOT INVERTER BOARD NO. 3. This OR logic may be of known type such as Cutler-Hammer DSL THREE INPUT "OR" BOARD NO. 2. Conductor 6 also connects 0 volts to an input of each AND logic A3 and A4 to drop out these logics. Logic A4 applies 0 volts to reset terminals M to reset counters CDC and CUC to 0 condition.

This +10 volts from signal converter SC2 is further applied to one of the two inputs of OR logic circuit OR2. As a result, OR logic OR2 applies +10 volts to the first input of AND logic circuit A5 that feeds back a lockup signal to this OR logic as hereinafter described. The second input of AND logic A5 receives +10 volts from signal converter SC3, assuming that interlock contact RGSS is closed. This is a reject gate solenoid supply relay contact that closes when such supply power is turned on. Thus, a.c. voltage is applied through this interlock contact to signal converter SC3. The third input of AND logic A5 receives +10 volts from NOT logic circuit N3 that has its input connected to a momentary inhibiting circuit.

This momentary inhibiting circuit has a resistor R3, a diode D1 in its forward low impedance direction and a capacitor C1 connected in series in that order between 0 volts and +10 volts with the input of NOT logic N3 being connected to the junction between the diode and capacitor. This circuit inhibits lockup of AND logic A5 and OR logic OR2 when power is first applied to the system. Thus, when the power including the +10 volts is first applied, capacitor C1 charges through the baseemitter of a transistor in NOT logic N3. During this charging time, there is enough positive voltage at its input to maintain the output of NOT logic N3 at 0 volts. This holds AND logic A5 off. When capacitor C1 has fully charged, the input of NOT logic N3 goes to 0 volts to apply +10 volts from its output to condition AND logic A5 for operation as hereinbefore described.

This AND logic having now +10 volts on all three inputs applies +10 volts from its output as a feedback to the other input of OR logic OR2 to lock up these two logics into operating condition until power is again disconnected. This AND logic also applies +10 volts to the third input of power AND unit PA1 to condition this unit for operation as hereinafter described. A known power AND unit such as the Cutler-Hammer DSL THREE INPUT FAIL-SAFE 10V POWER "AND" BOARD NO. 32 may be used herein.

After momentary closing, the reset pushbutton switch is released to allow it to reopen. As a result, conductor 4 returns to 0 volts and conductor 6 returns to +10 volts. The system is now ready for operation and all that is required is for the operator to press the OPEN GATE pushbutton switch OG to divert the next sheet that reaches inductoswitch IS. If a sheet is already under the inductoswitch when the pushbutton is pressed, the system will reject the following sheet.

Assuming now that a sheet is approaching inductoswitch IS, the operator observes this sheet to be defective and presses the OPEN GATE pushbutton switch. This causes alternating current to be applied to signal converter SC4 so that its output goes from 0 to +10 volts. This output is applied to one of the two inputs of OR logic circuit OR1.

As a result, OR logic OR1 provides an output of +10 volts that is applied to the second of three inputs of AND logic circuit A2. The first input of AND logic A2 receives +10 volts from NOT logic circuit N4 there being no output from terminal T of shift register SR. Also, the third input of AND logic A2 receives +10 volts from NOT logic circuit N2 through conductor 6 as hereinbefore described.

As a consequence of the three input signals, AND logic A2 provides a +10 volts output that is applied back to the first input of OR logic OR1 to lock up these two logics as a memory whereby the information is retained for the approaching sheet. This AND logic A2 also applies +10 volts to terminal S of shift register SR to condition the latter for a set-in operation upon the detection of an approaching sheet as hereinafter described.

Referring to FIG. 1, when the leading edge of a sheet is detected by sensor switch IS, its contact shown in FIG. 2 closes and remains closed until the sheet passes out from under the sensor switch. Switch IS applies a.c. voltage to signal converter SC5. The output of the signal converter goes from 0 volts to +10 volts to apply a positive pulse through capacitor C2 to the second input of AND logic A1. The +10 volts is also applied from the signal converter to the second input of AND logic A4 to terminate the reset interval of the binary counters.

The binary counters including countdown counter CDC and countup counter CUC are reset while the space between sheets is going by inductoswitch IS. At such time, the inductoswitch IS contact is open so the that 0 volts is applied from the output of signal converter SC5 to the second input of AND logic A4. As a result, the output of this AND logic is at 0 volts to apply a long negative pulse to reset terminals M of the 4-bit binary units of each binary counter CDC and CUC. This resets these counters to 0 volts at all outputs T, P, K, and C thereof. As will be apparent, each counter is made up of two 4-bit binary units cascaded by connecting terminal B of the first unit to input terminal U of the second unit. This provides an 8-bit binary counter capable of counting up to 255 pulses. A suitable 4-bit binary counter for use herein is the Cutler-Hammer DSL FOUR BIT BINARY COUNTER BOARD NO. 16.

The aforesaid AND logic A1 that was pulsed at its second input when a sheet was detected receives +10 volts at its first input due to shear run control interlock contact SRCR being closed. Its third input receives +10 volts from a supply as aforesaid.

As a result of the foregoing, AND logic A1 applies a +10 volts pulse to an input of OR logic circuit OR3 causing it to apply a +10 volts pulse to the second input of AND logic A3. The first input of this AND logic receives +10 volts from the output of NOT logic circuit N5 since the input of the latter is at 0 volts.

5

This 0 volts comes from the output of NOT logic circuit N6 at the lower portion of FIG. 2, having a +10 volt input from terminal T of Coincidence circuit CIC. This coincidence circuit has a +10 volts output when its left and right sets of terminals do not have coincidence signals. The output changes to 0 volts when coincidence occurs as hereinafter described. A suitable coincidence circuit for use herein is the Cutler-Hammer DSL DIGITAL COINCIDENCE MODULE BOARD NO. 38.

Continuing with AND logic A3, its third input receives +10 volts from conductor 8. As a result, a feedback of +10 volts is applied from the output of AND logic A3 to an input of OR logic OR3 to lock up these two logics until count coincidence takes place as hereinafter described.

This +10 volts output of AND logic A3 is also applied to the input of a pulser P2 that is similar to pulser P1. This causes the pulser to put out a negative pulse from its long pulse output LP. This negative pulse may consist of the voltage dropping from +10 volts to +5 volts for a duration of 1 millisecond. With +10 volts on terminal S of the shift register, this negative pulse at terminal F causes the shift register to perform a set-in operation whereby an output of +10 volts appears at its first output T. If an input is present at terminal S during this pulse, this output is inverted in NOT logic N4 to change the voltage on the first input of AND logic A2 from +10 volts to 0 volts thereby to release the lockup of logics OR1 and A2 since the information indicating that the reject gate is to be opened is now in the shift register.

The +10 volts output of AND logic A3 is also applied to the second input of AND logic circuit A7. Since the third input of this AND logic is connected to the +10 volt supply, this AND logic is now gated for receiving normal frequency pulses from binary coded decimal counter BCD and passing these pulses to input terminal U of the first unit of countup counter CUC. At this same time, ten times normal frequency pulses will be gated to the countdown counter as hereinafter described.

In order to gate pulses to the countdown counter, timer operation is initiated. For this purpose, the +10 volts output of AND logic A3 is also applied through conductor 10 to the third input of AND logic circuit A8 and to the input terminal of timer TM. This timer is of the type that times after energization and its time interval is adjusted by resistor R1 connected in series with resistor R2 between its terminals on the input side. The output of this timer remains at 0 volts from the time of application of its input signal for its time interval and then changes to +10 volts as indicated in FIG. 2. By inverting the output of the timer in NOT logic circuit N7, there is provided a signal that remains at +10 volts for the timed interval and this signal is applied to the second input of AND logic A8. These two inputs gate AND logic A8 so that it will pass pulses for the delay time. Since these pulses are received at ten times the normal frequency to afford fast computing, the time of timer TM is set at one-tenth the actual delay time.

The pulses are produced at a frequency proportional to inspection conveyor speed. For this purpose, rotopulser RP is mechanically coupled to the inspection conveyor as indicated by broken lines in FIGS. 1 and 2. These pulses are applied to trigger unit TU. This trigger unit is of known type and the details have not been shown to avoid complicating the drawings. A suitable one is the Louis Allis Co. Type 80TB. This trigger unit is energized from an a.c. voltage source and provides 6 volt negative output pulses. These pulses are put through an OR logic circuit OR4 as a pulse conditioner to provide negative pulses that change from +10 volts to 0 volts. These pulses are then applied to the first input of AND logic A8 and passed therethrough for the duration of the aforementioned timed interval. Between pulses AND logic A8 turns on to provide a +10 volt output. Each negative pulse turns AND logic A8 off to provide a negative pulse to input terminal U of the first unit of countdown counter CDC. The positive-going trailing end this negative pulse registers a digit in the counter.

This is a countdown counter when considered together with the NOT logic circuits connected to its 8 outputs. When this

6

counter is reset, all of its outputs are at 0 voltage but due to inversion the outputs of the NOT logics are at +10 volts that is equivalent to a full count presented to the eight left terminals of coincidence circuit CIC. From this full count that is 255 for an 8-bit counter, the counter counts down as input pulses are received.

These pulses coming from the rotopulser are put into the countdown counter at a high frequency of 60 pulses per inch of conveyor travel during the compute period to establish the delay distance DL as shown in FIG. 1. On the other hand, the pulses going to the countup counter are at a frequency of 6 pulses per inch or a 10 to 1 ratio with the compute pulses. This high frequency is used so that the compute time, timer TM timing interval, consumes only a small part of the time during which the sheet travels from inductoswitch IS to the reject gate. This avoids having to put the inductoswitch far upstream and allows a greater range of speed adjustment of the inspection conveyor.

Also, the compute time is made fast at 10 times normal frequency to limit DT to less than 54 inches. If DT is greater than 54 inches, more than one sheet (up to 40 inches long with a 14 inch spacing between sheets) could be in the control zone requiring circuitry to track the sheets. DT is set at 42.5 inches because it is less than 54 inches and is easily adapted to a binary counting scheme of an 8-bit counter, that is a 255 total count pulses of an 8-bit counter divided by 6 pulses per inch is 42.5 inches.

The 60 pulses per inch are also applied from OR logic OR4 to input U of a frequency divider that conveniently takes the form of a binary coded decimal counter BCD. This counter is like one of the 4-bit binary units of countdown counter CDC or countup counter CUC except that is is internally wired to reset on the 10th pulse rather than on the 16th pulse as in the case of normal binary counting. Binary counters of this type altered for binary coded decimal counting are well known and the details have not been shown to avoid complicating the drawing. A suitable counter unit for use herein is the Cutler-Hammer DSL FOUR BIT BINARY COUNTER, BOARD NO. 16.

It will be apparent that for 10 to 1 frequency division purposes, it is only necessary to take the output from the fourth output terminal C that provides one pulse for each set of 10 successive input pulses to counter BCD. This output pulse from counter BCD is a positive pulse, terminal C going from 0 to +10 volts in response to the 8th input pulse and going back to 0 volts when reset in response to the 10th input pulse. The positive going leading edge of this output pulse is gated through AND logic A7 to register a digit in countup counter CUC.

Countup counter CUC is a binary counter consisting of two 4-bit binary units cascaded like counter CDC to provide an 8-bit binary counter capable of counting up to 255. It will countup from 0 toward 255.

It will be apparent from the foregoing that both counters start counting at the same time upon the sheet detecting inductoswitch sensing the leading edge of a sheet and gating AND logics A7 and A8. Counter CDC counts at 10 times the rate of counter CUC so that the lead distance count can be put therein quickly. When timer TM times out, its output goes to +10 volts that is inverted in NOT logic N7 to 0 volts that is applied to the 2nd input of AND logic A8. This shuts off AND logic A8 so that no further pulses reach counter CDC.

However, counter CUC continues counting at normal rate until coincidence occurs. The countdown counter output is applied from NOT logics N8-15 to the left inputs U, R, N, L, J, F, D and B of the coincidence circuit. At the same time, the countup counter output is applied to the right inputs V, S, P, M, K, H, E and C of the coincidence circuit. When the up count reaches the value of the registered down count, which occurs when the leading edge of the sheet reaches the START CONTROL point in FIG. 1, output T of the coincidence circuit goes from +10 volts to 0 volts.

This is the signal that starts the reject gate opening operation that is completed when the leading edge of the sheet reaches the CONTROL POINT in FIG. 1. This 0 voltage signal is no inverted in NOT logic N6 and applied through conductor 12 to NOT logic N5 and to the input of pulser P1. NOT logic N5 applies 0 volts to the first input of AND logic A3 to shut it off. This causes release of the lockup between logics OR3 and A3.

This +10 volts input to pulser P1 causes operation thereof to apply a long negative pulse of 1 millisecond or the like from its long pulse output LP to "shift" input L of shift register SR. This will cause the shift register output of +10 volts to appear at its second output P, it being recalled that a prior set-in operation brought about the output at terminal T. Immediately following the long pulse, pulser P1 applies a short negative pulse of 5 microseconds or the like from its short pulse output SP to "step" input R of the shift register to restore its first output T to 0 volts.

This shifting action causes energization of the reject gate solenoid RGO. For this purpose, the +10 volts from the shift register is applied to the second input of power AND unit PA1. This unit receives +10 volts at its first input from a supply. The third input of the power AND unit receives +10 volts if three conditions exist at AND logic A5, that is, contact RGSS is closed to indicate that the reject gate solenoid supply has been turned on, power has been turned on a sufficient time before so that capacitor C1 is fully charged, and the reset button has been depressed to reset the system and lock up logics OR2 and A5.

Under these conditions, power AND unit PA1 provides a +10 volts output that is amplified in an SCR output amplifier AMP that in turn energizes reject gate solenoid RGO to open the gate.

The shifting of the output of the shift register causes the 0 volts at output T to be inverted in NOT logic N4 to apply +10 volts to the first input of AND logic A2. This conditions this AND logic for further use.

The reject gate is reclosed in response to detection of the leading edge of the first sheet that is not to be rejected. It will be apparent that when the first sheet that is not to be rejected is detected, the system operates as before except that a set-in operation of shift register SR is not performed since pushbutton OG has not been pressed. Although pulser P2 puts out a set-in pulse, it has no effect on the shift register because its terminal S is at 0 volts rather than at +10 volts as is required for set-in. However, when coincidence in the counts occurs, pulser P1 operates to shift the output of the shift register from output P to output K. As a result, the reject gate solenoid is deenergized to cause reclosing of the reject gate just ahead of the leading edge of the sheet.

This controlled closing of the gate within the space between the sheets avoids scratching of the last rejected sheet by too soon a closure. Also, opening the gate just ahead of the leading edge of the sheet to be rejected and within the space between sheets avoids scratching the trailing end portion of the last sheet going thereover.

The shift register now has an output on unconnected output K but it can have no effect. This output is eliminated the next time that pulser P1 performs a shift operation wherein the short pulse restores all the outputs to 0 volts except the one that is shifted and held by the long pulse.

The countdown and countup counters are reset when the trailing end of the sheet that is being rejected passes the inductoswitch. This causes reopening of the inductoswitch contacts to change the +10 volts on the second input of AND logic A4 to 0 volts. As a result, a like reduction in voltage is applied from the AND logic to reset terminals M of the four 4-bit binary units to reset them to 0. This causes all the outputs of counter CUC to go to 0 voltage and causes all the outputs of NOT logics N8-15 to go to +10 volts.

FIGS. 3, 4 and 5 show a lead distance compensation system for deenergizing magnets and a magnet sequencing system for reenergizing these magnets in a timed sequence. Its purpose is

to detect a sheet as it arrives on a carryover conveyor and to drop the sheet accurately at a predetermined point when its trailing edge passes a particular magnet row of a top lapping conveyor. This system also controls reenergization of the top lapping conveyor magnets in such a way that minimum spacing is required between sheets. This is done by reenergizing each successive group of magnets immediately after the trailing edge has passed beyond its influence.

As shown in FIG. 3, the sheets are arranged to arrive along a carryover conveyor to a control point defined by a top lapping conveyor and a bottom lapping conveyor. A sensor switch such as an inductoswitch IS is positioned over the carryover conveyor a predetermined distance ahead of the control point to detect the arrival of a sheet as in FIG. 1.

The carryover conveyor terminates adjacent the entry ends of a top lapping conveyor and a bottom lapping conveyor. The top lapping conveyor slightly overlaps the exit end of the carryover conveyor and is provided with a plurality of rows of electromagnets, 17 rows being shown, for picking up the sheet and carrying it over the bottom lapping conveyor onto which the sheet is dropped tail first as hereinafter described. The bottom lapping conveyor is below the top lapping conveyor and also slightly below the level of the carryover conveyor for receiving the sheets in overlapped relation as they are dropped as shown in FIG. 3.

A rotopulser RP is driven by the top lapping conveyor for developing electrical pulses for controlling the system of FIG. 5. Total distance DT, lead distance DL, and the difference DT-DL are similar to those in FIG. 1.

The system in FIG. 5 is partly similar to the system of FIG. 2 and like reference characters have been used for those elements that are alike in the two systems. Also, those portions that are alike will be described generally, whereas a more detailed description will be given of the remaining parts that differ or that are additional to FIG. 2.

The purpose of this system is to pickup magnetically the leading edge of the sheet as it comes along the carryover conveyor, to drop the sheet accurately tail end first when its trailing edge reaches the first row of controlled magnets (row 3), and to reenergize pairs of magnet rows in sequence as the trailing edge passes beyond their influence.

This is done by detecting the trailing edge of the sheet to put a delay time count into a countdown counter at 10 times normal frequency (60 pulses per inch) and at the same time to start putting normal frequency pulses (6 pulses per inch) into a countup counter, and upon coincidence resetting a shift register to deenergize all except the first two rows of magnets. This will cause the trailing edge to start falling when it reaches the third row of magnets, rows 3—8 being fast acting and the remaining rows being slow acting.

For reenergization, the countup counter continues counting after coincidence and reaches count out when the trailing edge reaches the third row of magnets. This count out starts gating pulses into an additional counter made up of divide by 9 and divide by 8 counters to provide 1 pulse per foot for controlling the shift register to reenergize pairs of rows of magnets in sequence. To allow the trailing edge to pass three inches beyond the third row before rows 3—4 are reenergized, the divide by 8 counter is preset to a count of two and the output is taken from the third bit output of the 4-bit counter.

As in the case of the system of FIG. 2, this magnet control system of FIG. 5 must initially be reset so that the logic units are in the proper position for operation. Thereafter, the system resets itself automatically preparatory to each operation thereof.

For this purpose, there are provided a pair of pushbutton switches, a master reset switch MR and a magnet control reset switch MCR. These switches are in parallel so that either one may be used to reset the system. Each of these switches, when closed momentarily, connects an AC voltage to an associated signal converter SC6 or SC7. As a result, the associated signal converter applies +10 volts to one of the two inputs of an OR logic circuit OR5. This OR logic applies +10 volts to conduc-

tor 14, to the input of NOT logic circuit N16 and to an input of OR logic circuit OR6.

This OR logic OR6 and the following AND logic circuit A9 form a lockup pair. In response to its input +10 volts, logic OR6 applies +10 volts to the second input of AND logic A9. The first and third inputs of AND logic A9 receives +10 volts if three conditions exist to operate AND logic A10. One of these conditions is that the lapping mode of operation must have been selected so that lapping mode selector relay contact LMSR is closed. This contact connects a.c. voltage to signal converter SC8 which applies +10 volts to the first input of AND logic circuit A10. Another of these conditions is that the magnets power supply must have been turned on to close magnet power supply relay contact MPS, This contact similarly connects a.c. voltage to signal converter SC9 which applies +10 volts to the second input of AND logic A10. The third of these conditions is that the system power must have been on a long enough time for disturbances to settle down to steady state condition. This time is determined by capacitor C1 being fully charged to apply 0 voltage to the input of NOT logic circuit N17. As a result, this logic applies +10 volts to the third input of AND logic A10.

In view of the three inputs thereto, AND logic A10 applies +10 volts to the first and third inputs of AND logic A9. This causes the latter to apply +10 volts to the second and third inputs of AND logic A11 and to the first and third inputs of AND logic A12. Since the first input of AND logic A11 receives +10 volts from a supply, it operates to apply +10 volts to power AND logic PA2 at its second and third inputs. As the first input of this power And logic receives +10 volts from a supply, it operates to energize magnet control reset relay MCRR. This relay closes its contact to light lamp L to indicate that the system has been reset which occurs at the same time therewith as hereinafter described.

Since the second input of AND logic A12 receives +10 volts from a supply, this logic operates and applies +10 volts to the second and third inputs of power AND logic PA3. The first input of the latter being connected to the +10 volt supply, power AND logic PA3 operates to energize magnet group relay MG1 which closes its contact to energize rows 1 and 2 of the magnets. These two rows remain energized throughout the operation as will become apparent.

AND logic A9 also feeds back +10 volts to an input of logic OR6 to lock up these two logics thereby to maintain rows 1 and 2 of the magnets energized and to maintain indicator lamp L lit.

The aforementioned +10 volts on conductor 14 is applied to an input of OR logic OR7 at the lower portion of FIG. 5. This OR logic applies +10 volts to the second input of AND logic A13. The first and third inputs of the latter receive +10 volts from OR logic OR8 since both of its inputs are at +10 volts. This is due to the fact that the output T of coincidence circuit CIC is normally at +10 volts when there is lack of coincidence as now and the output of NOT logic N18 is at +10 volts, there being no output from AND logic A13. As a result, AND logic A13 operates to apply +10 volts back to an input of logic OR7 to lock up these two logics preparatory to drop out thereof upon coincidence occurring as hereinafter described.

This +10 volts is also applied from conductor 14 through logic N16 to the input of pulser P3. This causes a long negative pulse of 1 millisecond or the like to be applied from long pulse output LP to reset terminal M of a 9 pulse counter 9BC to reset this counter to 0 condition. This long negative pulse is also applied to an input of AND logic A14 to bring the output of the latter to 0 volts. This 0 volts is applied to reset terminal M of 8 pulse counter 8BC to reset it to 0 condition.

The aforementioned +10 volts input from conductor 14 to NOT logic N16 causes 0 volts to be applied from its output to conductor 16. This 0 voltage signal will drop out lockup pairs OR10-A15 and OR11-A16 in the event they were previously operated. This dropout of A16 causes resetting of counters CDC and CUC to their 0 output conditions by applying 0 volts to their terminals M.

AND logic A13 also applies +10 volts through conductor 18 to the third input of AND logic A15 to prepare the latter for operation when a sheet id detected. This +10 volts of AND logic A13 is inverted in NOt logic N18 and 0 volts is applied through conductor 20 to an input of OR logic OR8, to an input of OR logic OR11 and to an input of OR logic OR9 to prepare these logics for operation when coincidence occurs.

When the reset switches MR and MCR reopen, conductor 14 returns to 0 volts.

The system of FIG. 5 is now ready for operation and will operate when a sheet is detected. The carryover conveyor of FIG. 3 runs and operates rotopulser RP. This rotopulser operates trigger unit TU to supply negative pulses to signal conditioning OR logic OR4. As a result, the latter applies +10 volt to 0 volt negative pulses to conductor 22. However, these pulses cannot get to either countdown counter CDC or countup counter CUC until a sheet is detected which will now be described.

When the leading edge of a sheet is sensed, the contact of inductoswitch IS closes to apply a.c. voltage to signal converter SC10. As a result, the latter applies +10 volts to the first and second inputs of AND logic A17 and to NOT logic N19. The latter applies 0 volts to the third input of AND logic A18 to hold this logic off presently. The output of NOT logic N19 is inverted in NOT logic N20 to apply +10 volts to the third input of AND logic A17.

This causes AND logic A17 to apply +10 volts output to logic OR10. As a result, the latter applies +10 volts to the second input of AND logic A15. Since the first input of the latter receives +10 volts from conductor 16 and the third input thereof receives +10 volts from conductor 18, AND logic A15 feeds back +10 volts to an input of logic OR10 to lock up these two logics.

AND logic A15 also applies +10 volts over conductor 24 to third inputs of power AND units PA4, PA5, PA6 and PA7 to prepare these units for operation by shift register SR. It will be seen that AND logic A11 that applies +10 volts to power AND unit PA2 at the upper right portion of FIG. 5 also applies +10 volts to the first inputs of power AND units PA4, PA5, PA6 and PA7. Thus, these power AND units are in readiness for operation by the shift register as hereinafter described.

The system now remains in this condition with logic N19 holding logic A18 ungated until the trailing edge of the sheet passes inductoswitch IS. At such time, the contact of the inductoswitch reopens to change the output of logic N19 from 0 to +10 volts and to apply it to the third input of logic A18. This starts the counting action to measure the lead distance.

For this purpose, the +10 volts output of logic A18 is applied to an input of OR logic OR11 that consequently provides a +10 volts output to the second input of logic A16. The first input of AND logic A16 receives +10 volts from conductor 16 as aforesaid. The third input of logic A16 receives +10 volts from NOT logic N21 through conductor 26. For this purpose, when the output of logic OR7 goes to +10 volts during the resetting operation, the output of logic N21 is momentarily held at 0 volts to prevent inadvertent initiation of counting in counter CDC. As capacitor C3 charges, the output of logic N21 goes to +10 volts that is applied through conductor 26 to logic A16.

Logic A16 now has +10 volts on all three inputs and applies an output of +10 volts as a feedback to an input of logic OR11 to lock up these two logics. Logic A16 also applies +10 volts to conductor 28 and therethrough to the input of timer TM. As described in connection with FIG. 2, timer TM whose time interval is set proportional to the magnet delay time by resistors R1 and R2 maintains its output at 0 volts for its time interval and then changes it to +10 volts. At the beginning of the time interval, the +10 volts is also applied from conductor 28 to the third input of AND logic A8. The 0 voltage of timer TM is inverted in NOT logic N7 to apply +10 volts to be the second input of AND logic A8. This gates AND logic A8 so that it sill pass pulses for the delay time from conductor 22 to counter CDC as described in connection with FIG. 2. The

final count of this counter is then applied through logics N8-15 to the left terminals of coincidence circuit CIC. This count that is equal to the delay time required for the magnets to deenergize is put into the countdown counter rapidly at 10 times the frequency of the pulses going into the countup counter which will now be described.

The trigger unit pulses after being reformed in logic OR4 are also applied to a frequency divider such as binary coded decimal counter BCD which operates to provide 1 +10 volts pulse at its 8th pulse output C for each ten input pulses thereto as hereinbefore described in connection with FIG. 2. These pulses are gated through a two-input AND logic circuit A19 by the output of logic A16 and go to input U of the first 4-bit binary unit of countup counter CUC.

When the countup count reaches the countdown count at the START CONTROL point in FIG. 3, coincidence circuit CIC in FIG. 5 operates to change its output from +10 volts to 0 volts. This 0 volts signal is applied through logic OR8 to logic A13 to drop out this logic and its preceding logic OR7 that were locked up as hereinbefore described.

As a result, the voltage on conductor 20 changes from 0 volts to +10 volts which is a magnet dropout signal. This signal is applied from conductor 20 through logic OR9 to the clear input CL of pulser P4. This causes a short negative pulse of five microseconds or the like to be applied from its short pulse output SP to reset terminal R of shift register SR to reset all output terminals T, P, K, E and C of the latter to 0 condition. This causes power AND units PA4, PA5, PA6 and PA7 to deenergize magnet relays MG1 through MG4 to open their contacts and deenergize rows 3—4, 5—6, 7—8 and 9—N of magnets schematically shown in FIG. 4b. Rows 1—2 of the magnets remain energized as depicted in FIG. 4c. The manner in which rows 3—N of the magnets are energized will be described later.

Since it takes a delay time equal to lead distance DL for the magnets to actually lose their magnetism, the trailing end of the sheet will break free from the top lapping conveyor as its trailing edge reaches the third row of magnets as shown in 4d. As depicted in FIG. 4c by the relative heights of the magnets, rows 3—4, 5—6 and 7—8 are fast deenergizing magnets and the rest of the rows 9—N are slow deenergizing as shown by curves in FIG. 4a. Therefore, when the trailing edge arrives at the third row, the flux in rows 3—8 will have decreased below the level needed to hold the sheet and its tail end will start to fall from the top lapping conveyor as shown in FIG. 4d. The leading end of the sheet will still be held by the remaining flux in the slow magnets. Soon thereafter the flux in the slow magnets will decay to a level below what is required to hold the sheet and the leading end will also drop as shown in FIGS. 4e, f and g. This prevents the leading end from nose-diving or floating into the pile below. with metal sheets, nose-diving might cause the falling sheet to scratch the sheet below it. Floating might cause the sheet to bang into the end stop causing damage to the sheet or the end stop that is used to aline the sheets into a pile.

The rows of magnets are reenergized in sequence as soon as the trailing edge has passed to prepare them for the next sheet, shown in FIGS. 4d—g, and to avoid having to provide large spaces between sheets. As soon as the trailing edge passes a few inches beyond the pole faces of the third row of magnets, the third and fourth rows are reenergized. This is permissible because the south poles in the fourth row as shown in FIG. 4b cannot attract the sheet when the sheet does not complete the magnetic circuit to the north poles in row 3.

The +10 volts on conductor 20 is also applied to logic OR11 to inhibit input pulses from going into counter 9BC while it is being reset. This is done by holding input terminal U of counter 9BC at +10 volts during this resetting time.

The +10 volts on conductor 20 is also applied through logic OR9 to the input of pulser P3. As a result, the pulser applies a negative pulse from its terminal LP to terminal M to reset counter 9BC to 0 and through logic A14 to terminal M to reset counter 8BC to 0. This pulser pulse functions to turn logic

A14 off for counter 8BC resetting purposes on every count except count 8. On count 8, counter 8BC resets itself by applying +10 volts from its output C that is inverted in NOT logic N22 to 0 volts. This 0 volts turns logic A14 off to reset counter 8BC.

The signal that caused magnet dropout is also applied from the output of logic OR9 through isolating AND-OR logic A0 to terminal P of 8-pulse counter 8BC. AND-OR logics of this type are well known and the details have not been shown to avoid complicating the drawing. A suitable one for use herein is the Cutler-Hammer DSL AND-OR BOARD NO. 37. This +10 volts on output P of counter 8BC presets this counter to a count of 2. This two pulse preset is equal to 2 out of 8 pulses or 3 inches out of 12 inches.

To explain the purpose of presetting counter 8BC to a count of 2, it is to allow the trailing edge of the sheet to travel 3 inches further before rows 3—4 of the magnets are reenergized. This is done to insure that the dropping sheet is not interferred with by the reenergization. As will be apparent, the 60 pulses per inch of the rotopulser is divided by 10 in counter BCD to provide 6 pulses per inch for the countup counter CUC. This frequency of 6 pulses per inch is divided by 9 in counter 9BC to obtain 8 pulses per foot which is divided by 8 in counter 8BC to get 1 pulse per foot for reenergizing the magnet groups at 1 foot intervals with a 3 inch delay on the first one as hereinafter described.

The signal that caused magnet dropout is also applied from conductor 20 to logic OR8 which applies +10 volts to the first and third inputs of logic A13 to prepare the latter for operation when final coincidence circuit FC operates as hereinafter described.

Following magnet dropout as hereinbefore described, countup counter CUC continues counting until it reaches its full count of 255. This full count is applied to the left terminals of final coincidence circuit FC whereas its right terminals are connected to +10 volts. At this full count, coincidence occurs and the trailing edge of the sheet is directly below the third row of magnets.

At this time it is desirable to allow the sheet to travel 3 inches to the position of FIG. 4d before starting to reenergize rows 3 and 4 of the magnets to avoid affecting the dropping of the sheet. After the 3 inch delay, rows 3 and 4 are reenergized, rows 5—6 and 7—N are reenergized in succession at 1 foot intervals of sheet travel as shown in FIGS. 4e and 4f. This 3 inch delay is obtained by presetting counter 8BC to a count of 2 whereas its output is taken from count 4 output terminal K that goes to +10 volts once for 8 input pulses. This means that counter 8BC will provide an output pulse at terminal K after receiving 2 pulses which when added to the preset of 2, totals 4. There is then a 2 pulse delay out of counter 8BC. Since this is an 8 pulse counter, 2 out of 8 pulses for a foot of travel equals 3 inches. Thus, the sheet travels 3 inches beyond the third row of magnets before counter 8BC puts out the first pulse.

The coincidence condition causes the output at terminal T of circuit FC to go from +10 volts to 0. This signal is inverted in NOT logic N23 to apply +10 volts to an input of logic OR7, the other inputs of the latter being at 0 volts. This causes logic OR7 to apply +10 volts to the second input of logic A13 causing its output to change from 0 to +10 volts. Logics A13 and OR7 lock up through the feedback as before. The output of logic A13 is inverted in logic N18 to 0 volts to terminate the inhibiting signal that was being applied from conductor 20 to logic OR11. As a result, count pulses now can flow from output terminal B of counter BCD through logic OR11 to input U of counter 9BC.

This nine pulse binary counter 9BC to count 9 pulses. For this purpose, the first 8 pulses are counted in direct binary fashion resulting in a +10 volts output at terminal C. This voltage is fed back to an input of logic OR11 as in inhibit signal that is applied to its input U to prevent the ninth pulse from being registered. The 9 ninth pulse will be applied directly to input E causing the fourth stage of counter 9BC to reset to

change the output at terminal C to 0 volts and to change the output at terminal B to +10 volts. Thus, the counter becomes reset on the ninth input pulse and provides one output pulse from output B to input U of counter 8BC.

Upon receiving input pulses, counter 8BC being preset at 5 count two, provides a +10 volts output at terminal K initially on the second input pulse and thereafter on the tenth pulse, eighteenth pulse, etc. This +10 volts is applied to the input of pulser P4. As a result, pulser P4 provides a long negative pulse from output LP followed by a short negative pulse from ter- 10 minal SP to terminals L and R, respectively, of the shift register. Since serial input terminal U of this shift register is connected to +10 volts supply, the input pulse to its terminal L causes an output of +10 volts at output T. This voltage is applied to power AND unit PA4 to energize relay MG1. This 15 relay closes its contact to reenergize rows 3—4 of the magnets.

In this manner, as each additional pulse is applied to the shift register, it provides additional +10 volt outputs at P and 20 K in sequence to energize succeeding pairs of rows of magnets, rows 5—6 from shift register output P and rows 7–N from output K. As shown in FIG. 4a, rows 7—8 of magnets are fast acting while rows 9—N are slower acting. The +10 volts at terminal U prevents preceding outputs T and P from resetting 25 to 0.

Each time that counter 8BC reaches a count of 8, it is automatically reset to 0. At the count of 8, +10 volts appears at output C which is inverted to 0 volts by NOT logic N22 and applied to AND logic A14. The latter applies 0 volts to reset 30 terminal M to reset counter 8BC to 0. It then starts counting again. Plus 10 volts appears only once at its output K during each 8 pulse count to divide the frequency as hereinbefore described.

While the frequency of the pulses going into the countdown 35 counter has been disclosed as being 10 times the normal frequency of the pulses going into the countup counter, it will be apparent that some other ratio may be used either smaller or larger than the 10 to 1 ratio. This would require a different ratio frequency divider in place of binary-coded decimal 40 counter BCD in FIGS. 2 and 5. Also, reenergization of the magnets in FIG. 5 could be arranged to take place at other than the 1 foot intervals disclosed by changing the frequency division ratio of counters 9BC and 8BC. Furthermore, while the reject gate in FIG. 2 is reclosed in response to detection of 45 the leading edge of the next sheet, it will be apparent that a trailing edge detector as shown in FIG. 5 could be used for this purpose with proper adjustment of the delay distance.

While the apparatus hereinbefore described is effectively adapted to fulfill the objects stated, it is to be understood that 50 the invention is not intended to be restricted to the particular preferred embodiments of lead distance compensation and magnet sequencing control systems for article conveyors disclosed, inasmuch as they are susceptible of various modifica- 55 tions without departing from the scope of the appended claims.

We claim:

1. An article conveyor system comprising:
   means for performing a controlled function on an article at 60
   a fixed control point along the conveyor, which means inherently requires a substantially fixed time interval to reach a proper operating condition prior to arrival of the article thereat, this fixed time interval being equivalent to a variable lead distance from said control point back to a 65 start control point that is proportional to conveyor speed; and
   lead distance compensation means for adjusting automatically the lead distance when the conveyor speed changes to enable the controlled function performing means to 70 reach its proper operating condition when the article reaches the control point regardless of variation in conveyor speed comprising:
   an article detector ahead of the start control point;
   a pulse generator driven by the conveyor; 75

a countdown counter capable of counting a fixed number of pulses indicative of the lead distance and a countup counter capable of counting a fixed number of pulses indicative of the distance traveled beyond the sheet detector;
means for gating pulses from said pulse generator into one of said counters at a normal frequency when the article detector detects an oncoming article as a measure of article movement from said detector to said start control point;
means comprising a timer for gating pulses from said pulse generator into the other of said counters at a high frequency when the article detector detects an oncoming article for a time interval sufficient to accumulate a count determinative of the required lead distance for the corresponding speed of the conveyor;
means operable when an article is approaching said detector for making a selection of that article for a controlled function to be performed thereon; and
means operable when the counts in the two counters reach coincidence and the selected article is at the start control point for initiating operation of said controlled function performing means.

2. The invention defined in claim 1, wherein said means for initiating operation of the controlled function performing means comprises:
   a coincidence circuit; and
   means responsive to operation of said coincidence circuit when the normal frequency count reaches the value of the accumulated high frequency count if said selection has not been made for the next sheet for restoring the control function performing means by the time such next article reaches the control point.

3. The invention defined in claim 1, wherein the article is a sheet and said article detector comprises: means for detecting the leading edge of the sheet.

4. The invention defined in claim 1, wherein the article is a sheet and said article detector comprises: means for detecting the trailing edge of the sheet.

5. The invention defined in claim 1, wherein said means for performing a control function comprises:
   a reject gate; and
   means for opening said gate to divert said article to a reject conveyor.

6. A sheet conveyor system comprising:
   means for performing a directive function on a sheet at a fixed control point as it is being moved by the conveyor system which means inherently requires a fixed time interval after initiation of operation to reach a proper operating condition prior to arrival of the sheet at said control point, this fixed time interval being equivalent to a variable lead distance from said control point back to a start control point that is proportional to conveyor speed; and
   lead distance compensation means for adjusting automatically said lead distance when the conveyor speed changes to enable the directive function performing means to reach its proper operating condition when the sheet reaches the control point regardless of variation in conveyor speed comprising:
   a sheet detector ahead of the start control point and means controlled thereby;
   a pulse generator driven by the conveyor for generating high frequency pulses;
   a countup counter capable of counting a fixed number of pulses indicative of the distance traveled beyond the sheet detector and a countdown counter capable of counting a fixed number of pulses indicative of the lead distance;
   means responsive to said sheet detector controlled means for gating pulses from said pulse generator into one of said counters at a normal frequency that is substantially less than said high frequency when the sheet detector

detects an oncoming sheet as a measure of article movement from said detector to said start control point;

means comprising a timer responsive to said sheet detector controlled means for gating pulses from said pulse generator into the other of said counters at said high frequency when the sheet detector detects an oncoming sheet for a time interval sufficient to accumulate a count determinative of the required lead distance for the corresponding speed of the conveyor; and

means operable when the counts in the two counters reach coincidence and the sheet is at said start control point for initiating operation of said directive function performing means.

7. The invention defined in claim 6, together with:

means operable when a sheet is approaching said detector for making a selection of that sheet for a directive function to be performed thereon;

said means for initiating operation of said directive function performing means; and comprises: means operable when such selection has been made and said counts reach coincidence for initiating such operation.

8. The invention defined in claim 6, wherein said sheet detector controlled means comprises:

means for detecting the leading edge of a sheet;

said means for performing a directive function sheet; and

a reject gate; and

means for opening said reject gate to divert the sheet off the conveyor.

9. The invention defined in claim 6, wherein said sheet detector controlled means comprises:

means for detecting the trailing edge of a sheet; and

said means for performing a directive function comprises:

groups of controllable magnets that hold the sheet to a top lapping conveyor in its forward movement; and

means for deenergizing said groups of magnets to drop the sheet.

10. The invention defined in claim 9, together with:

a third counter for performing a predetermined frequency division;

means responsive to said normal frequency counter reaching its full count for gating said normal frequency pulses into said third counter; and

means responsive to predetermined output pulses from said third counter for reenergizing said groups of magnets in sequence whereby each group of magnets is reenergized after the trailing edge of the dropped sheet has passed thereby to prepare the magnets for the next sheet.

11. The invention defined in claim 10, wherein said means responsive to predetermined output pulses from said third counter comprises:

a shift register having a plurality of output terminals; and

means responsive to successive pulses from said third counter for energizing said output terminals in progression thereby to reenergize said groups of magnets in sequence and to maintain them energized.