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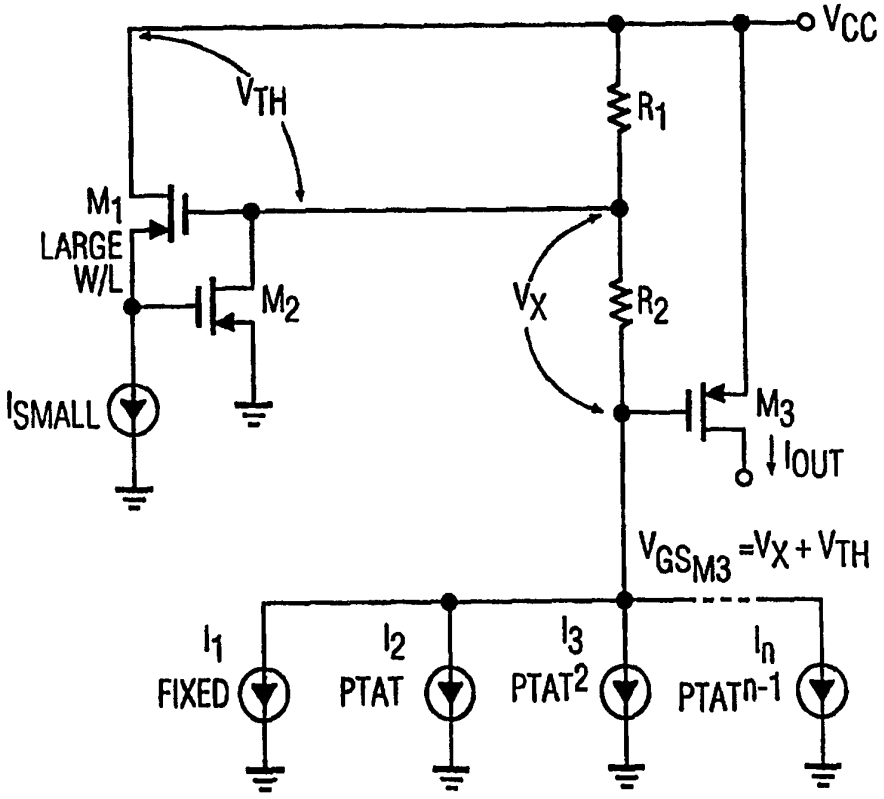
(54) Title: A REFERENCE CIRCUIT HAVING A CONTROLLED TEMPERATURE DEPENDENCE

(57) Abstract

Mobility in a FET is used as a time standard to develop a resistance (or a transconductance or a current) reference which may be fully integrated and which is temperature stable to an arbitrary desired accuracy (or which varies with temperature in a desired fashion). The large temperature dependence of mobility is compensated (or adjusted to a desired variation characteristic) by applying a gate bias voltage having a predetermined variation in value with respect to temperature. In one embodiment the bias voltage of the FET is given a temperature dependence which results in the drain current of the FET being substantially constant with respect to temperature. This current is then used to charge or discharge a capacitor, yielding a precise R-C product which may be implemented fully in integrated form.



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A reference circuit having a controlled temperature dependence.

This invention generally relates to circuits for producing reference voltages and reference currents, and to time reference circuits which use reference voltages and/or currents to create the time reference, such as oscillators, filters, time delay circuits and clocks, and more specifically relates to a reference circuit which is completely formed as an integrated circuit (i.e., having no external components) and which has either a controlled temperature dependence or substantially no dependence on temperature.

In U.S. Patent 4,843,265, a temperature and processing compensated time delay circuit is described which can be fabricated in a monolithic integrated circuit. This circuit is shown in Figure 1. A bias voltage connected to the gate of a field effect transistor (FET) M_{12} is deliberately designed to have a non-linear variation with temperature which substantially matches and compensates for the variation in temperature exhibited by the mobility of the FET, so as to make the drain current of the FET have a value which is not very much dependent upon temperature. The drain current of the FET is then used to discharge a capacitor (not shown) to provide a time constant. This approach promises to achieve the high accuracy desired, but the disclosed circuit implementation still has a number of disadvantages.

The gate bias voltage is given a temperature dependence in this circuit by subtracting three negative temperature coefficient base-emitter voltages ($3V_{be}$), generated by bipolar transistors Q_1, Q_2 and Q_3, from a scaled and temperature-invariant bandgap reference voltage (V_{BG}). The threshold voltage in FET M_{12} is cancelled by level-shifting the gate bias voltage up with another FET M_{54}. Buffers are used to scale the bandgap reference and to provide a low impedance drive for the current source transistor M_{12}.

This circuit has the disadvantage that the negative temperature coefficient term cannot be arbitrarily scaled. The coefficient of 3 can be reduced to 2 or increased to 4 by deleting or adding a bipolar transistor to substract or add a base-emitter voltage (V_{be}), but coefficients in between cannot be selected. This either makes the compensation only approximate (i.e., still leaves a significant temperature variation) or else constrains the drain current of FET M_{12} to a single predetermined value that corresponds to the number of V_{be}

voltages subtracted by the circuit.

Another disadvantage stems from the fact that the circuit does not assure that FET M_{54} will have its source at the same potential as the source of FET M_{12}. If the two sources are not at the same potential, the threshold voltages of the two FETs are not the same and there will not be exact cancellation of the threshold voltage in FET M_{12}! The Figure 1 circuit also is unduly complex since an operational amplifier A_1 is needed to scale up V_{BG} and another operational amplifier A_2 is needed to match impedances.

Still another disadvantage is that the Figure 1 circuit has no way of more accurately matching the temperature variation characteristic of mobility than by the $3V_{be}$ term. This term does not provide an exact match. Furthermore, the circuit is strictly designed for temperature compensating the drain current of an FET connected so as to discharge a capacitor. While this automatically temperature compensates the time delay produced by the capacitor being discharged, there are many other circuit configurations where the time constant will not be temperature compensated properly by the bias voltage dependence on temperature that is created by the Figure 1 circuit.

One example of a circuit where a different temperature dependence is needed for the bias voltage is in a current source reference or a time reference that uses a current for the reference, such as a transconductance type filter. In this case, the drain current of the FET that needs to be temperature compensated is not proportional to the bias voltage, as is assumed in the Figure 1 circuit, but instead is proportional to the bias voltage squared. An entirely different temperature dependence is needed for the bias voltage in such a circuit if the time constant is expected to be constant with respect to temperature variation.

There are also situations where it is desired to have a time reference value depend upon temperature, but where the temperature dependence characteristic of mobility in an FET is not the desired temperature dependence characteristic. It would be desirable to be able to arbitrarily tailor the temperature dependence of a time reference (or more generally the temperature dependence of a current source, or the temperature dependence of a bias voltage for an FET.

It is an object of this invention to provide an accurate time reference with an integrated circuit that requires no external components or connections other than usual supply voltages.

Another object is to provide a current reference circuit which may be fully integrated (i.e., not requiring any external component or timing signal) with a capacitor and

other integrated circuit components to produce an accurate time reference.

Still another object is to provide a current reference circuit which may be fabricated as a monolithic integrated circuit and which may provide a current which has an arbitrary predetermined variation in value with respect to temperature variation.

It is a further object to provide a current reference circuit which may be fabricated as a monolithic integrated circuit and which may provide a current of arbitrary value that does not vary with respect to temperature variation.

It is also an object to provide a bias voltage for an FET which may be fabricated fully in integrated form and which exhibits an arbitrary predetermined variation in value with respect to temperature variation.

Another object is to provide a circuit that may be fabricated entirely in integrated form and which provides an accurate transconductance of arbitrary value and which does not vary with respect to temperature variation.

These and further objects and features have been achieved by using mobility in an FET as a time standard to develop a resistance (or a transconductance or a current) which is temperature stable to an arbitrary desired accuracy (or which varies with temperature in a desired fashion). The large temperature dependence of mobility is compensated (or adjusted to a desired variation characteristic) by applying a gate bias voltage having a predetermined variation in value with respect to temperature.

In one embodiment the bias voltage of the FET is given a temperature dependence which results in the drain current of the FET being substantially constant with respect to temperature when it charges or discharges a capacitor, yielding a precise R-C product.

Figure 1 is a prior art circuit in which the drain current of an FET is stabilized with respect to temperature variation in order to produce a temperature stable time constant.

Figure 2 is a simple R-C filter circuit in which the resistance is implemented with an MOS FET having a gate bias voltage of $V_X + V_{TH}$.

Figure 3 shows a current source implemented by a MOS FET biased into saturation by a gate voltage $V_X + V_{TH}$.

Figure 4 shows the Figure 3 circuit in more detail and in which the gate voltage $V_X + V_{TH}$ is generated so as to make the output current temperature invariant.

Figure 5 is a circuit for use in experimentally determining proportionality factors for the PTAT sources in Figure 4.

Figure 6 is an example curve of V_X as a function of temperature determined using the circuit of Figure 5.

Figure 7 is a circuit which converts a bandgap voltage reference into a constant current reference using the present invention.

Figure 8 is a generalized bias circuit for providing $V_X + V_{TH}$ in accordance with this invention.

Figure 9 is a oneshot circuit that uses the Figure 8 circuit to bias an MOS FET for constant current operation that is invariant to temperature.

Figure 10 is a prior art Gm/C filter stage in which transconductance may be controlled by controlling the bias voltage of an FET current source using the present invention.

It is generally desirable for integrated circuits to be fabricated entirely in integrated form (i.e., without any external components or external time references being needed), because an external connection to a component or time reference is a potential source of noise injection or other board or package parasitic problems. The external connection and component also add considerable complexity and significant cost. There are some circuits, however, such as oscillators and filters, which are inherently difficult to fabricate entirely in integrated form, because they require an accurate time constant, and accurate time constants are not readily implemented entirely in integrated form.

Time constants are typically derived from an R-C, L-C or crystal resonator time reference. Crystal resonators cannot be fabricated in an integrated circuit, so use of a crystal resonator inherently involves an external component and connection. Inductors can be fabricated in integrated form, but only in small values as a practical matter, so the use of integrated L-C circuits is limited to high-frequency applications. Internal resistors and capacitors are easy to fabricate in integrated form, but they have inaccurate values with a resulting R-C time constant tolerance in the +/- 30-60% range.

Hybrid circuits have been used to improve on the inaccuracy of integrated R-C time constants. Using an external capacitor improves the tolerance by about 10% and makes big time constants possible, but this becomes unwieldy and expensive if multiple time constants are required. The external connection is also a disadvantage, as noted above, and the inaccuracy of integrated R-C time constants is due mostly to variation of the resistance value with processing and temperature. Since integrated capacitors are usually temperature stable, combining them with an external resistor can yield a time constant accuracy in the

range of 15%. It's also easy to use a single master resistor to achieve multiple time constants, but the external connection is still a significant disadvantage. A big jump in accuracy is achieved when trimmed internal resistors having a low temperature coefficient (TC) are used, but unfortunately this results in a big jump in process complexity and product cost.

Perhaps the most popular approach to timing accuracy at this time is to use an accurate external clock for driving switched capacitor circuits. Assuming the availability of such a clock, the system is made more complex by the presence of switching noise and the need for anti-alias and smoothing filters. Continuous-time filters can also be locked to an external clock, but this generally requires an additional phase locked loop (PLL) in the design. Both of these approaches also suffer from the disadvantage of requiring an external connection.

Many applications require an accuracy in timing variation in the range of 5% or better. Accordingly, there is a need for an integrated circuit design for producing a time constant having an accuracy of 5% or better without requiring any external component, clock, or trimming.

The embodiments shown use mobility in a MOS FET as a time reference. Mobility is sensitive to doping concentration and temperature. For native devices (low doping), mobility is insensitive to processing, and for typically implanted devices (eg., $1X10^{17}$ NMOS), 10% doping change causes only a 2.6% mobility shift. The units for mobility are cm-squared per volt-seconds. Since area is invariant and voltage can be controlled by design, the remaining parameter is seconds. Control of mobility is fairly tight with standard processing. For native devices, mobility is fairly independent of doping, so there is even less variability when the time (or current or voltage) reference is made in accordance with this invention using a native FET device.

Referring now to Figure 2, a simple single-pole, low-pass MOS FET filter is shown. Capacitance is equal to capacitor area A times C_{OX}, and the triode region resistance is equal to

$$\frac{1}{\mu C_{OX}(\frac{W}{L})(V_{GS}-V_{TH})}$$

where μ is mobility, C_{OX} is the oxide capacitance per unit area, W is the width of the

channel, L is the length of the channel, V_{GS} is the gate to source voltage, and V_{TH} is the threshold voltage. Therefore the R-C time constant is

$$RC=\frac{1}{\mu C_{OX}(\frac{W}{L})(V_{GS}-V_{TH})}AC_{OX}$$

whic

h reduces to

$$RC=\frac{A}{\mu(\frac{W}{L})(V_{GS}-V_{TH})}$$

If we bias V_{GS} with a voltage V_X plus V_{TH}, as shown in Figure 2, and substitute V_X + V_{TH} for V_{GS}, the time constant reduces further to

$$RC=\frac{A}{\mu(\frac{W}{L})V_X}$$

Capacitor area and W/L are well defined and temperature invariant. Mobility only varies a few percent in production, but it has a large temperature coefficient, typically varying with temperature to the -3/2 power. Overall temperature invariance may be achieved by designing V_X to have an amplitude that varies with temperature opposite to the temperature variation of μ, namely by giving V_X a temperature coefficient (tc) proportional to absolute temperature T to the +3/2 power. Scaling of the corner frequency may be done by changing capacitor area, device W/L, or the nominal value of V_X. Simple programming is also possible by using a single control voltage switched to the gates of different sized transistors connected in parallel. There are some disadvantages to this circuit architecture, however. Any DC voltage across the MOS FET device and/or body effect will make the on-resistance vary, so circuitry needs to be added to compensate.

A more practical reference may be built using a MOS FET device in saturation, as shown in Figure 3. Assuming saturation

$$I_{OUT}=\frac{\mu C_{OX}}{2}(\frac{W}{L})V_X^2$$

An

equivalent resistance may be defined as V_X divided by I_{OUT}.

$$R_{EQ}=\frac{V_X}{I_{OUT}}=\frac{2}{\mu C_{OX}\frac{W}{L}V_X}$$

The principle is the same. As with the previous case, constant resistance is achieved by having V_X vary with T to the 3/2 power. For constant current in the Figure 3 circuit without variation due to temperature change

$$\frac{dI}{dT}=(\frac{C_{OX}}{2})(\frac{W}{L})(\frac{d\mu}{dT}V_X^2+2\mu V_X\frac{dV_X}{dT})=0$$

This condition simplifies to

$$(\frac{1}{V_X})\frac{dV_X}{dT}=-(\frac{1}{2})(\frac{1}{\mu})\frac{d\mu}{dT}$$

Therefore, for constant current, V_X needs to vary with T to the 3/4 power, or half of the mobility drift. This current source furthermore is proportional to C_{OX}, and will therefore track timing capacitor variation. This reference can also be used in applications other than timing circuits if the tolerance due to C_{OX} variation is acceptable. The reference can also be scaled via programming to account for measured, non-nominal C_{OX}.

The circuit in Figure 3 thus requires a bias voltage V_X that has either approximately $T^{3/2}$ absolute temperature variation (for constant resistance) or else a temperature variation of approximately $T^{3/4}$ (for a constant current). Figure 4 is a generalized circuit representation illustrating functionally how a circuit may be implemented which produces either one of these bias voltages (or for that matter any other desired arbitrary bias voltage temperature dependence characteristic). In Figure 4, current sources I_1 through I_n are shown. Current source I_1 is a constant current source that does not vary with temperature. Current source I_2 is a current source that is proportional to absolute temperature (known as PTAT). Current source I_3 is a current source which is proportional to absolute temperature squared ($PTAT^2$). Current source I_n is a current source which is proportional to absolute temperature to the n-1 power ($PTAT^{n-1}$). As will become more apparent as this description proceeds, the value of n may vary from 2 upwards to whatever

number is required to produce a desired V_{GS} temperature characteristic of an arbitrary accuracy. In general, values of n between 2 and 4 should provide reasonable accuracy. Furthermore, one or more of the PTAT current sources in a series might have a value so low that a suitable circuit may be designed with acceptable accuracy without actually implementing one or more of the small PTAT terms in the series.

As will become more apparent in connection with later description of practical circuits, each of these current sources is actually implemented by creating a corresponding voltage source (V_1 for I_1; V_2 for I_2; etc.) having the right temperature characteristic (i.e., invariant for V_1; PTAT for V_2; $PTAT^2$ for I_3; $PTAT^3$ for I_4; etc.) and applying the voltage source across a resistance. The temperature characteristic of the resistances used to implement the current sources and the temperature characteristic of the R2 resistance are the same in the same integrated circuit. Therefore, each one of the voltage sources V_1 to V_n produces a voltage component contribution to the total voltage V_X that is equal to a resistor ratio times the value of the voltage source used to implement that current source. Since resistor ratios determine the coefficients of each component of V_X, temperature dependence of the resistances has no effect. If for each component portion of V_X, we let K_i be the amplitude and T^{i-1} be the temperature dependency, V_X becomes

$$V_X=\sum_{i=1}^{n} K_i T^{i-1}$$

which more closely resembles the form in which V_X is actually implemented in the preferred embodiments.

Still referring to Figure 4, the current-source PMOS, M_3, and the threshold-cancelling device, M_1, are operated with a common source-voltage for improved matching and elimination of body effect. No amplifiers are needed as well because M_2 provides feedback from the drain of M_1 to the gate of M_1, thereby providing a low-impedance output for V_{TH} and yielding a smaller, more-accurate circuit. A small current flows through large device M_1, forcing its V_{GS} to approximately its threshold value V_{TH}. The key design decision is determining the proper ratio of the various current sources I_1 to I_n (or more accurately the voltage sources V_1 to V_n that implement these current sources) to best match the mobility temperature drift of M_3.

Figure 5 shows a circuit that may be used to experimentally determine the right proportions for the current (or voltage) source terms. An opamp drives the gate of M1 to the

gate-source voltage necessary for a drain current equal to a desired fixed current load I. We assume here that we want to determine the V_X curve which makes I_{OUT} of M_3 (Figure 4) constant. I is selected to have the amplitude desired for I_{OUT}. If a temperature dependence is desired for I_{OUT}, I (in Figure 5) is given this dependence! Large device M2 operates at low current to make V_{GS} equal to the threshold voltage. The temperature T of the circuit is then swept over the range of interest (also varying I with the temperature dependence of I_{OUT} if a temperature dependence is desired for I_{OUT}) and V_X is measured as a function of temperature. Figure 6 shows a curve which might be obtained using this method and three points on this curve at temperatures T_0, T_1 and T_2 with corresponding voltage values V_0, V_1 and V_2. The design task then becomes one of synthesizing this experimentally determined curve with the various temperature dependent sources. V_X as a function of temperature can be defined as

$$V_X(T)=k_1+k_2\frac{T}{T_0}+k_3(\frac{T}{T_0})^2+...k_n(\frac{T}{T_0})^{n-1}$$

where k_1 is a temperature independent term, k_2 is the amplitude of a PTAT term, k_3 is the amplitude of a $PTAT^2$ term, and k_n is the amplitude of a $PTAT^{n-1}$ term. If a straight-line approximation is good enough, then only the first two terms are needed and simultaneous equations can be solved using the values of V_X at T_0 and T_1. A more exact approximation can be done by developing three simultaneous equations using the values of V_X at T_0, T_1, and T_2. Four (or more) voltage values may be used to solve four (or more) simultaneous equations in the same way.

Once the synthesis terms are known, the actual circuit is simple to implement, especially if a temperature invariant voltage reference is already available somewhere else in the design. Figure 7 is a circuit which may be used to convert a bandgap voltage reference V_{BG} into a constant current reference I_{OUT}. Going up a V_{be} at Q_1 and down a V_{be} at Q_2, the base voltage of Q_3 is also equal to V_{BG}. Therefore, the collector current IC2 of Q_2 is approximately V_{BG}/R_1. Since the emitter voltage of Q_3 is V_{BG}-V_{be}, the collector current IC3 of Q_3 will be PTAT. These two currents IC2 and IC3 are combined in R_4 to provide the bias voltage V_X. M5 is also biased for constant current, so the Q_1 and Q_2 base emitter voltages nearly track over temperature. Long channel device M4 provides a low current for the large threshold cancelling device M6. Both M6 and the current source device M8 are split in half to allow common centroid layout of these critical components.

The Figure 7 circuit was built on a test mask in a 200 Angstrom gate process. The cancellation of mobility drift resulted in a variation in I_{OUT} of only +/- 1.3% from -40 to 120 degrees C.

Figure 8 is a more generalized bias circuit designed to operate in multiple applications. This circuit provides both a temperature stable voltage reference, V_{REF}, and the bias for a temperature stable current reference, V_{BIAS}. Positive tc (temperature coefficient) current is derived with a conventional PTAT generator consisting of Q3, Q2, R4, and the M12-M10 mirror. In addition to biasing the bases of Q2 and Q3, M5 provides a negative tc current with a value of V_{be} of Q3 divided by R3. These currents are combined in different proportions to get V_{REF} and V_X. PMOS transistor MVT operates at low current for V_{GS} equal to V_{TH}, and Q1 has been added to provide NPN base current compensation. Note that this circuit doesn't have second order correction, which could have been added with a translinear multiplier operating on the PTAT current to get a $PTAT^2$ current. V_{REF} is set at 2V, with taps at 1.5V and 1V available for various applications. This circuit will now be used in a circuit applications, in which this Figure 8 reference circuit is labelled "PREFQ".

Figure 9 is a oneshot circuit that uses the reference circuit PREFQ to bias PMOS MR for constant current. With V_{IN} high, capacitor CT is held at zero volts. When V_{IN} goes low, the constant drain current of MR ramps the voltage on CT. The reference circuit PREFQ also provides a 2 volt reference at the comparator negative input. When the ramp reaches this level, the output switches, and hysteresis is applied by switching the comparator negative input to a 1 volt reference. In the off state with V_{IN} high, the drain of M2 is held low. Diode Q_1 is off, so no current flows through ramp reset switch M3. This resets the voltage on CT to zero without the need for a large device, minimizing loading of the timing capacitor and glitching due to feedthrough of the input voltage.

Another application of this invention is for transconductance control, which is especially useful for filtering. Figure 10 shows a prior art Gm/C filter stage. For this simple Gm/C stage, the transconductance of the input device M2 is

$$Gm_2=\sqrt{2\mu C_{OX}(\frac{W}{L})I_2}$$

Letting the gate-source voltage of M1 be $V_X + V_{TH}$, the transconductance turns out to be

$$Gm_2=\mu C_{OX}V_XK$$

where K is a constant set by the device areas. Designing V_X for approximately a $T^{3/2}$ dependence will therefore yield temperature invariant filtering.

What has been described is how a mobility reference can provide a temperature invariant current source proportional to C_{OX}, or with a different tc a transconductance proportional to C_{OX}. These components can be combined with capacitors to build temperature stable oscillators, delay blocks, or filters, without the need for external components or trimming. While the specific circuits described use BICMOS technology, the fact that bandgap references are built in CMOS shows that the same principles can be applied there. It should also be possible to use parasitic MOS devices available in many bipolar processes to build time references. Although various embodiments of the present invention have been shown and described in detail, many other embodiments that incorporate the teachings of this invention may be easily constructed by those skilled in this art. Furthermore, modifications, improvements and variations upon any of these embodiments would be readily apparent to those of ordinary skill and may be made without departing from the spirit and scope of this invention. For example, wherever PMOS transistors are used, NMOS transistors could be used instead by substituting V_{CC} for ground and ground for V_{CC} and by reversing the directions of current sources and polarities of voltage sources. The device M2 can be a field effect transistor or a bipolar transistor. Thus, the control electrode of device M2 is a gate or a base, respectively, the first main electrode is a drain or a collector, respectively, and the second main electrode is a source or an emitter, respectively.

CLAIMS:

1. A reference circuit for producing an output reference current having an arbitrary predetermined temperature dependence, comprising:

a first field effect transistor (M3), and

a bias circuit for applying a total bias voltage to a gate of said first field effect transistor (M3), said bias circuit comprising:

a second field effect transistor (M1) for providing a first bias voltage component substantially corresponding to a threshold voltage of said first field effect transistor (M3), said first bias voltage component being generated between the gate and the source of the second field effect transistor (M1),

an adding circuit for adding a plurality of bias voltage components, said plurality comprising said first bias voltage component, a sum of said plurality of bias voltage components being applied as a gate-source voltage to said first field effect transistor (M3).

2. The reference circuit of Claim 1, characterised in that said second field effect transistor (M1) is included in a control loop for providing a low impedance characteristic to said first bias voltage component.

3. The reference circuit of Claim 2, characterised in that said control loop comprises:

a first current source coupled to the drain of the second field effect transistor (M1),

a third transistor (M2), having a control electrode, a first and a second main electrode, the control electrode being coupled to the drain of said second field effect transistor (M1), and the second main electrode being coupled to the gate of the second field effect transistor (M1).

4. The reference circuit of Claim 3, characterised in that said adding circuit comprises:

a first resistor (R_1), coupled between the gate and the source of the second field effect transistor (M1),

a second resistor (R_2), coupled between the gate of the first field effect transistor (M3) and the gate of the second field effect transistor (M1),

further characterised in that at least a current source (I_1) is provided, said current source (I_1) being coupled to the gate of the first field effect transistor (M3) for providing a second bias voltage component across the second resistor (R_2).

5. The reference circuit of Claim 1, 2, 3 or 4, characterised in that said plurality of bias voltage components comprises a second bias voltage component, said second bias voltage component being proportional to approximately $T^{3/4}$ over a temperature range of interest.

6. The reference circuit of Claim 1, 2, 3 or 4, characterised in that said plurality of bias voltage components comprises a second bias voltage component, said second bias voltage component being proportional to approximately $T^{3/2}$ over a temperature range of interest.

7. The reference circuit of Claim 4, characterised in that further current sources ($I_2..I_n$) are provided, said current sources ($I_2..I_n$) being coupled to the gate of the first field effect transistor (M3) for providing respective bias voltage components across the second resistor (R_2).

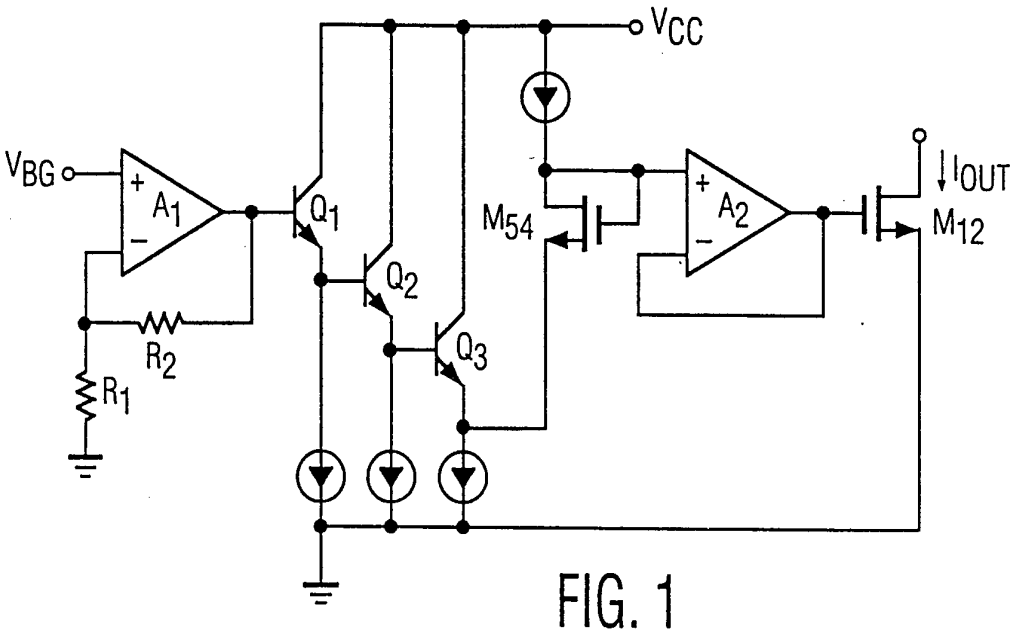


FIG. 1

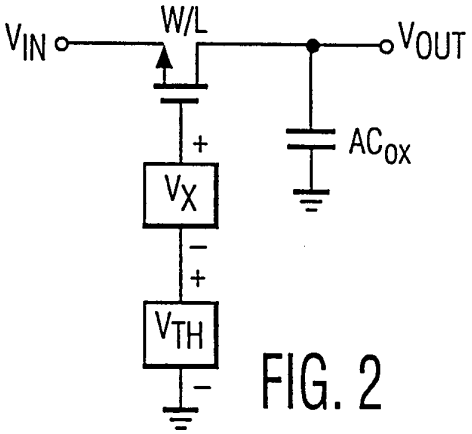


FIG. 2

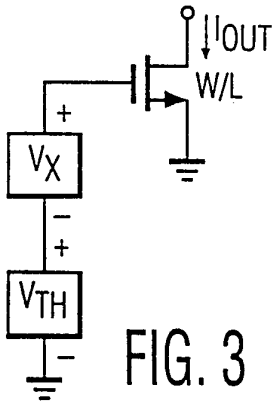
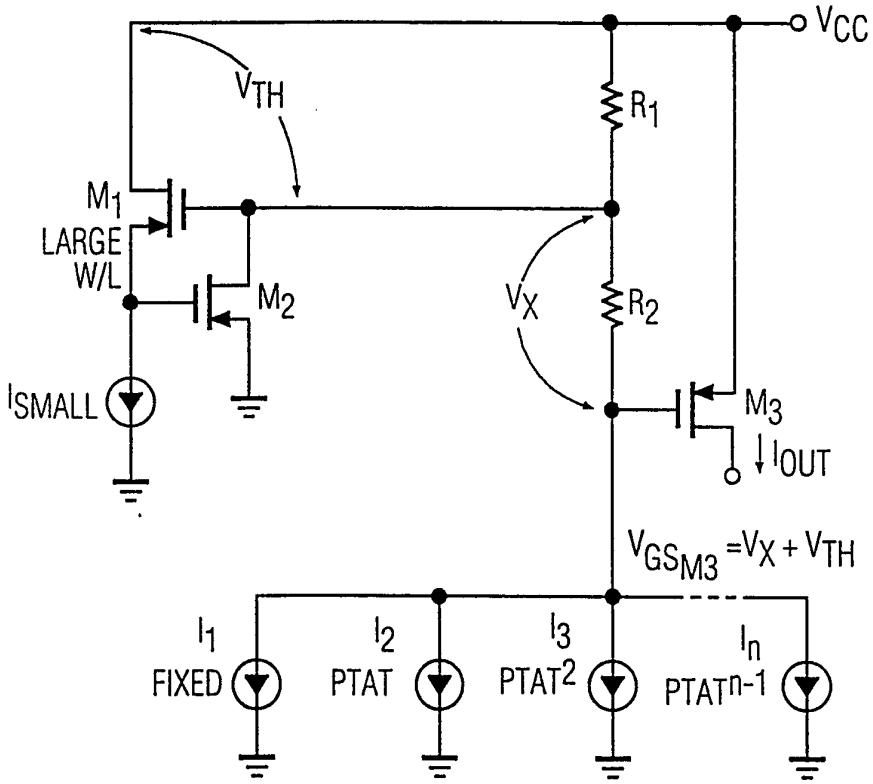


FIG. 3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VTH
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M1
LARGE
W/L
M2
VX
R2
ISMALL
M3
IOUT
VGSM3 =VX + VTH
I1
FIXED
I2
PTAT
I3
PTAT2
In
PTATn-1

FIG. 4

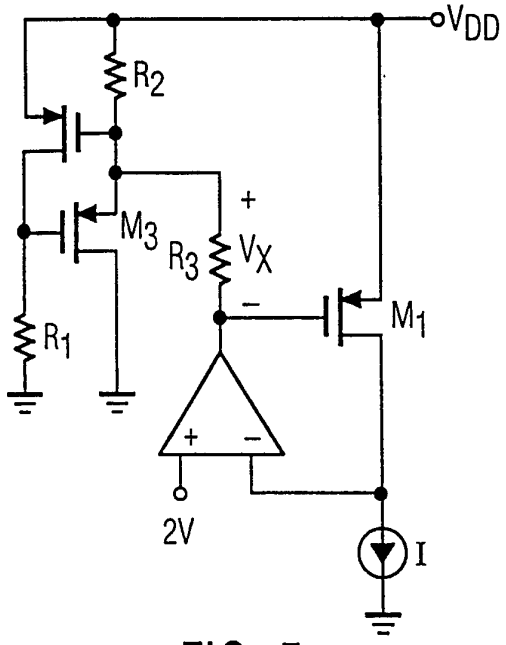

FIG. 5

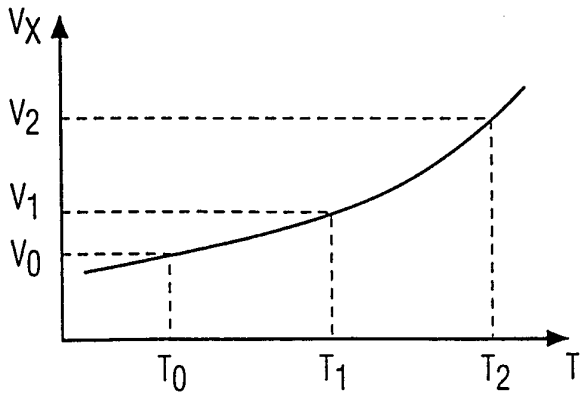

FIG. 6

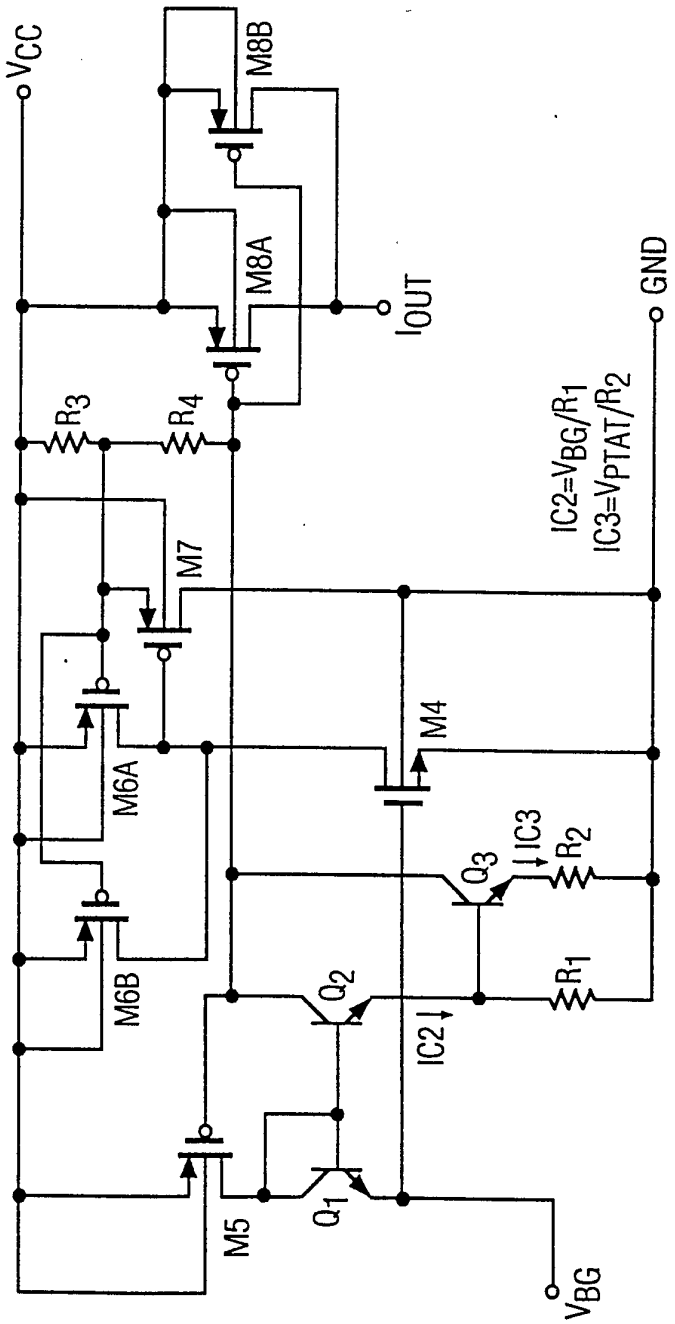
VCC
M8B
M8A
IOUT
GND
R3
R4
M7
IC2=VBG/R1
IC3=VPTAT/R2
M4
M6A
M6B
Q3
IC3
R2
R1
Q2
IC2
M5
Q1
VBG

FIG. 7

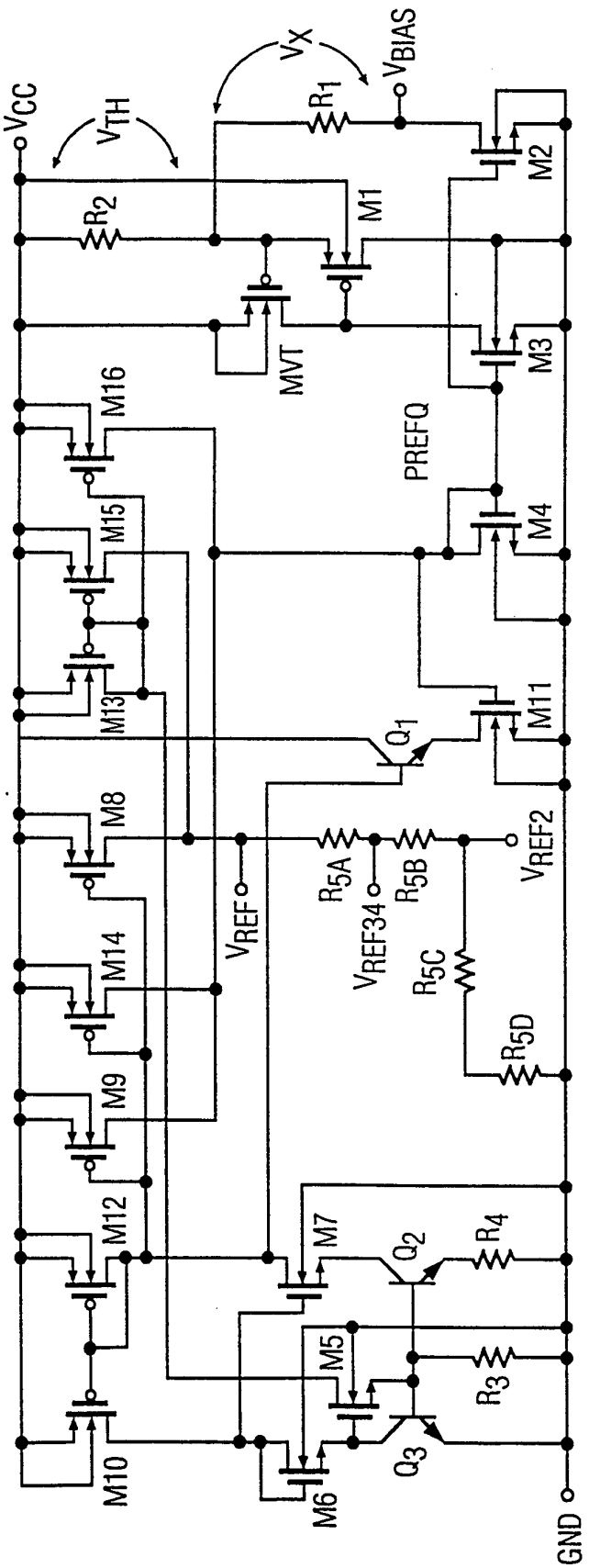
VCC
VTH
VX
VBIAS
R1
R2
M1
M2
MVT
M3
M16
M15
M13
PREFQ
M4
M11
Q1
M8
M14
M9
M12
M7
Q2
R4
M5
R3
M10
M6
Q3
GND
VREF
R5A
R5B
VREF2
VREF34
R5C
R5D

FIG. 8

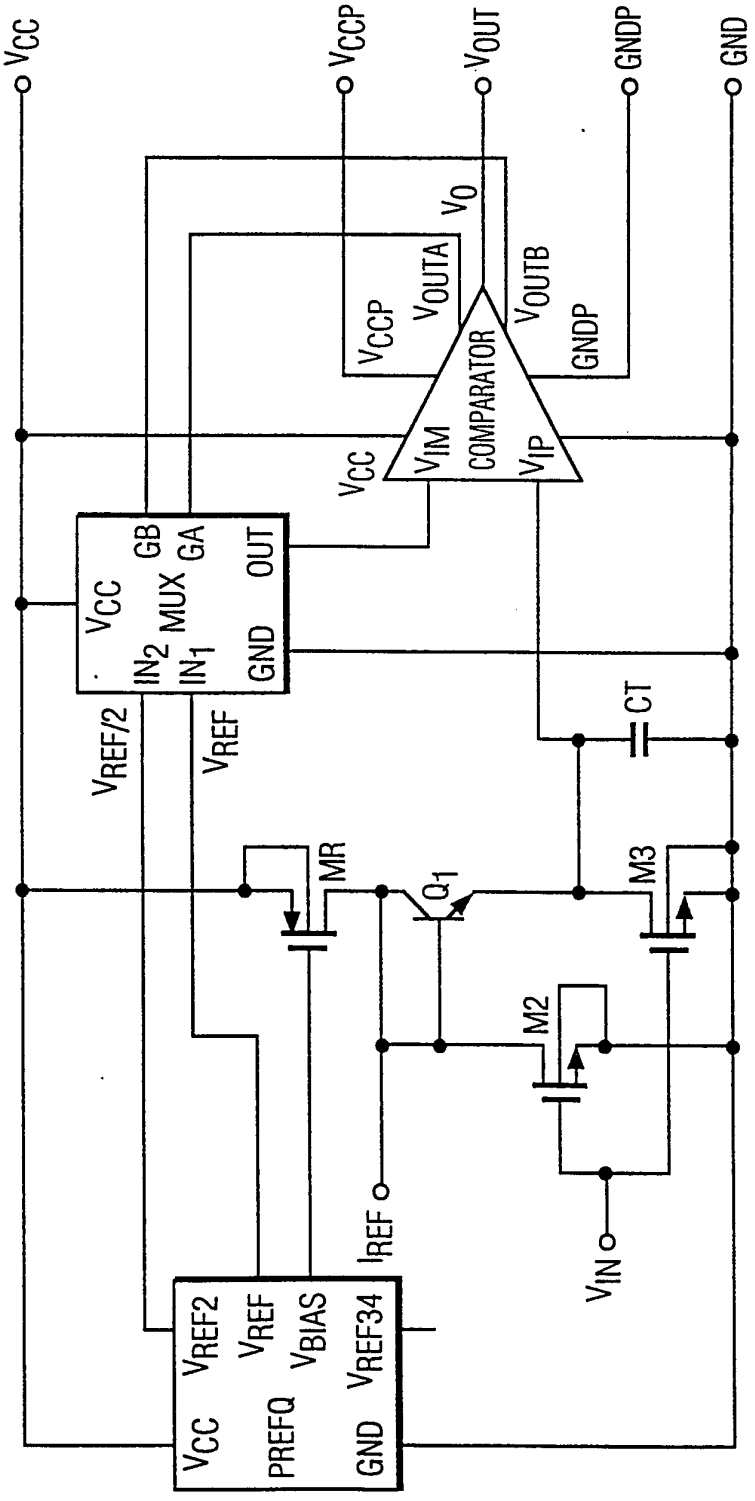
VCC
VCCP
VOUT
GNDP
GND
VO
VCCP
VOUTA
VOUTB
GNDP
COMPARATOR
VCC
VIM
VIP
VCC
GB
GA
OUT
MUX
IN2
IN1
GND
VREF/2
VREF
CT
MR
Q1
M3
M2
IREF
VIN
VCC
VREF2
VREF
VBIAS
VREF34
PREFQ
GND

FIG. 9

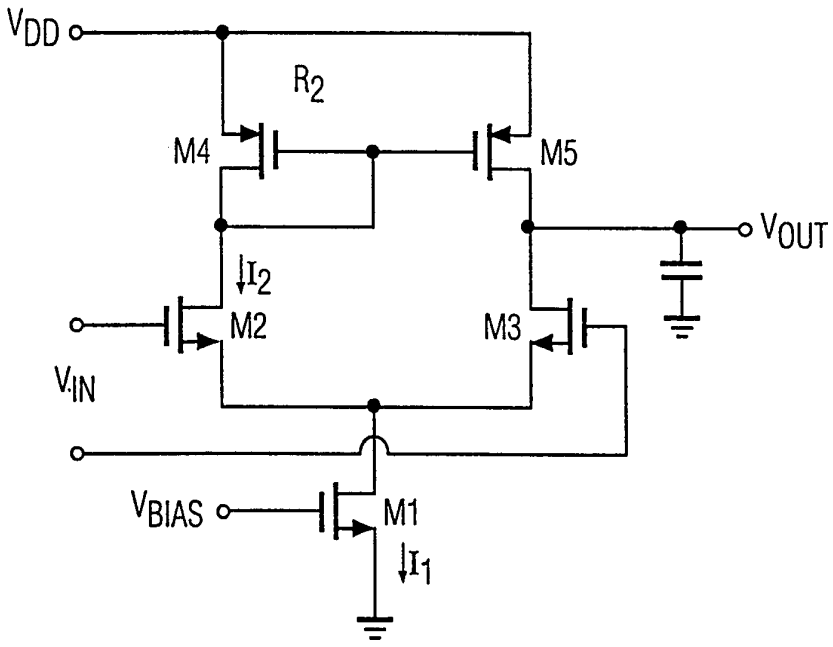

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 95/00098

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: G05F 3/24, G05F 1/46
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: G05F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP, A1, 0504983 (N.V. PHILIPS' GLOEILAMPENFABRIEKEN), 23 Sept 1992 (23.09.92), column 1, line 40 - column 3, line 3 --	1
A	EP, A2, 0492117 (MOTOROLA, INC.), 1 July 1992 (01.07.92), column 1, line 55 - column 3, line 14 --	1
A	Patent Abstracts of Japan, Vol 13,No 572, P-978, abstract of JP, A, 1-240917 (RICOH CO LTD), 26 Sept 1989 (26.09.89) --	1

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
2 June 1995	07 -06- 1995
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Håkan Sandh Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 95/00098

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 5281906 (D.C. THELEN, JR.), 25 January 1994 (25.01.94), column 1, line 58 - column 2, line 36 -- --------	1

INTERNATIONAL SEARCH REPORT

Information on patent family members

03/05/95

International application No.
PCT/IB 95/00098

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A1- 0504983	23/09/92	JP-A- 5083048	02/04/93
EP-A2- 0492117	01/07/92	JP-A- 4293275	16/10/92
		US-A- 5198701	30/03/93
US-A- 5281906	25/01/94	WO-A- 9309487	13/05/93