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(54) Title: BIAS CURRENT GENERATING TECHNIQUES

(57) Abstract: Various implementations described herein are directed to multi-stage system. The system may include a first stage having a current bias generator that generates a biasing current. The system may include a second stage that is coupled to the first stage, and the second stage may include a load that utilizes the biasing current generated by the current bias generator.

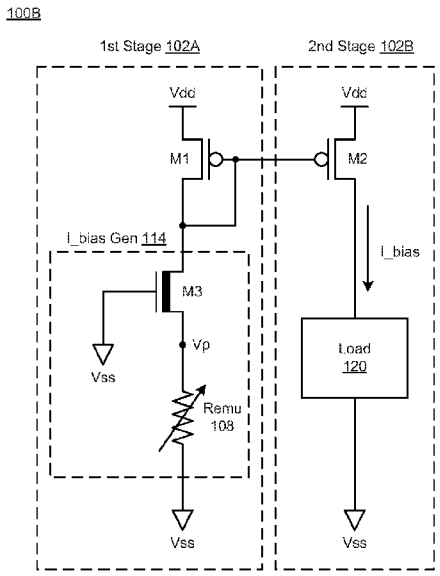

FIG. 1B

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BIAS CURRENT GENERATING TECHNIQUES

[0001] The present disclosure was made with Government support under Agreement No. HR0011-17-9-0025, awarded by DARPA. The Government may have certain rights in reference to the present disclosure.

BACKGROUND

[0002] This section is intended to provide information relevant to understanding the various technologies described herein. As the section's title implies, this is a discussion of related art that should in no way imply that it is prior art. Generally, related art may or may not be considered prior art. It should therefore be understood that any statement in this section should be read in this light, and not as any admission of prior art.

[0003] In modern wireless infrastructure, Internet-of-Things (IoT) devices typically use ultra low power sensor nodes for operation in remote environments. To prolong usage time of battery-powered or battery-less IoT devices, ultra low power operation of IoT sensors are increasingly demanded, and as such, there exists a need for ultra low power current generators for these IoT sensors in a wide array of IoT applications.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Implementations of various techniques are described herein with reference to the accompanying drawings. It should be understood, however, that the accompanying drawings illustrate only various implementations described herein and are not meant to limit embodiments of various techniques described herein.

[0005] Figures 1A-1C illustrate various diagrams of bias current generating circuitry in accordance with various implementations described herein.

[0006] Figure 2 illustrates a diagram of a reference voltage generating circuitry in accordance with various implementations described herein.

[0007] Figure 3 illustrates a process diagram of a method for providing bias current generating circuitry in accordance with implementations described herein.

DETAILED DESCRIPTION

[0008] Various implementations described herein are directed to integrated circuitry (IC) that uses bias current generating schemes and techniques for implementing various sensing type applications. For instance, the various schemes and techniques described herein may provide for a low temperature-dependent, self-stabilizing, and area-efficient bias current generator for Internet-of-Things (IoT) sensing applications in a low current (e.g., nano-ampere) range of operation. In some implementations, the nano-ampere bias current generator may reduce or eliminate instability and temperature-dependency.

[0009] Various implementations of bias current generating schemes and techniques will be described in detail herein with reference to Figures 1A-3.

[0010] Figures 1A-1C illustrate various diagrams of bias current generating circuitry in accordance with various implementations described herein. In particular, Figure 1A refers to a diagram of bias current generating circuitry 100A, Figure 1B refers to another diagram of bias current generating circuitry 100B, and Figure 1C refers to another diagram of bias current generating circuitry 100C. In some instances, the bias current generating circuitry may be implemented as integrated circuitry (IC) in a system or a device having various circuit components arranged and coupled together as an assemblage or combination of parts that provide for a physical circuit design and related structures. In some instances, a method of designing, providing and building the bias current generating circuitry as an IC may involve use of the various circuit components described herein so as to thereby implement bias current generating schemes and techniques associated therewith. Also, the bias current generating circuitry may be implemented as an IC with various embedded systems for various electronic, mobile and Internet-of-things (IoT) applications.

[0011] As shown in Figure 1A, the bias current generating circuitry 100A may include a reference voltage (Vref) generator 104 and an emulated resistor (Remu) 108. The Vref generator 104 may be coupled between a supply voltage (Vdd) and ground (Vss or Gnd), and the Vref generator 104 may be configured to generate and provide a reference gate voltage (Vgate/Vref) to the Remu 108. The Remu 108 includes one or more transistors (T1, T2, ... , TN) that are coupled between a node voltage (Vp) and ground (Vss or Gnd). In some instances, a number (N) of transistors (T1, T2, ... , TN) may be coupled together in series between the node voltage (Vp) and ground (Vss or Gnd). For instance, a first transistor (T1) may be coupled between the node voltage (Vp) and a second transistor (T2), and some number (N) of transistors (T2, ... , TN) may be coupled between the first

transistor (T1) and ground (Vss or Gnd). Also, in some implementations, the transistors (T1, T2, ... , TN) may include N-type metal-oxide-semiconductor (NMOS) transistors. However, in other instances, P-type MOS (PMOS) transistors may be used.

[0012] As shown in Figure 1B, the bias current generating circuitry 100B may include multiple stages including, e.g., a first stage 102A and a second stage 102B that are coupled together and arranged to provide a biasing current (I_bias). In some instances, the first stage 102A may include a current bias generator (I_bias Gen) 114 that generates a biasing current (I_bias). The current bias generator (I_bias Gen) 114 may have a native device structure (e.g., M3) with a gate coupled to ground (Vss or Gnd), wherein the native device structure (e.g., M3) may be a transistor (e.g., an N-type MOS) that is associated with process variation. The current bias generator (I_bias Gen) 114 may include a resistor structure (e.g., Remu 108) that is coupled between a source terminal of the native device structure (e.g., M3) and ground (Vss or Gnd). For instance, as shown in Figure 1B, the resistor structure (e.g., Remu 108) may be coupled between transistor (M3) at node (Vp) and ground (Vss or Gnd). In some instances, the resistor structure (e.g., Remu 108) may have a first plurality of stacking transistor structures (e.g., T1, T2, ... , TN) that are coupled in series, and the reference voltage (Vgate/Vref) may be used to activate the first plurality of stacking transistor structures (e.g., T1, T2, ... , TN) that operate in a triode region and behave as resistors. Also, in some instances, the native device structure (e.g., M3) may be an NMOS transistor. However, a PMOS transistor may be used.

[0013] The second stage 102B may be coupled to the first stage 102A, and the second stage 102B may have a load 120 that utilizes the biasing current (I_bias) generated by the current bias generator (I_bias Gen) 114. In some instances, the second stage 102B may be coupled in parallel with the first stage 102A, and the first stage 102A may include a first stacking transistor structure (e.g., M1) that is coupled between the supply voltage (e.g., Vdd) and the current bias generator (I_bias Gen 114). The current bias generator (I_bias Gen) 114 may be coupled between the first stacking transistor structure (e.g., M1) and ground (Vss or Gnd). The first stacking transistor structure (e.g., M1) may be coupled as a diode. The second stage 102B may include a second stacking transistor structure (e.g., M2) that is coupled between the supply voltage (Vdd) and the load 120, and also, the load 120 may be coupled between the second stacking transistor structure (e.g., 102) and ground (Vss or Gnd). Also, a gate of the first stacking transistor structure (e.g., M1) may be coupled to a gate of the second stacking transistor structure (e.g., M2). In some

instances, the biasing current (I_bias) may develop as an output from the second stacking transistor structure (e.g., M2) to the load 120. In some implementations, transistors (M1, M2) may be PMOS transistors. However, NMOS transistors may be used.

[0014] As shown in Figure 1C, the bias current generating circuitry 100C may include a first stage 122A and a second stage 122B that are implemented differently than the first and second stages 102A, 102B of Figure 1B. For instance, the first stage 122A may be coupled between the second stage 122B and ground (Vss or Gnd), and the second stage 122B may be coupled in series with the first stage 122A. The second stage 122B may be coupled between the supply voltage (Vdd) and the first stage 122A, and also, the biasing current (I_bias) may develop as an output from the second stage 122B to the first stage 122A. In some instances, the first stage 122A may only include the current bias generator (I_bias Gen 114), and the second stage 122B may only include the load 120.

[0015] In some implementations, the source of the native NFET (M3) may be coupled to the resistor (Remu 108), and the gate of the native NFET (M3) may be biased at ground voltage (Vss or Gnd). The resistor (Remu 108) may be implemented with the regular Vth NFETs (T1, T2, ... , TN) that operate in a triode-region and that may be digitally-tuneable against process shift. The gate of the triode-region operated NFETs (T1, T2, ... , TN) may be biased by a 4-transistor (4T) based temperature-compensated voltage reference (Vref Gen 104). In some instances, the native NFET (M3) and the resistor (Remu 108) form a negative-feedback source degenerator that self-stabilizes. Since the drain-source voltage of M3 is large, I_bias may be derived as:

$$I_{BIAS} \approx \mu_3 C_{ox} \frac{W_3}{L_3} (1 - m_3) V_T^2 e^{\left(\frac{-V_P}{m_3 V_T}\right)} \qquad (1)$$

and

$$V_P \approx 1.5 m_3 V_T \quad \text{and} \quad \mu_3 \propto T^{-1.5} \qquad (2)$$

[0016] where m_3 and μ_3 refer to a sub-threshold slope factor and carrier mobility of native NFET (M3), respectively; V_T is thermal voltage; T is absolute temperature. M3 sits in a lightly-doped p-substrate, so temperature dependence of μ_3 mainly obeys lattice scattering behavior. Also, it may be seen that $I_{BIAS} \propto T^{0.5}$.

[0017] Figure 2 illustrates a diagram of reference voltage generating circuitry 200 in accordance with various implementations described herein. In some implementations,

the reference voltage generating circuitry 200 may refer to the reference voltage generator (Vref) 104 as shown in Figure 1A.

[0018] As shown in Figure 2, the reference voltage generator 104 may be configured to generate the reference voltage (Vref/Vgate), and the reference voltage generator 104 may include a native device structure (e.g., L1, a native NMOS or NFET) and a second plurality of stacking transistor structures (e.g., L2, L3, L4) that may be coupled in series between the supply voltage (Vdd) and ground (Vss or Gnd).

[0019] In some implementations, as shown, the reference voltage generator 104 may include a first transistor (L1), a second transistor (L2), a third transistor (L3), and a fourth transistor (L4) that are coupled in series between the supply voltage (Vdd) and ground (Vss or Gnd). The first transistor (L1) may be coupled between the supply voltage (Vdd) and the second transistor (L2) at an output node (n1), and also, the output of the reference voltage generator 104 may be provided from the output node (n1) as an output of the first transistor (L1). The second transistor (L2) may be coupled between the first transistor (L1) and the third transistor (L3), and a gate of the first transistor (L1) may be coupled to an output of the second transistor (L2), and a gate of the second transistor (L2) may be coupled to the output node (n1). The third transistor (L3) may be coupled between the second transistor (L2) and the fourth transistor (L4), and a gate of the third transistor (L3) may be coupled to the output of the second transistor (L2). The fourth transistor (L4) may be coupled between the third transistor (L3) and ground (Vss or Gnd), and a gate of the fourth transistor (L4) may be coupled to the output of the third transistor (L3).

[0020] In some implementations, the first transistor (L1) may be an NMOS transistor having a native device structure, and the first transistor (L1) may be referred to as a native NFET (i.e., an N-type field effect transistor that is associated with process variation). Also, the second transistor (L2), the third transistor (L3), and the fourth transistor (L4) may be NMOS transistors, and the transistors (L2, L3, L4) may be referred to as regular NFETs with regular or standard voltage thresholds (Vth). In other implementations, one or more of the transistors (L1, L2, L3, L4) may be PMOS transistors.

[0021] In some implementations, the reference voltage generator (Vref Gen) 104 may be embodied as a 4-transistor (4T) voltage reference for generating Vgate/Vref for biasing Remu 108 in the I_bias generator 114. The stacked, diode-connected, regular-Vth NFETs (T1, T2, ... , TN) may be configured to provide a Vgate/Vref voltage of less than 1.4V, with

a total power in this 4T voltage reference of less than 250pW. For instance, the stacked, diode-connected, regular-Vth NFETs (T1, T2, ... , TN) may be configured to effectively increase the Vgate/Vref voltage, e.g., to about 0.9V, with a total power in this 4T voltage reference of about 160pW at Vdd=1.2V with temperature at about 25°C.

[0022] Figure 3 illustrates a process diagram of a method 300 for providing bias current generating circuitry in accordance with implementations described herein.

[0023] It should be understood that even though method 300 may indicate a particular order of operation execution, in some cases, various certain portions of the operations may be executed in a different order, and on different systems. In other cases, additional operations and/or steps may be added to and/or omitted from method 300. Also, method 300 may be implemented in hardware and/or software. If implemented in hardware, the method 300 may be implemented with various circuit elements, such as described herein above in reference to Figures 1A-2. If implemented in software, the method 300 may be implemented as a program and/or software instruction process that may be configured for providing bias current generating techniques as described herein. Also, if implemented in software, instructions related to implementing the method 300 may be stored in memory and/or a database. For instance, a computer or various other types of computing devices having a processor and memory may be configured to perform method 300.

[0024] As described and shown in reference to Figure 3, method 300 may be used for designing, creating, routing, fabricating and/or manufacturing an integrated circuit (IC) that implements bias current generating schemes and techniques described herein. Also, in reference to Figure 3, method 300 may be configured to translate the physical design of an integrated circuit (IC) while preserving logical behaviors and characteristics.

[0025] At block 310, method 300 may couple a gate of a native device structure to ground (Vss or Gnd). The native device structure may be a native transistor (e.g., NMOS) that is associated with process variation. Also, at block 320, method 300 may couple a resistor structure between the native device structure and ground (Vss or Gnd), and the resistor structure may be coupled between a source terminal of the native device structure and ground. In some instances, the resistor structure may have a first plurality of stacking transistor structures coupled in series, and a reference voltage may be used to activate the first plurality of stacking transistor structures. At block 330, method 300 may couple a load to the native device structure, and at block 340, method 300 may generate a biasing

current (I_bias) for the load with the native device structure and the resistor structure. In some implementations, method 300 may include generating the reference voltage with a reference voltage generator, and also, the reference voltage generator may have another native device structure and a second plurality of stacking transistor transistors that are coupled in series between a supply voltage and ground.

[0026] In some implementations, the native device structure is configured to receive a supply voltage (e.g., Vdd, via a pass transistor), and the native device structure may have a gate coupled to ground (Vss or Gnd). The resistor structure may be coupled between the native device structure and ground, and the native device structure and the resistor structure may be configured to generate the biasing current (I_bias) for the load. Also, the resistor structure has a first plurality of stacking transistor structures coupled in series, and the reference voltage may be used to activate the first plurality of stacking transistor structures. In some instances, a reference voltage generator may be used to generate the reference voltage, and the reference voltage generator may have another native device structure and a second plurality of stacking transistor transistors that are coupled in series between the supply voltage (e.g., Vdd) and ground (Vss or Gnd). Also, in some instances, the load may be coupled in parallel with the native device structure and the resistor structure. Otherwise, in other instances, the load may be coupled in series with the native device structure and the resistor structure. Also, in some instances, method 300 may provide a current bias generator that generates the biasing current (I_bias) for Internet-of-Things (IoT) applications.

[0027] Described herein are various implementations of a system. The system may include a first stage having a current bias generator that generates a biasing current. The system may include a second stage coupled to the first stage, and the second stage has a load that utilizes the biasing current generated by the current bias generator.

[0028] Described herein are various implementations of a device. The device may include a native device structure that is configured to receive a supply voltage, and the native device structure has a gate coupled to ground. The device may include a resistor structure coupled between the native device structure and ground, and the native device structure and the resistor structure are configured to generate a biasing current for a load.

[0029] Described herein are various implementations of a method. The method may include coupling a gate of a native device structure to ground. The method may include

coupling a resistor structure between the native device structure and ground. The method may include coupling a load to the native device structure. The method may include generating a biasing current for the load with the native device structure and the resistor structure.

[0030] It should be intended that the subject matter of the claims not be limited to the implementations and illustrations provided herein, but include modified forms of those implementations including portions of implementations and combinations of elements of different implementations in accordance with the claims. It should be appreciated that in the development of any such implementation, as in any engineering or design project, numerous implementation-specific decisions should be made to achieve developers' specific goals, such as compliance with system-related and business related constraints, which may vary from one implementation to another. Moreover, it should be appreciated that such a development effort may be complex and time consuming, but would nevertheless be a routine undertaking of design, fabrication, and manufacture for those of ordinary skill having benefit of this disclosure.

[0031] Reference has been made in detail to various implementations, examples of which are illustrated in the accompanying drawings and figures. In the following detailed description, numerous specific details are set forth to provide a thorough understanding of the disclosure provided herein. However, the disclosure provided herein may be practiced without these specific details. In some other instances, well-known methods, procedures, components, circuits and networks have not been described in detail so as not to unnecessarily obscure details of the embodiments.

[0032] It should also be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element. The first element and the second element are both elements, respectively, but they are not to be considered the same element.

[0033] The terminology used in the description of the disclosure provided herein is for the purpose of describing particular implementations and is not intended to limit the disclosure provided herein. As used in the description of the disclosure provided herein and appended claims, the singular forms "a," "an," and "the" are intended to include the

plural forms as well, unless the context clearly indicates otherwise. The term "and/or" as used herein refers to and encompasses any and all possible combinations of one or more of the associated listed items. The terms "includes," "including," "comprises," and/or "comprising," when used in this specification, specify a presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components and/or groups thereof.

[0034] As used herein, the term "if" may be construed to mean "when" or "upon" or "in response to determining" or "in response to detecting," depending on the context. Similarly, the phrase "if it is determined" or "if [a stated condition or event] is detected" may be construed to mean "upon determining" or "in response to determining" or "upon detecting [the stated condition or event]" or "in response to detecting [the stated condition or event]," depending on the context. The terms "up" and "down"; "upper" and "lower"; "upwardly" and "downwardly"; "below" and "above"; and other similar terms indicating relative positions above or below a given point or element may be used in connection with some implementations of various technologies described herein.

[0035] While the foregoing is directed to implementations of various techniques described herein, other and further implementations may be devised in accordance with the disclosure herein, which may be determined by the claims that follow.

[0036] Although the subject matter has been described in language specific to structural features and/or methodological acts, it is to be understood that the subject matter defined in the appended claims is not necessarily limited to the specific features or acts described above. Rather, the specific features and acts described above are disclosed as example forms of implementing the claims.

What Is Claimed Is:

1. A system, comprising:

a first stage having a current bias generator that generates a biasing current; and

a second stage coupled to the first stage, wherein the second stage has a load that utilizes the biasing current generated by the current bias generator.

2. The system of claim 1, wherein the current bias generator has a native device structure with a gate coupled to ground.

3. The system of claim 2, wherein the current bias generator has a resistor structure coupled between a source terminal of the native device structure and ground.

4. The system of claim 3, wherein the resistor structure has a first plurality of stacking transistor structures coupled in series, and wherein a reference voltage is used to activate the first plurality of stacking transistor structures that operate in a triode region and behave as resistors.

5. The system of claim 4, further comprising:

a reference voltage generator that generates the reference voltage,

wherein the reference voltage generator has another native device structure and a second plurality of stacking transistor structures that are coupled in series between the supply voltage and ground.

6. The system of claim 1, wherein:

the second stage is coupled in parallel with the first stage,

the first stage has a first stacking transistor structure coupled between a supply voltage and the current bias generator, and

the current bias generator is coupled between the first stacking transistor structure and ground.

7. The system of claim 6, wherein the first stacking transistor structure is coupled as a diode.

8. The system of claim 6, wherein the second stage has a second stacking transistor structure coupled between the supply voltage and the load, and wherein the load is coupled between the second stacking transistor structure and ground.

9. The system of claim 8, wherein a gate of the first stacking transistor structure is coupled to a gate of the second stacking transistor structure.

10. The system of claim 1, wherein:
the second stage is coupled in series with the first stage,
the first stage is coupled between the second stage and ground, and
the second stage is coupled between a supply voltage and the first stage.

11. A device, comprising:
a native device structure that is configured to receive a supply voltage, wherein the native device structure has a gate coupled to ground; and
a resistor structure coupled between the native device structure and ground,
wherein the native device structure and the resistor structure are configured to generate a biasing current for a load.

12. The device of claim 11, wherein the resistor structure has a first plurality of stacking transistor structures coupled in series, and wherein a reference voltage is used to activate the first plurality of stacking transistor structures.

13. The device of claim 12, further comprising:
a reference voltage generator that generates the reference voltage,
wherein the reference voltage generator has another native device structure and a second plurality of stacking transistor transistors that are coupled in series between the supply voltage and ground.

14. The device of claim 11, wherein the load is coupled in parallel with the native device structure and the resistor structure.

15. The device of claim 11, wherein the load is coupled in series with the native device structure and the resistor structure.

16. The device of claim 11, wherein the device comprises a current bias generator that generates a biasing current for Internet-of-Things (IoT) applications.

17. A method, comprising:

coupling a gate of a native device structure to ground;

coupling a resistor structure between the native device structure and ground;

coupling a load to the native device structure; and

generating a biasing current for the load with the native device structure and the resistor structure.

18. The method of claim 17, wherein the resistor structure is coupled between a source terminal of the native device structure and ground.

19. The method of claim 18, wherein the resistor structure has a first plurality of stacking transistor structures coupled in series, and wherein a reference voltage is used to activate the first plurality of stacking transistor structures.

20. The method of claim 19, further comprising:

generating the reference voltage with a reference voltage generator,

wherein the reference voltage generator has another native device structure and a second plurality of stacking transistor transistors that are coupled in series between a supply voltage and ground.

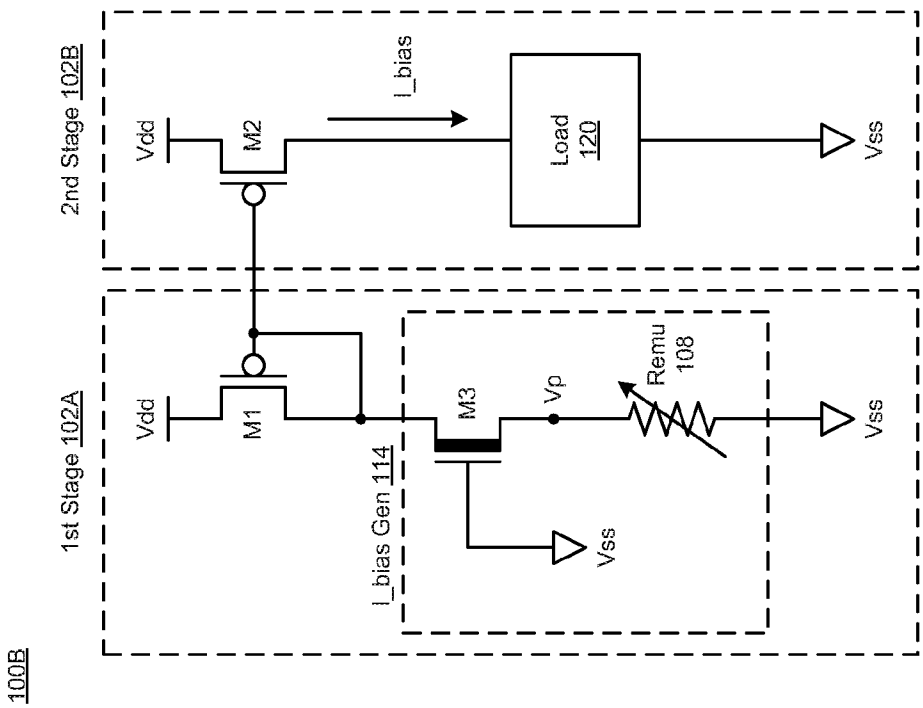
100B
2nd Stage 102B
Vdd
M2
I_bias
Load 120
Vss
1st Stage 102A
Vdd
M1
I_bias Gen 114
M3
Vp
Remu 108
Vss
Vss

FIG. 1B

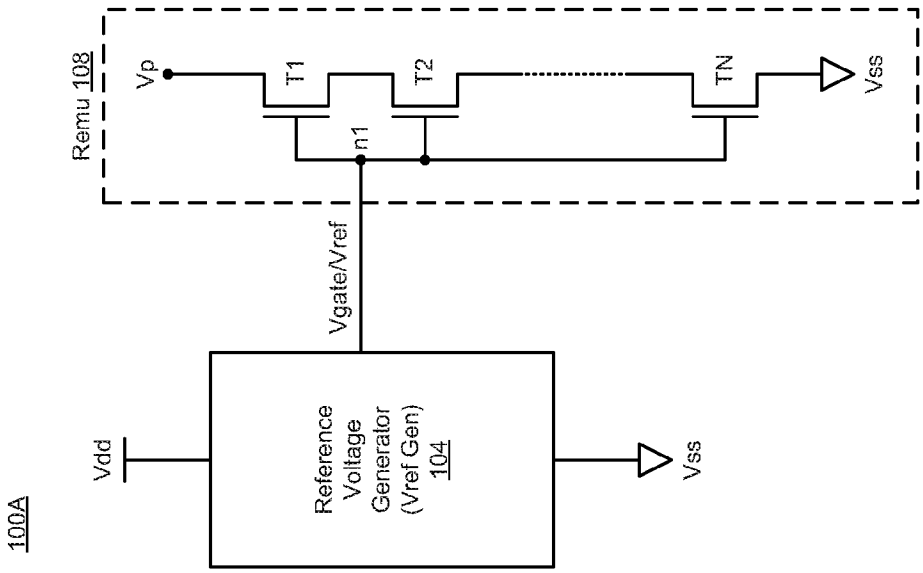
100A
Remu 108
Vp
T1
T2
TN
Vss
n1
Vgate/Vref
Vdd
Reference Voltage Generator (Vref Gen) 104
Vss

FIG. 1A

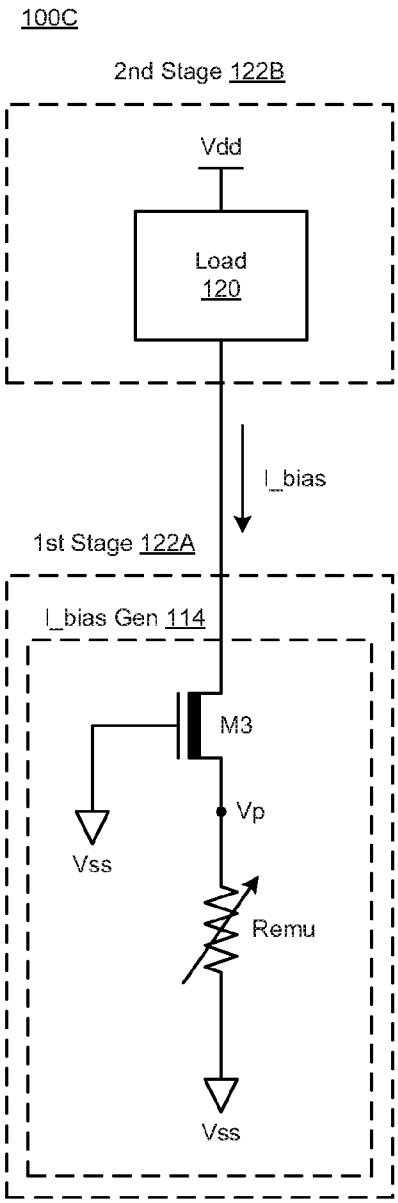
100C
2nd Stage 122B
Vdd
Load
120
I_bias
1st Stage 122A
I_bias Gen 114
M3
Vp
Vss
Remu
Vss

FIG. 1C

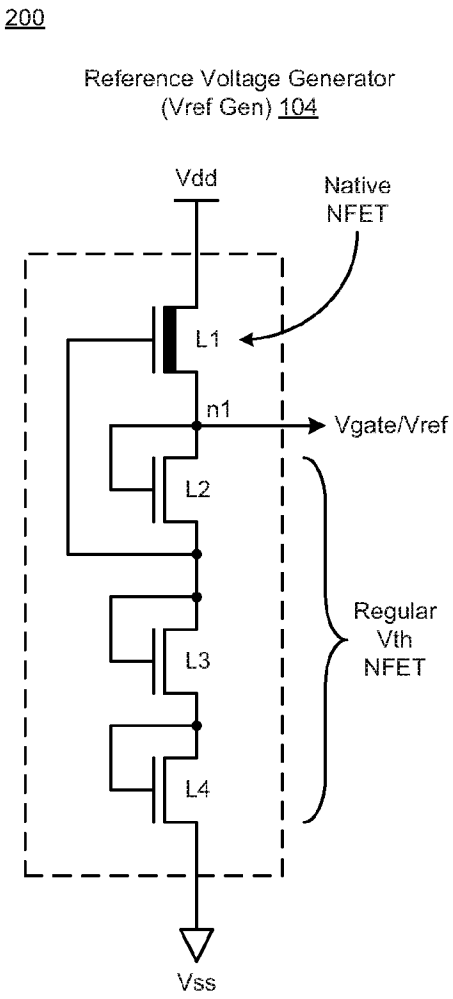
200
Reference Voltage Generator
(Vref Gen) 104
Vdd
Native
NFET
L1
n1
Vgate/Vref
L2
Regular
Vth
NFET
L3
L4
Vss

FIG. 2

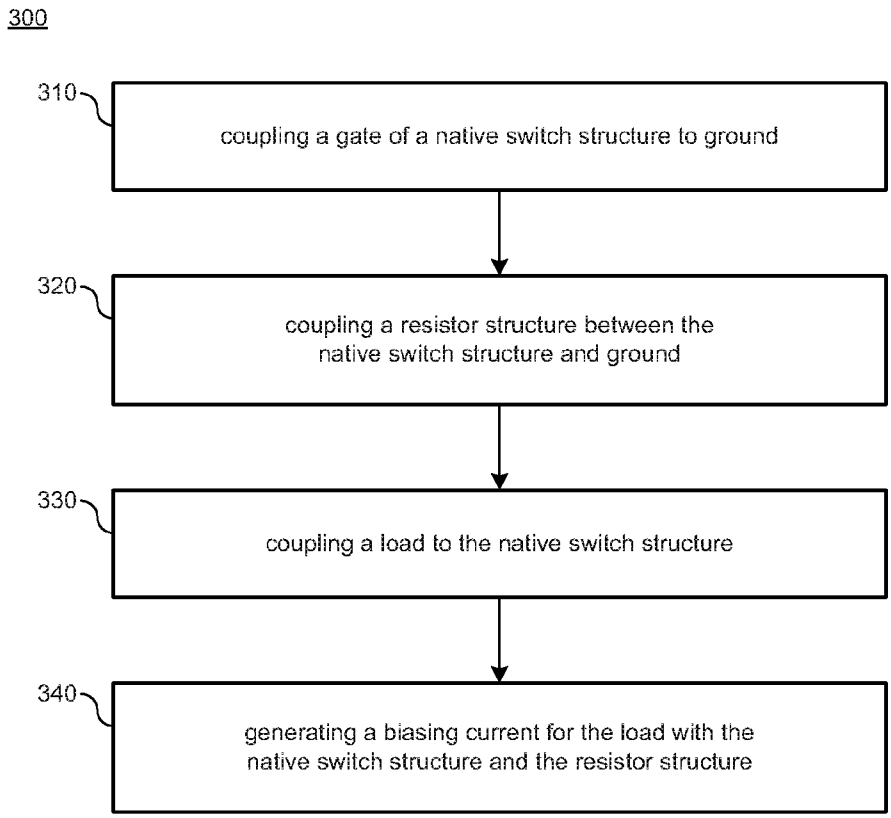
300
310
coupling a gate of a native switch structure to ground
320
coupling a resistor structure between the native switch structure and ground
330
coupling a load to the native switch structure
340
generating a biasing current for the load with the native switch structure and the resistor structure

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2020/051655

A. CLASSIFICATION OF SUBJECT MATTER
INV. G05F3/24
ADD. G05F3/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G05F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014/266140 A1 (IRIARTE SANTIAGO [ES] ET AL) 18 September 2014 (2014-09-18)	1-3, 6-11, 14-18
Y	abstract; figure 12	4,5,12, 13,19,20

Y	US 2019/149146 A1 (TANG WEI-CHENG [TW] ET AL) 16 May 2019 (2019-05-16) abstract; figure 3	4,5,12, 13,19,20

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 September 2020	24/09/2020

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Arias Pérez, Jagoba

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2020/051655

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	ARNAUD ALFREDO ET AL: "An asymmetrical bulk-modified composite MOS transistor with enhanced linearity", 2019 IEEE 10TH LATIN AMERICAN SYMPOSIUM ON CIRCUITS & SYSTEMS (LASCAS), IEEE, 24 February 2019 (2019-02-24), pages 49-52, XP033530948, DOI: 10.1109/LASCAS.2019.8667576 [retrieved on 2019-03-14] figure 6	1-20
A	US 2013/069716 A1 (SHIUE MUH-TIAN [TW] ET AL) 21 March 2013 (2013-03-21) abstract; figure 3A	1-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/GB2020/051655

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014266140 A1	18-09-2014	NONE	
US 2019149146 A1	16-05-2019	TW 201919338 A	16-05-2019
		US 2019149146 A1	16-05-2019
US 2013069716 A1	21-03-2013	TW 201212532 A	16-03-2012
		US 2013069716 A1	21-03-2013