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(71) Applicant *(for all designated States except US):* **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, MS: RNB-4-150, Santa Clara, California 95052 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only):* **ZIERATH, Daniel J.** [US/US]; 1009 NW Hoyt #207, Portland, Oregon 97209 (US). **CHOWDHURY, Shaestagir** [US/US]; 2679 NW 166th Terrace, Beaverton, Oregon 97006 (US). **TSANG, Chi-Hwa** [US/US]; 18550 S.W. Rigert Road, Beaverton, Oregon 97007 (US).

(74) Agent: **MALONEY, Neil, F.;** Finch & Maloney PLLC, c/o CPA Global, P.O. Box 52050, Minneapolis, Minnesota 55402 (US).

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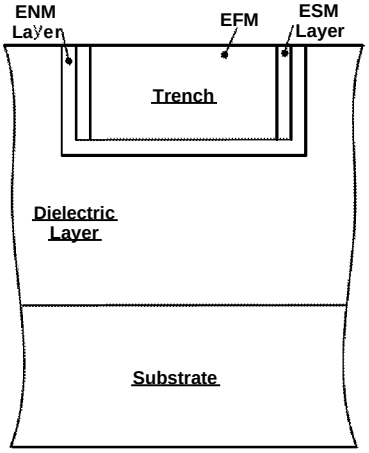

Fig. 1G

(57) Abstract: Techniques are disclosed that enable interconnects, vias, metal gates, and other conductive features that can be formed through electroless material deposition techniques. In some embodiments, the techniques employ electroless fill in conjunction with high growth rate selectivity between an electroless nucleation material (ENM) and electroless suppression material (ESM) to generate bottom-up or otherwise desired fill pattern of such features. Suitable ENM may be present in the underlying or otherwise existing structure, or may be provided. The ESM is provisioned so as to prevent or otherwise inhibit nucleation at the ESM covered areas of the feature, which in turn prevents or otherwise slows down the rate of electroless growth on those areas. As such, the electroless growth rate on the ENM sites is higher than the electroless growth rate on the ESM sites.

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ELECTROLESS FILLED CONDUCTIVE STRUCTURES

Inventors:
Daniel J. Zierath
Shaestagir Chowdhury
Chi-Hwa Tsang

BACKGROUND

In the manufacture of integrated circuits, interconnects are generally formed on a semiconductor substrate using a copper dual damascene process. Such a process typically begins with a trench being etched into a dielectric layer and then filled with a barrier/adhesion layer and a seed layer using a physical vapor deposition (PVD) sputtering process. An electroplating process is then used to fill the via and trench with copper metal to form the interconnect. However, as device dimensions scale down and the features become narrower, the aspect ratio of the features becomes more aggressive. The line-of-sight PVD process gives rise to issues such as trench overhang of the barrier/adhesion, and seed layers, leading to pinched-off trench and via openings during plating, and inadequate gap fill.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-G' illustrate formation of example conductive trench structures in accordance with various embodiments of the present invention.

Figures 2A-F' illustrate formation of example conductive dual damascene interconnect structures in accordance with embodiments of the present invention.

Figures 3A-G' illustrate formation of example conductive dual damascene interconnect structures in accordance with other embodiments of the present invention.

Figures 4A-E" illustrate formation of example conductive dual damascene interconnect structures in accordance with other embodiments of the present invention.

Figures 5A-B each illustrate an example method for forming an interconnect or other conductive structure in accordance with an embodiment of the present invention.

Figure 6 illustrates an example computing system having one or more devices implemented with conductive structures formed in accordance with an embodiment of the present invention.

As will be appreciated, the figures are not necessarily drawn to scale or intended to limit the claimed invention to the specific configurations shown. For instance, while some figures generally indicate straight lines, right angles, and smooth surfaces, an actual implementation of a structure may have less than perfect straight lines, right angles, and some features may have

surface topology or otherwise be non-smooth, given real world limitations of the processing equipment and techniques used. In short, the figures are provided merely to show example structures.

DETAILED DESCRIPTION

Techniques are disclosed that enable interconnects, vias, metal gates, and other conductive features that can be formed through electroless material deposition techniques. In some embodiments, a layer of electroless nucleation material (ENM) and a layer of electroless suppression material (ESM) are used in conjunction to enable bottom-up fill of the feature. In some cases, the ENM is deposited first and then covered by ESM, which is then selectively etched to expose particular areas of ENM. Alternatively, the ESM can be deposited first and then be covered by ENM, which is then selectively etched and/or reflowed to expose particular areas of ESM. In still other cases, the ENM layer is an underlying or otherwise pre-existing metal layer that can be leveraged to provide desired nucleation sites. Electroless filler material (EFM) can then be deposited to fill the structure, in accordance with some embodiments. In general, the EFM nucleates on exposed ENM, but not on exposed ESM (or otherwise nucleates more slowly on the ESM than the ENM). Thus, a bottom-up electroless fill is enabled, thereby eliminating or otherwise reducing problems associated with line-of-sight trench deposition techniques.

General Overview

As previously explained, conventional interconnect processing involves barrier and copper seed layer deposition, followed by an electroplated gapfill process. The scaling of such conventional processes can be difficult because of, for instance, available real-estate and line-of-sight problems such as trench overhang of the barrier, adhesion, and seed layers, which in turn lead to pinched-off trench and via openings during plating, and inadequate gap fill.

Thus, and in accordance with one embodiment, a method for forming various conductive features, such as interconnects, trenches, dual damascene features (trench/vias), and through-vias, uses electroless fill in conjunction with high growth rate selectivity between an electroless nucleation material (ENM) and electroless suppression material (ESM) to generate bottom-up or otherwise desired fill pattern of such features. Suitable ENM may be present in the underlying or otherwise existing structure, or may be provided for the specific purpose of enabling a bottom-up or other desired fill process as described herein. An ESM is provisioned so as to prevent or otherwise inhibit nucleation at the ESM covered areas of the feature, which in turn prevents or otherwise slows down the rate of electroless growth on those areas. As such, the electroless growth rate on the ENM sites is higher than the electroless growth rate on the ESM sites. Thus, an electroless fill pattern can be customized by provisioning specific exposed areas

of ENM within a conductive feature to be filled. To generate a bottom-up fill in accordance with some embodiments of the present invention, the nucleation rate of electroless metal growth on ENM relative to ESM is greater than one.

Selectivity of ESM deposition can be achieved in a number of ways. For instance, the ESM can be blanket deposited and then etched using any number of etch techniques, including for instance, wet and/or dry etching, isotropic and/or anisotropic etching, plasma etching, laser ablation, or other suitable etch processes. Alternatively, the ESM can be selectively deposited using directional deposition, such that ESM is only provided in areas where electroless growth is undesirable. Alternatively, a mask that is naturally selective to the ESM can be deployed using standard lithography, such that the ESM will only deposit on areas not having the mask material (or the inverse situation where the ESM will only deposit on areas having the mask material). Numerous techniques for providing the ESM in the desired areas where nucleation is to be prevented or otherwise inhibited will be apparent in light of this disclosure.

The areas where nucleation is desired, and hence where exposed ENM is desired, will depend on the given application and structure. In any such cases, electroless techniques can be used to deposit electroless filler material (EFM), which will nucleate on the ENM, but not on the ESM (or at a slower rate relative to the ENM), thereby generating the desired fill pattern. In some such example embodiments, the desired fill pattern is a bottom-up fill wherein the EFM nucleates on the bottom surface of the trench or structure being filled, but not on the sidewalls, thereby eliminating or otherwise significantly reducing the occurrence of trench overhang and pinch-off conditions. In such a case, the area of the feature with exposed ENM is the bottom surface of the feature (e.g., trench or via). In a more general sense, ENM can be selectively provisioned within a feature to be filled in any manner to enable a corresponding desired fill pattern.

Consistent with another embodiment, an ESM is layered on a feature (e.g., trench or via structure) to prevent electroless growth. Suitable ENM is then selectively deposited onto the feature only in areas where electroless growth is desirable (e.g., using directional deposition techniques). Alternatively, a non-selectively deposited layer ENM can be reflowed to cause the ENM to flow to a bottom surface of the feature to be filled, to expose underlying ESM on the sidewalls of the feature. As will be appreciated, this reflow can be carried out at a temperature high enough to reflow the ENM but not high enough to reflow the ESM. In another alternative, a layer of ENM can be non-selectively deposited and then etched using any number of suitable etch techniques, including for instance, wet and/or dry etching, isotropic and/or anisotropic etching, plasma etching, laser ablation, or other suitable etch processes to expose the underlying ESM in areas where electroless growth is undesirable (e.g., sidewalls of high-aspect ratio vias

and/or trenches). Electroless techniques can then be used to deposit an EFM or multiple EFMs, which will nucleate on the ENM at a higher rate than on the ESM, generating the desired fill pattern. In some such embodiments, the desired fill pattern is a bottom-up fill wherein the EFM nucleates on the bottom surface of the trench or structure being filled faster.

Consistent with a further embodiment, multiple EFMs or multiple depositions of the same EFM can be used to fill the same feature. In some such embodiments, the second or otherwise later deposited EFM may nucleate on the previous EFM. In other such embodiments, an additional layer of ENM can be deposited on the previous EFM such that the subsequent EFM may nucleate on the additional layer of ENM. Note that additional layers of ESM can be used to facilitate processing in accordance with some such embodiments of the present invention.

Consistent with still another embodiment, the feature may only be partially filled by the EFM or EFMs and all subsequent fill can be completed, for example, by depositing a cap material directly onto the exposed EFM. The cap material can be deposited, for instance, by atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), electroplating, or electroless processes. In some such cases, a diffusion barrier layer can be interposed between the EFM and the cap material. Such a barrier layer may be desirable, for instance, to prevent the formation of a galvanic couple at the interface of differing EFM depositions.

While specific embodiments of conductive feature fabrication processes and structures provided herein include, for instance, ENM layers, ESM layers, and electroless metal fill materials, numerous material and fill-pattern schemes will be apparent in light of this disclosure and the claimed invention is not intended to be limited to conductive structures having a particular ENM-ESM-EFM scheme. In addition, various example processing techniques are provided herein (e.g., ALD, CVD, PVD, electroplating, electroless deposition, etc), but other suitable processing techniques may also be used to provide structures fabricated as described herein.

Conductive Structures

Figures 1A-1G', 2A-2F', 3A-3G', and 4A-4E'' illustrate formation of example conductive structures configured in accordance with various embodiments of the present invention. Each of these examples generally include trench or dual damascene recesses that can be used, for example, as conductive pathways, contacts, transistor gates, vias, interconnects, or other such metal features. As can be seen in these cross-section side-views, the trenches and dual damascene structures are fabricated in a dielectric layer deposited on or otherwise formed in a substrate. Other conductive structures having any number of profiles, geometries, and functions

can benefit from an embodiment of the present invention, as will be appreciated in light of this disclosure.

Any number of suitable substrates can be used to implement the substrate, including bulk substrates (e.g., silicon, germanium, III-V materials, etc), semiconductor-on-insulator substrates (XOI, where X is a semiconductor material such as silicon, germanium or germanium-enriched silicon), and multi-layered structures. In one specific example case, the substrate is a silicon bulk substrate. In other implementations, the substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, silicon germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. Further materials classified as group III-V or group IV materials may also be used to form the substrate. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which an integrated circuit having interconnects and/or conductive features may be built falls within the spirit and scope of the claimed invention.

The dielectric layer may be implemented with any suitable dielectric or insulator materials, including those commonly used in integrated circuit applications, such as oxides (e.g., silicon dioxide, carbon doped oxide), silicon nitride, or organic polymers (e.g., perfluorocyclobutane or polytetrafluoroethylene), fluorosilicate glass, and organosilicates (e.g., silsesquioxane, siloxane, or organosilicate glass). The dielectric material may be low-k or high-k depending on the desired isolation, and may include pores or other voids to further reduce its dielectric constant. Although only one trench/via structure is generally shown, the dielectric layer may include multiple such structures (such as shown in the example configuration of Figure 2A), and some embodiments may include multiple dielectric layers. The dielectric layer thickness can vary greatly, but in some example embodiments is in the range of 50 nm to 5000 nm. Numerous dielectric layer configurations can be used and the claimed invention is not intended to be limited to any particular set of material systems or geometries.

The via and/or trench can be formed in the dielectric layer, for example, using standard lithography including via and/or trench patterning and subsequent etch processes followed by planarization, polishing, cleans, or other desired processing. The patterning and etch processes can be carried out, for instance, using wet and/or dry etch techniques. The trench and via dimensions can vary, depending on the application. In some example cases, the trench opening is about 10 nm to 100 nm (e.g., 20 to 50 nm) and the via opening is about 5 nm to 50 nm (e.g., 10 to 25 nm), and the entire structure has an aspect ratio in the range of about 10:1 to 1:1 (e.g., 5:1). As will be appreciated, the via and/or trench geometry will vary from one embodiment to the next, and the claimed invention is not intended to be limited to any particular configuration.

As will be further appreciated in light of this disclosure, the structure to be filled may or may not interact with other features or structures formed in other layers of the dielectric. For instance, in the cross-section of the example integrated circuit shown in Figures 1A-1G, the trench does not conductively couple with other features above or below the trench, in that particular cross-section as illustrated. In such cases, the trench may simply be, for instance, a narrow conductive trace that runs from one point to another point on a given layer (which may be the only layer of the structure or one layer in a stack of layers), so as to electrically connect two components or other features (e.g., I/O pin, transistor electrode, capacitor electrode, etc) disposed on that layer. In contrast, in the cross-sections of the example integrated circuits shown in Figures 1G', 2A-2F', 3A-3G', and 4A-4E", the conductive feature being filled is a damascene structure that conductively couples with other features above and/or below that structure. Such a stacked via and/or trench configuration can be used, for instance, in a memory array or other multi-layer integrated circuit. One such example structure is further illustrated in Figure 2A', which generally shows a dynamic random access memory (DRAM) integrated circuit that includes a plurality of stacked interconnect layers (two shown) on top of the substrate. This DRAM circuit will be discussed in turn.

Figures 1A-G' illustrate formation of example conductive trench structures in accordance with various embodiments of the present invention. In general, the demonstrated process enables a bottom-up fill of electroless metal for trenches using diffusion barrier removal from feature bottom. Figure 1A shows formation of the trench in the dielectric layer. This can trench formation be carried out as previously explained. The trench may serve any number of functions, such as a conductive run, a gate of a field effect transistor (FET), or a contact.

Figure IB illustrates deposition of an ENM layer on the trench recess, in accordance with an embodiment of the present invention. The ENM may be a pure metal in some example embodiments, while in other example embodiments may be a doped alloy to make it amorphous in nature and thereby improve its diffusion barrier properties and adhesion to the dielectric layer. In some specific cases, the ENM layer is implemented with gold, nickel, copper, cobalt, ruthenium, tungsten, aluminum, palladium, tin, silver, cobalt boride, cobalt phosphide, nickel boride, nickel phosphide, palladium boride, palladium phosphide, ruthenium boride, ruthenium phosphide, tungsten boride, tungsten phosphide, combinations thereof, or any other suitable nucleation material is deposited using PVD, CVD, ALD, or other suitable deposition technique (e.g., electroless, electroplating), to provide a selectively located and/or continuous and conformal ENM layer. The thickness of the ENM layer can vary, and in some such embodiments is in the range of one-to-several monolayers to several hundred nanometers. In a more general sense, any ENM layer thickness sufficient for nucleation of the desired fill metal

and to promote electroless growth at a desired rate can be used, and the claimed invention is not intended to be limited by any particular range of ENM layer thicknesses or other dimensions.

As shown in Figure 1C, a layer of ESM is deposited or otherwise formed on the ENM layer. In some embodiments the ESM can be a metal or dielectric or diffusion barrier material, such as tantalum, titanium, tantalum nitride, titanium nitride, tungsten nitride, molybdenum nitride, silicon nitride, silicon dioxide, aluminum oxide, or other suitable material that will suppress or otherwise inhibit electroless metal growth on feature sidewalls or other feature areas. Just as with the ENM layer thickness, the thickness of the ESM layer can vary, and any ESM layer thickness sufficient to suppress or otherwise sufficiently inhibit ENM growth to enable a desired fill pattern can be used. An example range of ESM layer thickness is one-to-several monolayers to several hundred nanometers. The ESM can be deposited or formed in a number of ways. In some example embodiments, for example, a nitrogen (N_2), oxygen (0_2) or carbon based gas in a plasma, CVD, ALD, or thermal process is used to modify the surface of the ENM layer to effectively provide an ESM layer. In some such example cases, the modification of the ENM surface should be tunable so the bulk of the ENM is intact and conductive, while the modified ENM surface can suppress or otherwise sufficiently inhibit electroless growth. In other embodiments, an ultra-thin (e.g., one-to-several monolayers thick) layer of dielectric material such as an oxide or nitride (e.g., silicon nitride, silicon dioxide, aluminum oxide, etc) is deposited or otherwise formed on the ENM layer to provide the ESM layer. In still other embodiments, an ultra-thin (e.g., one-to-several monolayers thick) layer of conductive diffusion barrier material (e.g., tantalum, titanium, tantalum nitride, titanium nitride, tungsten nitride, molybdenum nitride, etc) is deposited by, for example, PVD, CVD or ALD on the ENM layer to provide the ESM layer. Just as with the ENM, the ESM can be chosen or otherwise configured to provide acceptable diffusion barrier properties.

After the ESM layer is provided, it can then be etched, as best shown in Figure ID. Recall, however, that in some embodiments, the ESM can be selectively deposited (e.g., directional deposition), such that no or only minimal etching would be necessary. When appropriate, the ESM can be etched using any number of etch techniques as previously explained, including for instance, wet and/or dry etching, isotropic and/or anisotropic etching, plasma etching, laser ablation, or other suitable etch processes. In one specific example embodiment, a tuned argon ion (Ar+) etch is used to remove the ESM from the field and bottom of the trench, leaving ESM only on the trench sidewalls. In a more general sense, the ESM is left in areas where electroless growth is undesirable. An example resulting structure after the etch (or selective deposition of the ESM layer) is shown in Figure IE, which shows the remaining ESM only on the trench

sidewalls. In other embodiments, ESM may be left in other locations as well, such as on the surfaces to the left and/or right of the trench, if so desired.

As shown in the example embodiment of Figure IF, EFM can be deposited to at least partially fill the trench using, for example, electroless techniques. In some example embodiments, conventional selective electroless techniques are used to deposit at least one metal such as, for example, copper, nickel, silver, gold, platinum, cobalt, tungsten, or alloys thereof such as copper-cobalt, copper-tin, cobalt phosphorous tungsten, nickel-phosphorous-tungsten, or any other suitable EFM that will nucleate on the ENM but not on the ESM (or otherwise at a slower rate than on the ENM). In the example shown in Figure IF, this will yield a bottom-up fill of the trench. The growth rate selectivity (GRS) of this EFM deposition can generally be defined as the electroless growth rate on the ENM divided by the electroless growth rate on ESM. In general, the higher the GRS, the greater the rate of bottom-up fill for the EFM. As will be appreciated, while the EFM will not nucleate and grow on the ESM layer as fast as it does on the ENM layer, there may be some marginal or otherwise negligible nucleation and growth of EFM on the ESM layer, but a bottom-up fill is still enabled. The electroless chemistry and ENM/ESM can be selected to maximize selectivity.

As will be apparent in light of this disclosure, other processes and/or alternate process sequencing may be executed in accordance with various embodiments of the present invention. One example such process is chemical-mechanical planarization (CMP) which, in some embodiments, can be used to remove excess ENM, ESM, EFM, and/or other excess materials, as shown in the example resulting structure of Figure 1G. Examples of other such additional processing include, for instance, various clean processes (e.g., to prepare exposed ENM layer for subsequent electroless deposition of EFM), and deposition of passivation layers and any necessary planarization and/or polishing, so that another layer can be formed thereon.

Figure 1G' shows an alternative embodiment of a trench structure that is filled without depositing an ENM layer into the trench. Rather, in this example case, the previously described trench etch process not only forms the trench structure in the dielectric layer, but also exposes an underlying metal at the bottom of the trench. The underlying metal may be, for example, formed earlier in the fabrication process for the specific purpose of providing a landing pad and nucleation site for the subsequent trench etch and EFM deposition process, or alternatively an existing metal structure that serves some other purpose but can also be leveraged as a nucleation site. In one specific example case, the underlying metal layer is a conductive cap (e.g., copper) from the previous metal layer, suitable for electroless metal growth. In some cases, the ESM layer deposition is selective (e.g., directional deposition), such that the deposition is only on the trench sidewalls, but not on the underlying metal or field surfaces. In other embodiments, the

deposition is non-selective and then etched accordingly, to expose the underlying metal. Note that the ESM layer could be, for example, a diffusion barrier (e.g., tantalum) that is selectively removed from bottom of trench to facilitate an electroless bottom-up metal fill as described herein. After the EFM is provided, the resulting integrated circuit structure can then be planarized and/or otherwise further processed as desired.

Figures 2A-F' illustrate formation of example conductive dual damascene interconnect structures in accordance with embodiments of the present invention. In general, the demonstrated process enables a bottom-up fill of electroless metal for dual damascene features using diffusion barrier removal from the feature bottom. Figure 2A shows the etched dual damascene recess in the dielectric layer. This etch process can be carried out as previously explained. The dual damascene feature in this example includes a trench portion and a via portion. Note that previous discussion with respect to various details and aspects of the techniques provided herein is not always repeated but is equally applicable to related aspects of other embodiments provided herein, as will be appreciated in light of this disclosure.

As can be further seen, the etch lands on an underlying metal, which as previously explained can be, for example, a conductive cap of a lower metal layer or feature, or other previously provided metal suitable for electroless metal growth. Figure 2A shows a specific example embodiment where the underlying metal landing pad is a metal line of a lower layer in a DRAM integrated circuit structure. As can be further seen, the substrate is configured with various DRAM cell components integrated therein, such as access transistor T and word line WL. Such DRAM devices typically include a plurality of bit cells, with each cell generally including a storage capacitor communicatively coupled to a bitline by way of an access transistor that is gated by a word line. Other typical DRAM components and features not shown can also be included (e.g., row and column select circuitry, sense circuitry, power select circuitry, etc). Each layer includes various metal lines (Ml, MΓ, M2, and M2') and corresponding vias (V0, VO', VI, and VI') formed within an interlayer dielectric (ILD) material. Note that the layout shown is not intended to implicate any particular feature spacing or density. Rather, this layout is simply an arbitrary example, and any number of layout designs can benefit from an embodiment of the present invention, where trenches, vias, and other interconnect or conductive features are formed as described herein. Each layer in this example structure is generally isolated or otherwise demarcated from neighboring layers by an etch stop layer. In addition, each metal line and via of this example embodiment is configured with a barrier layer, at least some of which are formed with ENM and/or ESM layers implemented as described herein to enable electroless bottom-up fill. Other embodiments may include fewer or more such layers. In this particular example case, Figures 2A and 2A' show how via VI electrically connects metal

line M2 to the underlying metal line Ml. Thus, the metal line M2 shown in Figure 2A' is the underlying metal shown in Figure 2A.

As shown in Figure 2B, a layer of ESM is deposited or otherwise formed on the dual damascene trench. The previous discussion with reference to the ESM layer in Figure 1C is equally applicable here, except that the ESM layer in this example configuration is deposited directly onto the dielectric layer. As will be appreciated in light of this disclosure, a continuous doped ENM layer may allow for better diffusion barrier properties and better adhesion to the dielectric layer. However, the ESM layer can also be deposited or otherwise formed directly on the dielectric layer, and then etched (if necessary) to expose the underlying metal, as best shown in Figure 2C. The previous discussion with respect to etching of the ESM layer (e.g., Ar ion etch or some other plasma/chemical etch technique) is equally applicable here. Note that not only is the underlying metal exposed at the feature via bottom, but also the flats of the trench portion, thereby exposing the dielectric layer in those areas.

As shown in the example embodiment of Figure 2D, EFM can then be deposited to at least partially fill the via portion. In addition, the same or a different EFM can then be deposited to fill the trench portion using the same or different deposition technique (e.g., electroless, etc), as best shown in Figure 2E. The previous discussion with reference to provisioning the EFM as well as the GRS is equally applicable here. However, in such cases where there is exposed trench surface (dielectric layer), dopants can be used in the EFM to assist in forming a strong metal-dielectric interface. For example, assuming the dielectric layer is an oxide such as silicon dioxide, the EFM (e.g., copper alloy) deposited in the trench portion can be doped with, for example, antimony, silver, or other dopant that will react with the exposed oxide dielectric in the flat to form a strong metal-oxide interface. Other dopant and adhesion promotion techniques can be used as well, as will be appreciated in light of this disclosure. After the EFM is provisioned, the resulting structure can be planarized/polished, as previously described with reference to Figure 1G (e.g., using CMP), and as best shown in Figure 2F.

In some example embodiments where a subsequent EFM is deposited on a first layer of EFM, the subsequent EFM deposition can be made using the same EFM used in the first deposition or an additional suitable EFM material can be used, as previously indicated. In such embodiments the subsequent EFM or EFMs may nucleate directly on the previous layer of EFM as shown in Figures 2E and 2F, or a layer of ENM can be interposed between two EFM layers as shown in Figures 2E' and 2F'. As further shown in Figures 2E' and 2F', an additional layer of ESM can also be used to facilitate processing. In cases where these additional ENM and ESM layers are used such as, for example, ESM Layer 1 and ESM Layer 2, depicted in Figures 2E' and 2F', the materials chosen for each layer may be independently selected for each layer.

Accordingly, materials used for ENM and ESM layers may, for example, be the same throughout the structure or each may be comprised of a different material. The structure shown in Figure 2F' is the planarized version of the structure shown in Figure 2E'.

Figures 3A-G' illustrate formation of example conductive dual damascene interconnect structures in accordance with other embodiments of the present invention. As will be appreciated, these example structures are similar to those of Figures 2A-2F', except that an ENM layer is provided on the trench/via recess and flats. Other various distinctions will now be discussed in turn.

Metal Cap

Figure 3A shows formation of the etched dual damascene recess in the dielectric layer, which can be carried out as previously explained. As can be further seen, the etch lands on an underlying metal cap layer in this example embodiment, which is in turn disposed on an underlying EFM layer. In addition, underlying ENM and ESM layers are shown. Such an integrated circuit structure may be, for example, similar to the memory circuit shown in Figure 2A.

Figure 3B illustrates deposition of an ENM layer on the dual damascene recess, in accordance with an embodiment of the present invention. The previous discussion with respect to the ENM layer of Figure 1B and the various ENM deposition processes is equally applicable here. As best shown in Figures 3C and 3D, a layer of ESM is deposited or otherwise formed on the ENM layer, and then etched so that the ESM is removed from the via bottom and trench flats. The previous discussion with reference to provisioning and etching the ESM layer (such as with reference to Figures 1C-D and 2B-C) is equally applicable here.

As shown in the example embodiment of Figure 3E, EFM can then be deposited to fill the via portion and at least part of the trench portion of the dual damascene recess. The previous discussion with reference to provisioning the EFM (such as that discussion with reference to Figures 1F and 2E-E') is equally applicable here, but in this example embodiment, the electroless fill process is stopped before it completely finishes filling the trench.

As shown in Figure 3F, a layer of cap material can then be deposited on the EFM using, for example, PVD, CVD, ALD, electroplating, electroless deposition, or other suitable deposition technique. Such a capping layer can be used, for instance, to improve conductivity, process integration and/or to minimize the possibility of galvanic corrosion. In some example embodiments, the cap material can be, for instance, copper, cobalt, nickel, titanium, tantalum, ruthenium, palladium, silver, tungsten, alloys and combinations thereof, or any other suitable cap material that will provide the desired performance (e.g., conductivity, tune resistance, corrosion resistance, reliability, ease of polish, etc). Any cap material layer thickness can be used with

various embodiments of the present invention and the thickness may vary widely. Figure 3G illustrates the resulting integrated circuit structure after planarization, which can be implemented as previously explained, to remove excess cap material, etc.

To further reduce the risk of galvanic corrosion, a diffusion barrier layer may be disposed between the EFM and the cap material as best illustrated in Figure 3F'. In some such embodiments, the diffusion barrier can be, for example, tantalum, tantalum nitride, titanium, titanium nitride, ruthenium, cobalt, nickel, any alloy or combination thereof, or any other suitable material for forming a diffusion barrier capable of reducing a risk of galvanic corrosion. In one specific example case, where copper is used for the cap material and galvanic corrosion becomes a concern due to electroless metal/cap, an ultra-thin ALD (or CVD/PVD) diffusion barrier could be used, having a thickness of, for instance, one-to-several monolayers. In a more general sense, the thickness of the capping material layer can be optimized to, for example, reduce process and consumables costs and defect performance, and improve reliability. The structure shown in Figure 3G' is the planarized version of the structure shown in Figure 3F'.

ENM Reflow Process

Figures 4A-E" illustrate formation of example conductive dual damascene interconnect structures in accordance with other embodiments of the present invention. In this example case, bottom-up fill of EFM for the conductive structure is enabled by an ENM layer formed on the bottom of the feature using a reflow process. Similar principles and techniques previously described herein equally apply, with certain distinctions specific to this embodiment noted in turn.

Figure 4A shows formation of the etched dual damascene recess in the dielectric layer, which can be carried out as previously explained. As can be further seen, the etch lands on an underlying metal cap layer in this example embodiment, and as discussed with reference to Figure 3A.

Figure 4B illustrates conformal deposition of an ESM layer on the dual damascene recess, in accordance with an embodiment of the present invention. The previous discussion with reference to provisioning ESM layer (such as with reference to Figures 1C, 2B, and 3C) is equally applicable here. Note in this specific example case that the ESM layer is formed directly on the recess in the dielectric layer, and is not etched to expose any underlying ENM layer.

Figure 4C illustrates deposition of an ENM layer on the ESM layer, in accordance with an embodiment of the present invention. The previous discussion with respect to provisioning the ENM layer (such as with reference to Figures 1B and 3B) is equally applicable here. In one specific such example case, a thin layer (e.g., one-to-several monolayers to 100 nm) of ENM having a low melting point (e.g., gold, nickel, copper, cobalt, aluminum, palladium, tin, or other

suitably low melting point nucleation material) is provisioned through ALD, CVD or PVD deposition (other deposition techniques, such as electroless or electroplating can used if so desired, as will be appreciated). In some such cases, this deposition can be done with low bias to maximize the amount of material at the feature bottom and minimize the amount of material on the feature sidewall. As will be appreciated in light of this disclosure, the melting point of the ENM must be lower than the melting point of the ESM layer.

Figure 4D illustrates the resulting structure after heating the structure to reflow the ENM, thereby causing any ENM on the feature sidewalls to move or otherwise flow to the feature bottom. In one such embodiment, the goal is to maximize the amount of ENM at the feature bottom and eliminate the ENM on the feature sidewalls, so as to expose the underlying ESM (which can be any provisioned barrier layer) on the feature sidewall. In one specific example case, the ENM layer is implemented with PVD copper ENM, but any number of materials and deposition systems can be used. The copper ENM layer reflow temperatures are in the range of about 75°C to 450°C, in some such cases. As will be appreciated, other ENM layer materials may have different reflow temperature ranges. Note that the reflow can be done, for example, during the ENM layer deposition or after the ENM layer deposition. If residual ENM resides on the field post-reflow, and such residual ENM is undesired, note that subsequent processing can remove that residual material. For example, after reflow, the feature can be filled with a dielectric, for instance. Subsequent processing can then be used to remove the dielectric and residual ENM in the field, such as a CMP process. The dielectric could then be removed from the feature, during subsequent processing steps.

The rest of the fabrication process can proceed as previously described, with EFM deposition and planarization, as best shown in Figure 4E. An alternative embodiment shown in Figure 4E' uses a similar formation process, but is configured with a cap material layer (such as discussed with reference to Figures 3F-3G). Another alternative embodiment shown in Figure 4E" uses a similar formation process, but is configured with a diffusion barrier between the cap material layer and the EFM (such as discussed with reference to Figures 3F'-3G').

A number of observations will be apparent in light of this disclosure. For instance, and in accordance with some specific embodiments of the present invention, the cap material layer can be configured with a low aspect ratio to fill, thereby allowing for an all PVD cap deposition (no electroplating needed). In addition, the techniques provided are not limited to dual damascene structures. For instance, the techniques can also be used for high aspect ratio through-semiconductor vias as well.

Electroless Grow Rate Selectivity

Figure 5A x-ray diffraction (XRD) micrograph of electroless metal growth on an example substrate having a high electroless growth rate (ENM layer) compared to an example substrate having a low electroless growth rate electroless (ESM layer). In particular, the graph shows electroless copper (Cu) growth on 50A PVD copper substrate and on a tantalum nitride (TaN) substrate. As can be seen, Cu (111) peak is observed even for 1 minute deposition, and becomes progressively greater as time goes on, showing a significant electroless copper growth rate on the copper substrate. In contrast, no or negligible Cu (200) peak was observed on the tantalum nitride substrate up to 8 minutes as shown (and continuing up to 20 minutes) of electroless copper deposition. Figure 5B further illustrates the comparison of the electroless growth rates of the example EFM (Cu) on the example ENM (Cu) and ESM (TaN) layers. As can be seen, the electroless copper thickness as a function of deposition time on 50A PVD Cu and TaN substrates is substantially different, as early in the electroless deposition as around 60 seconds, and reaches a difference of about 240 angstroms (A) after 480 seconds. This growth rate trend continues with further deposition time.

Example System

Figure 6 illustrates a computing system 1000 implemented with one or more interconnect or other conductive structures configured in accordance with an example embodiment of the present invention. As can be seen, the computing system 1000 houses a motherboard 1002. The motherboard 1002 may include a number of components, including but not limited to a processor 1004 and at least one communication chip 1006, each of which can be physically and electrically coupled to the motherboard 1002, or otherwise integrated therein. As will be appreciated, the motherboard 1002 may be, for example, any printed circuit board, whether a main board or a daughterboard mounted on a main board or the only board of device 1000, etc. Depending on its applications, computing system 1000 may include one or more other components that may or may not be physically and electrically coupled to the motherboard 1002. These other components may include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). Any of the components included in computing system 1000 may include one or more conductive structures as described herein (e.g., having a metal gate, conductive run, trench, via, dual damascene, and/or other structure or feature implemented with ENM and ESM having different electroless growth rates). These conductive structures can be used, for instance, to implement an on-board processor cache

or memory array or a transistor circuit. In some embodiments, multiple functions can be integrated into one or more chips having one or more interconnect structures (e.g., for instance, note that the communication chip 1006 can be part of or otherwise integrated into the processor 1004).

The communication chip 1006 enables wireless communications for the transfer of data to and from the computing system 1000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.1 1 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing system 1000 may include a plurality of communication chips 1006. For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 1004 of the computing system 1000 includes an integrated circuit die packaged within the processor 1004. In some embodiments of the present invention, the integrated circuit die of the processor includes onboard memory circuitry that is implemented with one or more conductive structures having a trench, via, dual damascene, and/or other structure, as variously described herein. The term "processor" may refer to any device or portion of a device that processes, for instance, electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1006 may also include an integrated circuit die packaged within the communication chip 1006. In accordance with some such example embodiments, the integrated circuit die of the communication chip includes one or more conductive structures as described herein (e.g., metal gates or conductive runs, trenches, dual damascene interconnects, etc). As will be appreciated in light of this disclosure, note that multi-standard wireless capability may be integrated directly into the processor 1004 (e.g., where functionality of any chips 1006 is integrated into processor 1004, rather than having separate communication chips). Further note that processor 1004 may be a chip set having such wireless capability. In short, any

number of processor 1004 and/or communication chips 1006 can be used. Likewise, any one chip or chip set can have multiple functions integrated therein.

In various implementations, the computing system 1000 may be a laptop, a netbook, a notebook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the device 1000 may be any other electronic device that processes data or employs one or more integrated circuits having conductive structures as described herein.

Numerous embodiments will be apparent, and features described herein can be combined in any number of configurations. One example embodiment of the present invention provides a semiconductor device. The device comprises a dielectric layer configured with a recess having sidewalls and a bottom area. The device further includes electroless nucleation material at the bottom area of the recess, and electroless suppression material on the sidewalls of the recess but not covering the bottom area of the recess. The device further includes an electroless fill metal disposed in the recess on the electroless nucleation material and the electroless suppression material. In some cases, the device includes a metal cap over the electroless fill metal. In one such case, the device further includes a diffusion barrier between the metal cap and the electroless fill metal. In some cases, the electroless nucleation material is deposited into the recess. In one such case, the electroless nucleation material is reflowed to the trench bottom area after deposition. In some other cases, the electroless nucleation material is underneath the trench. In some cases, each of the electroless nucleation material (ENM) and electroless suppression material (ESM) has an electroless growth rate, and the ratio of ENM growth rate / ESM growth rate is greater than 1. In some cases, the electroless nucleation material comprises a pure metal or a doped alloy, and the electroless suppression material comprises a diffusion barrier material. In some cases, the electroless nucleation material comprises copper, and the electroless suppression material comprises tantalum. In some cases, the electroless fill metal comprises a plurality of electroless fill metals. Numerous other suitable materials will be apparent in light of this disclosure. In some cases, the trench is configured as at least one of an interconnect, trench, dual damascene feature, via, conductive run, and/or metal gate. Numerous variations and configurations will be apparent in light of this disclosure. For instance, another embodiment of the present invention provides an electronic system comprising a printed circuit board having one or more semiconductor devices as defined in any of the preceding claims. In some cases, the one or more semiconductor devices comprise at least one of a communication chip and/or a processor. In some cases, the system is a computing system.

Another embodiment of the present invention provides a semiconductor device. The device includes a dielectric layer configured with a plurality of recesses each having sidewalls and a bottom area. The device further includes electroless nucleation material at the bottom area of each recess, and electroless suppression material on the sidewalls of each recess but not covering the bottom area of each recess. The device further includes electroless fill metal disposed in each recess on the electroless nucleation material and the electroless suppression material. Each of the electroless nucleation material (ENM) and electroless suppression material (ESM) has an electroless growth rate, and the ratio of ENM growth rate / ESM growth rate is greater than 1. In some cases, the device further includes a metal cap over the electroless fill metal of each recess. In some such cases, the device may further include a diffusion barrier between each metal cap and the electroless fill metal. In some cases, the electroless nucleation material is underneath at least one of the recesses (as opposed to being formed in the recess).

Another embodiment of the present invention provides a method for forming a semiconductor device. The method includes providing a dielectric layer configured with a recess having sidewalls and a bottom area. The method further includes providing electroless nucleation material at the bottom area of the recess, and providing electroless suppression material on the sidewalls of the recess but not covering the bottom area of the recess. The method further includes providing, by electroless deposition, electroless fill metal disposed in the recess on the electroless nucleation material and the electroless suppression material. In some cases, the method further includes providing a metal cap over the electroless fill metal. In some such cases, the method further includes providing a diffusion barrier between the metal cap and the electroless fill metal. In some cases, providing the electroless nucleation material at the bottom area of the recess is a deposition process. In one such case, providing the electroless nucleation material at the bottom area of the recess the electroless nucleation material comprises reflowing the electroless nucleation material to the recess bottom area after deposition. In some cases, providing the electroless nucleation material at the bottom area of the recess includes etching the recess to expose electroless nucleation material underneath the recess (such as when the recess itself it being etched). In some cases, each of the electroless nucleation material (ENM) and electroless suppression material (ESM) has an electroless growth rate, and the ratio of ENM growth rate / ESM growth rate is greater than 1. In some cases, the electroless nucleation material comprises a pure metal or a doped alloy, and the electroless suppression material comprises a diffusion barrier material.

The foregoing description of example embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light

of this disclosure. For instance, while an electroless deposition process is used to provide the EFM, other layers including the ESM, ENM, diffusion barrier, and/or cap layers may be provided by any suitable deposition technique (e.g., PVD, CVD, ALD, electroplating, electroless deposition, or other suitable deposition technique). In this sense, the terms 'electroless nucleation material' (or 'ENM') and 'electroless suppression material' (or 'ESM') are not intended to be limited electroless deposition techniques. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a dielectric layer configured with a recess having sidewalls and a bottom area;

electroless nucleation material at the bottom area of the recess;

electroless suppression material on the sidewalls of the recess but not covering the bottom area of the recess; and

electroless fill metal disposed in the recess on the electroless nucleation material and the electroless suppression material.

2. The device of claim 1 further comprising:

a metal cap over the electroless fill metal.

3. The device of claim 2 further comprising:

a diffusion barrier between the metal cap and the electroless fill metal.

4. The device of any of claims 1 through 3 wherein the electroless nucleation material is deposited into the recess.

5. The device of claim 4 wherein the electroless nucleation material is reflowed to the recess bottom area after deposition.

6. The device of any of claims 1 through 3 wherein the electroless nucleation material is underneath the recess.

7. The device of any of the preceding claims wherein each of the electroless nucleation material (ENM) and electroless suppression material (ESM) has an electroless growth rate, and the ratio of ENM growth rate / ESM growth rate is greater than 1.

8. The device of any of the preceding claims wherein the electroless nucleation material comprises a pure metal or a doped alloy, and the electroless suppression material comprises a diffusion barrier material.

9. The device of any of the preceding claims wherein the electroless nucleation material comprises copper, and the electroless suppression material comprises tantalum.

10. The device of any of the preceding claims wherein the recess is configured as at least one of an interconnect, trench, dual damascene feature, via, conductive run, and/or metal gate.

11. The device of any of the preceding claims wherein the electroless fill metal comprises a plurality of electroless fill metals.

12. An electronic system comprising:

a printed circuit board having one or more semiconductor devices as defined in any of the preceding claims.

13. The electronic system of claim 12 wherein the one or more semiconductor devices comprise at least one of a communication chip and/or a processor.

14. The electronic system of claims 12 or 13 wherein the system is a computing system.

15. A semiconductor device, comprising:

a dielectric layer configured with a plurality of recesses each having sidewalls and a bottom area;

electroless nucleation material at the bottom area of each recess;

electroless suppression material on the sidewalls of each recess but not covering the bottom area of each recess; and

electroless fill metal disposed in each recess on the electroless nucleation material and the electroless suppression material;

wherein each of the electroless nucleation material (ENM) and electroless suppression material (ESM) has an electroless growth rate, and the ratio of ENM growth rate / ESM growth rate is greater than 1.

16. The device of claim 15 further comprising at least one of:

a metal cap over the electroless fill metal of each recess; and

a diffusion barrier between each metal cap and the electroless fill metal.

17. The device of any of claims 14 through 16 wherein the electroless nucleation material is underneath at least one of the recesses.

18. A method for forming a semiconductor device, comprising:

providing a dielectric layer configured with a recess having sidewalls and a bottom area;

providing electroless nucleation material at the bottom area of the recess;

providing electroless suppression material on the sidewalls of the recess but not covering the bottom area of the recess; and

providing, by electroless deposition, electroless fill metal disposed in the recess on the electroless nucleation material and the electroless suppression material.

19. The method of claim 18 further comprising:

providing a metal cap over the electroless fill metal.

20. The method of claim 19 further comprising:

providing a diffusion barrier between the metal cap and the electroless fill metal.

21. The method of any of claims 18 through 20 wherein providing the electroless nucleation material at the bottom area of the recess is a deposition process.

22. The method of claim 21 wherein providing the electroless nucleation material at the bottom area of the recess the electroless nucleation material comprises reflowing the electroless nucleation material to the recess bottom area after deposition.

23. The method of any of claims 18 through 20 wherein providing the electroless nucleation material at the bottom area of the recess comprises etching the recess to expose electroless nucleation material underneath the recess.

24. The method of any of claims 18 through 23 wherein each of the electroless nucleation material (ENM) and electroless suppression material (ESM) has an electroless growth rate, and the ratio of ENM growth rate / ESM growth rate is greater than 1.

25. The method of any of claims 18 through 24 wherein the electroless nucleation material comprises a pure metal or a doped alloy, and the electroless suppression material comprises a diffusion barrier material.

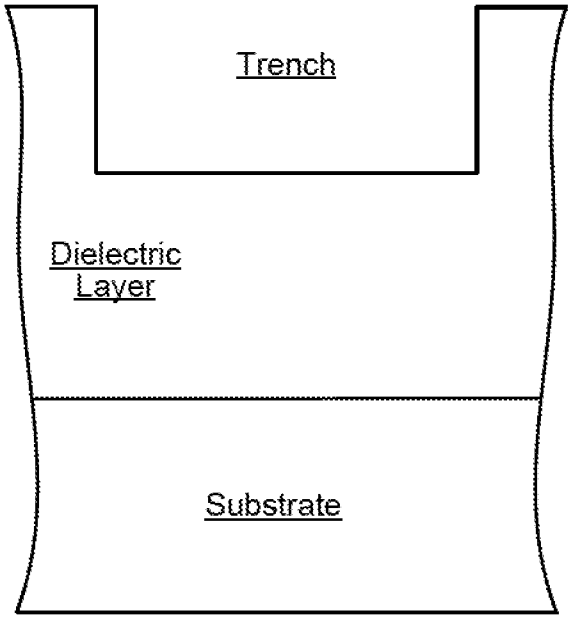


Fig. 1A

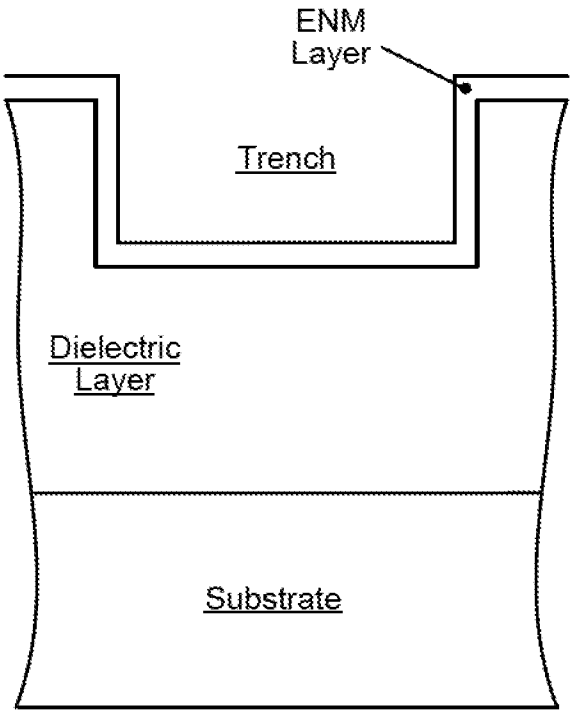


Fig. 1B

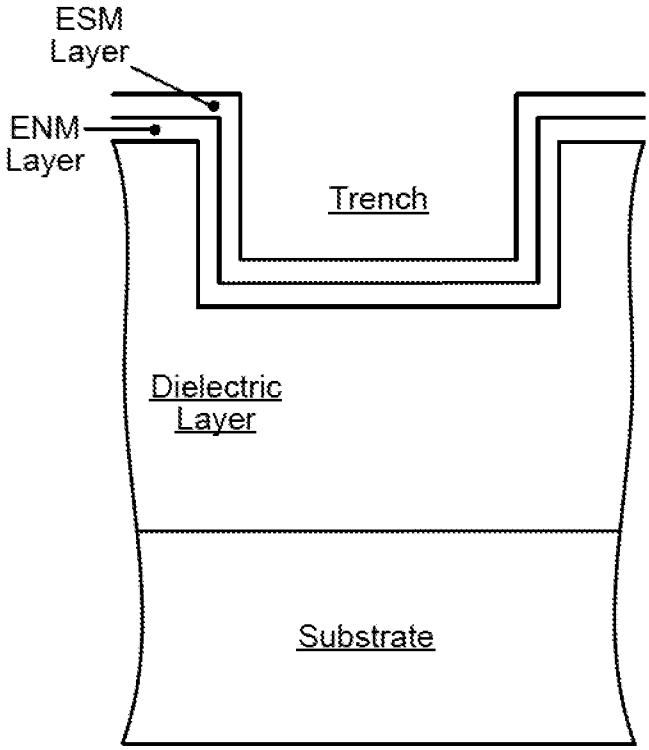


Fig. 1C

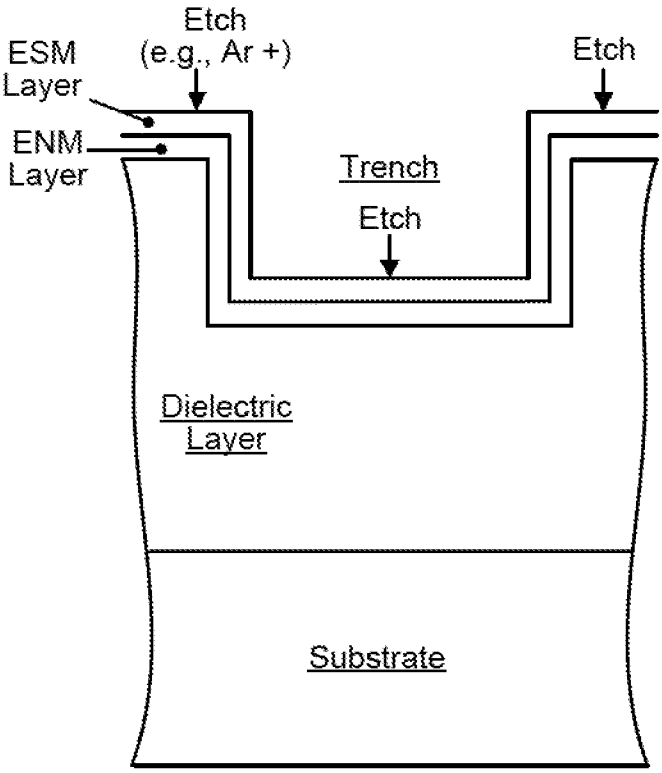


Fig. 1D

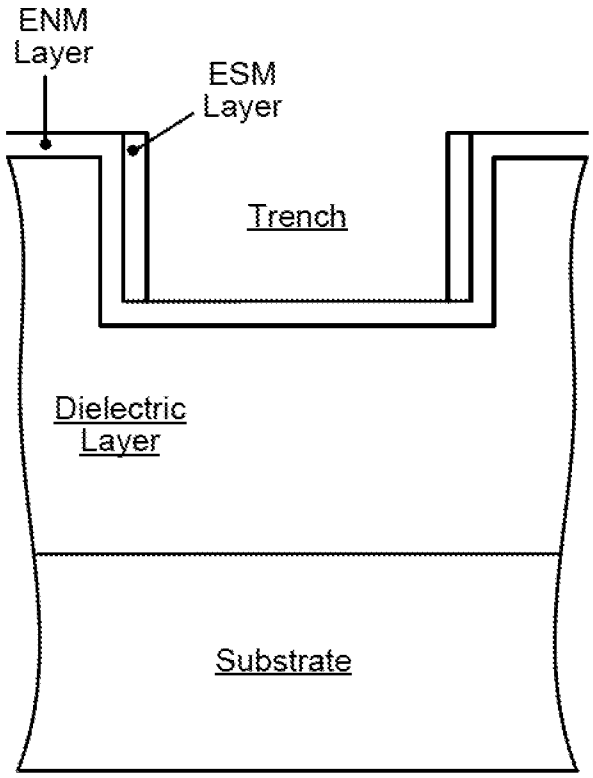


Fig. 1E

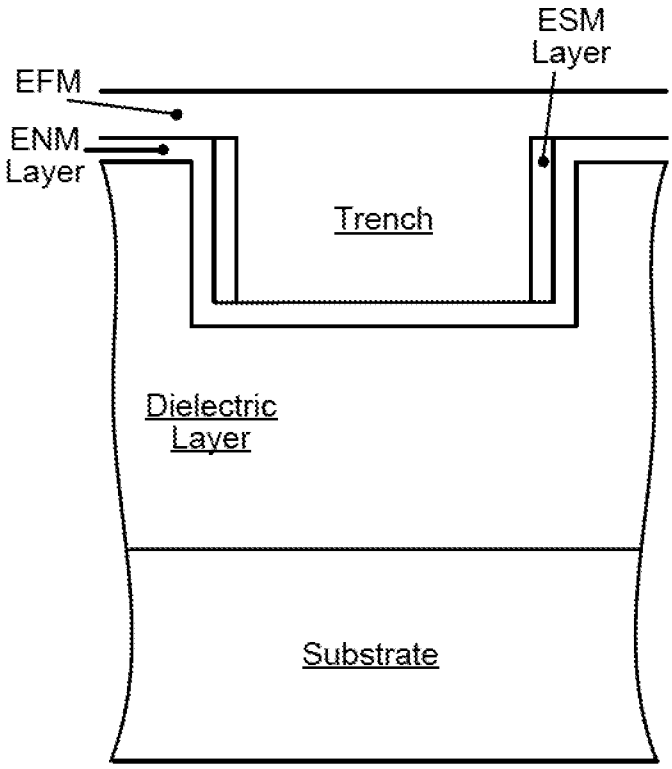


Fig. 1F

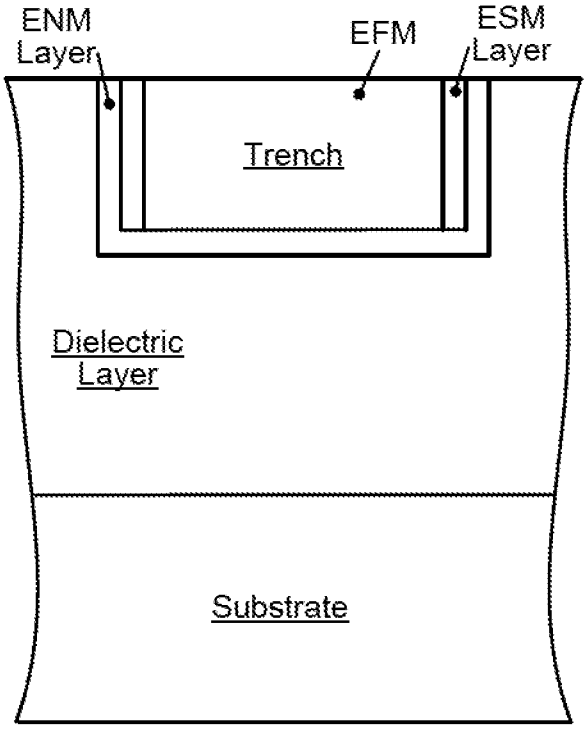


Fig. 1G

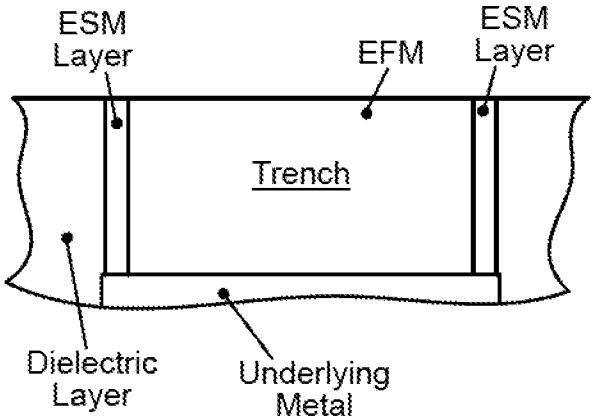


Fig. 1G'

Fig. 2A

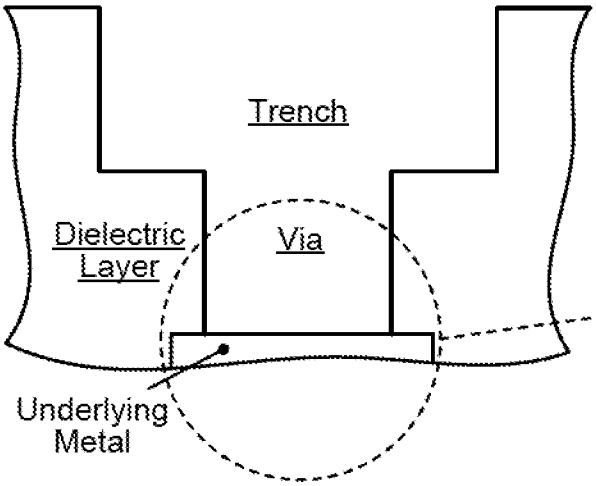


Fig. 2A'

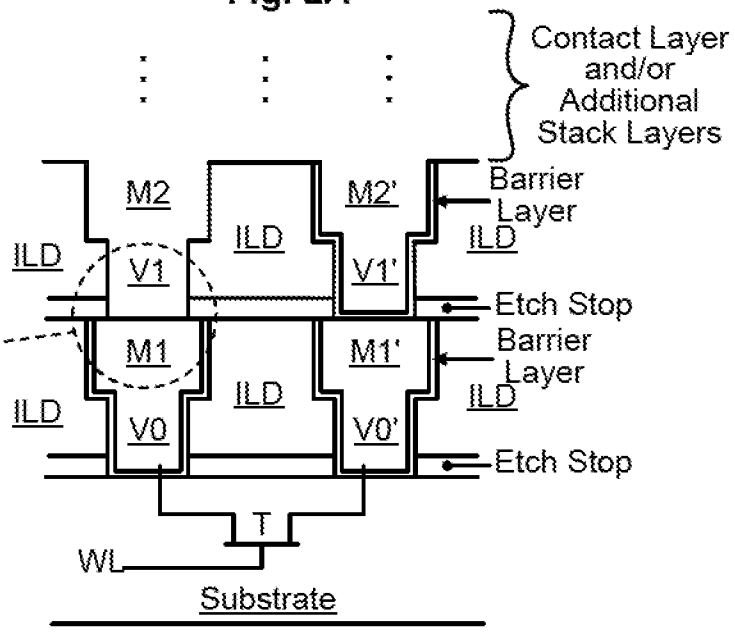


Fig. 2B

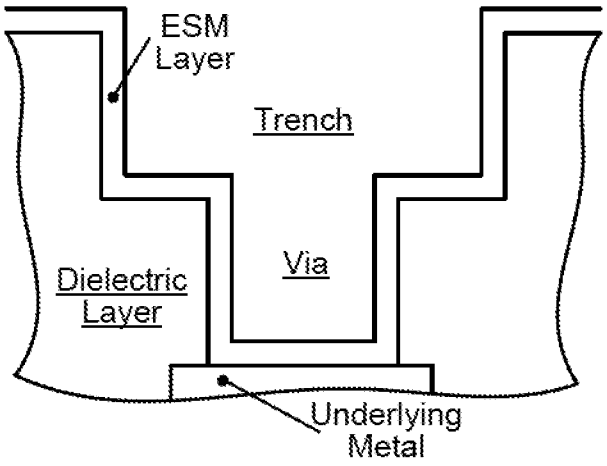


Fig. 2C

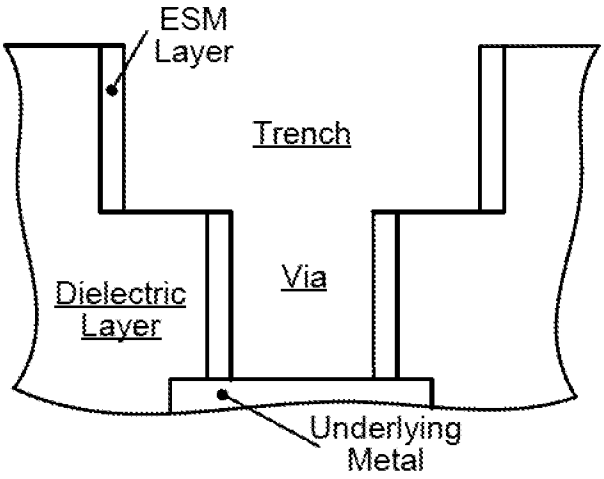


Fig. 2D

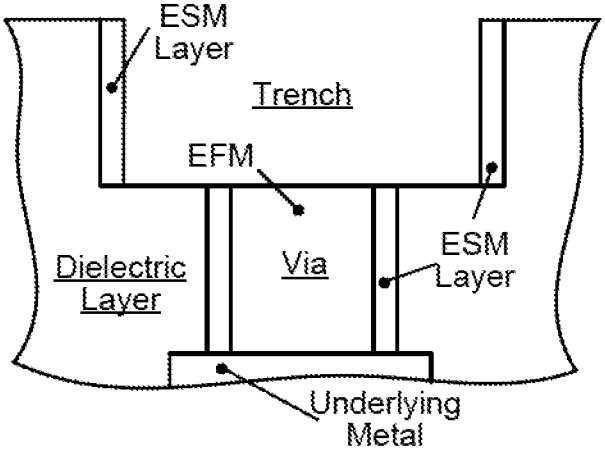


Fig. 2E

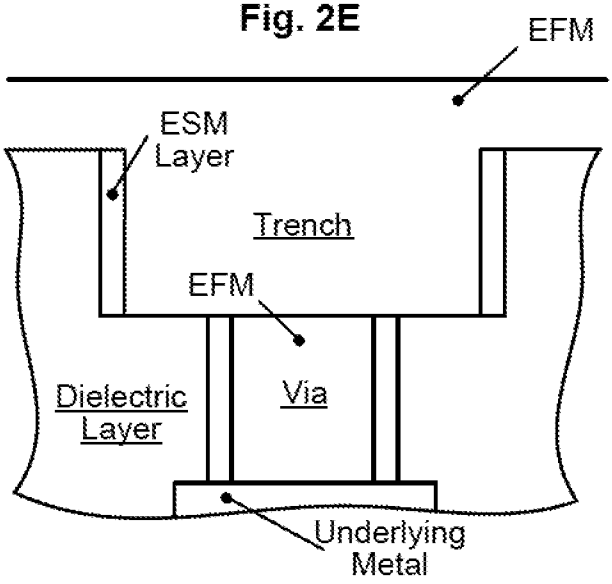


Fig. 2E'

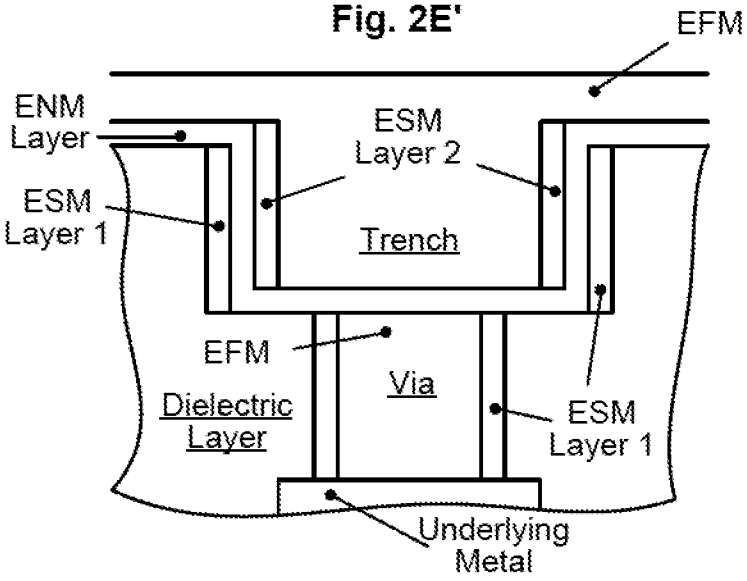


Fig. 2F

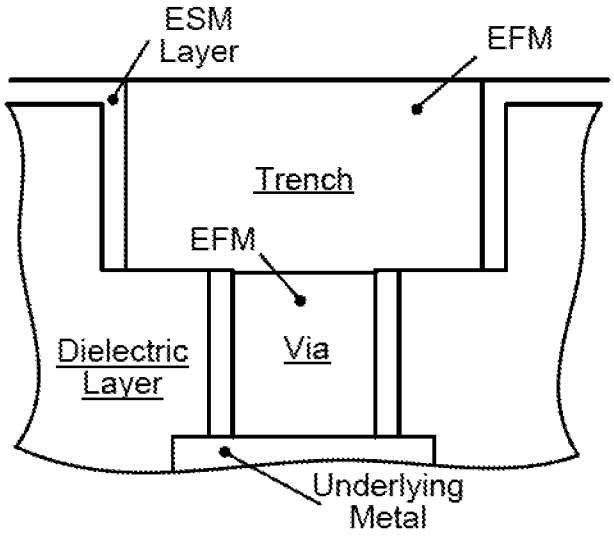


Fig. 2F'

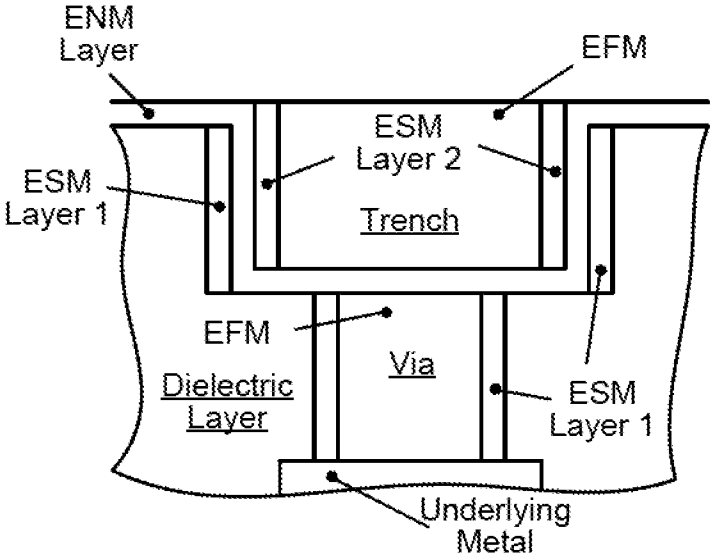


Fig. 3A

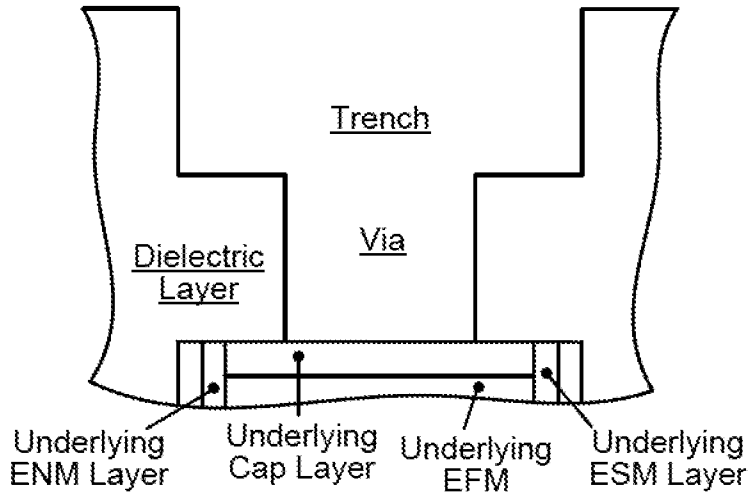


Fig. 3B

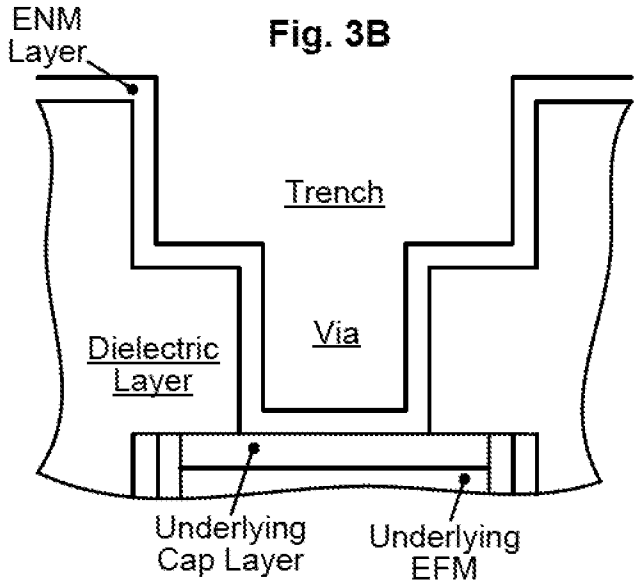


Fig. 3C

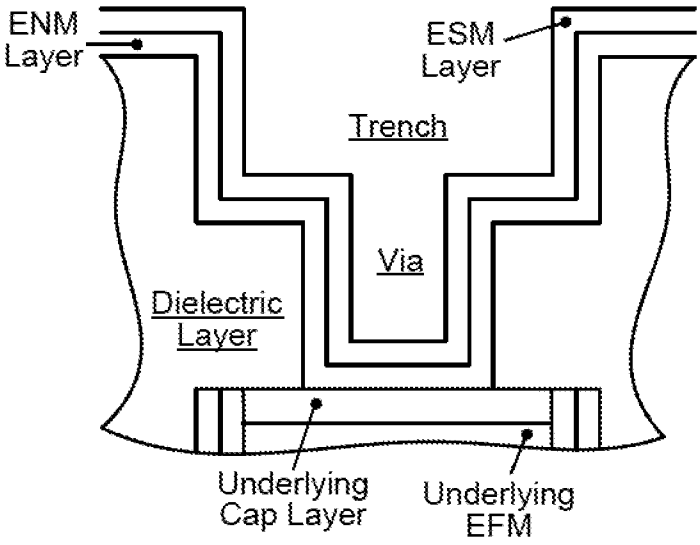


Fig. 3D

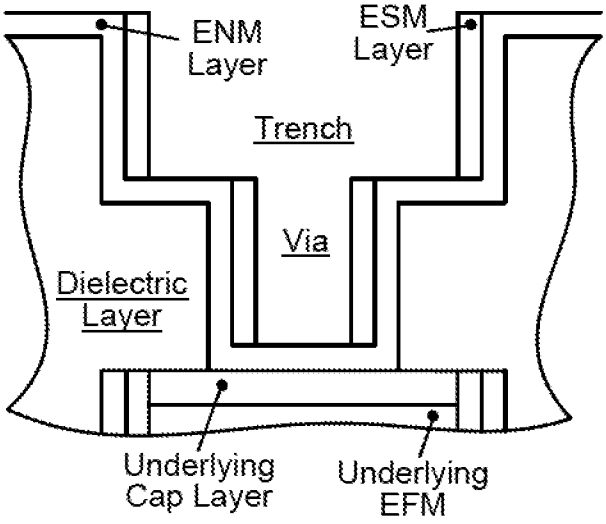


Fig. 3E

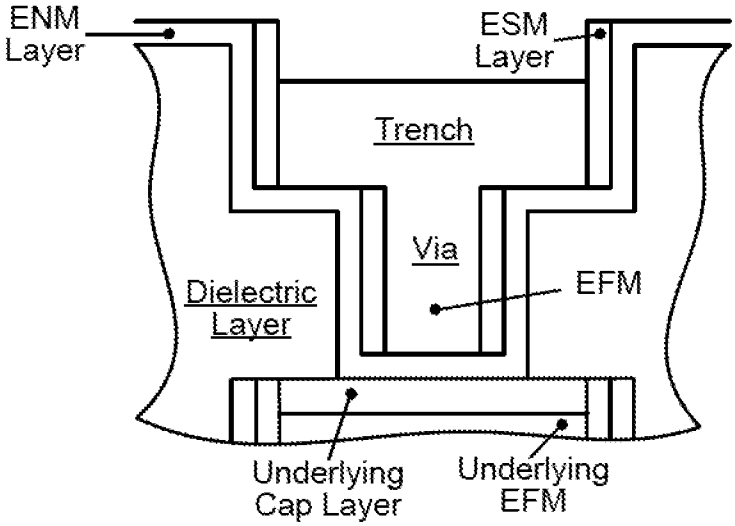


Fig. 3F

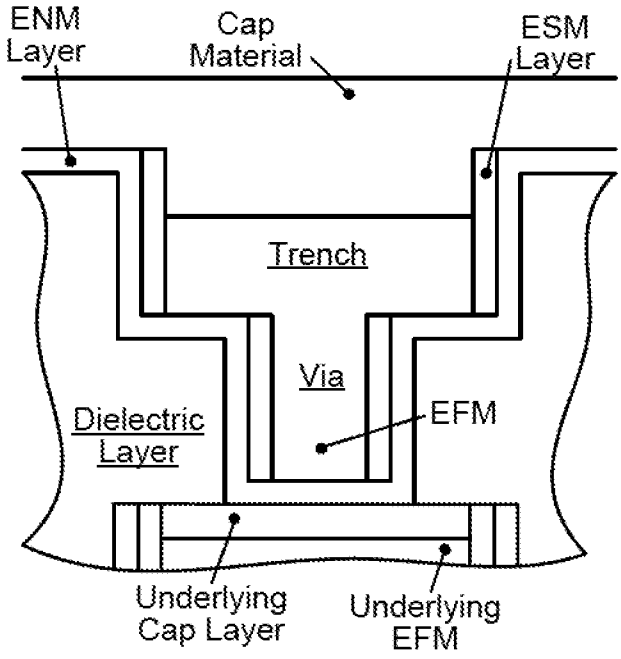


Fig. 3F'

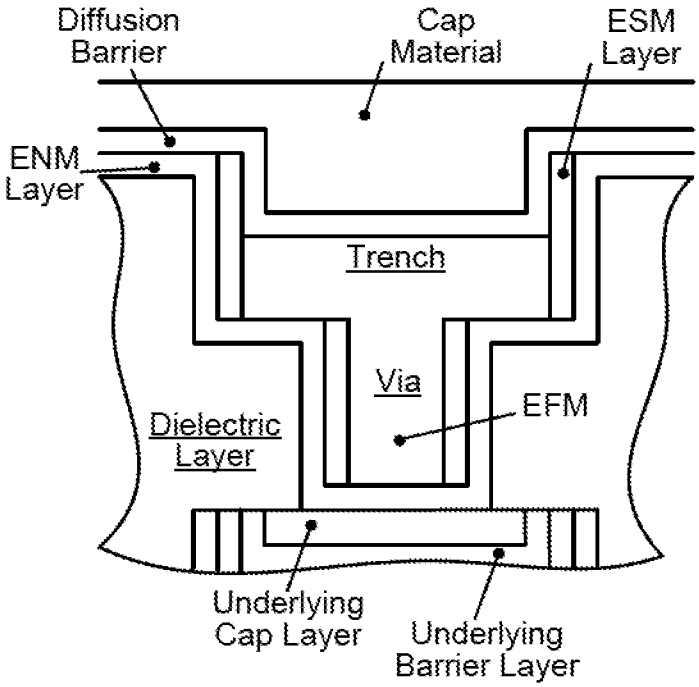


Fig. 3G

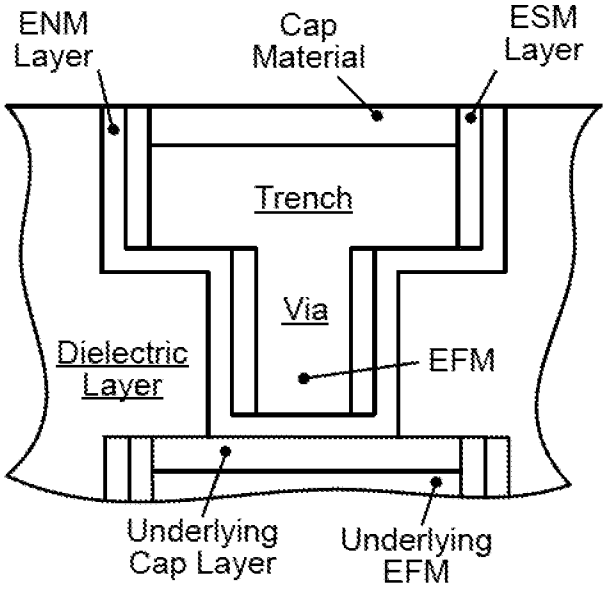


Fig. 3G'

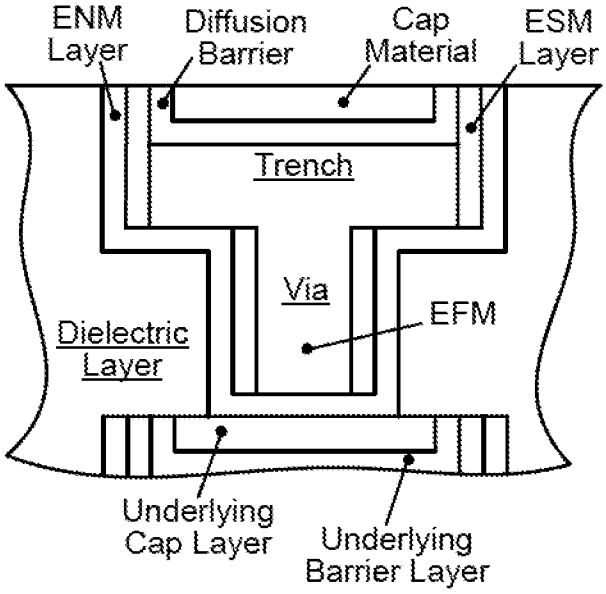


Fig. 4A

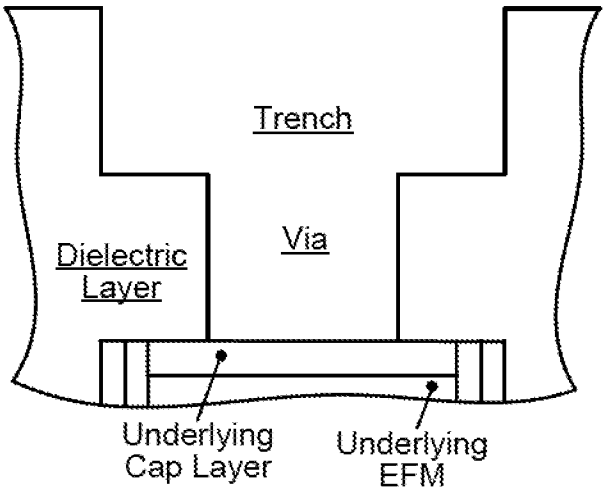


Fig. 4B

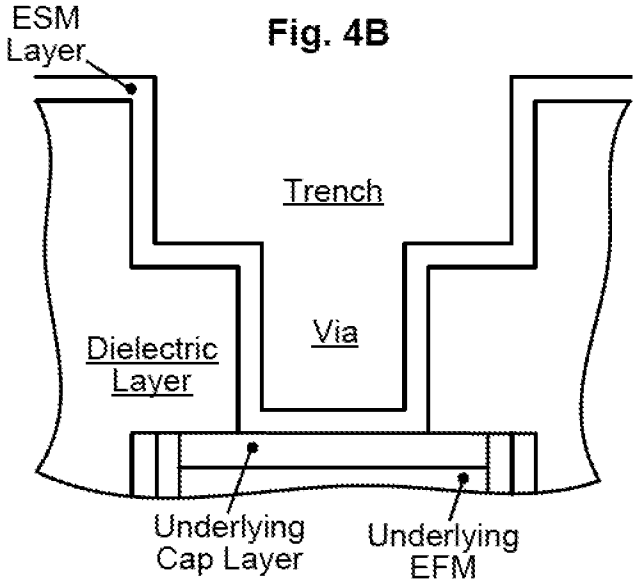


Fig. 4C

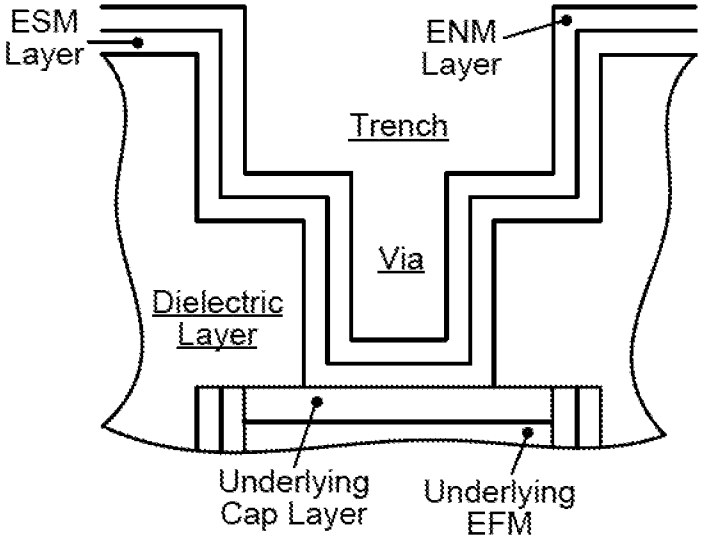


Fig. 4D

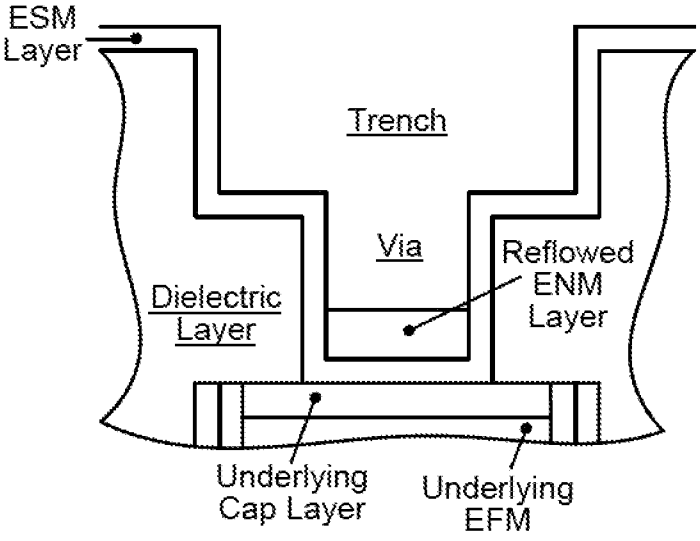


Fig. 4E

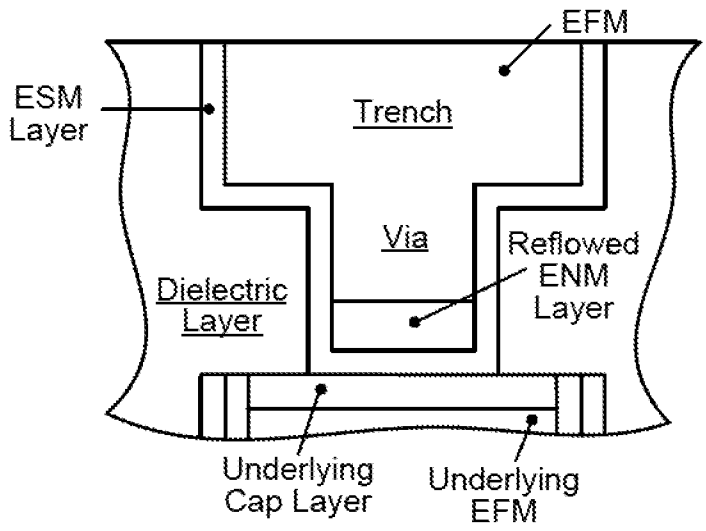


Fig. 4E'

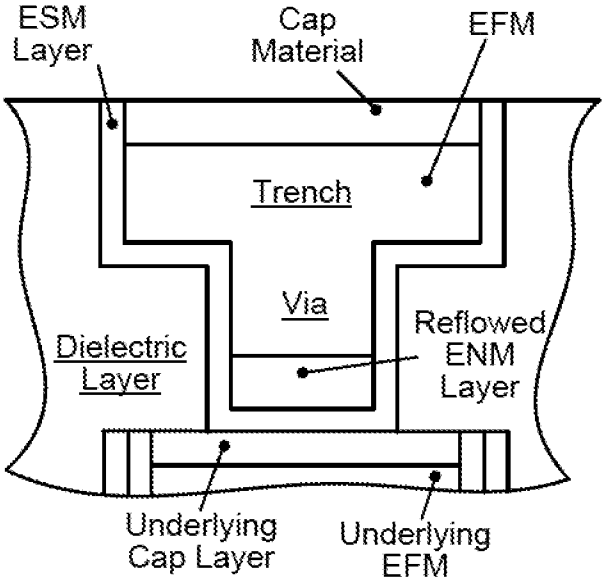
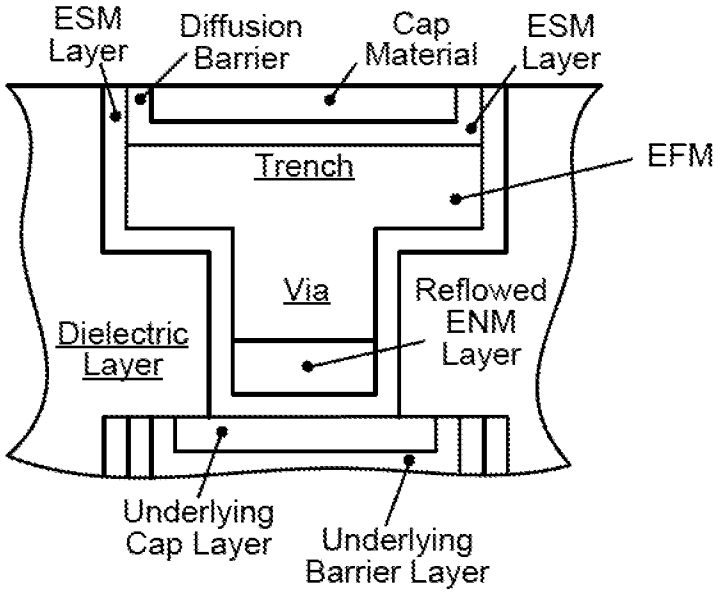


Fig. 4E''



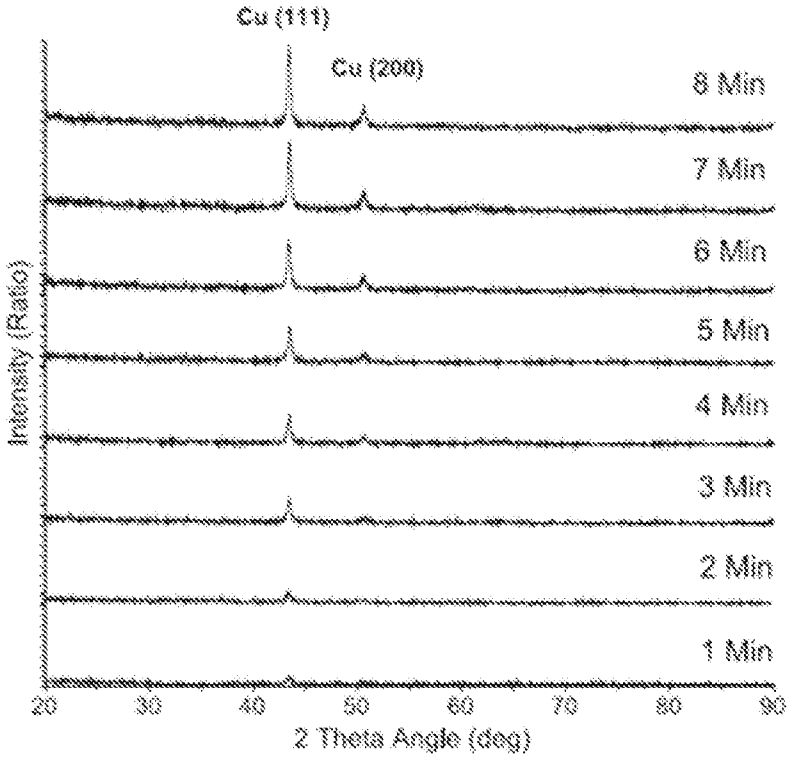

Cu (111)
Cu (200)
8 Min
7 Min
6 Min
5 Min
4 Min
3 Min
2 Min
1 Min
Intensity (Ratio)
20
30
40
50
60
70
80
90
2 Theta Angle (deg)

Fig. 5A

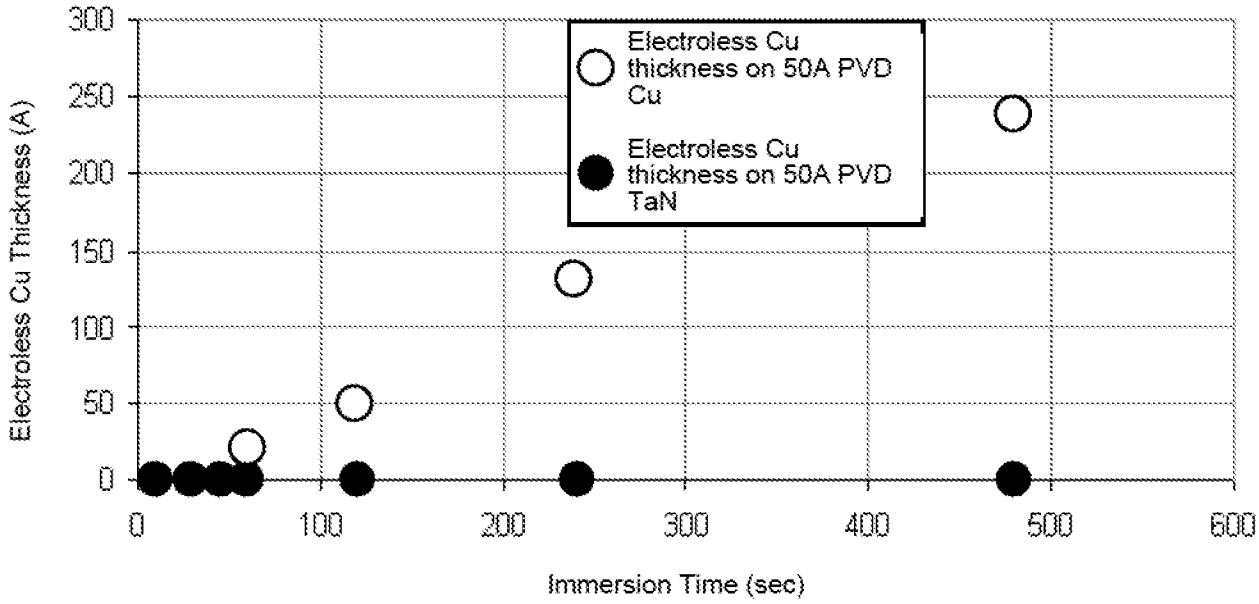

Electroless Cu thickness on 50A PVD Cu
Electroless Cu thickness on 50A PVD TaN
Electroless Cu Thickness (A)
300
250
200
150
100
50
0
0
100
200
300
400
500
600
Immersion Time (sec)

Fig. 5B

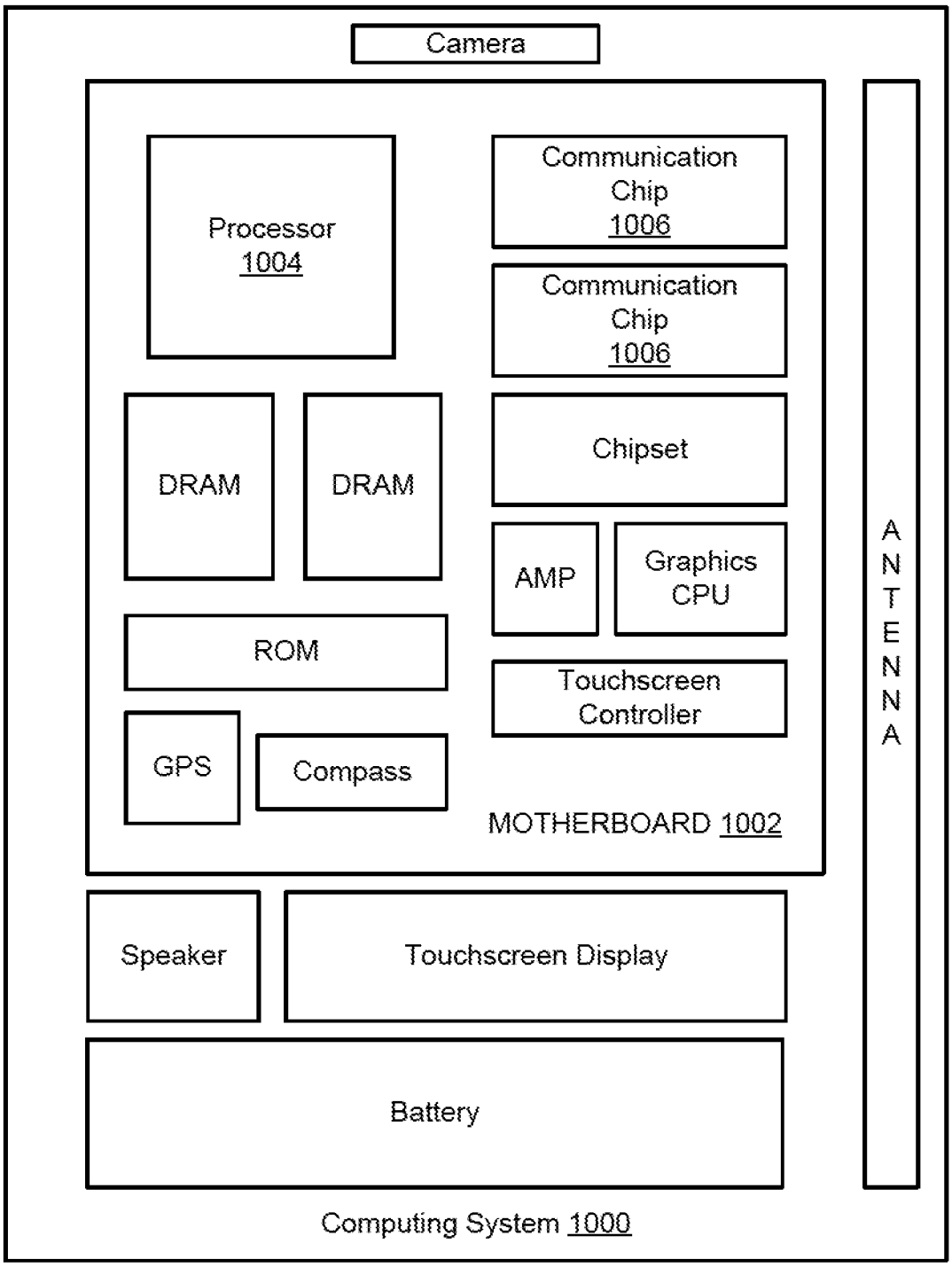

Camera
Processor
1004
Communication
Chip
1006
Communication
Chip
1006
DRAM
DRAM
Chipset
AMP
Graphics
CPU
ROM
Touchscreen
Controller
GPS
Compass
MOTHERBOARD 1002
ANTENNA
Speaker
Touchscreen Display
Battery
Computing System 1000

Fig. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US20 11/066477

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/28(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/28; H01L 21/20; H01L 21/3205

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: electroless nucleation material, electroless suppression material, electroless fill material

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 7651934 B2 (Lubomirsky, Dmitry et al.) 26 January 2010 See column 4 line 31 - column 9 line 30; and figure 1.	1-6, 15-23
Y	KR 10-2002-0090439 A (HYNIX SEMICONDUCTOR INC.) 05 December 2002 See page 2 line 28 - page 3 line 10; and figure 2.	1-6, 15-23
Y	KR 10-2011-0081155 A (TOKYO ELECTRON LTD.) 13 July 2011 See paragraph [0012] - paragraph [0041]; and figure 3.	2-6, 16, 17, 19-23
Y	KR 10-2008-0062563 A (HYNIX SEMICONDUCTOR INC.) 03 July 2008 See paragraph [0009] - paragraph [0055]; and figure 2.	5, 22

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 JULY 2012 (12.07.2012)	**12 JULY 2012 (12.07.2012)**

Name and mailing address of the ISA/KR
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea
Facsimile No. 82-42-472-7140

Authorized officer
Kim, Han Su
Telephone No. 82-42-481-8683

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/066477

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 13
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

Claim 13 is a dependent claim which refers to multiple dependent claim 12. Thus, claim 13 is so unclear and insufficiently disclosed that it is impossible to carry out a meaningful search.

3. ☒ Claims Nos.: 7-12, 14, 24, 25
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. Ill Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required addtional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2011/066477

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 7651934 B2	26.01.2010	US 2007-0042011 A1	04.01.2007
KR 10-2002-0090439 A	05.12.2002	None	
KR 10-2011-0081155 A	13.07.2011	CN 102165573 A	24.08.2011
		JP 2012-504347 A	16.02.2012
		TW 201027625 A	16.07.2010
		US 2010-0081274 A1	01.04.2010
		WO 2010-037074 A1	01.04.2010
KR 10-2008-0062563 A	03.07.2008	None	