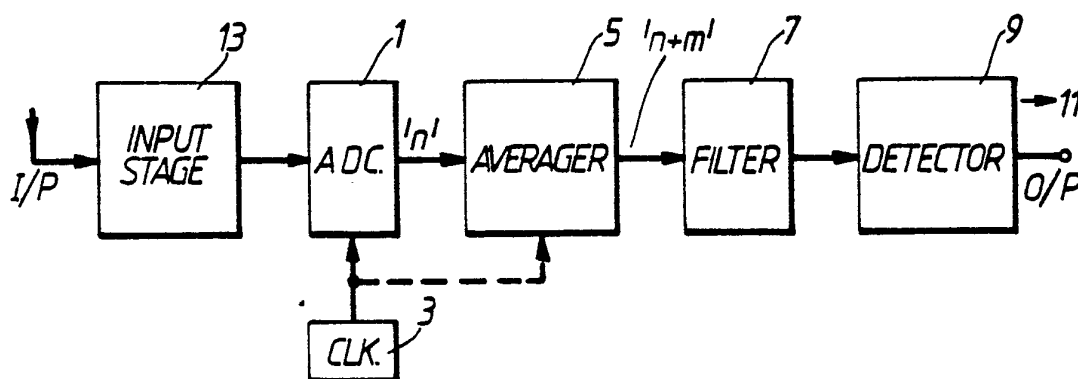




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁴ : H03M 1/20	A1	(11) International Publication Number: WO 87/ 04880 (43) International Publication Date: 13 August 1987 (13.08.87)
(21) International Application Number: PCT/GB87/00068 (22) International Filing Date: 30 January 1987 (30.01.87) (31) Priority Application Numbers: 8602227 8602230 (32) Priority Dates: 30 January 1986 (30.01.86) 30 January 1986 (30.01.86) (33) Priority Country: GB (71) Applicant (for all designated States except US): PLESSEY OVERSEAS LIMITED [GB/GB]; Vicarage Lane, Ilford, Essex IG1 4AQ (GB). (72) Inventor; and (75) Inventor/Applicant (for US only) : SAUL, Peter, Henry [GB/GB]; 51 Windsor Close, Towcester, Northants NN12 7JB (GB).		(74) Agent: FIELD, Howard, John; Intellectual Property Dept., Plessey Company plc, Vicarage Lane, Ilford, Essex IG1 4AQ (GB). (81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), FR (European patent), GB (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent), US. Published <i>With international search report.</i>

(54) Title: ANALOGUE TO DIGITAL CONVERSION: METHOD AND APPARATUS THEREFOR**(57) Abstract**

A converter for digital radio applications, consisting of a parallel analogue to digital converter (1) that provides sampling at signal carrier frequency, or preferably at a harmonic of this frequency. Successive samples $S(\Phi)$ are stored in a memory (14) and this is accessed at a lower rate to average numbers of samples. The ADC achieves greater resolution by virtue of this sampling. Filtering is provided by averaging action, but further filtering functions can be performed by an add-on filter (7). The converter (1) receives modulated analogue signal from an input stage (13), for example the rf. or if. circuit of a radio receiver. In a modified version of the apparatus (Fig. 6), several converters (1) may be utilized in parallel to afford increased data collection.

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ANALOGUE TO DIGITAL CONVERSION: METHOD AND
APPARATUS THEREFOR

Technical Field

The present invention concerns improvements in or relating to a method and apparatus for analogue-to-digital conversion most especially converters (ADC's) for digital radio applications.

5 The requirement for an ADC for use in a radio is particularly stringent. The dynamic range, if the ADC is used to convert the incoming signal without prefiltering, must exceed 100db and preferably be over 130db. This calls for accuracy of greater than 17 bits and ideally
10 more than 22bits.

Background Art

In digital radio applications, such converters, hitherto, have been limited in frequency to the audio range (baseband) and have therefore been preceeded by analogue
15 down-conversion circuitry, itself a source of error in cross- and intermodulation products of the order of -100db, ie. at the lowest acceptable limit for the system.

In a typical arrangement, the baseband signal is sampled at an arbitrarily high rf frequency, and, after
20 digital conversion, a large number of digitised samples accumulated to afford improved resolution or unwanted signal rejection. Such techniques have been described in the patent literature, for example:- United Kingdom Patent

Applications G.B. 1, 532, 538; G.B. 1, 580, 178; G.B. 2, 123, 233; and, G.B. 2, 144, 285; United States Patent Serial No. U.S. 3, 820, 111; and, International Patent Application W.O. 86/02217.

5 Disclosure of the Invention

 The present invention provides a method and an apparatus for analogue to digital conversion, adapted to offer enhanced resolution, and, suitable thus for digital
10 radio application.

 In accordance with the invention thus there is provided a method of analogue to digital conversion comprising the following steps:-
 acquiring a modulated analogue signal;
15 sampling and converting said signal, at a rate that is integer related to the carrier frequency for said signal, to generate thereby a multiplicity of digitised samples, each of n-bit word length;
 selecting from said multiplicity of samples a set thereof,
20 each sample as selected thus corresponding to a common phase but a successive cycle at said carrier frequency; and, averaging a number 2^m of consecutive samples of said set to generate an output word of n + m bit length.

 In further accordance with the invention there is
25 provided apparatus for analogue to digital conversion, this

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apparatus comprising:-

input means for acquiring a modulated analogue signal;

sampling means co-operative with said input means;

clocking means, co-operative with said sampling means to operate the same at a rate that is integer related to input

5 signal carrier frequency;

analogue to digital parallel conversion means to provide an

'n' bit digitised sample for each analogue sample;

a memory store comprised of 2^m memory elements each of n - bit word length;

10 sample selection means co-operative with both the conversion means and the memory store to direct to each element in turn a digitised sample, each sample as thus directed corresponding to a common phase () but a successive cycle at said carrier frequency; and,

15 sample averaging means, co-operative with the elements of said store, to provide an output word of n + m bit word length indicative of an average value of the 2^m samples stored therein.

20 With the provision of memory storage and averaging, n+m bit accuracy is thus attainable using only n bit conversion quantisation at front end.

The sampling means aforesaid may be incorporated as a

part of the conversion means (eg. as in a 'flash' ADC) or may be included as a dedicated sampling or sample-and-hold device.

5 The apparatus aforesaid may be followed by a digital filter and a digital detector. The filter may process signals either serially or in parallel if speed is requisite.

10 This apparatus may be applied to single sideband and amplitude modulation (AM), demodulation being performed by the action of the ADC sampling. The converter system may, with modification, also be used to process frequency modulated (FM) and frequency shift keyed (FSK) signals. Thus the sampling may be operated twice per cycle of the carrier frequency to provide in-phase and quadrature phase
15 sampling for this purpose.

As yet further modification, the sample clock may run at a rate equal to an harmonic multiple of the selected carrier frequency, to sample thus at several samples per cycle. The data then would be fed to separate locations
20 for respective sample phases and separate averaging performed serially or sequentially.

These and other aspects of the invention are set forth in the claims that follow hereinafter.

Brief Introduction of Drawings

25 In the drawings accompanying this specification, Figure 1 is a block schematic drawing showing the

arrangement of the component parts of an analogue to digital converter apparatus constructed in accord with this invention;

Figure 2 is a block schematic drawing showing memory and averaging parts of the converter apparatus shown in the preceding figure;

Figure 3 is an amplitude versus time graph showing synchronous of a modulated signal waveform;

Figure 4 is a block schematic drawing of apparatus, an extension of that shown in figure 2, adapted for multi-phase sampling;

Figure 5 is an amplitude versus time graph showing 4:1 oversampling of a modulated signal waveform;

Figure 6 is a block schematic drawing of apparatus, a variant of that shown in figure 4; and,

Figure 7 is a block schematic drawing of a phase and quadrature receiver circuit, one that may be added to the multi-phase conversion apparatus of figures 4 or 6.

Description of Preferred Embodiments

So that this invention may be better understood, embodiments thereof will now be described and reference will be made to the accompanying drawings. The description that follows is given by way of example only.

The ADC apparatus to be described below makes use of the essential differences between a true analogue to digital converter and the type of ADC apparatus which is

acceptable in a radio application. The first of these differences is that, provided the departures from the ideal transfer characteristic are not great the main consideration is the signal-to-noise ratio rather than the existence of all states. Existing high accuracy ADCs in the baseband radio systems mentioned above and in digital telephone systems exploit this feature. The second, and possibly more important factor is that one key piece of information about the incoming wanted signal is known .ie. the frequency. It is possible to assume in modern receiver systems that a clock signal can be generated at the incoming frequency or a multiple of it with arbitrary accuracy. It is then possible to devise a radio receiver system based on the arrangement shown in figure 1. This shows an essentially conventional ADC 1, of the 'flash' type (which needs no sample hold), sampling at the input carrier frequency under control of a clock 3, followed by a memory and averaging circuit 5, a digital filter 7, a digital detector 9 and an output circuit 11, which could take the form of a d-a converter and audio output stage, or could be in the form of further processing circuitry for digital signals. As shown, the analogue-to-digital converter 1 directly follows the 'rf' or 'if' stage 13 of a radio receiver, from which it receives modulated analogue signal.

25 A more detailed schematic of the ADC/memory

organisation is shown in figure 2. The memory and averaging circuit 5 shown comprises a store 14 having 2^m memory locations 15 each of which is of n-bit word length and is loaded sequentially by demultiplexing 17 the output from the ADC 1. Once loaded, each memory location 15 is read by microprocessor or other averaging circuitry 19 and an n+m bit word length signal generated at the circuitry output.

The ADC 1 could be essentially a conventional parallel "flash" type, of eight or more bits 'n'. It would preferably have a wide analogue input bandwidth to accommodate signals up to or above the top of the HF band (30MHz). With some compromise in performance, fewer than eight bits could be used; this may be more attractive at V.H.F.

The clock 3 in this simplest system is synchronous with the nominal input carrier frequency. Hence, successive samples $S_1; S_2; \dots$, occur at equal time intervals on the carrier waveform (see fig 3). If therefore a number of successive samples $S_1; S_2; \dots$, are stored and subsequently averaged, then the average value S will represent further bits of resolution in the equivalent ADC. For example, if " 2^m " samples $S_1; S_2; \dots; S_{2^m}$, are averaged, then "m" further bits of resolution will be obtained. The averaging would most advantageously be a "rolling" arrangement, with the oldest

samples S_1 , etc., being discarded in favour of new values $S_{2^m + 1}$, etc. In the simplest case, a level weighting would be imposed, but for increased output bandwidth it would be possible to weight the average
5 S to the newest samples ($\bar{S} = \sum_i \omega_i S_i$).

The total of "n+m" bits are then passed to a digital filter, which can be of many different forms: generic classes are "finite impulse response" (FIR) and "infinite impulse response" (IIR). The filtering provides, in
10 addition to the inherent filtering to be described below, the selectivity of the receiver.

The composite ADC apparatus figure 1, can be used to receive all classes of modulation by providing a suitable digital detector. Single sideband and amplitude
15 modulation will be demodulated by the action of the ADC sampling. If necessary a phase control (not shown) may be included to prevent sampling at zero-crossing points. Frequency modulation, or FSK can be demodulated using a phase and quadrature receiver of appropriate
20 characteristics, for example the receiver described in our United Kingdom patent application G.B. 8602227, brief details of which will follow below (fig 7). This leads to a modification of the scheme which may be generally advantageous. A phase shift at the carrier frequency is
25 needed for the FM demodulator cited and for certain others. This is achieved in the ADC apparatus described

here Fig.1 by providing two clock pulses to the ADC 1, with a 90 degree (ie. quadrature) relative phase shift. Data is then sorted in two separate (phase and quadrature, or I and Q) memories 14. The derived $n+m$ bits can then be processed through the filter by time interleaving, or could be passed through two separate filters for maximum speed. Again, for maximum speed of operation, two phased ADCs 1 could be used, but this would slightly degrade the I and Q channel matching.

10 The phase and quadrature receiver circuit shown in figure 7 comprises four digital multipliers 21, 23, 25 and 27, a difference amplifier 31 and a summing amplifier 33. The multipliers are arranged in pairs 21 and 23, 25 and 27 and are connected to receive the averaged sample outputs S_Q and S_I of the conversion apparatus, respectively. One multiplier 21, 27 in each pair receives an in-phase multiplicand, $\sin \omega_0 t$, whilst the other multiplier 23, 25 in each pair receives a quadrature multiplicand, $\cos \omega_0 t$. The output of each multiplier 21, 25 and 23, 27 is referred to the difference amplifier 31 and to the summing amplifier 33, respectively to generate in-phase I and quadrature Q detected digital signals.

 Returning to consider the ADC system fig. 1, several limitations can be identified. These are not major problems, but delineate the likely limits to operation. The most obvious limit is that the sample rate and hence

the incoming frequency must exceed $2^m \times$ (maximum modulation frequency $\times 2$) to allow for two samples per cycle of the modulation from 2^m successive samples of the carrier. An example would be for the averaging of
5 1024 samples ($m=10$) with 2kHz modulation, leading to a minimum input of 4MHz. With a 10 bit ADC this would give 120db dynamic range.

Unusually for an ADC system there is also a minimum for the modulation frequency, below which the coarse
10 initial quantisation will become more evident. This limit occurs when the slew rate of the input modulation is such that only a small fraction of the averaged samples in a quantisation level is distinguishable from the main group of samples. A closely related limit occurs when the input
15 signal is so small that it always remains at a single quantisation level of the coarse ADC 1. However, these are only a problem if there is no other interfering signal present which can carry the input to an adjacent level, at least for part of the time. The interfering signals,
20 which in practical systems will always be present, can be filtered out in the subsequent stages. The ultimate dynamic range is therefore limited by the combination of "n" and "m" achievable. It has been shown above that, at low frequencies, for a 10 bit ADC, 2^{10} memory
25 locations are required. Raising the signal/sample rate would ease the ADC requirement, at the cost of more

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memory. Clearly, current state of art systems can barely achieve the required dynamic range. While it is to be expected that developed systems will eventually achieve larger numbers of bits ("n") resolution, one further modification to the described arrangement (fig. 1) could remove the limitations due to finite word length in the ADC 1 by applying more memory 14 and processing 19. Since memory and digital processing power continues to fall in cost this is an advantageous route. This modification is to provide multiple samples $S(\phi_1); S(\phi_2); \dots S(\phi_p)$, per cycle of the carrier signal. These could be provided by a single ADC 1 (fig 4) sampled at a higher frequency, or, by several phased ADCs 1 (fig 6) if speed is a limitation. The data is then fed to a memory array, with separate stores 14 for respective sample phases $\phi_1; \phi_2; \dots \phi_p$. Averaging is carried out as before, but based on "p" separate samples $S(\phi_1)$ to $S(\phi_p)$ per cycle. An example of "p"=4 is shown in figure 5.

Filtering is again speed dependent. Fast systems (in relation to available processing speed) will use parallel digital filters, while slower systems may use the same filter 7 on a time-multiplexed basis. Data is then stored in a further memory (not shown) for sequential reconstruction. Essentially, the memories are polled at a rate which is either a submultiple of the original sample

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rate or is a multiple (at least twice) of the maximum output frequency. The output, after d/a conversion, is the recovered modulation. Again SSB, AM, FM or FSK modes are possible. The two sample per cycle method for FM
5 detection described above is clearly one case of the more general p-sample system just described.

A particular advantage of the multiple sampling scheme is that the filter at the output frequency consists of several identical sections. These can be
10 strictly separate filters for each successive sample interval. To great advantage, however, a single filter section instead could be used on a time multiplexed basis. The several section version of the filter has an analogue in the class of filters known as "N-path". The sequential
15 version could be regarded as a special case of "N-path" filtering.

Accuracy limitations of the basic ADC 1 form one limit of the cross and intermodulation characteristics of the system. The most obvious limit is the finite accuracy
20 of the steps in the ADC 1 transfer characteristic. However, since most of the steps are much more accurate than the worst case error, the dynamic range limitation due to this source of error is likely to be much better than the quantisation term of 6db per bit. Taking the 10
25 bit example above, the dynamic range for a practical system would substantially exceed $(n \times 6)$ ie. 60db and would

probably be over 100db, although this figure is difficult to quantify without precise knowledge of the types of ADC errors and a further study of their effects. Prefiltering of the R.F. signal may be necessary in some applications where significant signals are present at harmonics of the wanted signal. A higher degree of oversampling would in principle help here, but the sample rate would then need to be synchronous with the input and at a frequency at least twice that of the highest possible received frequency. The input would still need anti-alias low-pass input filtering, so each case should be considered on its merits. Prefiltering is commonly used in analogue systems and the requirement is only for a reduction in the harmonics of the received frequency; adjacent channel filtering is carried out by the digital system. The apparatus described above may be assembled from standard components. Thus, for example, it could be assembled using a Plessey SP9758 8-bit ECL - ADC; Plessey HA21 random access memories; and, averaging circuits constructed from small-scale integration (SSI) logic gates such as Plessey ECL III series devices.

From the foregoing description, the following advantageous features will be evident:-

- i) The inventive apparatus herein disclosed, incorporated as part of a digital radio receiver, offers wideband input capability;

ii) The apparatus, in general, requires little or no prefiltering;

iii) It is capable of integration onto a small number only of integrated circuits;

5 iv) Elaborate set-up procedures are unnecessary during system production;

v) It may be devised for AM, SSB, ISB or FM mode operation and is suited to software control;

10 vi) Associated filtering functions, as may be requisite, likewise can be readily implimented under software control; and,

vii) The system offers the capability of wide dynamic range performance.

15

20

CLAIMS

1. A method of analogue to digital conversion comprising the following steps:-
 - 5 acquiring a modulated analogue signal;
 - sampling and converting said signal, at a rate that is integer related to the carrier frequency for said signal, to generate thereby a multiplicity of digitised samples ($S_1; S_2; \dots$), each of n -bit word length;
 - 10 selecting from said multiplicity of samples ($S_1; S_2; \dots$) a set thereof, each sample ($S_1(\phi); S_2(\phi); \dots$) as selected thus corresponding to a common phase (ϕ) but a successive cycle at said carrier frequency; and, averaging a number 2^m of consecutive samples ($S_1(\phi)$ to $S_{2^m}(\phi)$) of said set to generate an output word ($\bar{S}(\phi)$) of $n + m$ bit length.
2. A method, as claimed in claim 1, wherein the steps of selection and averaging are performed repeatedly, to
 - 20 generate a string of output words $\bar{S}(\phi)$ each of $n + m$ bit length, and such that on each repeat said set of selected samples ($(S_1; S_2; \dots; S_{2^m}); (S_2; \dots; S_{2^m+1})$) includes a given number of the samples (S_2 to S_{2^m}) selected on the previous repeat.
3. A method, as claimed in either preceding claim,

wherein said sampling and converting step is performed at a rate that is an harmonic multiple of the carrier frequency, the multiplicity of digitised samples generated thus including samples of different carrier frequency phase;

5 and, the steps of selection and averaging are performed for a plurality of sample sets ($S(\phi_1); S(\phi_2); \dots; S(\phi_p)$) each set $S(\phi)$ corresponding to a respective different phase ($\phi_1; \phi_2; \dots; \phi_p$) at carrier frequency.

10 4. A method, as claimed in claim 3, wherein said sampling and converting step is performed at a rate that is the fourth harmonic of the carrier frequency, said sample sets $S(\phi)$ corresponding to phases ($\phi; \phi + \pi/2$) that differ by quadrature ($\pi/2$), in-phase (I) and quadrature (Q) term
15 output words (S_I, S_Q) being generated.

5. Apparatus (fig 1; fig 2; fig 4; fig 6) for performing the method as claimed in any one of the preceding claims, this apparatus comprising:-

20 input means (13) for acquiring a modulated analogue signal;
sampling means (1), co-operative with said input means (13);
clocking means (3), co-operative with said sampling means (1) to operate the same at a rate that is integer related to input signal carrier frequency;

analogue to digital parallel conversion means (1) to provide an 'n' bit digitised sample ($S_1; S_2; \dots$) for each analogue sample;
a memory store (14) comprised of 2^m memory elements (15) each of n - bit word length;
5 sample selection means (17) co-operative with both the conversion means (1) and the memory store (14) to direct to each element (15) in turn a digitised sample, each sample as thus directed corresponding to a common phase (ϕ) but a successive cycle at said carrier frequency; and,
10 sample averaging means (19), co-operative with the elements (15) of said store (14), to provide an output word (S) of n + m bit word length indicative of an average value of the 2^m samples ($S_1; S_2; \dots; S_{2^m}$) stored therein.

15

6. Apparatus, as claimed in claim 5, wherein:-
said sample selection means (17) is adapted to address each element (15) of said store (14) in a cyclic manner; and,
said sample averaging means (19) is controlled to provide
20 output words ($\bar{S}$) repeatedly, each word ($\bar{S}$) corresponding to a consecutive 'rolled' set of the digitised samples (S_1 to S_{2^m}); (S_2 to S_{2^m+1})) stored in the 2^m elements (15) of said store 14.

7. Apparatus, as claimed in either claim 5 or claim 6, wherein:-

said averaging means (19) is adapted to weight (ω_1 to ω_{2^m}) the samples (S_1 to S_{2^m}) of said set, the most recent (...; S_{2^m}) thereof being accorded highest weighting.

5

8. Apparatus (fig 4; fig 6;) as claimed in any one of preceding claims 5 to 7, wherein the clocking means (3) is co-operative with said sampling means (1) to operate the same at a rate that is an harmonic multiple of the input signal carrier frequency;

10 a plurality of memory stores (14) being provided, each comprised of 2^m memory elements (15);

said selection means (17) being arranged to direct to respective stores (14) sets of digitised samples ($S(\phi_1)$ to $S(\phi_p)$) each set being extracted for a different

15 respective phase (ϕ_1 to ϕ_p) of the carrier; and,

said sample averaging means (19) being co-operative with each store (14) to provide an output word $\bar{S}(\phi)$ for each respective phase (ϕ).

20

9. Apparatus, as claimed in claim 8, wherein the rate (fig 5) is the fourth harmonic of the carrier frequency, so that in-phase and quadrature term words ($\bar{S}_I$; $\bar{S}_Q$) shall be presented at output (O/P).

10. Apparatus, as claimed in claim 8 or 9, when followed

by a time-multiplexed filter (7).

11. Apparatus (fig 6), as claimed in any one of claims 8 to 10, wherein said analogue to digital conversion means
5 (1) comprises a plurality of phased parallel converters (1), said plurality of stores (14) being of like number, each converter (1) being co-operative with a respective one of said stores (14).

10 12. Apparatus (fig 4; fig 6), as claimed in claim 9, when in combination with a phase and quadrature digital receiver (fig 7) the inputs of which are connected to receive the in-phase and quadrature term output words.

15 13. Apparatus, as claimed in claim 12, wherein said receiver (fig 7) comprises:-
four digital multipliers (21, 23, 25 and 27);
a difference amplifier (31); and,
a summing amplifier (33); wherein,
20 first and second of these multipliers (21, 23) are connected at input to receive the quadrature term word ($\overline{S_Q}$), and are connected at output to the difference and summing amplifiers (31, 33) respectively;
third and fourth of these multipliers (25, 27) are connected at input to receive the in-phase term word ($\overline{S_I}$), are likewise connected at output to the difference

and summing amplifiers (31, 33) respectively; and,
in-phase and quadrature multiplicands ($\sin \omega_0 t$, $\cos \omega_0 t$)
are applied to the first and fourth multipliers (21, 27),
and to the second and third multipliers (23, 25),
5 respectively.

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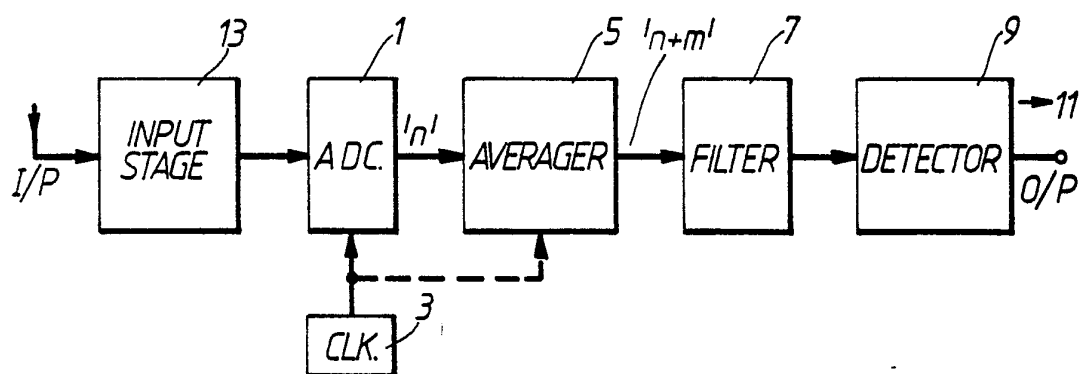


Fig.1.

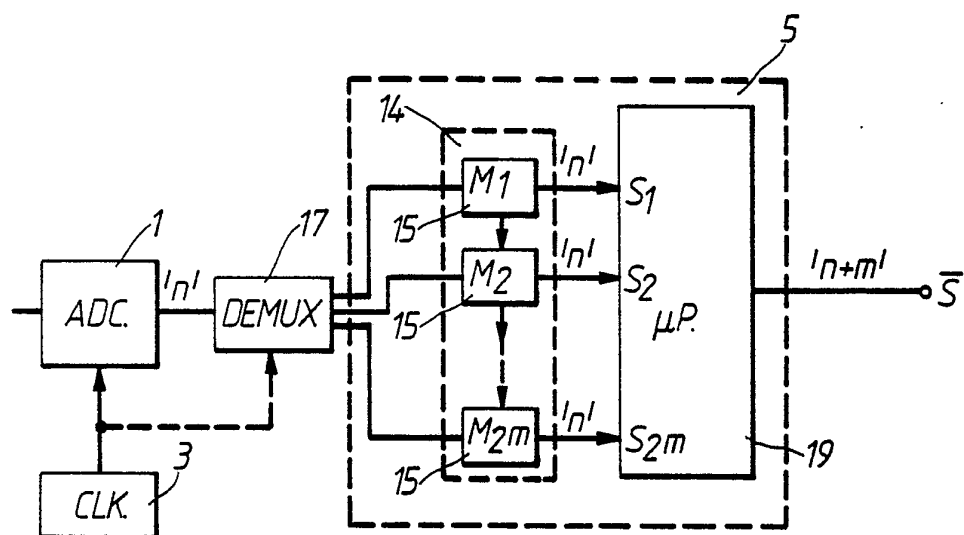


Fig.2.

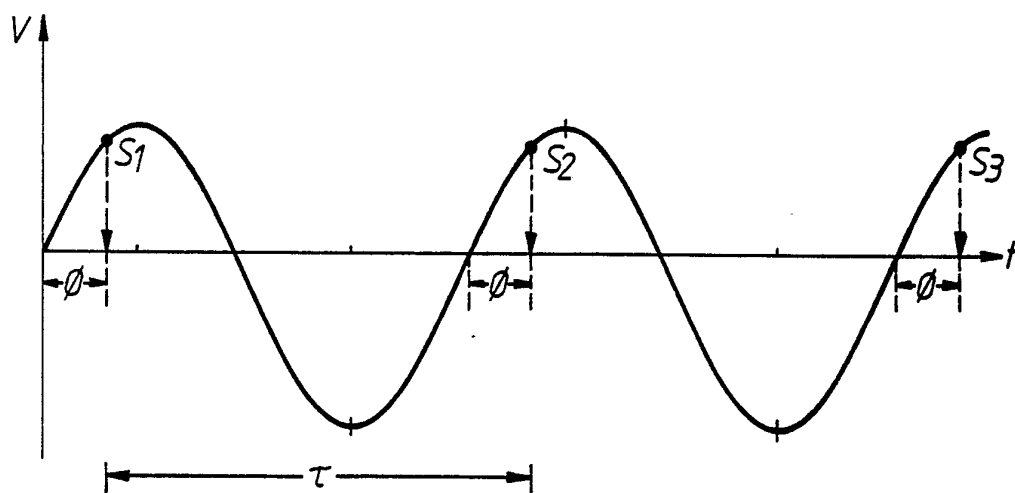


Fig.3. SUBSTITUTE SHEET

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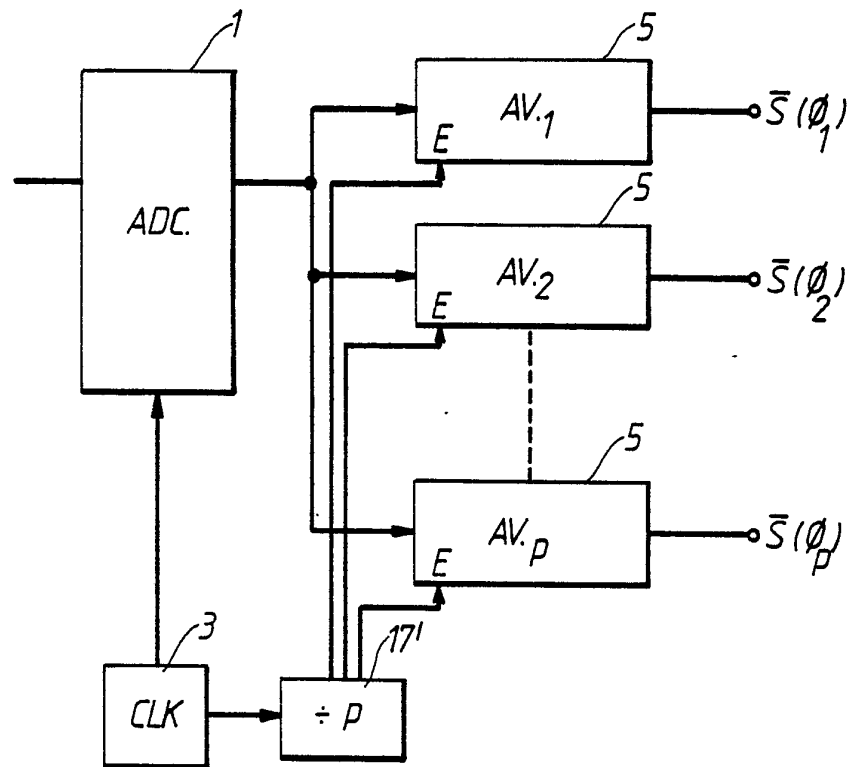


FIG.4.

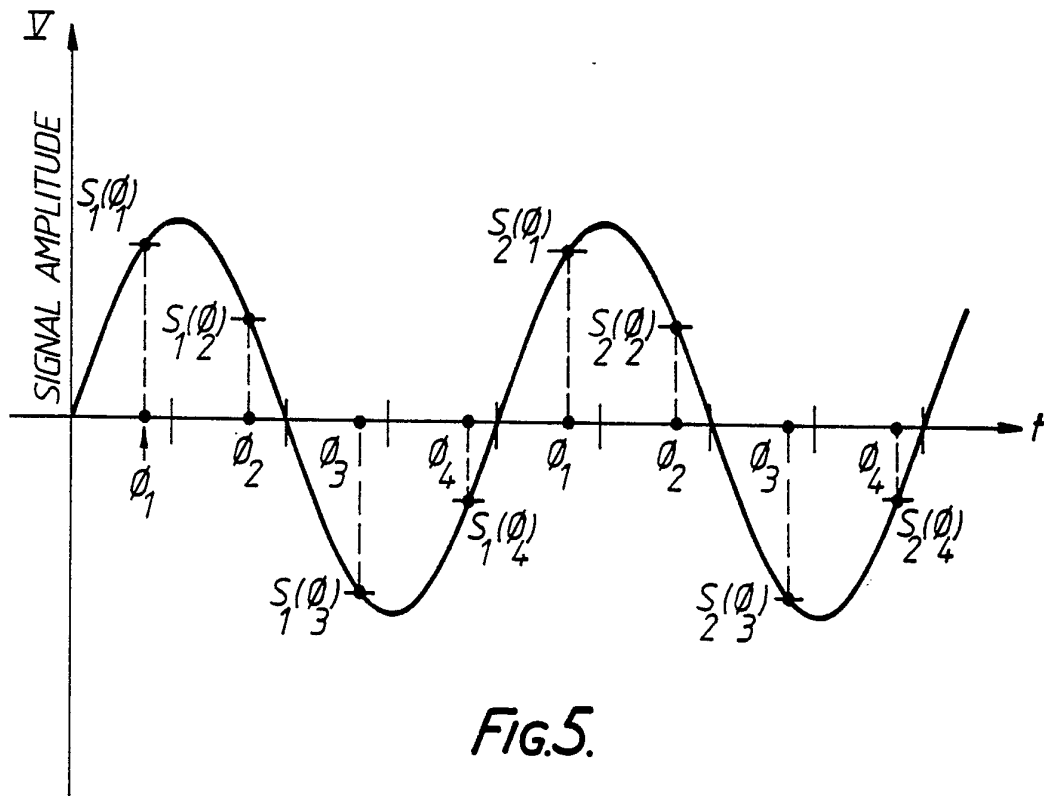
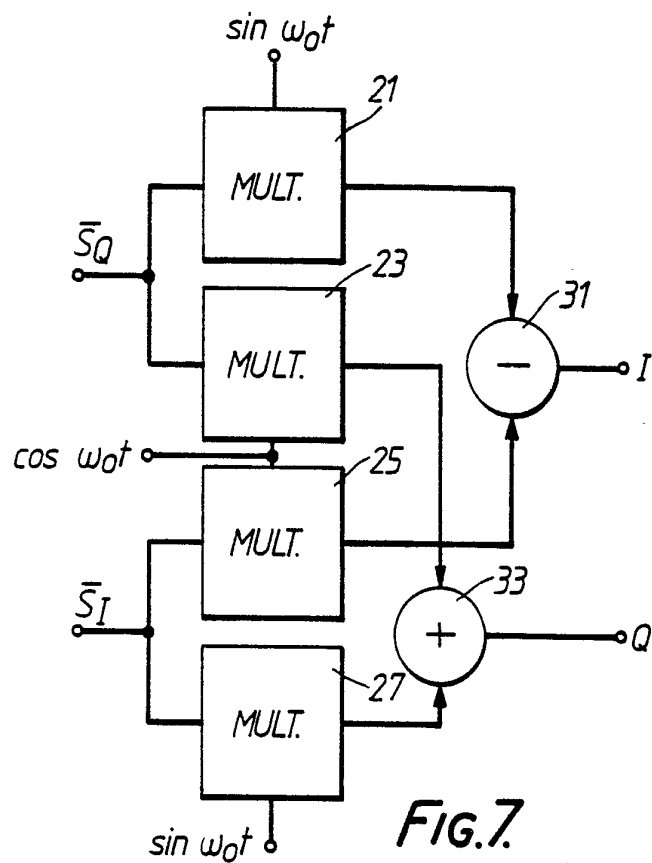
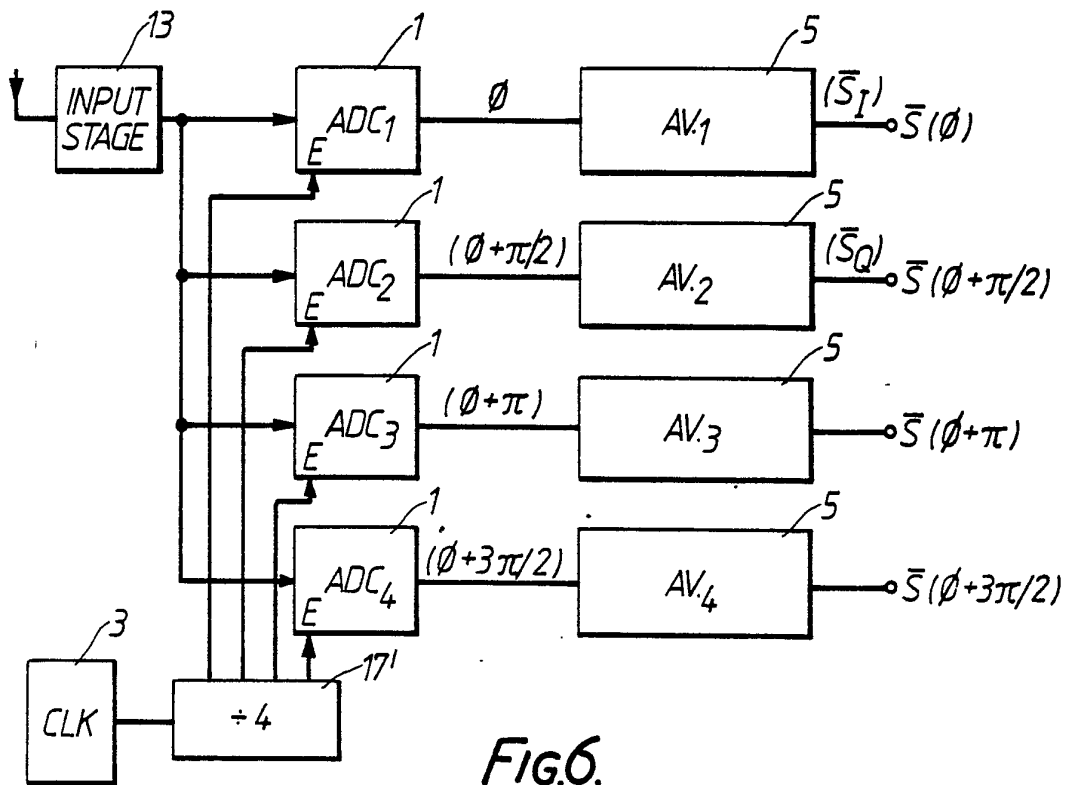


FIG.5.

SUBSTITUTE SHEET

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SUBSTITUTE SHEET

INTERNATIONAL SEARCH REPORT

International Application No **PCT/GB 87/00068**

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) *		
According to International Patent Classification (IPC) or to both National Classification and IPC		
IPC ⁴ : H 03 M 1/20		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁷		
Classification System	Classification Symbols	
IPC ⁴	H 03 M; H 03 H	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched *		
III. DOCUMENTS CONSIDERED TO BE RELEVANT *		
Category *	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³
A	US, A, 3820111 (CANDY) 25 June 1974 see figures 1,3; abstract; column 3, lines 1-12, 49-63; column 4, line 32 - column 5, line 12 cited in the application --	1
A	IEEE International Solid-State Circuits Conference, February 1985, (New York, US), M.W. Hauser et al.: "MOS ADC-filter combination that does not require precision analog components", pages 80-81,313 see page 80, column 2, lines 43-48; figure 4 --	1
A	IEEE International Solid-State Circuits Conference, February 1980, (New York, US), W.C. Black, Jr et al.: "Time inter- leaved converter arrays", pages 14-15, 254 see figure 1	1
* Special categories of cited documents: ¹⁰ "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report	
15th April 1987	22 MAY 1987	
International Searching Authority	Signature of Authorized Officer	
EUROPEAN PATENT OFFICE	M. VAN MOL 	

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/GB 87/00068 (SA 16006)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 11/05/87

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 3820111	25/06/74	None	

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