



- (51) **International Patent Classification:**
H01L 21/60 (2006.01) *H01L 23/31* (2006.01)
- (21) **International Application Number:**
PCT/US2016/018640
- (22) **International Filing Date:**
19 February 2016 (19.02.2016)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
62/119,579 23 February 2015 (23.02.2015) US
15/047,426 18 February 2016 (18.02.2016) US
- (71) **Applicant:** MARVELL WORLD TRADE LTD.
[BB/BB]; L'Horizon, Gunsite Road, Brittons Hill, St. Michael, Barbados, BB14027 (BB).
- (72) **Inventor:** WANG, Long-Ching; 7588 New Castle Drive, Cupertino, CA 95014 (US).
- (74) **Agents:** LEMON, Kevin, T. et al.; Lee & Hayes, PLLC, 601 W. Riverside Ave., Suite 1400, Spokane, WA 99201 (US).
- (81) **Designated States** (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM,

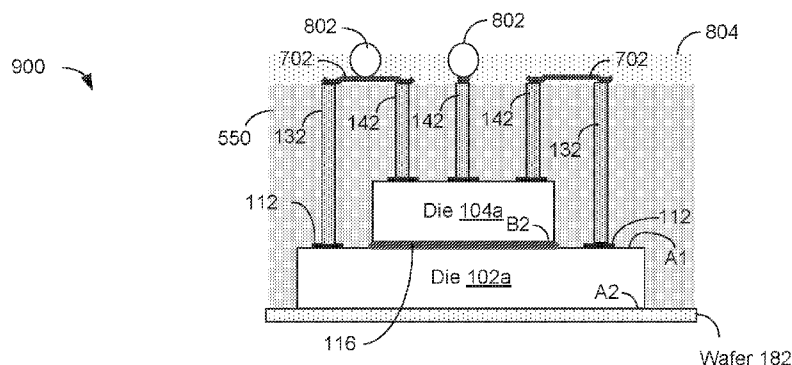
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) **Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

- with international search report (Art. 21(3))
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

(54) **Title:** METHOD AND APPARATUS FOR INTERCONNECTING STACKED DIES USING METAL POSTS

**Fig. 9A**

(57) **Abstract:** Embodiments include a semiconductor package comprising a first die having (i) a first side and (ii) a second side, wherein the first die (102a) comprises a first plurality of bond pads (112) formed on the first side of the first die; a second die (104a) having (i) a first side and (ii) a second side, wherein the second die comprises a second plurality of bond pads formed on the first side of the second die, wherein the second die is stacked on the first die; a first plurality of metal posts (132) formed on the first plurality of bond pads; a second plurality of metal posts (142) formed on the second plurality of bond pads; and a redistribution layer (702) configured to electrically couple (i) a first metal post of the first plurality of metal posts and (ii) a second metal post of the second plurality of metal posts.

METHOD AND APPARATUS FOR INTERCONNECTING STACKED DIES USING METAL POSTS

Cross Reference to Related Applications

[0001] This disclosure claims priority to U.S. Patent Application No. 15/047,426, filed February 18, 2016, which claims priority to U.S. Provisional Patent Application No. 62/119,579, filed on February 23, 2015, which is incorporated herein by reference in its entirety.

Technical Field

[0002] Embodiments of the present disclosure relate to stacking a die on another die, and in particular to interconnecting stacked dies via metal posts.

Background

[0003] Integrated circuit devices are formed on dies or chips that continue to scale in size to smaller dimensions. The shrinking dimensions of the dies and semiconductor packages are challenging conventional substrate fabrication and/or package assembly technologies that are currently used to route electrical signals to or from the dies. In an example, a semiconductor package includes a first semiconductor die stacked on top of a second semiconductor die. It is challenging to route signals between the two semiconductor dies, e.g., because of the stacking of the two semiconductor dies.

Summary

[0004] In various embodiments, the present disclosure provides a semiconductor package comprising a first die having (i) a first side and (ii) a second side disposed opposite the first side of the first die, wherein the first die comprises a first plurality of bond pads formed on the first side of the first die; a second die having (i) a first side and (ii) a second side disposed opposite the first side of the second die, wherein the second die comprises a second plurality of bond pads formed on the first side of the second die, wherein the second die is stacked on the first die such that the second side of the second die is attached to the first side of the first die; a first plurality of metal posts, wherein each of the first plurality of metal posts is formed on a

corresponding one of the first plurality of bond pads formed on the first side of the first die; a second plurality of metal posts, wherein each of the second plurality of metal posts is formed on a corresponding one of the second plurality of bond pads formed on the first side of the second die; and a redistribution layer configured to electrically couple (i) a first metal post of the first plurality of metal posts and (ii) a second metal post of the second plurality of metal posts.

[0005] In various embodiments, the present disclosure also provides a method of forming a semiconductor package comprising forming a first die, the first die comprising (i) a first side and (ii) a second side disposed opposite the first side of the first die; forming a first plurality of bond pads on the first side of the first die; forming a second die, the second die comprising (i) a first side and (ii) a second side disposed opposite the first side of the second die; forming a second plurality of bond pads on the first side of the second die; forming a first plurality of metal posts, wherein each of the first plurality of metal posts is formed on a corresponding one of the first plurality of bond pads formed on the first side of the first die; forming a second plurality of metal posts, wherein each of the second plurality of metal posts is formed on a corresponding one of the second plurality of bond pads formed on the first side of the second die; subsequent to forming the first plurality of metal posts and the second plurality of metal posts, stacking the second die on the first die such that the second side of the second die is attached to the first side of the first die; and forming a redistribution layer that electrically couples (i) a first metal post of the first plurality of metal posts and (ii) a second metal post of the second plurality of metal posts.

[0006] In various embodiments, the present disclosure also provides a semiconductor package comprising a first die having (i) a first side and (ii) a second side disposed opposite the first side of the first die, wherein the first die comprises a first bond pad formed on the first side of the first die; a second die having (i) a first side and (ii) a second side disposed opposite the first side of the second die, wherein the second die comprises a second bond pad formed on the first side of the second die, wherein the second die is stacked on the first die such that the second side of the second die faces the first side of the first die; a first redistribution layer formed on the first side of the first die, wherein the first redistribution layer comprises (i) a first

end attached to the first bond pad, and (ii) a second end that is opposite to the first end; a first metal post formed on the second end of the first redistribution layer; a second metal post formed on the second bond pad that is formed on the first side of the second die; and a second redistribution layer configured to electrically couple (i) the first metal post and (ii) the second metal post.

Brief Description of the Drawings

[0007] Embodiments of the present disclosure will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Various embodiments are illustrated by way of example and not by way of limitation in the figures of the accompanying drawings.

[0008] Figs. 1A-9A illustrate various operations associated with forming a semiconductor package assembly comprising a first die stacked on a second die, wherein the first die and the second die are interconnected via metal posts.

[0009] Fig. 9B illustrates a flow diagram of an example method for forming the semiconductor package assembly of Figs. 1A-9A.

[0010] Figs. 10A-14 illustrate formation a semiconductor package assembly comprising a first die stacked on a central section of an active surface of the second die, where second the die comprises bond pads disposed in the central section of the active surface of the second die.

Detailed Description

[0011] Figs. 1A-9A illustrate various operations associated with forming a semiconductor package assembly comprising a die 104a stacked on another die 102a, wherein the dies 102a, 104a are interconnected via metal posts. Referring to Fig. 1A, this figure illustrates an arrangement 100 comprising two semiconductor wafers 182 and 184. Each of the wafers 182, 184, for example, serves as a substrate on which a corresponding plurality of semiconductor dies (henceforth referred to as "dies") is formed. For example, a plurality of dies 102a, 102b, 102c, ..., 102N is formed on the wafer 182, and a plurality of dies 104a, 104b,

104c, ..., 102M is formed on the wafer 184. The wafers 182, 184 and the dies thereon are formed using any appropriate technique(s) for forming wafers and dies. Although Fig. 1A illustrates an example number and arrangement of the dies on the wafers 182, 184, the wafers 182, 184 can include any other number and/or arrangement of dies formed thereon.

[0012] Fig. 1B illustrates a cross sectional view of the dies 102a and 104a formed on the wafers 182 and 184, respectively, and Fig. 1C illustrates a top view of the dies 102a and 104a. Each of the dies 102a and 104a generally has an active side that includes a surface upon which a plurality of integrated circuit (IC) devices (not illustrated in the figures) such as transistors for logic and/or memory are formed, and an inactive side that is disposed opposite to the active side. In Fig. 1B, the active sides of the dies 102a and 104a are labeled as A1 and B1, respectively, while the inactive sides of the dies 102a and 104a are labeled as A2 and B2, respectively.

[0013] The surface of the die 102a on the active side of the die 102a is also referred to herein as an active surface of the die 102a, and the surface of the die 104a on the active side of the die 104a is also referred to herein as an active surface of the die 104a. In an example, the inactive side A2 of the die 102a is attached to the wafer 182, and the inactive side B2 of the die 104a is attached to the wafer 184. In an embodiment, the die 104a is smaller in size compared to the die 102a. For example, an area of the active surface of the die 104a is smaller than an area of the active surface of the die 102a, as illustrated in Figs. 1B and 1C.

[0014] Fig. 1C illustrates the top view of the two dies 102a and 104a. The top view of Fig. 1C illustrates the active sides A1 and B1 of the dies 102a and 104a, respectively. As illustrated in Figs. 1B and 1C, the die 102a comprises a plurality of bond pads 112, which are formed on the active side A1 of the die 102a (i.e., formed on the active surface of the die 102a). Individual ones of the bond pads 112 are electrically connected to one or more corresponding internal electrical components of the die 102a, and facilitates routing electric signals (e.g., input/output (I/O) signals, power signals, ground signals, etc.) to and/or from the die 102a.

[0015] In an embodiment, the bond pads 112 are arranged near a periphery of the die 102a. For example, as illustrated in Fig. 1C, the bond pads 112 are arranged along the four edges of the die 102a (although in another embodiment and not illustrated in the figures, the

bond pads 112 can be arranged along only one, two or three edges of the die 102a). Fig. 1C illustrates only one line or series of bond pads 112 along each edge of the die 102a. However, in another embodiment and although not illustrated in Fig. 1C, the bond pads 112 can be arranged in any other appropriate configuration near the periphery of the die 102. In an example, the bond pads 112 are arranged such that the bond pads do not occupy at least a central section of the active surface of the die 102a (e.g., such that there is enough space on the active surface of the die 102a to stack the die 104a thereon, as will be discussed in more detail herein later).

[0016] As illustrated in Figs. 1B and 1C, the die 104a comprises a plurality of bond pads 114, which are formed on the active side B1 of the die 104a (i.e., formed on the active surface of the die 104a). Individual ones of the bond pads 114 are electrically connected to one or more corresponding internal electrical components of the die 114, and facilitates routing electric signals (e.g., input/output (I/O) signals, power signals, ground signals, etc.) to and/or from the die 104a.

[0017] In an embodiment, the bond pads 114 can be arranged at any position on the active surface of the die 104a. For example, Fig. 1C illustrates the bond pads 114 being randomly arranged (e.g., arranged without any specific pattern) on the active surface of the die 104a (e.g., some of the bond pads are arranged near the periphery, while some are arranged near a central section of the active surface of the die 104a). In another example and although not illustrated in the figures, the bond pads 114 are arranged solely along the periphery of the die 104a. In yet another example and although not illustrated in the figures, the bond pads 114 are arranged in any other appropriate pattern on the active surface of the die 104a. That is, unlike the bond pads 112 on the die 102a, the bond pads 114 on the die 104a need not necessarily be arranged only near the periphery of the die 104a.

[0018] In an embodiment, the bond pads 112, 114 are respectively formed on the dies 102a, 104a while the dies 102a, 104a are still attached to the wafers 182, 184, respectively. In an embodiment, the bond pads 112, 114 can be replaced by any other appropriate structure that provides input/output connection to the dies 102a, 104a, e.g., replaced by corresponding bump pads.

[0019] Fig. 2 illustrates an arrangement 200, in which metal posts 132, 142 are respectively formed on ones of the bond pads 112, 114 of the dies 102a, 104a, respectively, of the arrangement 100 of Figs. 1A-1C. For example, each of the metal posts 132 is formed on a corresponding one of the bond pads 112 of the die 102a. For example, a bottom end of a metal post 132 is formed on, and makes electrical connection to a corresponding bond pad 112 of the die 102a. Similarly, each of the metal posts 142 is formed on a corresponding one of the bond pads 114 of the die 104a. For example, a bottom end of a metal post 142 is formed on, and makes electrical connection to a corresponding bond pad 114 of the die 104a.

[0020] In an embodiment, the metal posts 132, 142 are metal pillars formed from an appropriate metal or other conductive material. In an example, the metal posts 132, 142 comprise copper, while in another example, the metal posts 132, 142 comprise aluminum or another appropriate metal.

[0021] In an embodiment, all the metal posts of the metal posts 132 are substantially similar in height, and all the metal posts of the metal posts 142 are substantially similar in height. In an embodiment, the height of the metal posts 132 is smaller than the height of the metal posts 142. As illustrated in Fig. 2, in an embodiment, the metal posts 132, 142 are formed on the dies 102a, 104a, while the dies 102a, 104a are still attached to the corresponding wafers 182, 184.

[0022] Fig. 3 illustrates an arrangement 300, in which the wafer 184 of the arrangement 200 of Fig. 2 is singulated such that the die 104a is separated from the other dies 104b, 104c, ..., 104M of the wafer 184. For example, the wafer 184 is at least partially grinded or otherwise thinned (e.g., so that a thickness of the wafer 184 decreases, not illustrated in the figures), and then the wafer 184 is singulated, such that the die 104a is separated from the other dies of the wafer 184. In an embodiment, subsequent to grinding the wafer 184 and singulating the die 104a, a thin layer of the wafer 184 may still be attached to the inactive side B2 of the die 104a, although such a thin layer of the wafer 184 is not illustrated in Fig. 3. In another embodiment, the wafer 184 is substantially completely removed from the inactive side B2 of the die 104a, as illustrated in Fig. 3.

[0023] Figs. 4A and 4B illustrate an arrangement 400, in which the singulated die 104a of the arrangement 300 of Fig. 3 is placed on the die 102a. Fig. 4A illustrates a side view of the arrangement 400, and 4B illustrates a top view of the arrangement 400. In the arrangement 400, the die 104a is stacked on the die 102a. For example, the inactive side B2 of the die 104a is attached to the active side A1 of the die 102a. The die 104a is attached to the die 102a using, for example, an appropriate die attach material 116 (e.g., adhesive, paste, and/or another appropriate die attach material).

[0024] As discussed herein earlier, the metal posts 132 on the bond pads 112 of the die 102a are arranged such that the metal posts 132 do not occupy a section (e.g., a central section) of the active surface of the die 102a. In an embodiment, the die 104a is placed on the section of the active surface of the die 102a that is not occupied by any of the metal posts 132. Thus, for example, the die 104a is stacked on a central section of the active surface of the die 102a, while the metal posts 132 and the bond pads 112 are arranged near the periphery of the die 102a.

[0025] In an embodiment, the stacking of the die 104a on the die 102a is performed while the die 102a is still attached to the wafer 182. In an embodiment, the heights of the metal posts 132, 142 in the arrangement 200 of Fig. 2 are selected such that once the die 104a is stacked on the die 102a in the arrangement 400 of Figs. 4A and 4B, the top ends of the metal posts 132, 142 substantially lie in the same (or near same) plane.

[0026] Fig. 5 illustrates an arrangement 500, in which a molding compound 550 is formed on several components of the arrangement 400 of Figs. 4A and 4B. The molding compound 550 comprises any appropriate molding compound material, e.g., epoxy, resins, etc. In an embodiment, the molding compound 550 is deposited over the wafer 182, and substantially encapsulates the metal posts 132, 142, the bond pads 132, 142, and the dies 102, 104, as illustrated in Fig. 5.

[0027] Fig. 6 illustrates an arrangement 600, in which the molding compound 550 is at least in part removed from the arrangement 500 of Fig. 5. For example, a top surface of the molding compound 550 is grinded or otherwise removed such that the top end of the metal posts 132, 142 are exposed through the top surface of the molding compound 550. In an

embodiment, at least a part of the top ends of the metal posts 132, 142 are also removed along with removing the top surface of the molding compound 550, such that the top ends of the metal posts 132, 142 are substantially flush or are at the same plane with the top surface of the molding compound 550 (e.g., such that the top ends of the metal posts 132, 142 are exposed through the molding compound 550).

[0028] Fig. 7 illustrates an arrangement 700, in which one or more redistribution layers 702 are formed on the arrangement 600 of Fig. 6. For example, a redistribution layer 702 electrically connects a top end of a metal post 132 to a top end of a corresponding metal post 142. Thus, the one or more redistribution layers 702 routes signals between the metal posts 132 and metal posts 142, thereby routing signals between the dies 102a and 104a.

[0029] The one or more redistribution layers 702 can be formed, for example, by depositing and/or patterning an electrically conductive material such as, for example, a metal (e.g., copper or aluminum) or a doped semiconductor material (e.g., doped polysilicon) on the top surface of the molding compound 550. Other suitable electrically conductive materials can be used to form the one or more redistribution layers 702 in other embodiments.

[0030] The one or more redistribution layers 702 can include a variety of structures to route electrical signals such as, pads, lands, traces, and/or the like. Fig. 7 illustrates a single layer of the redistribution layers 702, although in another embodiment (and not illustrated in Fig. 7), more than one layer (e.g., two layers, three layers, etc.) of redistribution layers can also be used.

[0031] Fig. 8 illustrates an arrangement 800, in which a passivation layer 804 comprising an electrically insulative material such as polyimide, for example, is deposited on the redistribution layers 702 of the arrangement 700 of Fig. 7. In an embodiment, the passivation layer 804 is patterned to provide openings in the passivation layer 804. In an example, the openings are formed over one or more of the redistribution layers 702. One or more package interconnect structures 802 are placed in the openings.

[0032] The package interconnect structures 802 generally comprise an electrically conductive material. The package interconnect structures 802 can be formed in a variety of shapes including spherical, planar, or polygon shapes, and can be positioned in a variety of

positions including in a row or in an array of multiple rows. In an example, the package interconnect structures 802 comprise solder balls, metal posts, bumps, and/or the like.

[0033] In an embodiment, ones of the package interconnect structures 802 is attached to a corresponding one of the redistribution layers 702. The package interconnect structures 802 allow the dies 102a, 104a to route external signals (e.g., signals to and/or from another semiconductor package, a printed circuit board, etc., not illustrated in Fig. 8) to and/or from the dies 102a, 104a, e.g., via the bond pads 112, 114, the metal posts 132, 142, and the redistribution layers 702. The arrangement 800 forms a package assembly that is formed on the wafer 182. In an example, the package assembly of the arrangement 800 is a wafer level packaging.

[0034] Fig. 9A illustrates an arrangement 900, in which the wafer 182 is singulated such that the die 102a is separated from the other dies on the wafer 182. For example, the wafer 182 is singulated along the lines PP' and QQ' in Fig. 8. In an embodiment, the wafer 182 is at least partially removed prior to the singulation. For example, the wafer 182 is grinded to reduce a thickness of the wafer 182, prior to the singulation of the wafer 182. Accordingly, a thickness of the wafer 182 in the arrangement 900 of Fig. 9A is less than that in the arrangement 800 of Fig. 8. The arrangement 900, for example, forms a package assembly, e.g., a chip-scale package (CSP) assembly, in which the two stacked dies 102a, 104a are interconnected to each other (and also connected to external components) via the metal posts 132, 142. The package assembly of Fig. 9A can be connected to another component (e.g., an electronic device, a printed circuit board, another package assembly, etc.) via the package interconnect structures 802.

[0035] Figs. 1A-9A are directed to the die 104a being stacked on the die 102a. However, in another embodiment, more than two dies can be stacked on top of each other (e.g., one or more dies can be stacked on top of the die 104a to form three layers of stacked dies). In such an embodiment, the multiple layers of stacked dies can be interconnected using metal posts (e.g., which are similar to the metal posts 132, 142), as would be readily understood by those skilled in the art based on the teachings of this disclosure.

[0036] Fig. 9B illustrates a flow diagram of an example method 960 for forming the semiconductor package assembly of Figs. 1A-9A. At 964, a first die (e.g., die 102a of Figs. 1A-9A) is formed (e.g., formed on the wafer 182). In an example, the first die comprises (i) a first side (e.g., the active side A1) and (ii) a second side (e.g., the inactive side A2) disposed opposite the first side. Also at 964, a first plurality of bond pads (e.g., bond pads 112) is formed on the first side of the first die. Also at 964, a first plurality of metal posts (e.g., metal posts 132) is formed on the first die. In an example, each of the first plurality of metal posts is formed on a corresponding one of the first plurality of bond pads formed on the first side of the first die.

[0037] At 968, a second die (e.g., die 104a) is formed (e.g., formed on the wafer 184). In an example, the second die comprises (i) a first side (e.g., the active side B1) and (ii) a second side (e.g., the inactive side B2) disposed opposite the first side. Also at 968, a second plurality of bond pads (e.g., bond pads 114) is formed on the first side of the second die. Also at 968, a second plurality of metal posts (e.g., metal posts 142) is formed on the second die. In an example, each of the second plurality of metal posts is formed on a corresponding one of the second plurality of bond pads formed on the first side of the second die.

[0038] At 972, the second die is stacked on the first die such that the second side of the second die is attached to the first side of the first die, e.g., as illustrated in Figs. 4A and 4B. At 976, a redistribution layer (e.g., one of the redistribution layers 702 of Figs. 7 and 8) is formed. In an example, the redistribution layer electrically couples (i) a first metal post of the first plurality of metal posts and (ii) a second metal post of the second plurality of metal posts. In an example, the first die, the second die, the first and second plurality of metal posts, and the redistribution layer form a semiconductor package assembly. In an example, the first die communicates with the second die via at least the first metal post, the redistribution layer, and the second metal post.

[0039] In Figs. 1A-9A, the bond pads 112 (and the metal posts 132) are disposed near a periphery of the die 102a, but not disposed on a central section of the die 102a. However, in another embodiment, it may be desired to dispose the bond pads even in a central section of a die, on which another die is stacked.

[0040] Figs. 10A-14 illustrate formation a package assembly comprising a die 1004a stacked on a die 1002a, where the die 1002a comprises bond pads disposed even in a central section of an active surface of the die 1002a. Referring to Fig. 10a, this figure illustrates an arrangement 1000 in which the die 1002a is formed on a wafer 1082, and the die 1004a is formed on a wafer 1084. The wafers 1082, 1084 are substantially similar to the wafers 182, 184 of Fig. 1A, and hence, the wafers 1082, 1084 (and various dies formed on these wafers) are not discussed in further detail herein.

[0041] Fig. 10B illustrates a top view of the dies 1002a and 1004a. Similar to dies 102a, 104a of Figs. 1A and 1B, the dies 1002a, 1004a of Figs. 10A and 10B has bond pads 1012, 1014 disposed throughout an active surface of the dies 1002a, 1004a, respectively. However, unlike the die 102a of Figs. 1A and 1B (in which no bond pads were disposed in the central section of the die 102a), the die 1002a of Figs. 10A and 10B has bond pads 1012 disposed throughout an active surface of the die 1002a. For example, some of the bond pads 1012 are disposed on a central section of the die 1002a, while some of the bond pads 1012 are disposed near the periphery of the die 1002a.

[0042] Fig. 11 illustrates an arrangement 1100, in which one or more redistribution layers 1140 are formed on the die 1002a. For example, each of the redistribution layers 1140 has a first end attached to a corresponding one of the bond pads 1012, and a second end that is disposed near a periphery of the die 1002a. That is, none of the second ends of the redistribution layers 1140 is disposed on a central section of the die 1002a (although the central section of the die 1002a has at least some of the bond pads 1012 disposed thereon). The one or more redistribution layers 1140 can be formed, for example, by depositing and/or patterning an electrically conductive material such as, for example, a metal (e.g., copper or aluminum) or a doped semiconductor material (e.g., doped polysilicon) on the active surface of the die 1002a. Other suitable electrically conductive materials can be used to form the one or more redistribution layers 1140 in other embodiments.

[0043] Fig. 11 also illustrates a passivation layer 1150 comprising an electrically insulative material (such as polyimide, for example) being deposited on the redistribution layers 1140. In an embodiment, the passivation layer 1150 is patterned to provide openings in the

passivation layer. In an example, the openings are formed over the above discussed second ends of the redistribution layers 1140. Thus, the passivation layer 1150 encapsulates the bond pads 1012 and the first ends of the redistribution layers 1140 (e.g., where the first end of a redistribution layer 1140 is the end that is attached to a corresponding bond pad 1012), while the passivation layer 1150 exposes the second ends of the redistribution layers 1140 (e.g., where the second end of a redistribution layer 1140 is opposite to the first end of the redistribution layer 1140).

[0044] Fig. 12 illustrates an arrangement 1200, in which metal posts 1032 are formed on the second ends of the redistribution layers 1140 of the die 1002a, and metal posts 1042 are formed on the bond pads 1014 of the die 1004a. As the second ends of the redistribution layers 1140 are not disposed in the central section of the active surface of the die 1002a, the metal posts 1032 are also not disposed in the central section of the active surface of the die 1002a. The metal posts 1032, for example, are disposed along or near the periphery of the active surface of the die 1002a. Metal posts have been previously discussed herein in detail, and accordingly, a more detailed description of the metal posts 1032, 1042 is omitted herein.

[0045] Although not illustrated in the figures (and as discussed with respect to Fig. 3), the wafer 1084 in the arrangement 1200 is singulated such that the die 1004a is separated from other dies in the wafer 1084. As also discussed with respect to Fig. 3, the wafer 1084 is grinded to at least partially or completely remove the wafer 1084 from the inactive side of the die 1004a.

[0046] As illustrated in Fig. 13, in an arrangement 1300, the die 1004a is then stacked on the die 1002a, as discussed with respect to Figs. 4A and 4B previously herein. Although not illustrated in the figures, the arrangement 1300 is then processed in a manner that is at least in part similar to the processing discussed with respect to Figs. 5-9A. As illustrated in Fig. 14, such processing involves, for example, encapsulating the arrangement 1300 by a molding compound 1550, grinding the molding compound 1550 to expose the top ends of the metal posts 1032, 1042, forming redistribution layers 1072 on the top surface of the molding compound 1550, depositing passivation layer 1804 on the redistribution layers 1072, forming openings in the passivation layer 1804, forming package interconnect structures 1802 in the

openings of the passivation layer 1804, singulating the wafer 1082 to separate the die 1002a from other dies of the wafer 1082, and reducing a thickness of the wafer 1082. Such processing has been discussed in detail herein earlier, and will not be repeated for the sake of brevity. Such processing results in a final package assembly 1400, as illustrated in Fig. 14.

[0047] In an example, various operations discussed herein above can be appropriately modified. For example, Figs. 12 and 13 illustrate forming metal posts on the dies 1002a, 1004a, and subsequently stacking the die 1004a on the die 1002a. However, in another embodiment, the operations described with respect to Fig. 12 can be bypassed. For example, subsequent to the arrangement 1100 of Fig. 11, the die 1004a can be stacked on the die 1002a (e.g., prior to forming any metal posts on the dies 1004a, 1002a, not illustrated in the figures). Subsequent to stacking the die 1004a on the die 1002a, the metal posts 1032 can be formed on the second ends of the redistribution layers 1140 of the die 1002a, and the metal posts 1042 can be formed on the bond pads 1014 the die 1004a, thereby resulting in the arrangement 1300 of Fig. 13.

[0048] The arrangement 1400, for example, forms a package assembly, e.g., a chip-scale package (CSP) assembly, in which the two stacked dies 1002a, 1004a are interconnected to each other (and also connected to external components) via the metal posts 1032, 1042. The redistribution layers 1140 allow one or more of the bond pads 1012 to be formed even on a central section of the die 1002a, as discussed herein earlier. The package assembly of Fig. 14 can be connected to another component (e.g., an electronic device, a printed circuit board, another package assembly, etc.) via the package interconnect structures 1802.

[0049] Further aspects of the present invention relate to one or more of the following clauses. In an example, a semiconductor package comprises a first die having (i) a first side and (ii) a second side disposed opposite the first side of the first die, wherein the first die comprises a first plurality of bond pads formed on the first side of the first die; a second die having (i) a first side and (ii) a second side disposed opposite the first side of the second die, wherein the second die comprises a second plurality of bond pads formed on the first side of the second die, wherein the second die is stacked on the first die such that the second side of the second die is attached to the first side of the first die; a first plurality of metal posts, wherein each of the first

plurality of metal posts is formed on a corresponding one of the first plurality of bond pads formed on the first side of the first die; a second plurality of metal posts, wherein each of the second plurality of metal posts is formed on a corresponding one of the second plurality of bond pads formed on the first side of the second die; and a redistribution layer configured to electrically couple (i) a first metal post of the first plurality of metal posts and (ii) a second metal post of the second plurality of metal posts. In an example, each of the first plurality of metal posts comprises (i) a first end that is attached to the corresponding one of the first plurality of bond pads formed on the first side of the first die and (ii) a second end that is opposite the first end; each of the second plurality of metal posts comprises (i) a first end that is attached to the corresponding one of the second plurality of bond pads formed on the first side of the second die and (ii) a second end that is opposite the first end; and the redistribution layer is configured to electrically couple (i) a second end of the first metal post of the first plurality of metal posts and (ii) a second end of the second metal post of the second plurality of metal posts. In an example, the semiconductor package further comprises a substrate, wherein the second side of the first die is attached to the substrate. In an example, the semiconductor package further comprises a molding compound that substantially surrounds the first plurality of metal posts and the second plurality of metal posts. In an example, the semiconductor package further comprises die attach material, wherein the second side of the second die is attached to the first side of the first die via the die attach material. In an example, the semiconductor package further comprises a package interconnect structure formed on the redistribution layer, wherein the package interconnect structure is configured to route signals between (i) the semiconductor package and (ii) a component that is external to the semiconductor package. In an example, the first plurality of bond pads are formed near a periphery of the first side of the first die; and the second die is stacked on the first die such that the second side of the second die is attached to a central section of the first side of the first die. In an example, the second die is stacked on the first die such that the second side of the second die is attached to a first section of the first side of the first die; and no bond pad of the first plurality of bond pads is formed on the first section of the first side of the first die.

[0050] In an example, a method of forming a semiconductor package comprises forming a first die, the first die comprising (i) a first side and (ii) a second side disposed opposite the first side of the first die; forming a first plurality of bond pads on the first side of the first die; forming a second die, the second die comprising (i) a first side and (ii) a second side disposed opposite the first side of the second die; forming a second plurality of bond pads on the first side of the second die; forming a first plurality of metal posts, wherein each of the first plurality of metal posts is formed on a corresponding one of the first plurality of bond pads formed on the first side of the first die; forming a second plurality of metal posts, wherein each of the second plurality of metal posts is formed on a corresponding one of the second plurality of bond pads formed on the first side of the second die; subsequent to forming the first plurality of metal posts and the second plurality of metal posts, stacking the second die on the first die such that the second side of the second die is attached to the first side of the first die; and forming a redistribution layer that electrically couples (i) a first metal post of the first plurality of metal posts and (ii) a second metal post of the second plurality of metal posts. In an example, each of the first plurality of metal posts comprises (i) a first end that is attached to the corresponding one of the first plurality of bond pads formed on the first side of the first die and (ii) a second end that is opposite the first end, wherein each of the second plurality of metal posts comprises (i) a first end that is attached to the corresponding one of the second plurality of bond pads formed on the first side of the second die and (ii) a second end that is opposite the first end, and wherein forming the redistribution layer comprises: forming the redistribution layer such that the redistribution layer is attached to (i) a second end of the first metal post of the first plurality of metal posts and (ii) a second end of the second metal post of the second plurality of metal posts. In an example, forming the first die comprises forming a first plurality of dies on a first wafer, the first plurality of dies including the first die; forming the second die comprises forming a second plurality of dies on a second wafer, the second plurality of dies including the second die; the second side of the first die is attached to the first wafer and the second side of the second die is attached to the second wafer; forming the first plurality of metal posts comprises while the first die is attached to the first wafer, forming the first plurality of metal posts on the first die; and forming the second plurality of metal posts

comprises while the second die is attached to the second wafer, forming the second plurality of metal posts on the second die. In an example, the method further comprises subsequent to forming the second plurality of metal posts and prior to stacking the second die on the first die, removing the second die from the second wafer, wherein while the first die is attached to the first wafer, the second die is stacked on the first die. In an example, the method further comprises forming a molding compound that substantially surrounds the first plurality of metal posts and the second plurality of metal posts. In an example, stacking the second die on the first die comprises: stacking the second die on the first die such that the second side of the second die is attached to the first side of the first die via die attach material. In an example, the method further comprises forming a package interconnect structure on the redistribution layer; routing signals, via the package interconnect structure, between (i) the semiconductor package comprising the first die and the second die, and (ii) a component that is external to the semiconductor package. In an example, forming the first plurality of bond pads on the first side of the first die comprises forming the first plurality of bond pads near a periphery of the first side of the first die; and stacking the second die on the first die comprises stacking the second die on the first die such that the second side of the second die is attached to a central section of the first side of the first die. In an example, stacking the second die on the first die comprises stacking the second die on the first die such that the second side of the second die is attached to a first section of the first side of the first die; and no bond pad of the first plurality of bond pads is formed on the first section of the first side of the first die.

[0051] In an example, a semiconductor package comprises a first die having (i) a first side and (ii) a second side disposed opposite the first side of the first die, wherein the first die comprises a first bond pad formed on the first side of the first die; a second die having (i) a first side and (ii) a second side disposed opposite the first side of the second die, wherein the second die comprises a second bond pad formed on the first side of the second die, wherein the second die is stacked on the first die such that the second side of the second die faces the first side of the first die; a first redistribution layer formed on the first side of the first die, wherein the first redistribution layer comprises (i) a first end attached to the first bond pad, and (ii) a second end that is opposite to the first end; a first metal post formed on the second end of

the first redistribution layer; a second metal post formed on the second bond pad that is formed on the first side of the second die; and a second redistribution layer configured to electrically couple (i) the first metal post and (ii) the second metal post. In an example, the semiconductor package further comprises a passivation layer formed on the first side of the first die, wherein the passivation layer at least in part covers the first bond pad formed on the first side of the first die, wherein the second die is stacked on the first die such that the second side of the second die is over a section of the passivation layer that covers the first bond pad. In an example, the semiconductor package further comprises a molding compound that substantially surrounds the first metal post and the second metal post.

[0052] The description may use the phrases “in an embodiment,” or “in embodiments,” which may each refer to one or more of the same or different embodiments. The terms “comprising,” “having,” and “including” are synonymous, unless the context dictates otherwise. The phrase “A and/or B” means (A), (B), or (A and B). The phrase “A/B” means (A), (B), or (A and B), similar to the phrase “A and/or B.” The phrase “at least one of A, B and C” means (A), (B), (C), (A and B), (A and C), (B and C) or (A, B and C). The phrase “(A) B” means (B) or (A and B), that is, A is optional.

[0053] Although certain embodiments have been illustrated and described herein, a wide variety of alternate and/or equivalent embodiments or implementations calculated to achieve the same purposes may be substituted for the embodiments illustrated and described without departing from the scope of the present invention. This application is intended to cover any adaptations or variations of the embodiments discussed herein. Therefore, it is manifestly intended that embodiments in accordance with the present invention be limited only by the claims and the equivalents thereof.

Claims

What is claimed is:

1. A semiconductor package comprising:

a first die having (i) a first side and (ii) a second side disposed opposite the first side of the first die, wherein the first die comprises a first plurality of bond pads formed on the first side of the first die;

a second die having (i) a first side and (ii) a second side disposed opposite the first side of the second die, wherein the second die comprises a second plurality of bond pads formed on the first side of the second die, wherein the second die is stacked on the first die such that the second side of the second die is attached to the first side of the first die;

a first plurality of metal posts, wherein each of the first plurality of metal posts is formed on a corresponding one of the first plurality of bond pads formed on the first side of the first die;

a second plurality of metal posts, wherein each of the second plurality of metal posts is formed on a corresponding one of the second plurality of bond pads formed on the first side of the second die; and

a redistribution layer configured to electrically couple (i) a first metal post of the first plurality of metal posts and (ii) a second metal post of the second plurality of metal posts.

2. The semiconductor package of claim 1, wherein:

each of the first plurality of metal posts comprises (i) a first end that is attached to the corresponding one of the first plurality of bond pads formed on the first side of the first die and (ii) a second end that is opposite the first end;

each of the second plurality of metal posts comprises (i) a first end that is attached to the corresponding one of the second plurality of bond pads formed on the first side of the second die and (ii) a second end that is opposite the first end; and

the redistribution layer is configured to electrically couple (i) a second end of the first metal post of the first plurality of metal posts and (ii) a second end of the second metal post of the second plurality of metal posts.

3. The semiconductor package of claim 1, further comprising:
a substrate, wherein the second side of the first die is attached to the substrate.
4. The semiconductor package of claim 1, further comprising:
a molding compound that substantially surrounds the first plurality of metal posts and the second plurality of metal posts.
5. The semiconductor package of claim 1, further comprising:
die attach material, wherein the second side of the second die is attached to the first side of the first die via the die attach material.
6. The semiconductor package of claim 1, further comprising:
a package interconnect structure formed on the redistribution layer, wherein the package interconnect structure is configured to route signals between (i) the semiconductor package and (ii) a component that is external to the semiconductor package.
7. The semiconductor package of claim 1, wherein:
the first plurality of bond pads are formed near a periphery of the first side of the first die; and
the second die is stacked on the first die such that the second side of the second die is attached to a central section of the first side of the first die.
8. The semiconductor package of claim 1, wherein:
the second die is stacked on the first die such that the second side of the second die is attached to a first section of the first side of the first die; and
no bond pad of the first plurality of bond pads is formed on the first section of the first side of the first die.

9. A method of forming a semiconductor package, the method comprising:
- forming a first die, the first die comprising (i) a first side and (ii) a second side disposed opposite the first side of the first die;
 - forming a first plurality of bond pads on the first side of the first die;
 - forming a second die, the second die comprising (i) a first side and (ii) a second side disposed opposite the first side of the second die;
 - forming a second plurality of bond pads on the first side of the second die;
 - forming a first plurality of metal posts, wherein each of the first plurality of metal posts is formed on a corresponding one of the first plurality of bond pads formed on the first side of the first die;
 - forming a second plurality of metal posts, wherein each of the second plurality of metal posts is formed on a corresponding one of the second plurality of bond pads formed on the first side of the second die;
 - subsequent to forming the first plurality of metal posts and the second plurality of metal posts, stacking the second die on the first die such that the second side of the second die is attached to the first side of the first die; and
 - forming a redistribution layer that electrically couples (i) a first metal post of the first plurality of metal posts and (ii) a second metal post of the second plurality of metal posts.
10. The method of claim 9, wherein each of the first plurality of metal posts comprises (i) a first end that is attached to the corresponding one of the first plurality of bond pads formed on the first side of the first die and (ii) a second end that is opposite the first end, wherein each of the second plurality of metal posts comprises (i) a first end that is attached to the corresponding one of the second plurality of bond pads formed on the first side of the second die and (ii) a second end that is opposite the first end, and wherein forming the redistribution layer comprises:
- forming the redistribution layer such that the redistribution layer is attached to (i) a second end of the first metal post of the first plurality of metal posts and (ii) a second end of the second metal post of the second plurality of metal posts.

11. The method of claim 9, wherein:
 - forming the first die comprises
 - forming a first plurality of dies on a first wafer, the first plurality of dies including the first die;
 - forming the second die comprises
 - forming a second plurality of dies on a second wafer, the second plurality of dies including the second die;
 - the second side of the first die is attached to the first wafer and the second side of the second die is attached to the second wafer;
 - forming the first plurality of metal posts comprises
 - while the first die is attached to the first wafer, forming the first plurality of metal posts on the first die; and
 - forming the second plurality of metal posts comprises
 - while the second die is attached to the second wafer, forming the second plurality of metal posts on the second die.
12. The method of claim 11, further comprising:
 - subsequent to forming the second plurality of metal posts and prior to stacking the second die on the first die, removing the second die from the second wafer,
 - wherein while the first die is attached to the first wafer, the second die is stacked on the first die.
13. The method of claim 9, further comprising:
 - forming a molding compound that substantially surrounds the first plurality of metal posts and the second plurality of metal posts.

14. The method of claim 9, wherein stacking the second die on the first die comprises:
stacking the second die on the first die such that the second side of the second die is attached to the first side of the first die via die attach material.
15. The method of claim 9, further comprising:
forming a package interconnect structure on the redistribution layer;
routing signals, via the package interconnect structure, between (i) the semiconductor package comprising the first die and the second die, and (ii) a component that is external to the semiconductor package.
16. The method of claim 9, wherein:
forming the first plurality of bond pads on the first side of the first die comprises
forming the first plurality of bond pads near a periphery of the first side of the first die; and
stacking the second die on the first die comprises
stacking the second die on the first die such that the second side of the second die is attached to a central section of the first side of the first die.
17. The method of claim 9, wherein:
stacking the second die on the first die comprises
stacking the second die on the first die such that the second side of the second die is attached to a first section of the first side of the first die; and
no bond pad of the first plurality of bond pads is formed on the first section of the first side of the first die.
18. A semiconductor package comprising:
a first die having (i) a first side and (ii) a second side disposed opposite the first side of the first die, wherein the first die comprises a first bond pad formed on the first side of the first die;

a second die having (i) a first side and (ii) a second side disposed opposite the first side of the second die, wherein the second die comprises a second bond pad formed on the first side of the second die, wherein the second die is stacked on the first die such that the second side of the second die faces the first side of the first die;

a first redistribution layer formed on the first side of the first die, wherein the first redistribution layer comprises (i) a first end attached to the first bond pad, and (ii) a second end that is opposite to the first end;

a first metal post formed on the second end of the first redistribution layer;

a second metal post formed on the second bond pad that is formed on the first side of the second die; and

a second redistribution layer configured to electrically couple (i) the first metal post and (ii) the second metal post.

19. The semiconductor package of claim 18, further comprising:

a passivation layer formed on the first side of the first die, wherein the passivation layer at least in part covers the first bond pad formed on the first side of the first die,

wherein the second die is stacked on the first die such that the second side of the second die is over a section of the passivation layer that covers the first bond pad.

20. The semiconductor package of claim 18, further comprising:

a molding compound that substantially surrounds the first metal post and the second metal post.

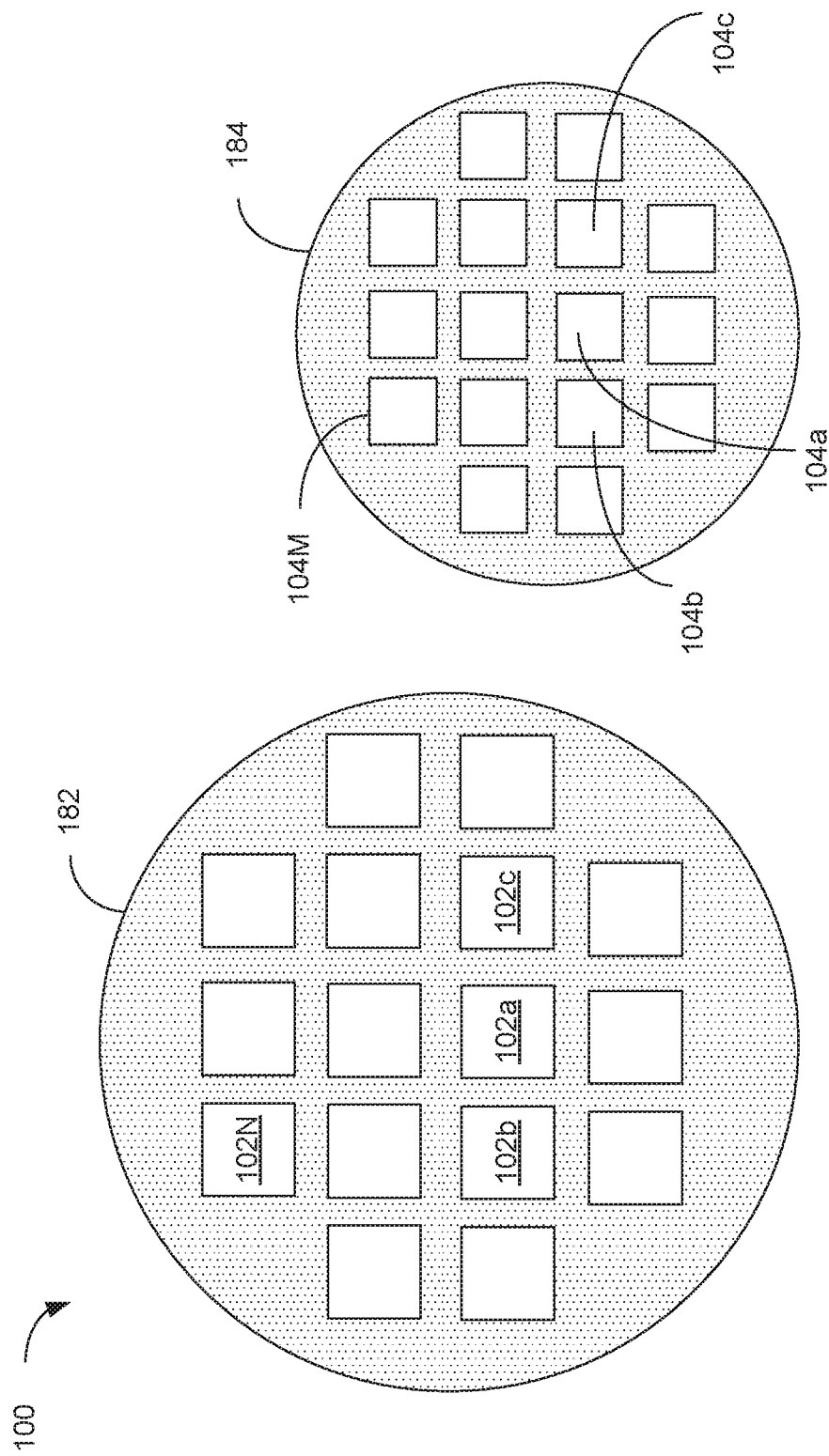


Fig. 1A

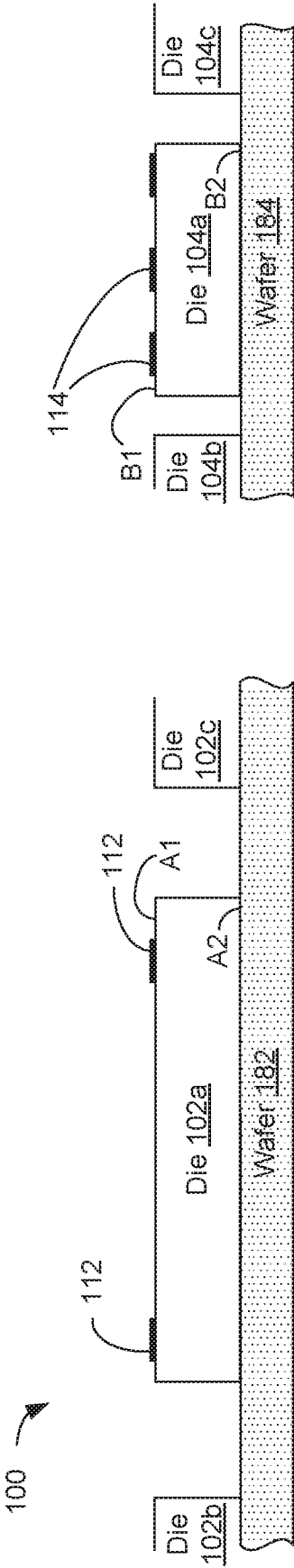


Fig. 1B

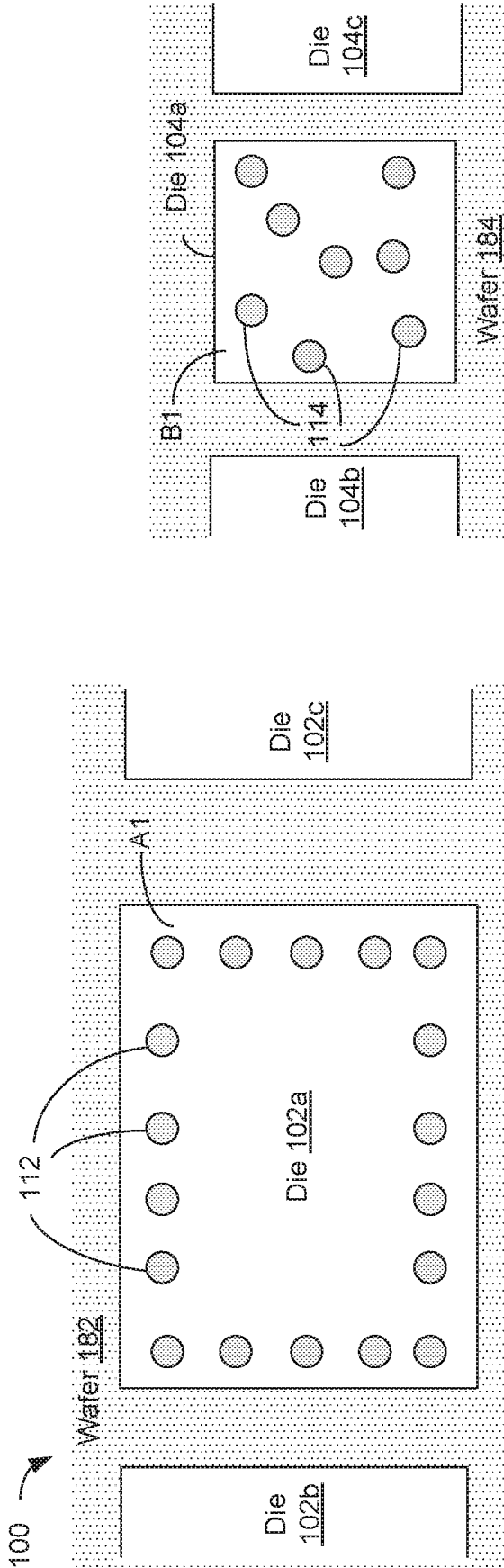


Fig. 1C

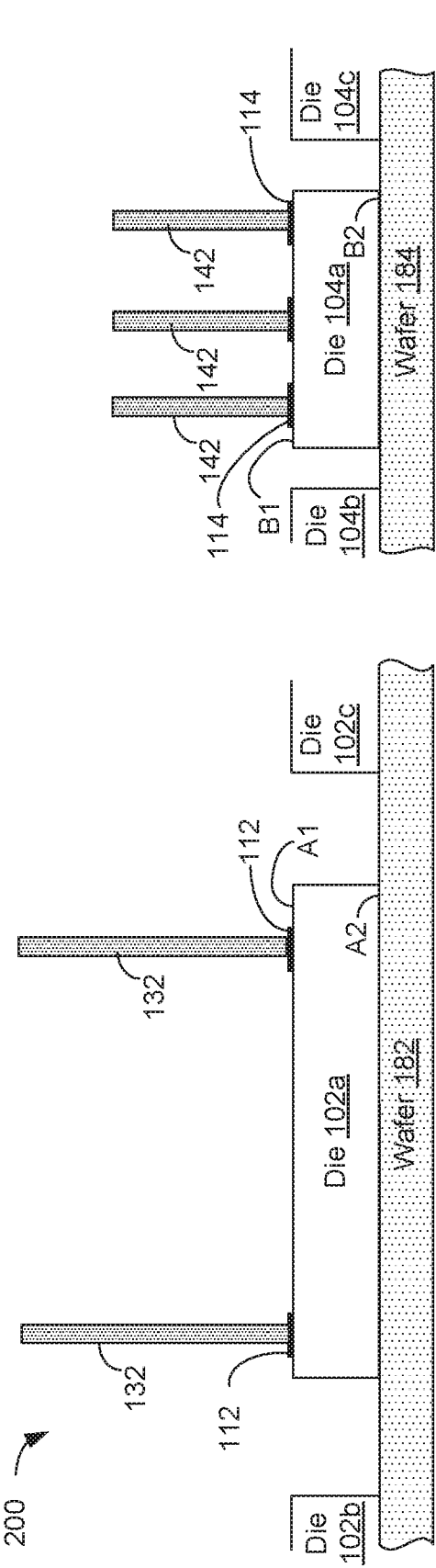


Fig. 2

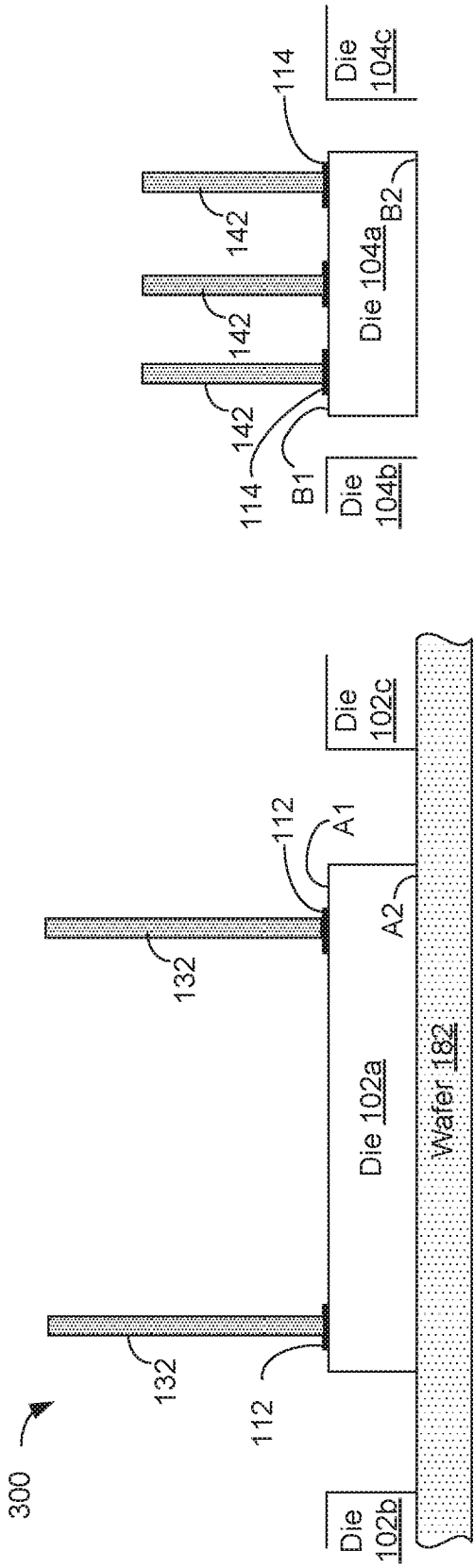


Fig. 3

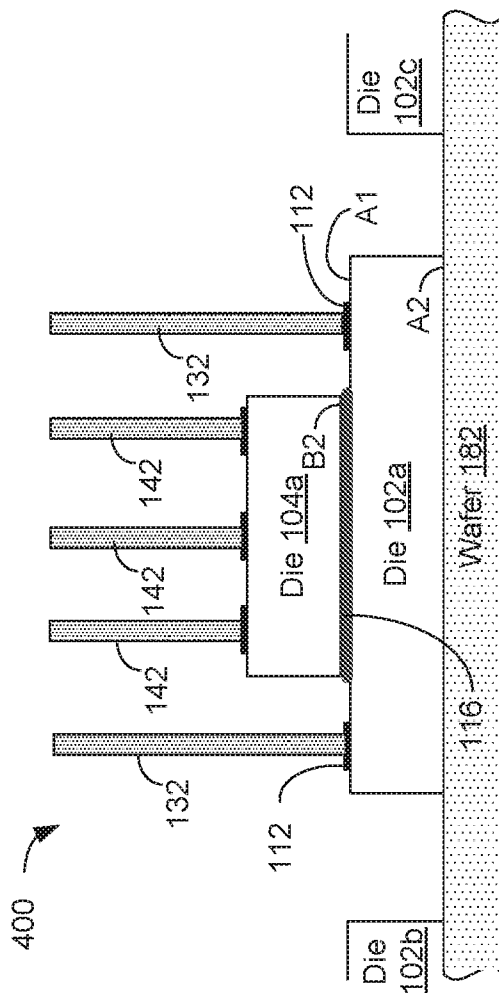
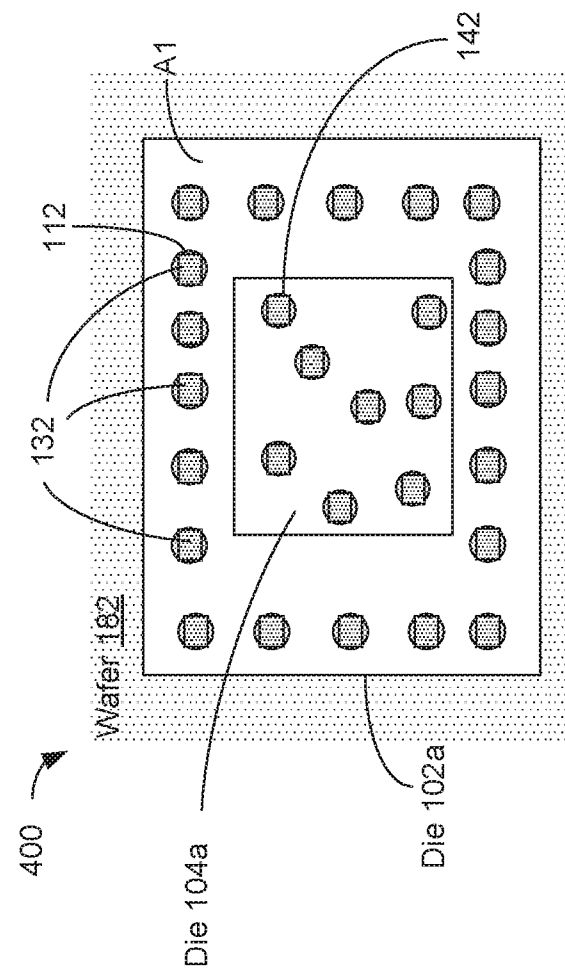
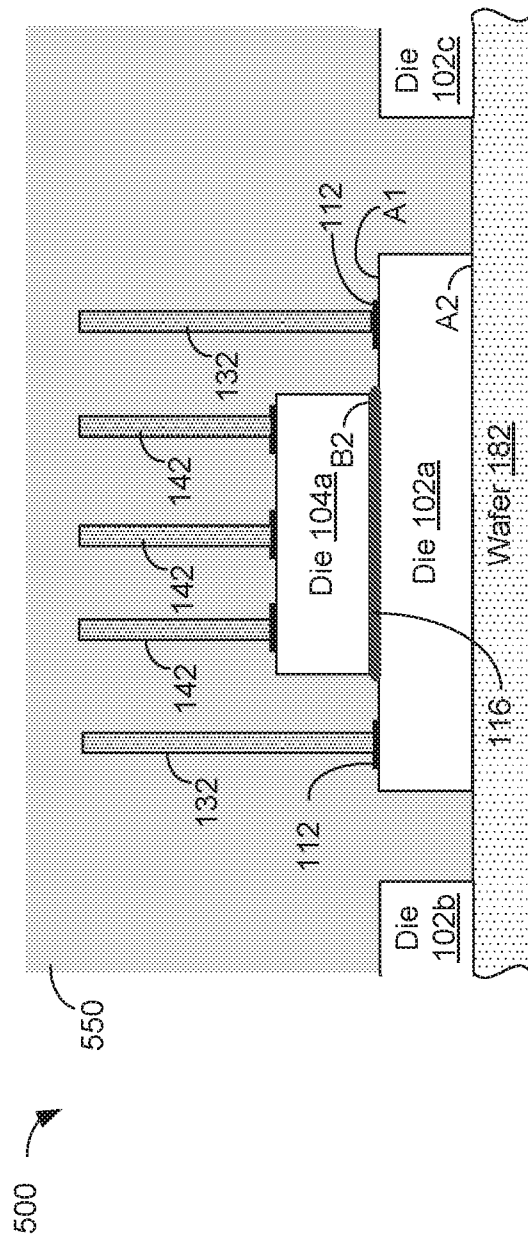


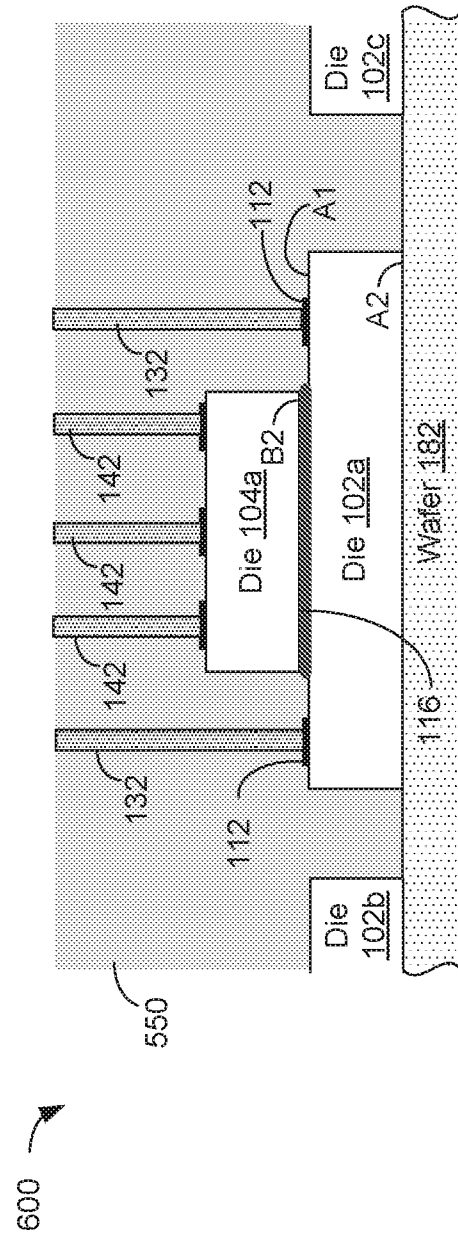
Fig. 4A







 DEPARTMENT OF HEALTH AND HUMAN SERVICES



The image shows a vertical sequence of four stages of a fractal construction. The top stage is a simple 'L' shape. The second stage is a more complex 'L' shape with a small square added to the top horizontal bar. The third stage is a more complex 'L' shape with a small square added to the top horizontal bar and a small square added to the vertical bar. The bottom stage is a highly complex 'L' shape with many small squares added to the top horizontal bar and the vertical bar, creating a fractal-like structure.

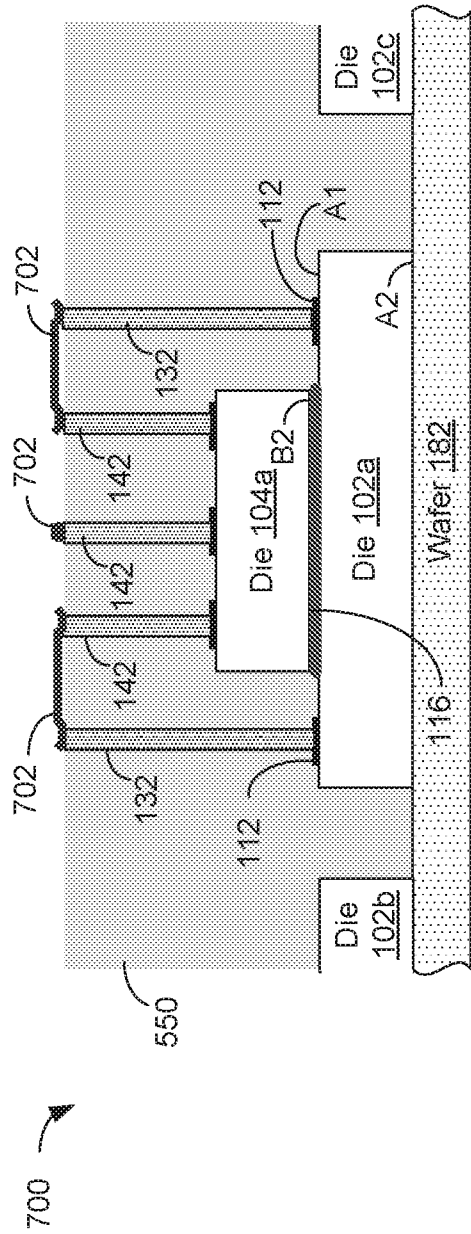


Fig. 7

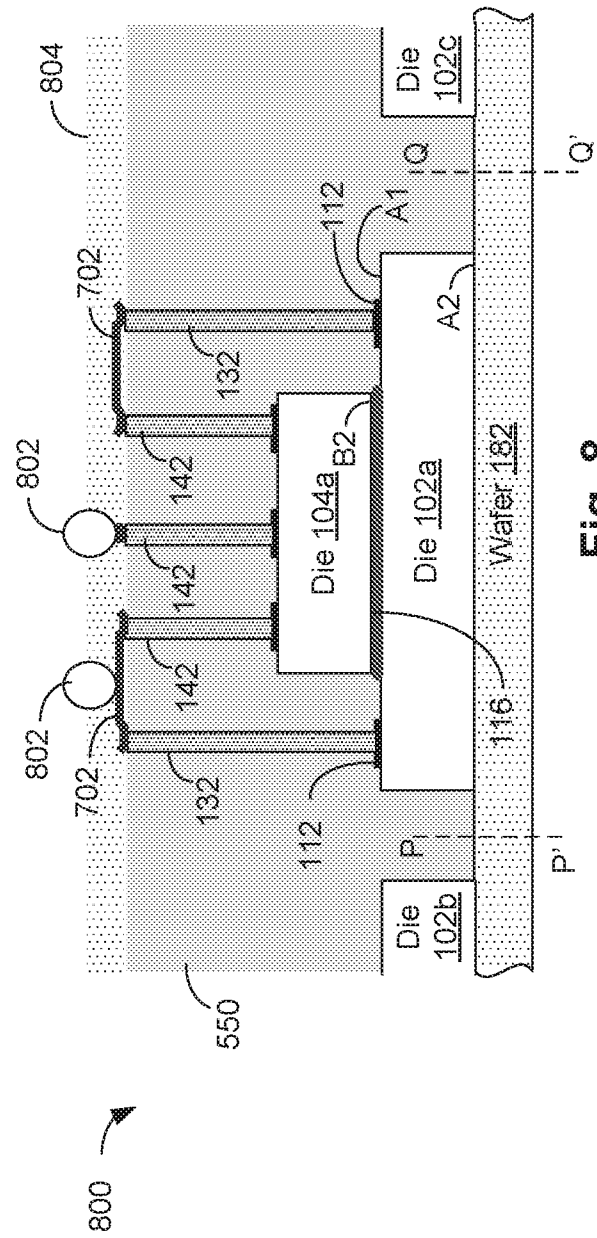
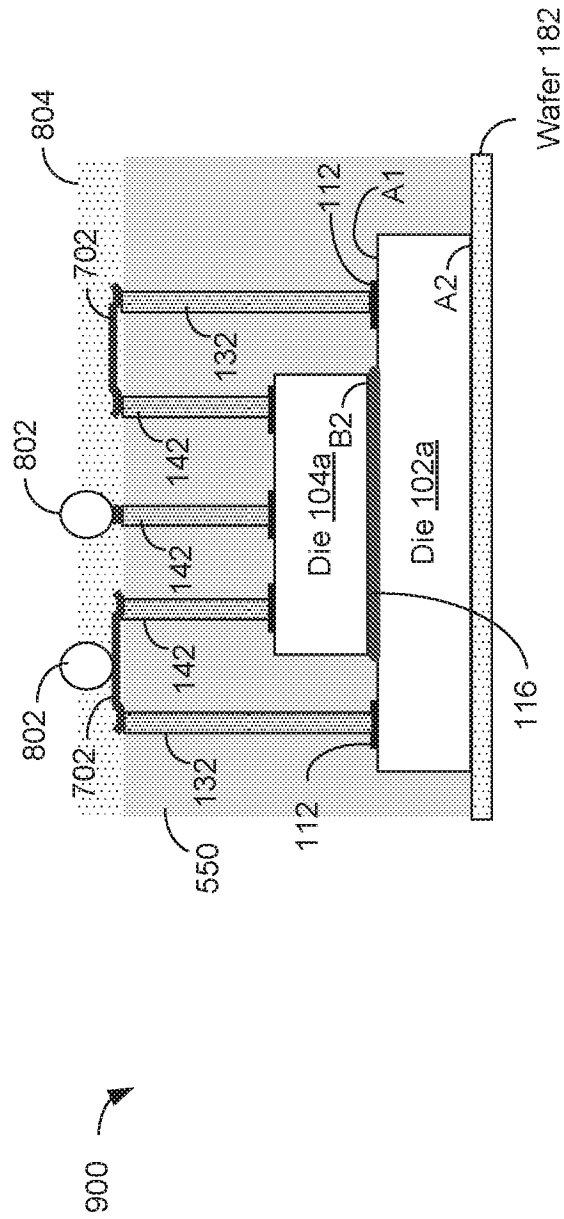
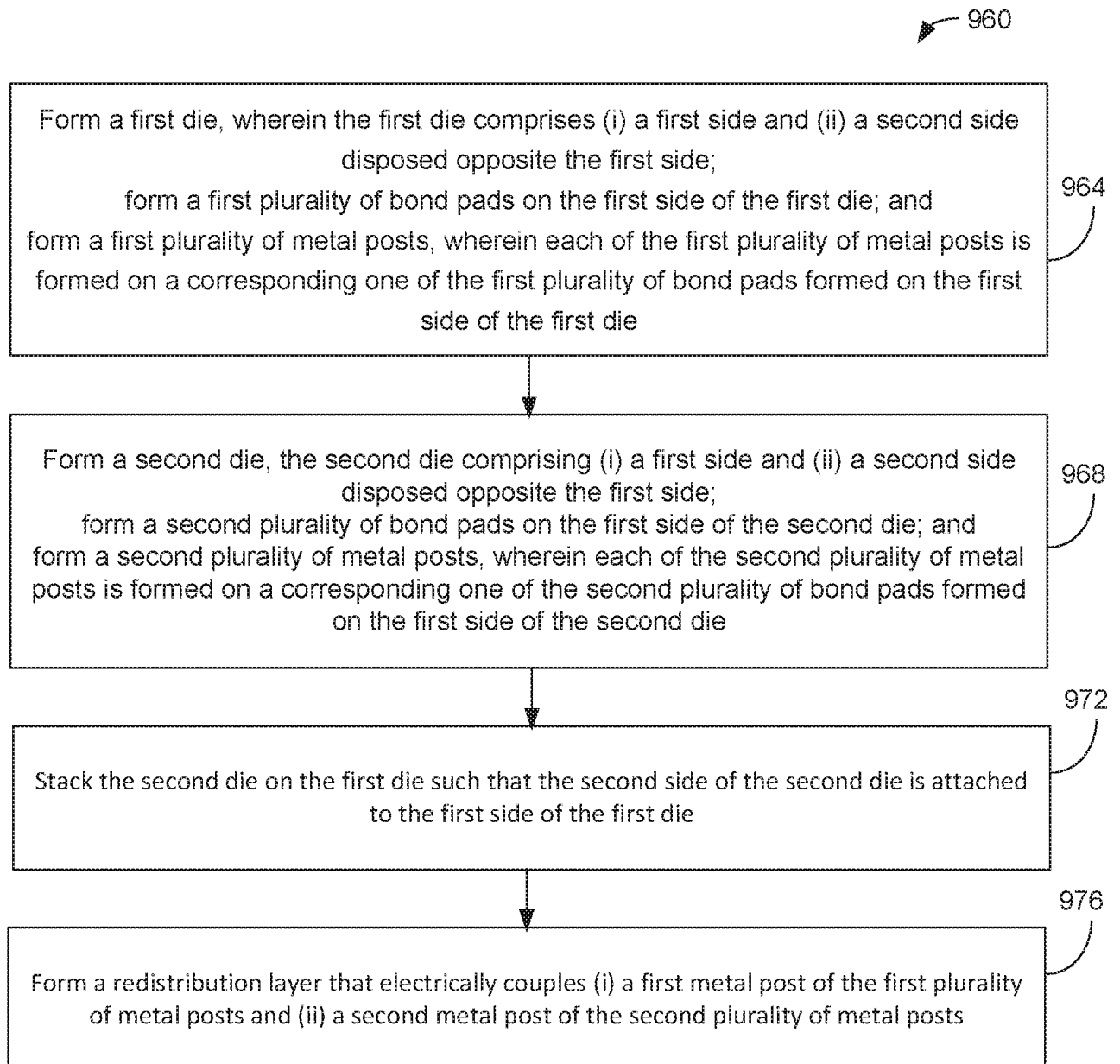


Fig. 8



**Fig. 9B**

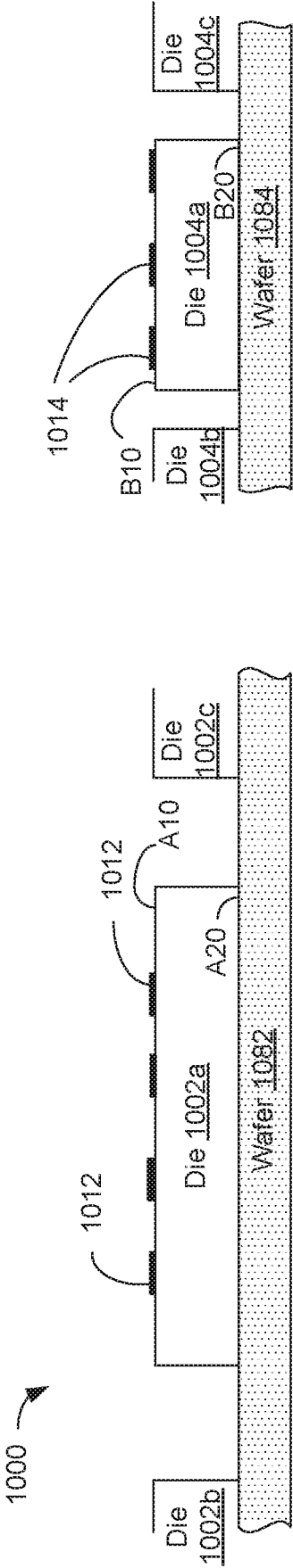


Fig. 10A

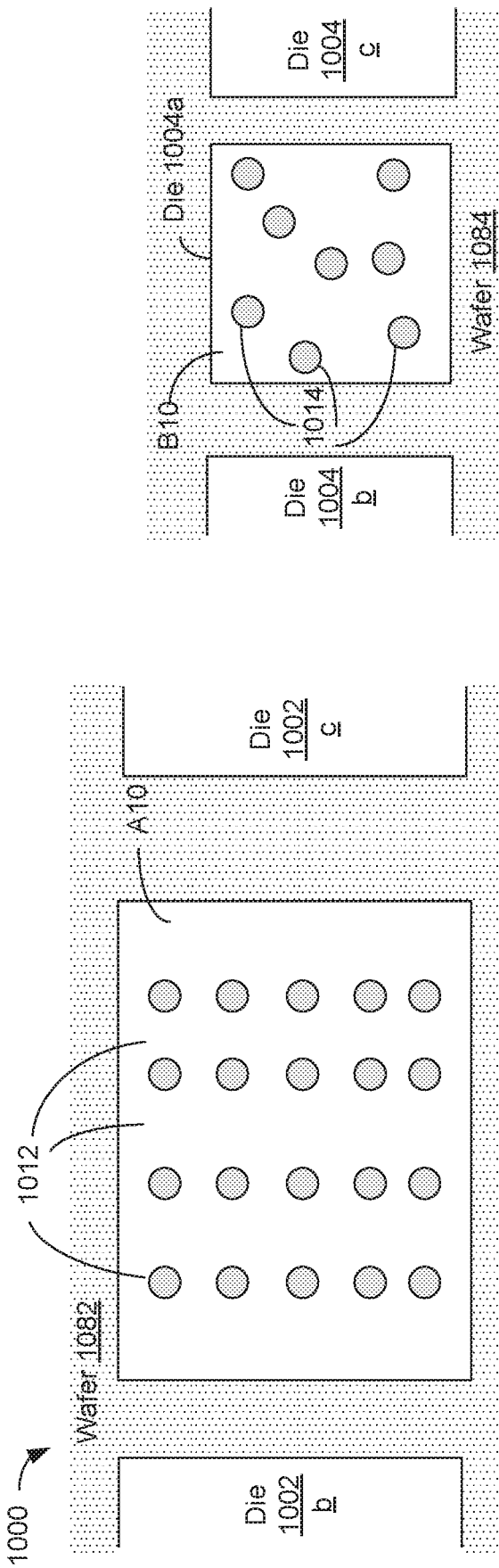


Fig. 10B

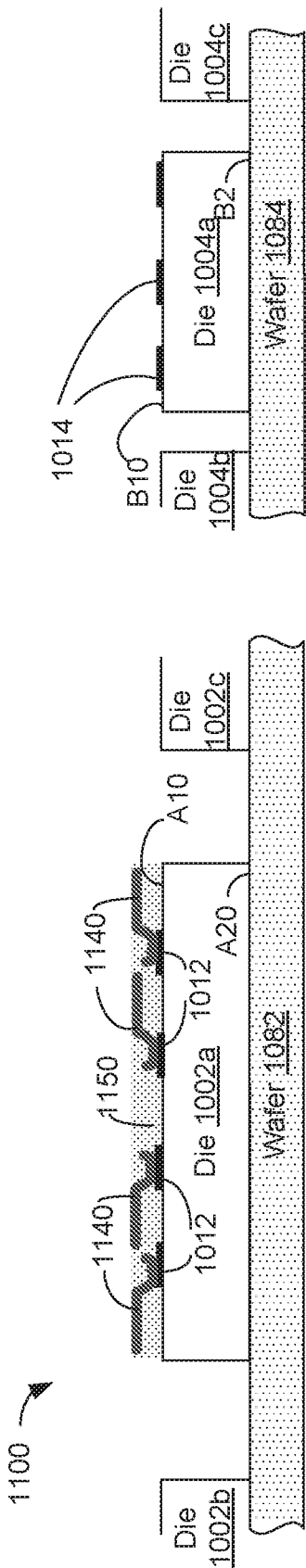


Fig. 11

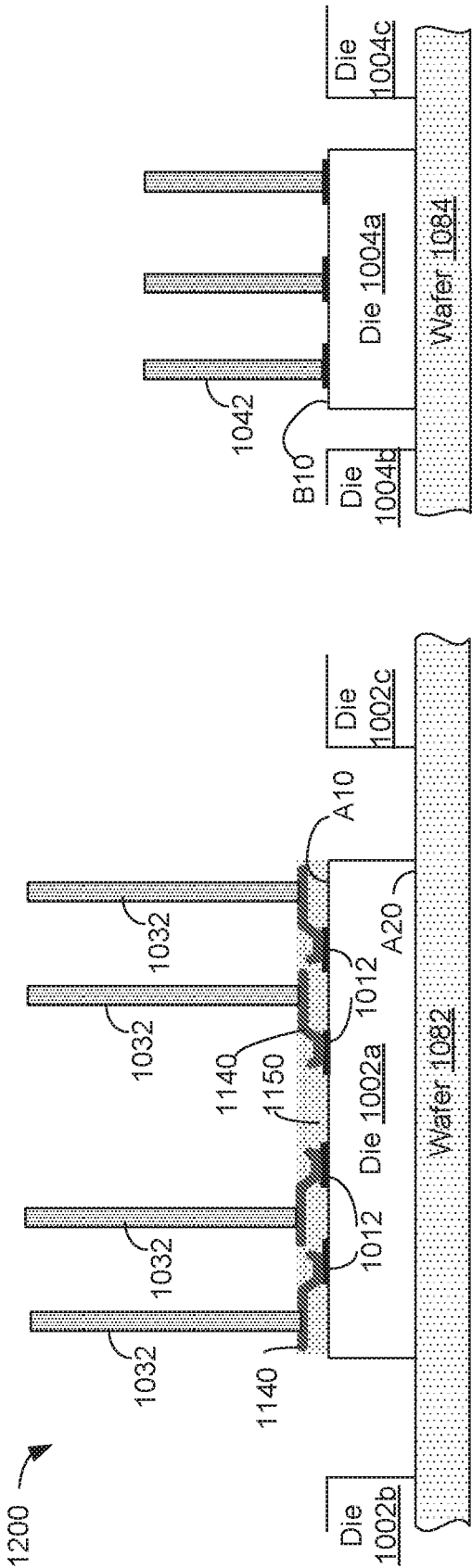


Fig. 12

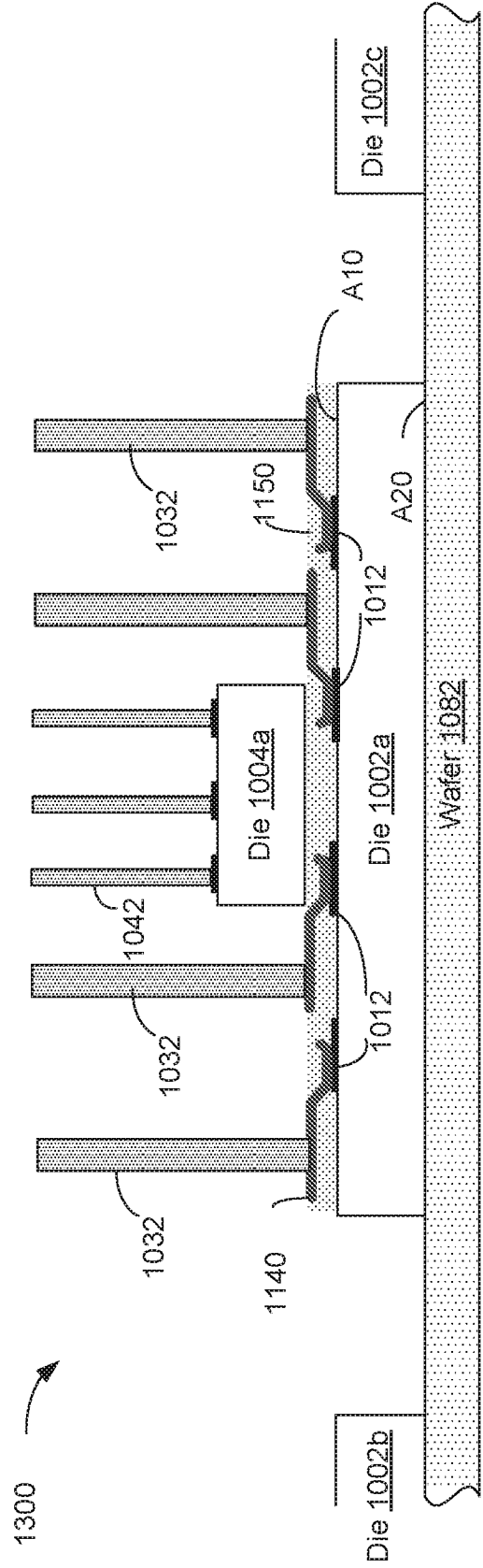


Fig. 13

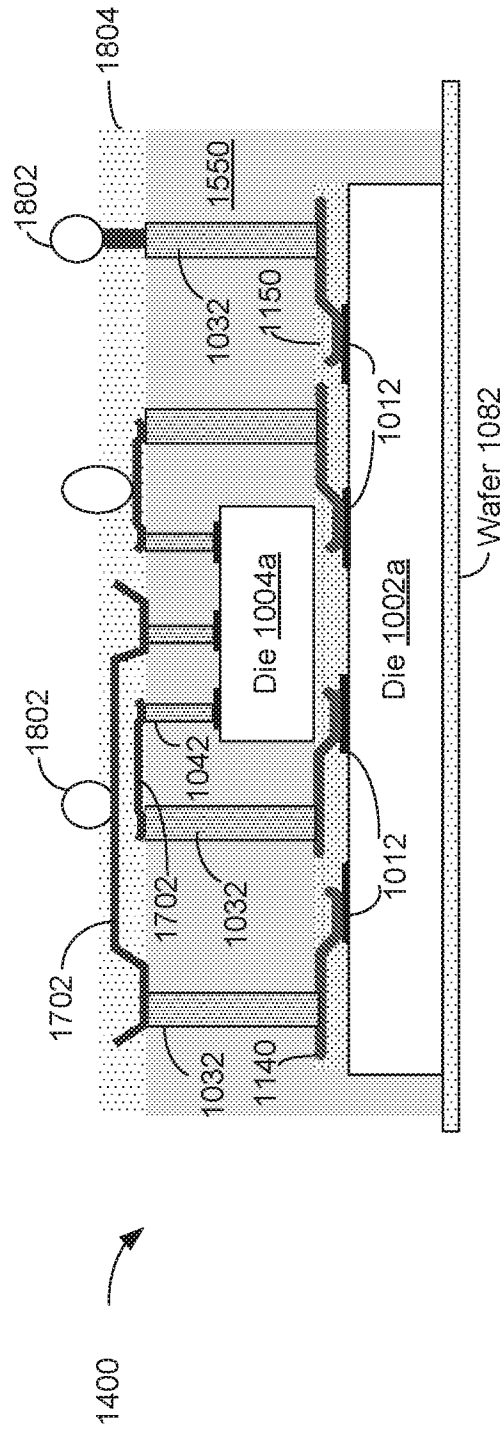


Fig. 14

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/018640

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/60 H01L23/31
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2009/022991 A1 (AGENCY SCIENCE TECH & RES [SG]; KRIPESH VAIDYANATHAN [SG]; ORATTI KALA) 19 February 2009 (2009-02-19) paragraphs [0032], [0040], [0042], [0043], [0045], [0046]; figures 1,2,3a-3j -----	1,2, 4-10, 13-17

☐

Further documents are listed in the continuation of Box C.

☒

See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

17 May 2016

Date of mailing of the international search report

02/08/2016

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Manook, Rhoda

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/018640

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1, 2, 4-10, 13-17

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1, 2, 4-10, 13-17

Group Ia: Directed to the subject matter of claims 1-2,4-10,11-17 (c.f. claims 2 and 10)

Re. cls. 2 and 10 the surplus technical features with respect to the known claims 1 and 9 (see the attached reasoning for the lack of novelty of claims 1 and 9 with respect to document W0 2009/022991 (D1)) is each of the first plurality of metal posts (108) comprises (i) a first end that is attached to the corresponding one of the first plurality of bond pads (136 - interconnect region - (par. 32) which define I/O pads of the die - see page 10, line 8-9) formed on the first side of the first die (102) and (ii) a second end that is opposite the first end (see fig. 3a and par. 42); each of the second plurality of metal posts (110) comprises (i) a first end that is attached to the corresponding one of the second plurality of bond pads (138 - interconnect region (par. 32) which define I/O pads of the die - see page 10, line 8-9) formed on the first side of the second die (104) and (ii) a second end that is opposite the first end (see fig. 3c and par. 43); and the redistribution layer (132) is configured to electrically couple (i) a second end of the first metal post of the first plurality of metal posts and (ii) a second end of the second metal post of the second plurality of metal posts (par. 46).

As all of the features of claims 2 and 10 are known from D1 (see figure 3h) none of them can form a contribution over the known prior art.

Although the surplus technical features of the dependent claim 4-8 and 13-17 are not the same, they could be searched without any additional effort and thus they form the basis of the 1st searched invention.

2. claims: 3, 11, 12

Group Ib: Claims 3, 11,12 (c.f claims 3 and 11)

Re. cl. 3 the surplus technical features with respect to the known claim 1 is a substrate, wherein the second side of the first die is attached to the substrate.

The problem to be solved by claims 3 and its corresponding method claim 11 is improving the mechanical stability of the package.

3. claims: 18-20

Group 2: Directed to the subject matter of claims 18-20 (c.f claim 18)

The surplus features of claim 18 surplus to this known common concept (between claims 1 and 18) are: the second die is stacked on the first die such that the second side of the

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

second die faces the first side of the first die; another (labelled first) redistribution layer formed on the first side of the first die, wherein the first redistribution layer comprises (i) a first end attached to the first bond pad, and (ii) a second end that is opposite to the first end; the first metal post is formed on the second end of the first redistribution layer;

The problem to be solved by the surplus features of claim 18 being directed to the formation of redistribution layer on the first side of the first die in order to solve the problem of being able to still use a first die having bond pads in the central region of the first die, yet still be able to electrically connect them to the second die which also sits on top of the first die (see also figs. 11-14 and paragraph 42 of the application).

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2016/018640

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2009022991 A1	19-02-2009	NONE	
