
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARO (BW, GI, GM, KE, LS, MW, NZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published: — with international search report

(88) Date of publication of the international search report: 21 December 2007

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Title: METHOD AND APPARATUS FOR ENFORCING INDEPENDENCE OF PROCESSORS ON A SINGLE IC

Abstract: A single-chip integrated circuit (100) comprising a first processor (103) for executing a plurality of applications, a second processor (104) for executing a plurality of applications, at least one of a) at least one embedded peripheral (105) and b) at least one memory (106), and a bus monitor (102) for allowing access to the at least one of a) the at least one embedded peripheral (105) and the at least one memory (106), if the access is allowed, wherein the bus monitor (102) comprises a mapping of access rights to the at least one of a) the at least one embedded peripheral (105) and b) the at least one memory (106) for the first processor (103) and the second processor (104) is disclosed.
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
   IPC: G06F 21/00 (2006.01); G06F 12/14 (2006.01)
   USPC: 726/9,20,21; 713/172
   According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
   Minimum documentation searched (classification system followed by classification symbols)
   U.S.: 726/9,20,21;713/172
   Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
   Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
   EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Y</td>
<td>US 6,195,733 (NAIR et al.) 27 February 2001 (27.02.2001), column 2, line 39-column 4, line 60.</td>
<td>1-10</td>
</tr>
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Further documents are listed in the continuation of Box C. 

See patent family annex.

Date of the actual completion of the international search
20 August 2007 (20.08.2007)

Date of mailing of the international search report
25 SEP 2007

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Form PCT/ISA/210 (second sheet) (April 2005)