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(54) DIGITAL DATA CODING AND RECORDING APPARATUS, AND METHOD OF USING THE SAME

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(57) **ABSTRACT**

A method of preparing data for a storage device includes writing unencoded main data to a memory buffer; reading the unencoded main data from the memory buffer; encoding the read main data; scrambling the encoded main data to provide address and parity information; writing the address and parity information, but not the encoded main data, to the memory buffer; reading the address and parity information and the unencoded main data from the memory buffer; and scrambling the unencoded main data.

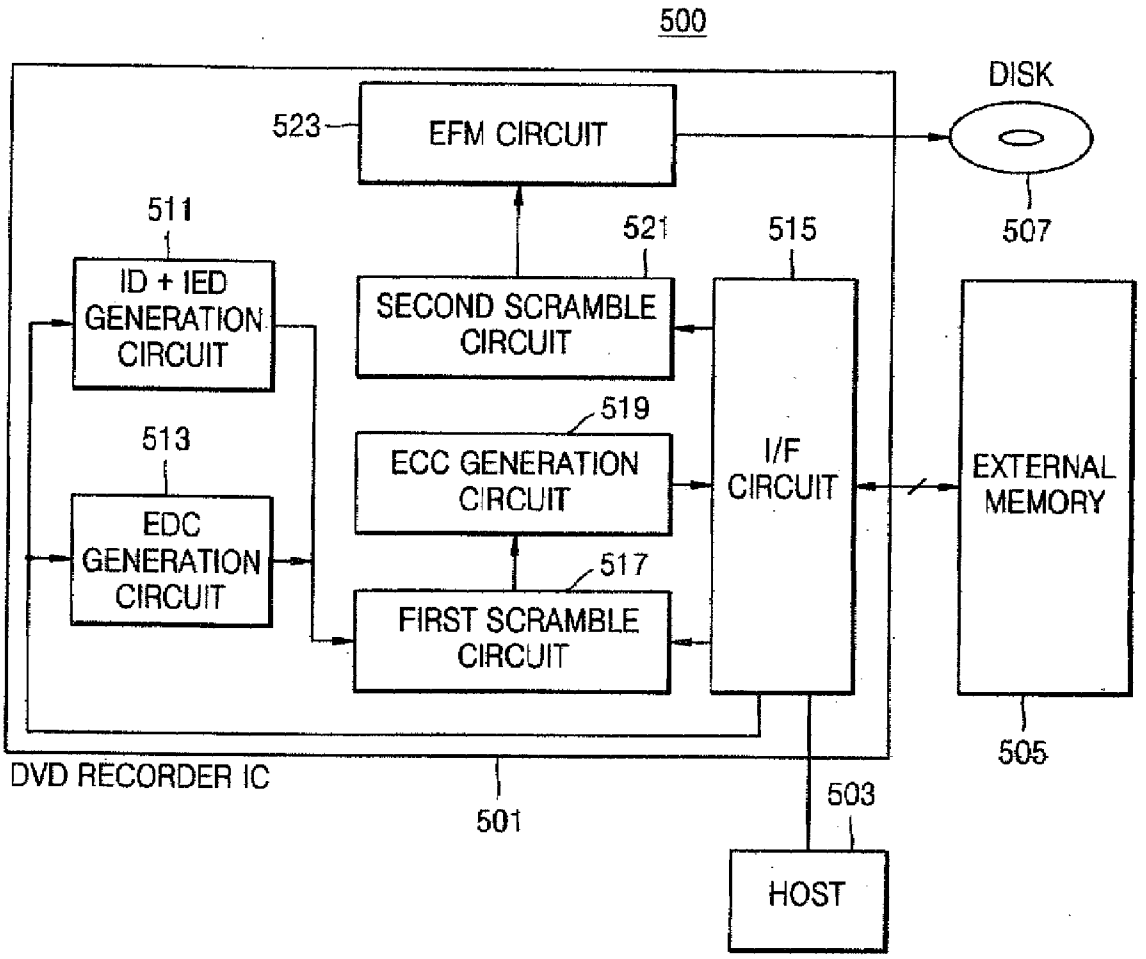


FIG. 1 (PRIOR ART)

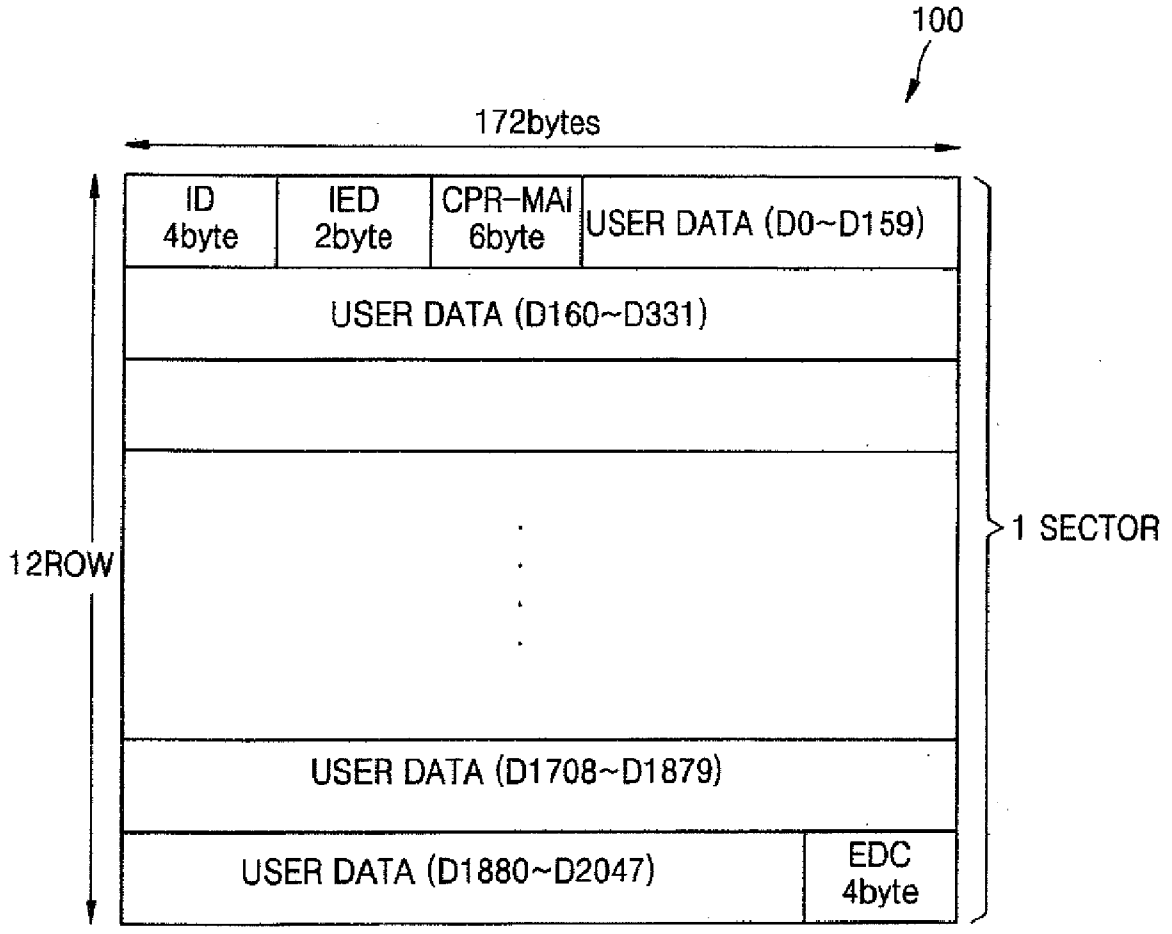


FIG. 2 (PRIOR ART)

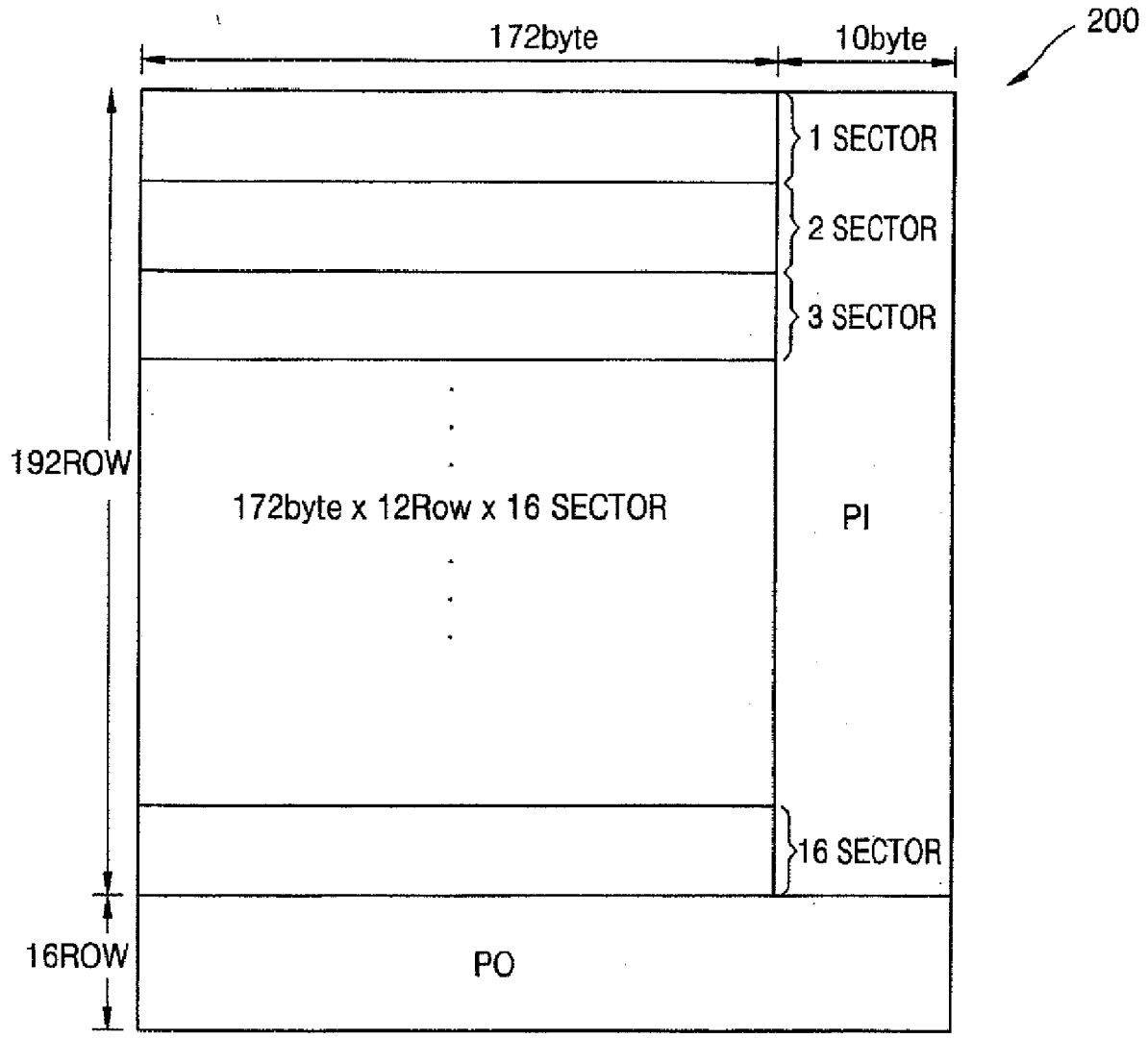


FIG. 3 (PRIOR ART)

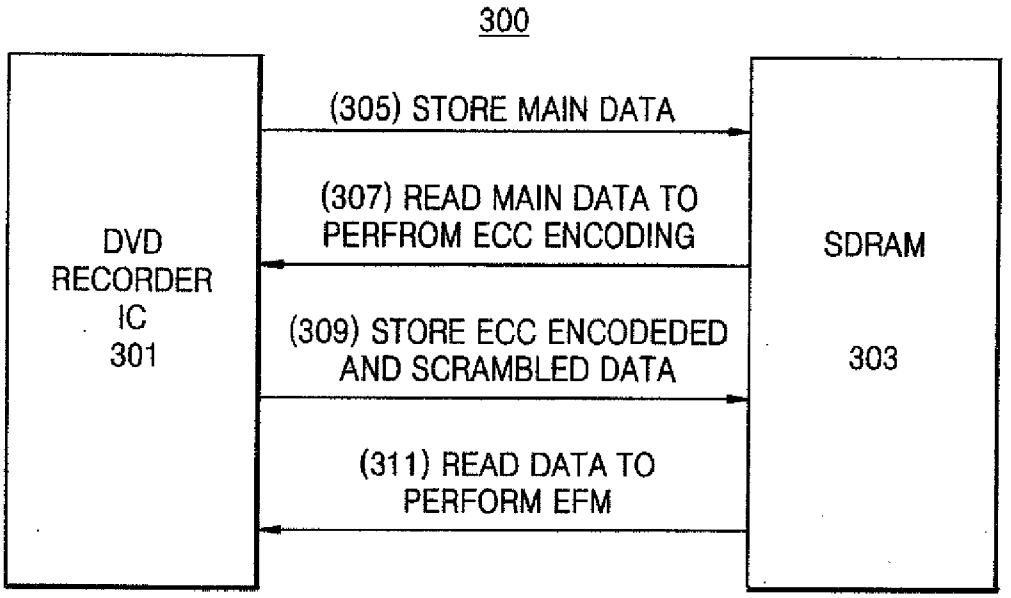


FIG. 4

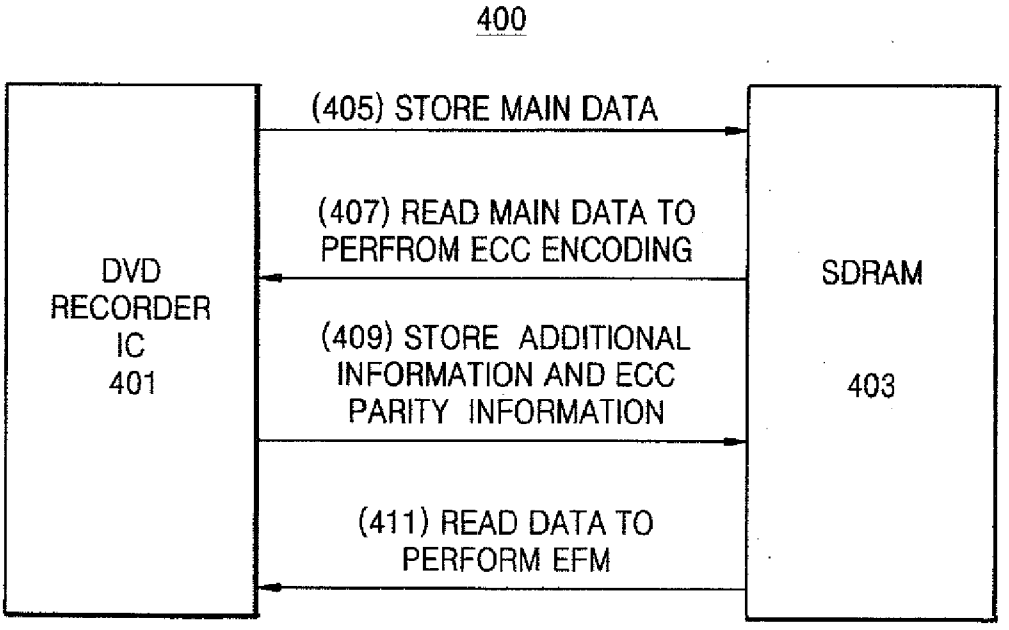


FIG. 5

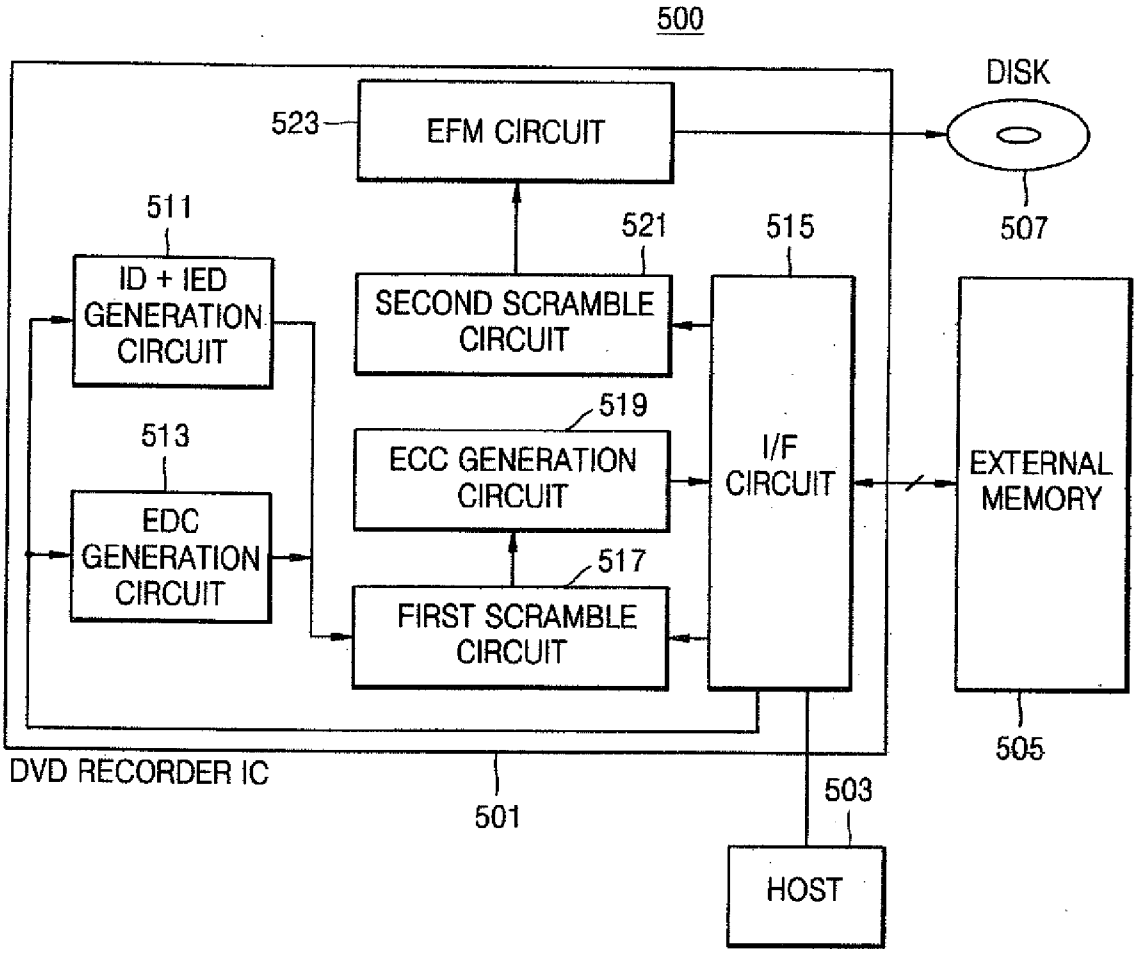
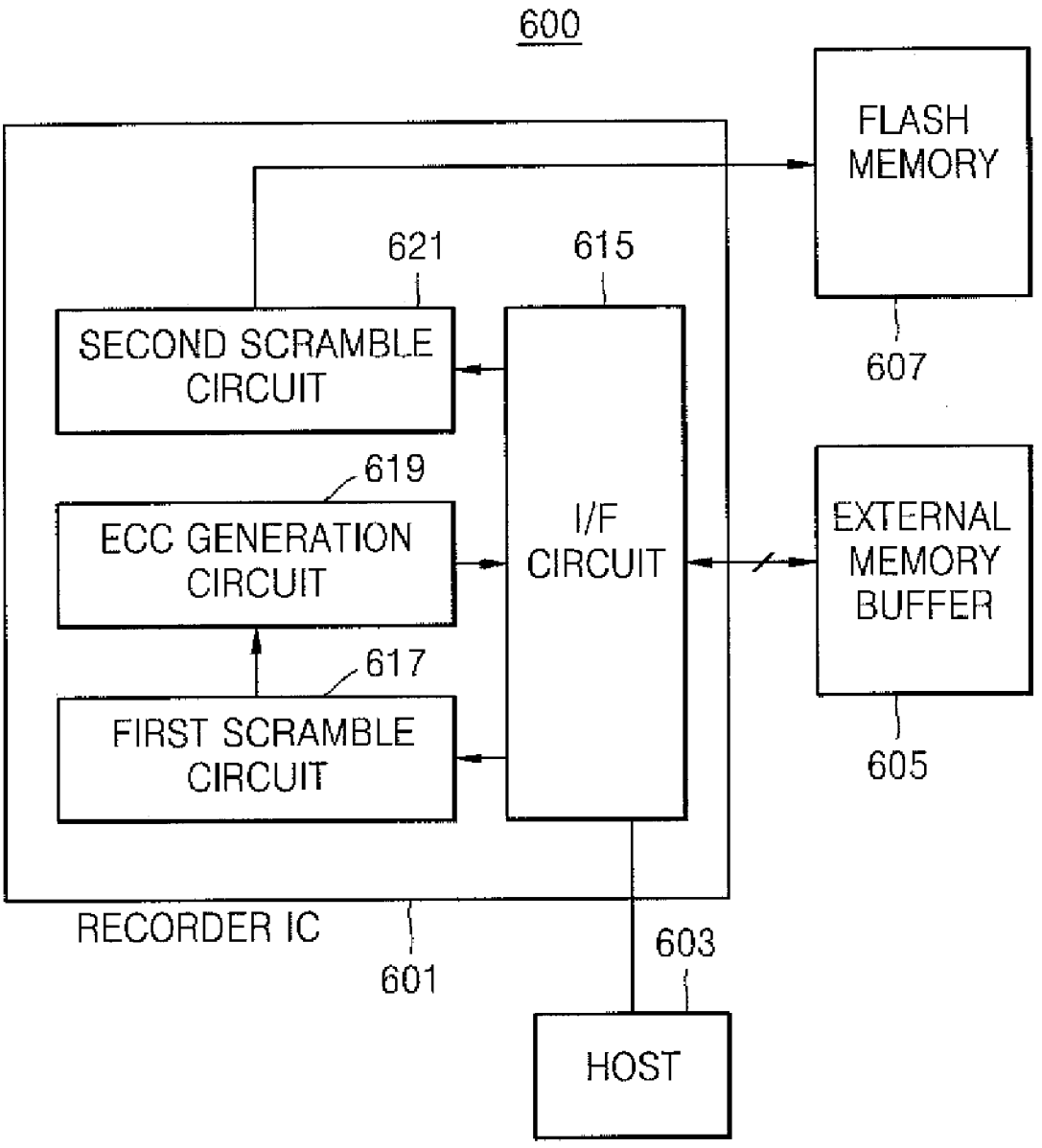

500
DISK
523
EFM CIRCUIT
507
511
521
515
ID + IED GENERATION CIRCUIT
SECOND SCRAMBLE CIRCUIT
519
513
ECC GENERATION CIRCUIT
I/F CIRCUIT
EXTERNAL MEMORY
EDC GENERATION CIRCUIT
517
FIRST SCRAMBLE CIRCUIT
505
DVD RECORDER IC
501
503
HOST

FIG. 6


600
FLASH MEMORY
607
621
615
SECOND SCRAMBLE CIRCUIT
619
ECC GENERATION CIRCUIT
617
FIRST SCRAMBLE CIRCUIT
I/F CIRCUIT
EXTERNAL MEMORY BUFFER
605
RECORDER IC
601
603
HOST

DIGITAL DATA CODING AND RECORDING APPARATUS, AND METHOD OF USING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation of co-pending U.S. patent application Ser. No. 11/121,884 (Attorney Dkt. No. 8021-322 (SS-21779-US)), filed on May 4, 2005, and entitled "DIGITAL DATA CODING APPARATUS, DVD RECORDING APPARATUS, AND METHOD OF USING THE SAME", which, in turn, claims foreign priority under 35 U.S.C. § 119 to Korean Patent Application No. 10-2004-0031352, filed on May 4, 2004, in the Korean Intellectual Property Office, the disclosures of which are incorporated by reference herein in their entireties.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present disclosure relates to digital recording apparatus, and more particularly, to digital data coding apparatus and recording apparatus capable of reducing the number of times a temporary memory buffer is accessed in order to code digital data to be recorded on a storage device.

[0004] 2. Description of the Related Art

[0005] The present disclosure is applicable to general storage devices. For example, one common type of storage device is a flash memory. Another common type of storage device is a Digital Versatile Disk (DVD).

[0006] A flash memory system generally processes data in units of data blocks. A DVD system generally processes data in units of data sectors. The data for any such general storage device may include an error correction code (ECC) block. The ECC block facilitates mass data transmission without errors.

[0007] In one example, each data sector includes 12 rows of 172 bytes. A first field of the data sector includes identifier (ID) data, IED data, and copyright management information (CPR_MAI) data, and a last field of the data sector includes an error detection code (EDC). An ECC block includes an information field having the data sector, 10 bytes of parity in (PI) parity, and 16 rows of parity out (PO) parity used to correct data errors of the information field.

[0008] FIG. **1** illustrates the structure of a data sector **100** to be recorded on a DVD. Referring to FIG. **1**, user data or main data to be recorded on the DVD from a host computer are classified in units of 2048 bytes. The data sector **100** comprises 4 bytes of ID data indicating address information for each data sector and sector power, 2 bytes of IED data that is an EDC of the ID data, and 6 bytes of CPR_MAI data indicating a reserve field or copyright management information. A first row of the data sector **100** includes 160 bytes of main data D**0** through D**159**. Each of second through eleventh rows includes 172 bytes of main data and a twelfth row includes 168 bytes of main data D**1880** through D**2047** and 4 bytes of EDC data. Each data sector consists of 2064 bytes (2048 bytes+16 bytes), that is, twelve 172-byte rows.

[0009] FIG. **2** illustrates the structure of an ECC block **200** comprising a plurality of the data sectors **100** shown in FIG. **1**. Referring to FIG. **2**, the ECC block **200** contains sixteen of the data sectors **100** to which ECC is added by calculating a Reed-Solomon code. The ECC block is recorded on the DVD to maintain data reliability. The ECC block is formed by calculating a Reed-Solomon code of one block that is formed from 16 data sectors and adding ECC.

[0010] The ECC block includes 10 bytes of ECC calculated from each row of the 16 data sectors in a horizontal direction, and the calculated ECC is added to the back of each corresponding row. A column of the added ECC forms a PI parity block having a size of 10 bytes×192 rows. The ECC block further includes 16 bytes of ECC calculated from each column of the data sectors and the PI parity block, and the calculated ECC is added in a vertical direction to the bottom of each corresponding column. The row of the added ECC forms a PO parity block having a size of (172+10) bytes×16 rows. Therefore, one digital data block to be recorded on the DVD is 182 bytes×208 rows=37,856 bytes.

[0011] An external memory buffer for temporarily storing data is required to process a signal used to code and modulate main data transmitted from a host computer Static dynamic random access memory (SDRAM) is used as the external memory buffer. An integrated circuit (IC) is used for coding data to be recorded to the DVD. The IC must frequently access the SDRAM in order to store the data into the SDRAM, and in order to read and process the stored data to be recorded to the DVD.

[0012] FIG. **3** is a diagram illustrating a process of accessing external memory in a conventional DVD recording apparatus. Referring to FIG. **3**, a recording apparatus **300** for recording digital data to a DVD includes a DVD recorder IC **301** and external memory or SDRAM **303**. Main data transmitted from a host computer are stored in the SDRAM **303** at step **305**. The DVD recorder IC **301** accesses the SDRAM **303** 32,768 times (2048×16 sectors) per data block.

[0013] The main data stored in the SDRAM **303** are read and ECC encoded at step **307**. The number of times when the SDRAM **303** is accessed is 2048×16 sectors=32,768 times per data block at step **307**, which is equal to the number of times for storing the main data. The DVD recorder IC **301** adds 4 bytes of ID data, 2 bytes of IED data, and 6 bytes of CPR_MAI data to each data sector, performs an EDC operation and adds the EDC. Each data sector contains 2064 bytes including 16 bytes of additional information added to 2048 bytes of main data. Thereafter, the data is scrambled. The scrambled data are ECC encoded in data block units by adding 10 bytes of PI parity to each row and adding 16 rows of PO parity to the block containing the PI parity. (10×192) bytes of PI parity and (182×16) bytes of PO parity are added as shown in FIG. **2**. Thus, one data block contains 182 bytes×208 rows=37,586 bytes.

[0014] The encoded data are stored in the SDRAM **303** at step **309**. At this time, the DVD recorder IC **301** accesses the SDRAM **303** 37,856 times per data block.

[0015] The DVD recorder IC **301** reads the data stored in the SDRAM **303** to perform eight-to-fourteen modulation (EFM) at step **311**. At this time, the DVD recorder IC **301** accesses the SDRAM **303** 37,856 times per data block.

[0016] The DVD recorder IC **301** performs the EFM for the read data and records the modulated data on the DVD Digital data are recorded on the DVD at a predetermined speed. The DVD recorder IC **301** must read and store data in the SDRAM **303**, which is an external buffer memory, within a designated time.

[0017] However, as recording apparatuses write or record data at higher speeds, the rate at which data is to be accessed from the external buffer memory must be increased. Therefore, when mass data are recorded on a storage device at high

speed, it is important to reduce the number of times that the external buffer memory is accessed with a recording speed of high transmission rate.

SUMMARY OF THE INVENTION

[0018] Exemplary embodiments of the present disclosure provide high-speed recording apparatus and methods in which the number of times that a recorder integrated circuit (IC) accesses a memory buffer can be reduced.

[0019] According to an aspect of the present disclosure, there is provided a method of recording data on a storage device, the method comprising: recording main data to be recorded on the storage device in a memory buffer; reading the recorded main data from the memory buffer to encode the main data; encoding and scrambling the main data; recording additional address information and parity information included in the encoded and scrambled data, except the main data, to the memory buffer; and reading the address information, the parity information, and the main data stored in the memory buffer and scrambling the read data before writing to the storage device.

[0020] According to another aspect of the present disclosure, there is provided a method of coding digital data to be recorded on a storage device, the method comprising: recording main data to be recorded on the storage device in a memory buffer; reading the recorded main data from the memory buffer to encode the main data; encoding and scrambling the main data; recording additional address information and parity information included in the encoded and scrambled data, except the main data, to the memory buffer; and reading the address information, the parity information, and the main data stored in the memory buffer and scrambling the read data before writing to the storage device.

[0021] According to another aspect of the present disclosure, there is provided an apparatus for recording digital data on a storage device, the apparatus comprising: a memory buffer for temporarily storing data to be recorded on the storage device; a first scramble circuit for scrambling the data in data units; an error correction code encoding circuit for adding parity-inner parity and parity-outer parity to the scrambled data in data units and error correction code encoding the added data; and a second scramble circuit for separately reading main data and error correction code parity from the memory buffer and scrambling the read data, wherein information in addition to the main data included in the error correction code encoded and scrambled data is stored in the memory buffer and, when the main data are read from the memory buffer to write to the storage device, the address information, the parity information and the main data stored in the memory buffer are read and scrambled by the second scramble circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] The above and other features and advantages of the present disclosure will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings, in which:

[0023] FIG. **1** is a schematic diagram that illustrates the structure of a sector of digital data to be recorded on a storage device;

[0024] FIG. **2** is a schematic diagram that illustrates the structure of an error correction code (ECC) bock comprising a plurality of the data sectors shown in FIG. **1**;

[0025] FIG. **3** is a schematic diagram illustrating a process of accessing external memory in a conventional recording apparatus;

[0026] FIG. **4** is a schematic diagram illustrating a process of accessing external memory in a recording apparatus according to an embodiment of the present disclosure;

[0027] FIG. **5** is a block diagram of a recording apparatus according to an embodiment of the present disclosure; and

[0028] FIG. **6** is a block diagram of a recording apparatus according to a flash memory embodiment of the present disclosure.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0029] A data coding apparatus and method for recording digital data on a storage device are provided, where the recording apparatus reduces the number of times that a memory buffer is written by temporarily storing only additional information and panty information when encoded data are present. Thus, the method performs data coding without loss of clock cycles by scrambling at least one field on-the-fly, that is without saving the at least one scrambled field to the memory buffer, when unscrambled data are read from the memory buffer, and writing the scrambled data to the storage device. The storage device may comprise any type of general storage device, such as a flash memory, a digital versatile disk (DVD), or a combination.

[0030] Hereinafter, the present disclosure is described more fully with reference to the accompanying drawings, in which embodiments of the disclosure are shown. Like reference numerals in the drawings may denote like elements. While exemplary embodiments are described for ease of understanding, alternate embodiments are contemplated, such as those supporting other types or combinations of storage devices.

[0031] FIG. **4** shows a process of accessing external memory in a recording apparatus according to an exemplary embodiment of the present disclosure. Referring to FIG. **4**, a recording apparatus and method **400** for recording digital data on a storage device, such as a flash memory or a digital versatile disk (DVD), for examples, includes a recorder integrated circuit (IC) **401** and an external buffer memory or static dynamic random access memory (SDRAM) **403**. The recorder IC **401** receives data transmitted from a host computer and stores the received data in the SDRAM **403** at step **405**. The recorder IC **401** accesses the SDRAM **403** 32,768 times (2,048×16 sectors) per data block at step **405**.

[0032] The recorder IC **401** reads main data stored in the SDRAM **403**, adds various pieces of additional information to the read main data, and scrambles and error correction code (ECC) encodes the added data at step **407**. To this end, the recorder IC **401** accesses the SDRAM **403** 32,768 times (2,048×16 sectors) per data block, which is equal to the number of times the recorder IC **401** accesses the SDRAM **403** to store the data.

[0033] The recorder IC **401** adds 4 bytes of ID data, 2 bytes of error detection code (EDC) of the ID information (IED) data, and 6 bytes of copyright management (CPR_MAI) data to each data sector and performs an EDC operation and adds the EDC. Each data sector contains 2,064 bytes including 16 bytes of additional information added to 2,048 bytes of main data. Thereafter, the data is scrambled. The scrambled data are ECC encoded in units of data blocks by adding 10 bytes of PI parity to each row and adding 16 rows of PO parity to the

block containing the PI parity. (10×192) bytes of PI parity and (182×16) bytes of PO parity are added as shown in FIG. **2**. Thus, one data block contains 182 bytes×208 rows=37,586 bytes.

[0034] Among the encoded data, additional information other than main data is stored in the SDRAM **403** at step **409**, where the additional information includes ID data, IED data, CPR_MAI data, EDC parity and ECC parity. At this time, the recorder IC **401** accesses the SDRAM **403** 5,088 times per data block ((4+2+4+6)×16 bytes comprising ID data, IED data, CPR_MAI data, EDC data)+10×192 (PI parity)+182×16 (PO parity)). Therefore, the number of times the SDRAM **403** is accessed is reduced by 12% by storing only additional information rather than all encoded data.

[0035] The recorder IC **401** reads the main data and the additional information stored in the SDRAM **403** and ECC parity information to perform eight to fourteen modulation (EFM) at step **411**. At this time, the recorder IC **401** can scramble only a main data field on-the-fly simultaneously while reading the main data, additional information, and ECC parity information, thereby obtaining a reading result equal to a conventional result without any clock loss. In addition, the recorder IC **401** can determine an initial value of a scramble linear feedback shift register (LFSR) while reading the ID information.

[0036] At this time, the recorder IC **401** accesses the SDRAM **403** 37,856 times per data block. The recorder IC **401** performs the EFM for the read data and records the modulated data on the storage device.

[0037] FIG. **5** is a block diagram of a recording apparatus according to an embodiment of the present disclosure, which is indicated generally by the reference numeral. Referring to FIG. **5**, the recording apparatus **500** comprises a recorder IC **501**, a host **503**, and an external memory **505**.

[0038] The recorder IC **501** receives digital data from the host **503**, codes the received digital data, and records the coded digital data on a storage device **507**. The external memory **505** temporarily stores digital data while the recorder IC **501** codes the received digital data.

[0039] The recorder IC **501** includes an ID+IED generation circuit (hereinafter, referred to as an ID generation circuit) **511**, an EDC generation circuit **513**, an I/F circuit **515**, a first scramble circuit **517**, an ECC generation circuit **519**, a second scramble circuit **521**, and an EFM circuit **523**.

[0040] The ID generation circuit **511** generates ID information, EDC of the ID information (IED data), and copyright information (CPR_MAI data) in data sector units. The EDC generation circuit **513** generates the EDC of data in data sector units. The I/F circuit **515** provides an interface between the recorder IC **501** and external devices **503** and **505** to transmit/receive data.

[0041] After additional information is added to the data and the added data are ECC encoded, the I/F circuit **515** stores only additional information and ECC parity information in the external memory **505**.

[0042] The first scramble circuit **517** scrambles the main data in data sector units read from the external memory **505**. The ECC generation circuit **519** receives the scrambled data and the information on ID, IED, CPR_MAI and EDC, combines the additional information with the main data, divides the combined data into bit streams with a predetermined length, and generates and adds the EDC of the bit stream divided into the bit streams with the predetermined length.

[0043] When the recorder IC **501** separately reads the additional information including the main data, the ID information, and the ECC parity, the second scramble circuit **521** s scrambles a predetermined field, i.e., the main data field, on-the-fly and transmits the scrambled data to the EFM circuit **523**. The EFM circuit **523** modulates the 8-bit scrambled data into 14-bit data and outputs the modulated data to the storage device **507**.

[0044] Referring to FIGS. **4** and **5**, a digital data recording operation is now described. The host **503** transmits user digital data, i.e., main data, to be recorded on the storage device **507** to the recorder IC **501**. The recorder IC **501** temporarily stores the main data in the external memory **505**. The first scramble circuit **517** combines the main data read from the external memory **507** with the ID, the IED, the CPR_MAI and the EDC parity generated by the ID generation circuit **511** and the EDC generation circuit **513**, and scrambles the combined data. The ECC generation circuit **519** performs an ECC operation and adds the ECC to the scrambled data to maintain reliability of the digital data. The data generated by the ECC generation circuit **519** consists of sixteen data sectors or one data block to generate ECC parity.

[0045] Meanwhile, when the ECC encoded data are temporarily stored in the external memory **505**, the external memory **505** does not store all the encoded data, but only the additional information and the parity, and not the main data.

[0046] When the recorder IC **501** reads data from the external memory **505** again to perform the EFM of the digital data, it scrambles a specific field, i.e., only a main data field, by an on-the-fly method, while reading the main data, the additional information, and the parity information. At this time, the recorder IC **501** can determine an initial value of the scramble LFSR while reading the ID information.

[0047] The number of times the recording apparatus **500** accesses the external memory **505** can be considerably less than the number of times a conventional recording apparatus accesses an external memory. The second scramble circuit **521** makes it possible to obtain the same data coding result as the conventional data coding result without any clock loss using the on-the-fly method.

[0048] In the recording apparatus and the recording method shown in FIGS. **4** and **5**, a digital data coding apparatus and a digital data coding method to record digital data on a storage device are provided.

[0049] The circuit shown in FIG. **5** can be implemented as one chip, i.e., a system on chip (SOC), thereby reducing the number of times the external memory **505** is accessed and increasing the bandwidth of a whole recording system.

[0050] As shown in FIG. **6**, a flash memory recording apparatus is indicated generally by the reference numeral **600**. The recording apparatus **600** includes a recorder integrated circuit (IC) **601**, a host **603**, an external memory buffer **605**, and a flash memory storage device **607**.

[0051] The recorder IC **601** includes an interface (I/F) circuit **615** connected to the host **603** and the external memory buffer **605**, a first scramble circuit **617** connected to the interface circuit **615**, an ECC generation circuit **619** connected between the first scramble circuit **617** and the interface circuit **615**, and a second scramble circuit **621** connected between the interface circuit **615** ant the flash memory storage device **607**.

[0052] In operation, the recorder IC **601** receives digital data from the host **603**, codes the received digital data, and records the coded digital data on the flash memory storage

device **607**. The external memory buffer **605** temporarily stores digital data while the recorder IC **601** codes the received digital data. The interface circuit **615** provides an interface between the recorder IC **601** and external devices **603**, **605** and **607** to transmit/receive data.

[0053] After additional information is added to the data and the added data are ECC encoded, the interface circuit **615** stores only additional information and ECC parity information in the external memory **605**. The first scramble circuit **617** scrambles the main data read from the external memory **605**. The ECC generation circuit **619** receives the scrambled data, combines additional information with the main data, and divides the combined data into bit streams with a predetermined length. When the recorder IC **601** separately reads the additional information including the main data and the ECC parity, the second scramble circuit **621** scrambles the main data field on-the-fly and transmits the scrambled data to the flash memory storage device **607**.

[0054] The digital data coding method and the digital data recording method make it possible to reduce the number of times an external memory or buffer is accessed and implement a high-speed recording system. When the recording system is implemented as a SOC, the number of times the external memory is accessed is reduced to increase the bandwidth of the system.

[0055] While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the pertinent art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the following claims.

What is claimed is:

1. A method of recording data on external media, the method comprising:

recording unencoded main data to a memory device;

reading the recorded main data from the memory device;

encoding the read main data with an error correction code (ECC);

scrambling the encoded main data to provide address and parity information;

recording the address and parity information, but not the encoded main data, to the memory device;

reading the address and parity information and the unencoded main data from the memory device; and

scrambling the unencoded main data to perform eight-to-fourteen modulation (EFM) on the main data.

2. The method of claim **1**, wherein the external media comprises a digital versatile disk (DVD).

3. The method of claim **1**, wherein the address and parity information includes an ID, error detected code (EDC) of the ID (IED), CPR_MAI, EDC parity and ECC parity, but not the main data.

4. The method of claim **1**, wherein the memory device is an SDRAM memory device.

5. The method of claim **1**, wherein scrambling the unencoded main data is performed on-the-fly and simultaneously with reading the address and parity information and the unencoded main data from the memory device.

6. The method of claim **2**, further comprising:

performing EFM on the scrambled unencoded main data; and

storing the EFM modulated data in the DVD.

7. The method of claim **3**, wherein the ECC encoding comprises dividing the main data into bit streams containing 2048 bytes each and adding 4 bytes of ID data indicating address information of each sector and sector power, 2 bytes of TED data that is EDC for the 4 bytes of ID data, 6 bytes of CPR_MAI data indicating copyright management information, and 4 bytes of EDC to each bit stream to form one data sector.

8. The method of claim **7**, wherein the ECC encoding further comprises adding parity inner (PI) parity information to each sector and adding parity outer (PO) parity information to sixteen of the data sectors and to the PI parity information to form one data block.

* * * * *