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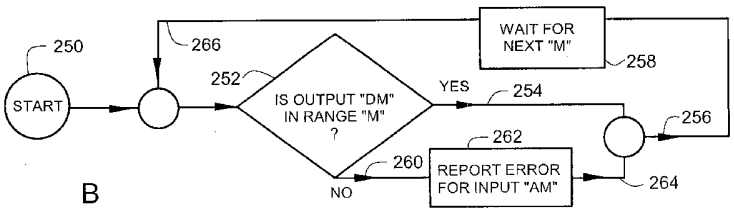
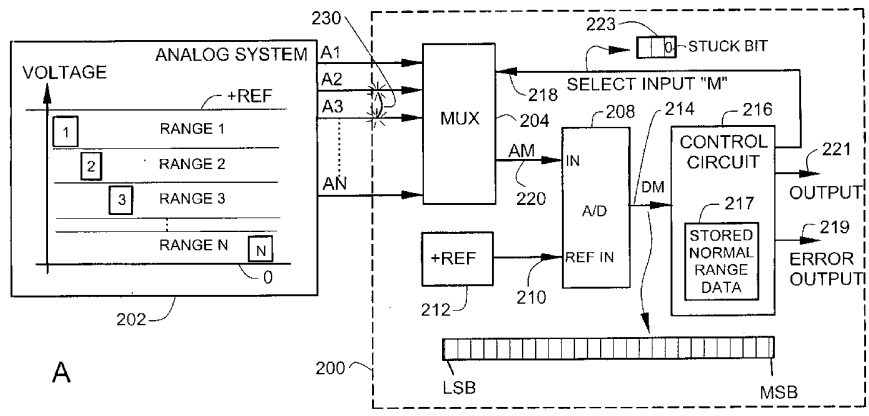
(54) Title: ANALOG-TO-DIGITAL CONVERTER WITH RANGE ERROR DETECTION





(57) Abstract: A circuit (200) includes a multiplexer (204), an analog-to-digital converter (208), and a processor (216) that compares a sequence (DM) of digital outputs from the analog-to-digital converter to a sequence (217) of normal ranges that correspond with the digital outputs in order to provide an error output (219) when one of the digital outputs is outside its normal range.

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ANALOG-TO-DIGITAL CONVERTER WITH RANGE ERROR DETECTION

BACKGROUND OF THE INVENTION

Multiplexed analog-to-digital (A/D) converters have input pins for receiving multiple analog inputs, and provide digital outputs that represent the analog inputs. The digital outputs are fed into a microcontroller which uses the digital outputs to generate a microcontroller output that is a function of the analog inputs. Typically, the A/D converter and microcontroller are part of an industrial process control transmitter and the microcontroller output represents a process variable that is compensated for temperature, power supply voltages, etc., all of which are analog inputs.

Various types of malfunctions can occur in the circuitry. One malfunction that can occur is a short between adjacent input pins of the multiplexer. Another malfunction that can occur is an A/D converter failure that results in one of the digital output bits becoming stuck at either a high level (1) or a low level (0).

When A/D converter systems are used in Safety Instrumented Systems (SIS), there is a need to identify when such malfunctions occur and provide an error or diagnostic output. A high degree of confidence is needed in the reliability of the A/D converter. A diagnostic output from the microcontroller is needed so that a process control

system supported by the A/D converter system is alerted to malfunctions.

SUMMARY OF THE INVENTION

A circuit comprises a multiplexer. The multiplexer has a select input and a sequence of analog outputs that are selected from a plurality of analog inputs. The circuit also comprises a reference source that provides a first reference.

The circuit comprises an analog-to-digital converter. The analog-to-digital converter receives the sequence of analog outputs and the first reference. The analog-to-digital converter provides a sequence of digital outputs.

The circuit comprises a control circuit. The control circuit actuates the select input to select the sequence of the analog outputs. The control circuit compares the sequence of digital outputs to a stored sequence of normal ranges that correspond with the digital outputs to provide an error output when at least one of the digital outputs is not in its normal range.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a PRIOR ART analog-to-digital converter system.

FIG. 2A illustrates a first embodiment of a circuit with a dynamically changing input range.

FIG. 2B illustrates a first simplified flow chart of a method of error checking in the circuit illustrated in FIG. 2A.

FIG. 3A illustrates a second embodiment of a circuit with a dynamically changing input range.

FIG. 3B illustrates a second simplified flow chart of a method of error checking in the circuit illustrated in FIG. 3A.

FIG. 4A illustrates a third embodiment of a circuit with a dynamically changing input range.

FIG. 4B illustrates a third simplified flow chart of a method of error checking in the circuit illustrated in FIGS. 4A, 5.

FIG. 5 illustrates a fourth embodiment of a circuit with a dynamically changing input range.

FIG. 6 illustrates an embodiment of a reference circuit.

FIG. 7 illustrates a block diagram of a transmitter circuit in which circuits and methods such as described above in FIGS. 2-6 can be used.

FIGS. 8A, 8B, 8C illustrate circuits that can be used in analog systems to provide scaling, inversion or level shifting of an analog input.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the embodiments illustrated in FIGS. 2-8, a circuit includes a multiplexer (MUX), an analog-to-digital converter (A/D) and a processor (typically a microcontroller (uC)). The processor provides digital output that represents analog inputs. In order to detect malfunctions, the processor compares a sequence of digital outputs from the analog-to-digital converter to a sequence of stored normal

ranges that correspond with the digital outputs. The processor provides an error output when one of the digital outputs is outside its normal range. The arrangement provide detection of shorted analog input pins on the multiplexer, stuck bits at the analog-to-digital convert output and other malfunctions. The arrangement is especially useful in process control applications where Safety Instrumented Systems (SIS) standards are in use.

FIG. 1 illustrates a PRIOR ART analog-to-digital converter system 100. An analog system 102 provides continuously variable (analog) voltages A1, A2, A3, ..., AN to a multiplexer 104. Each of the analog voltages A1, A2, A3, ..., AN has a normal voltage range indicated by vertical ranges of rectangles 1, 2, 3, ..., N at 106. The analog voltages A1, A2, A3, ..., AN can represent a process variable, a temperature, a voltage, a calibration pot setting and other analog variables. As part of the design process for the analog system 102, the analog voltages A1, A2, A3, ..., AN are scaled so that each analog voltage has a normal range of voltages that is within the input range of an analog-to-digital converter (A/D) 108. The input range of the A/D 108 ranges between zero (common) and a reference input 110 of the A/D 108. As part of the design process for the converter system 100, a reference 112 is selected which provides the desired input range (0 to +REF) to accommodate the normal ranges of all of the analog

voltages A1, A2, A3, ..., AN. Various engineering tradeoffs are made in the design process in an effort to select scaling for each analog input and a reference voltage so that the input range maximum is near the upper limit (+REF) in order to provide high resolution at a digital output 114 of the A/D 108. As a result of these engineering tradeoffs, the ranges of the analog voltage at 106 tend to be all near the upper limit (+REF) and vertically overlapping one another on a voltage scale as illustrated.

A digital output 114 of the A/D is coupled to a microcontroller 116. The microcontroller 116 provides a digital output (M) 118 that couples to the Multiplexer (MUX) 104. The multiplexer 104 receives the digital output 118 and selects one output AM to connect to the multiplexer output 120. The multiplexer output 120 couples to an analog input 122 of the A/D 108. The microcontroller 116 increments or steps the digital output M and obtains digital representations at output 114 for each of the relevant analog inputs A1, A2, A3, ..., AN. The microcontroller 116 calculates desired outputs 124 as a function of the digitized analog inputs A1, A2, A3, ... AN. Typically, the outputs 124 will represent process variables that are compensated for temperature, power supply voltages, calibration settings and the like that are obtained from the analog system 102.

Adjacent input pins on the multiplexer 104 are close together and subject to accidental or intermittent short circuiting by a short 130 during assembly or use of the multiplexer 104 on a printed wiring board. As explained above, analog voltages A1, A2, A3, ..., AN tend to have voltage ranges that are crowded together and are overlapping. When two adjacent pins are shorted together, the voltage at the two shorted together pins is typically in both of the voltage ranges for the shorted pins, and there is no "out of range" reading to identify the fact that there is a short circuit. Analog voltages that are only slightly different than correct voltages may be converted by the A/D 108 and there will be no indication of the short circuit. One or more of the output 124 will provide inaccurate data, and this inaccurate data can cause a process control system to malfunction without adequate warning.

The digital output 114 of the A/D 108 is a digital word 132 that includes a number of bits ranging from a least significant bit (LSB) to a most significant bit (MSB). The number of bits generally corresponds to the output resolution of the A/D. Each bit is generated by one or more switches internal to the A/D 108. These internal switches are subject to failure, and when a switch fails, typically one bit 134 of the digital word 132 becomes stuck at either a high (1) level or a low (0) level. This malfunction or failure can go unnoticed, particularly when the

bit is nearer the least significant bit (LSB) because the analog inputs tend to be in overlapping ranges and will be approximately equally affected by the stuck bit. The outputs 124 provide inaccurate data, and this inaccurate data can cause a process control system to malfunction without adequate warning.

The problems with the A/D system 100 are overcome as described below in connection with examples illustrated in FIGS. 2-8.

FIG. 2A illustrates a first embodiment of an circuit 200 with a dynamically changing input range and an error output 219. The circuit 200 is typically used to process analog variables in an industrial process variable transmitter such as the transmitter illustrated in FIG. 7, but can be used in a wide variety of other applications using multiplexed analog-to-digital conversion.

The circuit 200 receives a plurality of analog inputs A1, A2, A3, ... AN from an analog system 202. Each analog input has a normal operating range (RANGE 1, RANGE 2, RANGE 3, ... RANGE N) associated with it. The analog system 202 has been specially configured so that each analog input has a normal operating range that is different from the normal operating range of the other remaining analog inputs. In a preferred embodiment, the normal operating ranges of the analog inputs are non-overlapping. In a typical analog system 202, the analog inputs are conditioned by a combination of scaling, inversion or level

shifting to provide a unique normal operating range for each analog input A. Examples of conditioning circuits are described below in connection with FIGS. 8A, 8B, 8C.

The circuit 200 includes a multiplexer (MUX) 204 that receives the analog inputs A1, A2, A3, ... AN. The multiplexer 204 has a select input 218 that selects one of the analog inputs A1, A2, A3, ... AN to connect to a multiplexer output (AM) to provide a sequence of analog outputs 220. In a preferred arrangement, the multiplexer select input 218 is a multibit word and is simply counted up (or down) to sample the analog inputs in numerical order. The multiplexer 204 preferably comprises an integrated circuit analog multiplexer, for example, Analog Devices AD7501 available from Analog Devices, Inc. of Norwood, Massachusetts.

The circuit 200 also includes a reference source 212 that provides a first reference voltage to a reference input 210 of an analog-to-digital converter 208. In one preferred arrangement, a separate reference (such as a Zener diode or active reference) is provided in circuit 200. In another preferred embodiment, the reference source is simply a lead in circuit 200 that connects to a shared reference (such as a Zener diode or active reference) that is part of the analog system 202. In yet another preferred arrangement, a reference source that is part of a commercial A/D circuit 208 is used.

The analog-to-digital converter (A/D) 208 receives the sequence of analog outputs (AM) 220. The A/D 208 has a reference input 210 that receives the first reference voltage from reference 212. The A/D 208 converts the sequence of analog inputs (AM) 220 to a corresponding sequence of digital outputs (DM) 214. The multiplexer 204 presents the sequence of analog outputs (AM) 220 in a numerical sequence, and the sequence of digital outputs (DM) is also presented in a numerical sequence. The individual digital outputs DM can be presented in either a serial or a parallel format, depending on the type of A/D converter that is used. In one preferred embodiment, an Analog Devices AD571 A/D converter is used, for example. A digital output (for each serial or parallel digital output in the sequence), includes a number of bits ranging from a least significant bit (LSB) to a most significant bit (MSB) as illustrated.

The circuit 200 includes a control circuit 216. The control circuit 216 actuates the select input 218 with a numerical sequence that selects the sequence of the analog outputs to be read by the control circuit 216. The control circuit 216 compares the sequence of digital outputs 214 to a stored sequence of normal ranges 217 that correspond with the digital outputs 214 to provide or actuate an error output 219 when at least one of the digital outputs 214 is not in its stored normal range 217. The control circuit 216 preferably comprises a microcontroller, for

example, a National Semiconductor COP8SGE728M8. The error checking (normal range checking) runs in the background on the control circuit 216. The control circuit also provides a real time output 221 that represents some useful parameter of the analog system 202. In a typical transmitter application, the parameter of interest is a compensated pressure, temperature, or flow that is displayed or used for process control.

The arrangement illustrated in FIG. 2A provides for checking errors due to short circuits between analog inputs A1, A2, A3, ... AN which all have unique, non-overlapping normal ranges. When two analog inputs are shorted together by short 230, the resulting voltage can only be in a single one of the normal ranges and cannot lie in two different ranges because the ranges are non-overlapping. This results in at least one, and sometimes both of the shorted analog inputs being detected as outside of normal range. Short-circuiting of two of the plurality of analog inputs causes at least one of the digital outputs to exceed its corresponding normal range.

The arrangement illustrated in FIG. 2A also provides for checking errors due to one of the output bits of the A/D 208 being stuck. A bit is considered stuck when the bit remains at one logic state (0 or 1) continuously, or in other words is shorted to one of the power supply rails. When there is a stuck bit, because the analog inputs are each in a different

range, the effect of the stuck bit is different percentage for each output in the sequence, and there is a high probability that the control circuit 216 will detect that one of the digital outputs is out of its corresponding stored normal range. The sequence of digital outputs comprises digital words with a series of bits, and sticking of one of the bits causes at least one of the digital outputs to exceed its corresponding normal range.

FIG. 2B illustrates a simplified flow chart example of background error checking in the system illustrated in FIG. 2A. Program flow starts at START 250 and proceeds to compare the current output DM (i.e., the output D when the select input is M) to the stored normal range data for range M at decision block 252. If the output DM is in the normal range, then program flow continues along lines 254, 256 to function block 258. At function block 258, the background program waits for the select input M to change to the next number. If the output DM is not in the normal range at decision block 252, then program flow continues along line 260 to function block 262 which actuates the error output 219 (FIG. 2A) and then continues along lines 264, 256 to the function block 258. When the select input M changes, then program flow starts again and continues along lines 266 back to the decision block 252.

The arrangements illustrated in FIGS. 2A-2B have the advantage of a high certainty of detecting stuck

bits and shorted pins. The problem of providing inaccurate data to a digital output is solved by providing an error output that reliably warns of stuck bits and shorted input pins.

FIG. 3A illustrates a second embodiment of a circuit 300 with a dynamically changing input range and an error output 219. Reference numbers used in FIG. 3A that are the same as reference numbers used in FIG. 2A designate the same or similar features.

The circuit 300 receives a plurality of analog inputs A1, A2, A3, ... AN from an analog system 302. Each analog input has a normal operating range (RANGE 1, RANGE 2, RANGE 3, ... RANGE N) associated with it. The analog system 302 has been specially configured so that odd-numbered analog inputs (A1, A3,...) are in an odd normal operating range, and even-numbered analog inputs (A2, A4, ...) are in an even normal operating range. In a preferred embodiment, the odd and even operating ranges of the analog inputs are non-overlapping and each of the two operating ranges extends over about one half of the input range of the A/D 208. In another preferred arrangement, there is a small voltage spacing between the even and odd ranges to increase the likelihood of detecting errors. In a typical analog system 302, the analog inputs are conditioned by a combination of scaling, inversion or level shifting so that alternately numbered analog inputs are in alternating normal operating ranges. Shorting between adjacent pins (one even, one odd)

has a high probability of pulling one of the adjacent inputs outside of its normal range. A stuck bit at the output 214 produces errors that differ typically by a factor of two between even and odd outputs and the errors are thus easily recognized. Examples of conditioning circuits that can be used to scale, invert or level shift analog voltages are described below in connection with FIGS. 8A, 8B, 8C.

In circuit 300, the stored normal range data comprises even normal range data and odd normal range data. In other respects, the circuit 300 is similar to the circuit 200.

FIG. 3B illustrates an example of a simplified flow chart of background error checking useful in the system illustrated in FIG. 3A. Program flow begins at START 301 and continues along line 303 to decision block 304. At decision block 304, the current select input number "M" is tested to find out if it is even. If the input number "M" is even, then program flow continues along line 306 to decision block 308. If the number "M" is not even, then program flow continues along line 310 to decision block 312.

At decision block 308, the A/D output DM is tested to find out if DM is in the even stored normal range. If DM is in the even stored normal range, then program flow continues along line 314 and 316 to action block 318. Action block 318 provides a wait until the value of M is updated, and then program

flow continues along lines 320, 303 to start the process over for the next value of M.

If DM is not in the even stored normal range at decision block 308, then program flow continues along line 322 to action block 324. Action block 324 reports an error (actuates output 219 in FIG. 3A), and then program flow continues along lines 326, 316 to action block 318.

If DM is in the odd range at decision block 312, then program flow continues along lines 328, 316 to action block 318. If Dm is not in the odd range at decision block 312, then program flow continues along line 330 to action block 324.

The arrangements illustrated in FIGS. 3A-3B provide for error checking using only two stored normal ranges.

A single analog voltage, such as a power supply rail can be resistively scaled to provide one analog input in the upper (odd) range and another analog input in the lower (even) range. The control circuit 216 can compare the two readings and test for a constant ratio of resistive scaling as an additional error check.

FIG. 4A illustrates a third embodiment of a circuit 400 with a dynamically changing input range and an error output 219. Reference numbers used in FIG. 4A that are the same as reference numbers used in FIG. 3A identify the same or similar features.

Circuit 400 in FIG. 4A comprises a first switch 406 that couples to a reference input 210 on the A/D 208. A reference source 213 generates a first reference 402 and also generates a second reference 404 that is different than the first reference 402.

A control circuit 216 controls the first switch 406 to couple the first reference 402 to the analog-to-digital converter 208 when an odd-numbered analog input (A1, A3, ...) is selected. The control circuit 216 controls the first switch 406 to couple the second reference 404 to the analog-to-digital converter when an even-numbered analog input (A2, A4,...) is selected. The switching provided by the first switch 406 shifts the range of the output of the A/D converter 208. In simple terms, the output DM of the A/D converter is a digital word that is scaled to a product of voltage at the analog output AM divided by voltage at the reference input 210 times the count span of the A/D converter. Accordingly, data 215 in the control circuit 216 is stored shifted normal range data. The arrangement in FIG. 4A provides enhanced A/D converter resolution for the lower range while still providing the error detection between adjacent pins of the analog inputs. In other respects, the circuit 400 of FIG. 4A is similar to the circuit 300 of FIG. 3.

FIG. 4B illustrates a simplified flow chart of error checking in the system illustrated in FIG. 4A. Reference numbers used in FIG. 4B that are the same

as reference numbers used in FIG. 3B identify the same or similar features. In FIG. 4B, decision blocks 309, 313 test for DM to be in shifted ranges rather than ranges (FIG. 3B). In other respects, the flow chart in FIG. 4B is similar to the flow chart if FIG. 3B.

The arrangements illustrated in FIGS. 4A-4B provide for analog inputs in both the odd and even ranges to use a full output range of the A/D converter 208 because the reference input shifts to boost the lower valued analog inputs in the lower (even) range.

FIG. 5 illustrates a fourth embodiment of a circuit 500 with a dynamically changing input range and an error output 219. Reference numbers used in FIG. 5 that are the same as reference numbers used in FIG. 4A identify the same or similar features.

In FIG. 5, a circuit 500 comprises a second switch 502. The A/D converter 208 is provided with differential analog inputs +IN and -IN. The second switch 502 is coupled to the -IN differential input and the analog input AM is coupled to +IN differential input. The control circuit 216 controls the second switch 502 to connect a selected one of the second reference 404 and a common conductor 504 (zero volts) to the -IN differential input. The switches 406 and 502 are operated in synchronization so that both the upper and lower limits of the range of the A/D converter 208 can be shifted. This

arrangement allows enhanced error detection while retaining high A/D converter resolution. An odd range input value will produce a maximum count A/D output value DM if input into an even range switch configuration. Likewise, an even range input value will produce a minimum count A/D input value DM if input into an odd range switch configuration. In other respects, the circuit 500 in FIG. 5 is similar to the circuit 400 in FIG. 4A.

FIG. 6 illustrates an embodiment of a reference switching circuit 600 that provides a selectable level of reference voltage 602 to a reference input on an A/D converter. Selection of the level is controlled by a control line 604 from a control circuit such as a microcontroller.

The control line 604 activates a switch 606 to short out a resistor 608. Resistor 608 is in a resistive voltage divider 614 along with resistors 610, 612. The resistive voltage divider 614 provides a reference voltage on line 616 to a buffer circuit 618. The reference switching circuit 600 can be used in place of the reference 213 and the switch 406 in FIG. 4A, for example.

The reference switching circuit 600 is controlled to generate the first reference at a first level when an odd-numbered analog input is selected, and controlled to generate the first reference at a second level when an even-numbered analog input is selected.

FIG. 7 is a block diagram showing one example of a transmitter circuit 700 in which circuits and software such as described above in FIGS. 2-6 can be used. In FIG. 7, feature module electronics 750 is shown coupled to two wire process control loop 718 through a shunt regulator 699 and a loop feedback resistor 701. A series of cascaded voltage regulators 702, 704, 706 couple power from the loop 718 to the feature module electronics 750 and also to sensor module electronics 752. Sensor module electronics 752 is also shown coupled to a process variable through a process variable sensor 712. An optional output display 714 is also shown.

Loop override circuitry 762 serves as an error output and is partially implemented in microcontroller 738 which couples to a digital to analog (D/A) converter 722 and a multiplexed converter circuit 764 that includes an analog-to-digital (A/D) converter, multiplexer and reference as described above in connection with FIGS. 2-5. The multiplexed converter circuit 764 is configured to measure the sense voltage on resistor 701 (sensing loop current) and also senses regulated power supply voltages at nodes 703, 705, 707. The multiplexed converter circuit 764 also measures a voltage at node 709 which is representative of power supply current from voltage regulator 704.

In operation, the microcontroller 738 is configured to control the current I through loop 718,

and any digital data modulated onto that current, using D/A 722 and shunt regulator 699. The multiplexed converter circuit 764 provides outputs 765 (comparable to outputs 214 in FIGS. 2-5) that represents the various analog voltages that are sensed. The multiplexed converter circuit 764 can also be connected to other voltages or components within transmitter 700. The microcontroller 738 includes a memory 740 which stores normal range data (comparable to data 215, 217 in FIGS 2-5) used to detect errors such as shorted pins or a stuck output bit as described above in connection with FIGS. 2-5.

Upon the detection of a short circuit or stuck bit, the microcontroller 738 transmits an alarm signal on line 761 to activate loop override circuitry 762. The current I flowing through loop 718 is then set to a fixed current level. In some embodiments, circuitry within the device can be disconnected or shut off in order to provide enough power to other circuitry to provide a desired output. One technique to provide a loop override is to disconnect the device, or otherwise take the device offline from the process control loop. The change in loop current indicates a failure in the transmitter 700 to the loop 718 and this can be used by a control system connected to the loop to take action to shut down a controlled process using a Safety Instrumented System (SIS).

FIG. 7 also illustrates an optional watch dog circuit 750 coupled to microcontroller 738. The watch dog circuit 750, when used, must be periodically triggered by microcontroller 738. If microcontroller 738 stops triggering watch dog circuit 750, it can be assumed that a failure has occurred. Examples include, but are not limited to, improper program flow, microprocessor or memory failure, clock errors, etc. If watch dog circuit 750 is not triggered, watch dog circuit 750 sends a signal to loop override circuitry 762 to cause loop override circuitry 762 to drive an alarm current level on the process loop 718.

FIGS. 8A, 8B, 8C illustrate circuits that can be used in analog systems to provide scaling, inversion or level shifting of an analog input. FIG. 8A illustrates a conditioning circuit in which an analog voltage 800 from an analog system is amplified by an amplifier 802 to provide a scaled output 804 which can be coupled to an input of an A/D converter. FIG. 8B illustrates a conditioning circuit in which an analog voltage 810 from an analog system is scaled down by a factor controlled by a resistive voltage divider to provide a scaled down output 814 that can be coupled to an input of an A/D converter. FIG. 8C illustrates a conditioning circuit in which an analog voltage 820 is coupled to an inverting input 821 of an amplifier 822 via a resistor. A reference voltage 824 is also coupled to the inverting input 821 via a resistor. The arrangement shown in FIG. 8C provides

scaling, inversion and level shifting by the selection of resistor values and reference voltage 824 to provide an output 826 that can be coupled to an input of an A/D converter.

Features described in connection with one embodiment can be appropriately applied to other embodiments. Although the present invention has been described with reference to preferred embodiments, workers skilled in the art will recognize that changes may be made in form and detail without departing from the scope of the invention.

WHAT IS CLAIMED IS:

1. A circuit, comprising:

a multiplexer having a select input and a sequence of analog outputs that are selected from a plurality of analog inputs;

a reference source providing a first reference;

an analog-to-digital converter receiving the sequence of analog outputs and the first reference, and providing a sequence of digital outputs; and

a control circuit actuating the select input to select the sequence of the analog outputs, the control circuit comparing the sequence of digital outputs to a stored sequence of normal ranges that correspond with the digital outputs to provide an error output when at least one of the digital outputs is not in its normal range.

2. The circuit of Claim 1 wherein at least two of the normal ranges are non-overlapping.

3. The circuit of Claim 2 wherein short-circuiting of two of the plurality of analog inputs causes at least one of the digital outputs to exceed its corresponding normal range.

4. The circuit of Claim 2 wherein the sequence of digital outputs comprises digital words with a series of bits, and wherein a sticking of one of the bits causes at least one of the digital outputs to exceed its corresponding normal range.

5. The circuit of Claim 1, wherein each normal range is different and does not overlap another normal range.

6. The circuit of Claim 1, wherein:

the normal ranges comprise an odd range and an even range, and

the plurality of analog inputs are connected to the multiplexer in a numbered sequence such that odd-numbered analog inputs generate digital outputs that are in the odd range and even-numbered analog inputs generate digital outputs that are in the even range.

7. The circuit of Claim 6, further comprising:

a first switch;

wherein the reference source generates a second reference that is different than the first reference; and

wherein the control circuit controls the first switch to couple the first reference to the analog-to-digital converter when an odd-numbered analog input is selected, and controls the first switch to couple the second reference to the analog-to-digital converter when an even-numbered analog input is selected.

8. The circuit of Claim 7, further comprising:

a second switch; and

wherein the analog-to-digital converter comprises first and second differential

inputs, the analog output is connected to the first differential input; and the control circuit controls the second switch to connect a selected one of the second reference and a common conductor to the second differential input.

9. The circuit of Claim 1 wherein the control circuit controls the reference source to generates the first reference at a first level when an odd-numbered analog input is selected, and to generate the first reference at a second level when an even-numbered analog input is selected.

10. A method of detecting an error, comprising:

generating a sequence of analog outputs that are selected from a plurality of analog inputs as a function of a select input;

providing a first reference;

receiving the sequence of analog outputs and the first reference, and providing a sequence of digital outputs that represent the sequence of analog outputs; and

actuating the select input to select the sequence of the analog outputs; and

comparing the sequence of digital outputs to a stored sequence of normal ranges that correspond with the digital outputs to provide an error output when at least one of the digital outputs is not in its normal range.

11. The method of Claim 10 wherein at least two of the normal ranges do not overlap one another.

12. The method of Claim 11 wherein at least one of the analog inputs exceeds its corresponding normal range when two of the plurality of analog inputs short circuit to one another.

13. The method of Claim 11 wherein at least one of the digital outputs exceeds its corresponding normal range when one output bit in the digital outputs sticks.

14. The method of Claim 10, wherein each normal range differs from the other normal ranges and does not overlap another normal range.

15. The method of Claim 10, further comprising:

providing the normal ranges as an odd range and an even range, and

connecting the plurality of analog inputs to a multiplexer in a numbered sequence such that odd-numbered analog inputs generate digital outputs that are in the odd range and even-numbered analog inputs generate digital outputs that are in the even range.

16. The method of Claim 15, further comprising:

providing a first switch;

generating a second reference that is different than the first reference; and

controlling the first switch to couple the first reference to an analog-to-digital converter

when an odd-numbered analog input is selected, and controlling the first switch to couple the second reference to the analog-to-digital converter when an even-numbered analog input is selected.

17. The method of Claim 16, further comprising:

providing a second switch;

providing first and second differential inputs on the analog-to-digital converter,

connecting the analog output to the first differential input; and

controlling the second switch to connect a selected one of the second reference and a common conductor to the second differential input.

18. The method of Claim 10, further comprising:

controlling a reference source to generates the first reference at a first level when an odd-numbered analog input is selected, and

controlling the reference source to generate the first reference at a second level when an even-numbered analog input is selected.

19. A circuit, comprising:

a multiplexer having a select input and a sequence of analog outputs that are selected from a plurality of analog inputs;

a reference source providing a first reference;

an analog-to-digital converter receiving the sequence of analog outputs and the first

reference, and providing a sequence of digital outputs; and

means for actuating the select input to select the sequence of the analog outputs, and for comparing the sequence of digital outputs to a stored sequence of normal ranges that correspond with the digital outputs to provide an error output when at least one of the digital outputs is not in its normal range.

20. The circuit of Claim 19 wherein at least two of the normal ranges are non-overlapping.

21. The circuit of Claim 20 wherein short-circuiting of two of the plurality of analog inputs causes at least one of the digital outputs to exceed its corresponding normal range.

22. The circuit of Claim 20 wherein the sequence of digital outputs comprises digital words with a series of bits, and wherein a sticking of one of the bits causes at least one of the digital outputs to exceed its corresponding normal range.

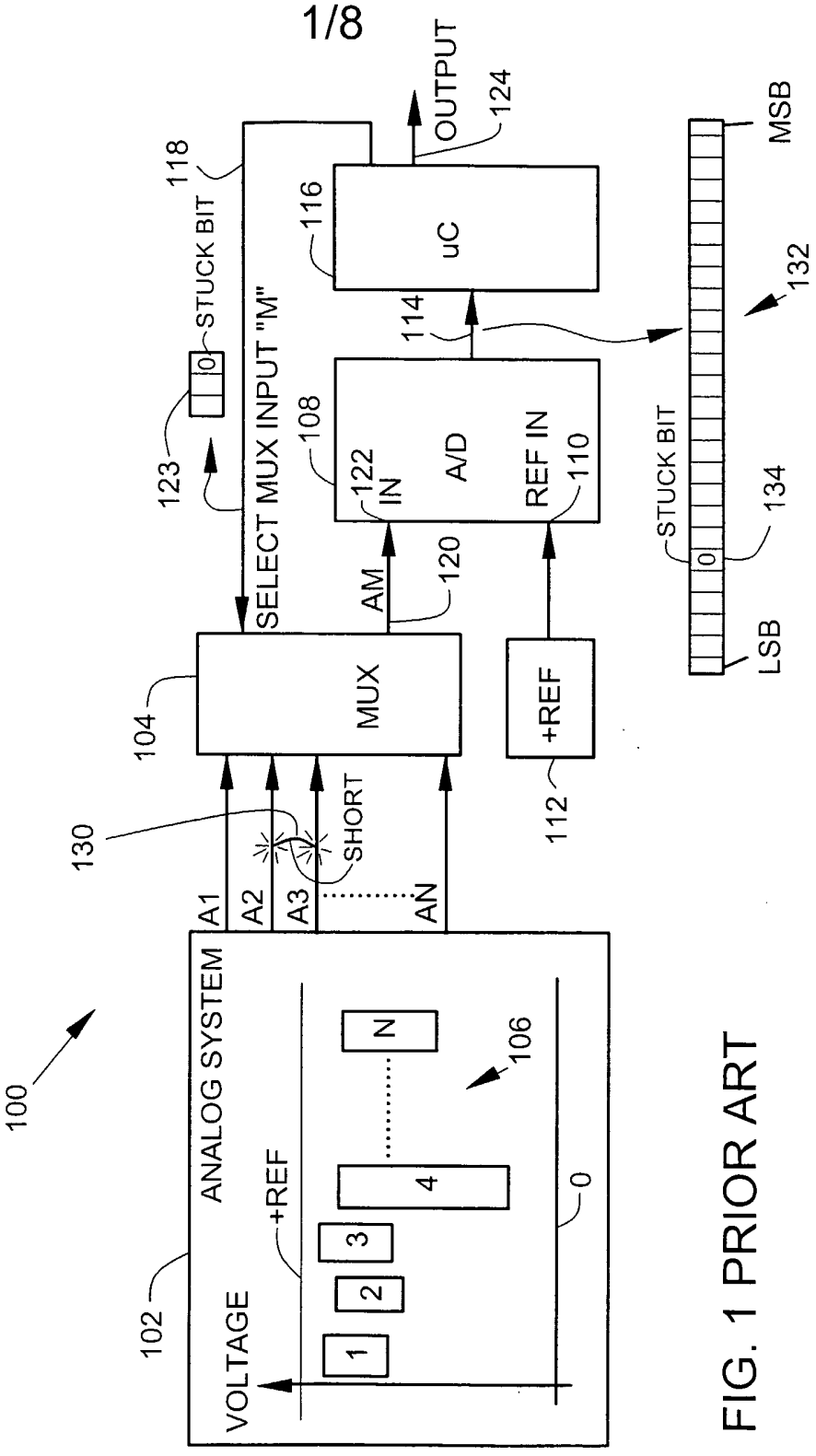

FIG. 1 PRIOR ART

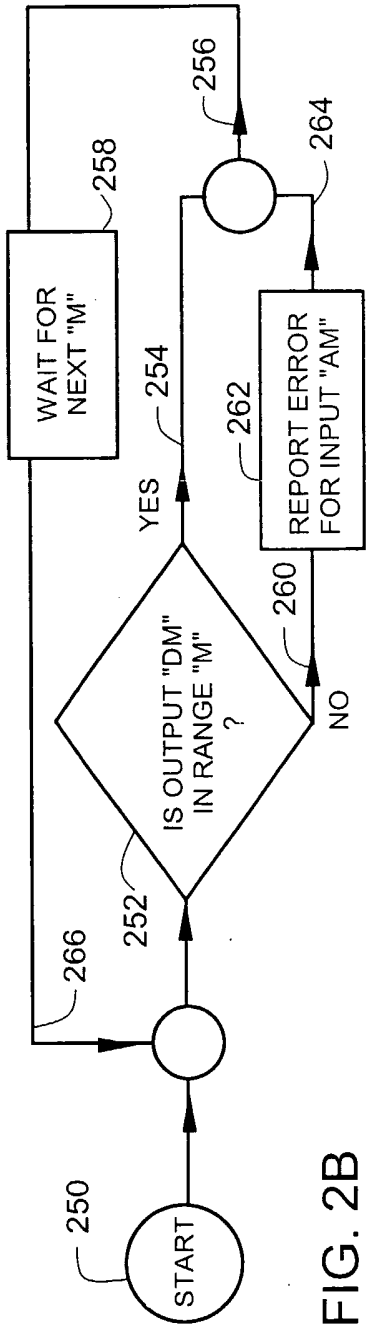
250
START
252
IS OUTPUT "DM" IN RANGE "M" ?
YES
254
NO
260
REPORT ERROR FOR INPUT "AM"
262
WAIT FOR NEXT "M"
258
256
264
266

FIG. 2B

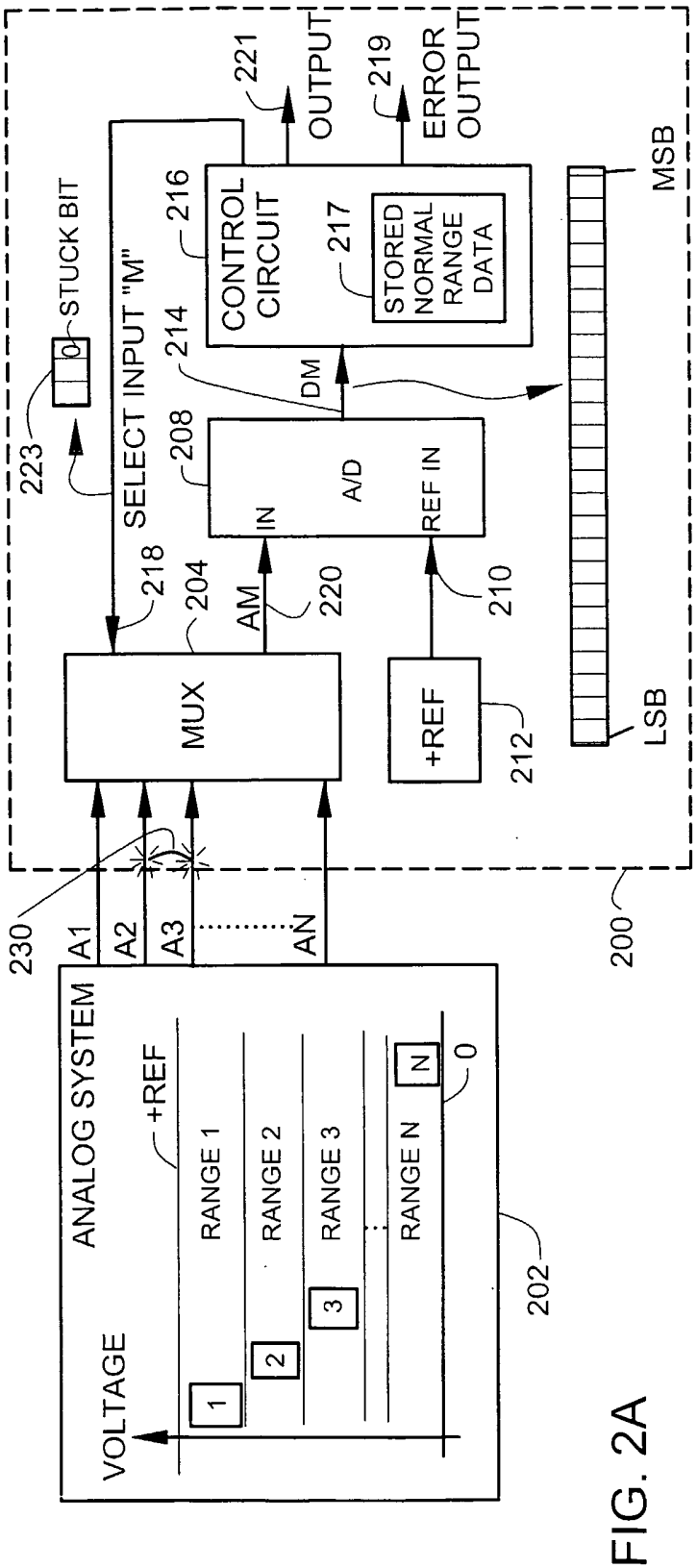
200
230
A1
A2
A3
AN
ANALOG SYSTEM
+REF
RANGE 1
RANGE 2
RANGE 3
RANGE N
VOLTAGE
1
2
3
N
0
202
MUX
204
AM
220
+REF
212
210
A/D
208
IN
REF IN
DM
214
SELECT INPUT "M"
218
STUCK BIT
223
CONTROL CIRCUIT
216
STORED NORMAL RANGE DATA
217
OUTPUT
221
ERROR OUTPUT
219
MSB
LSB

FIG. 2A

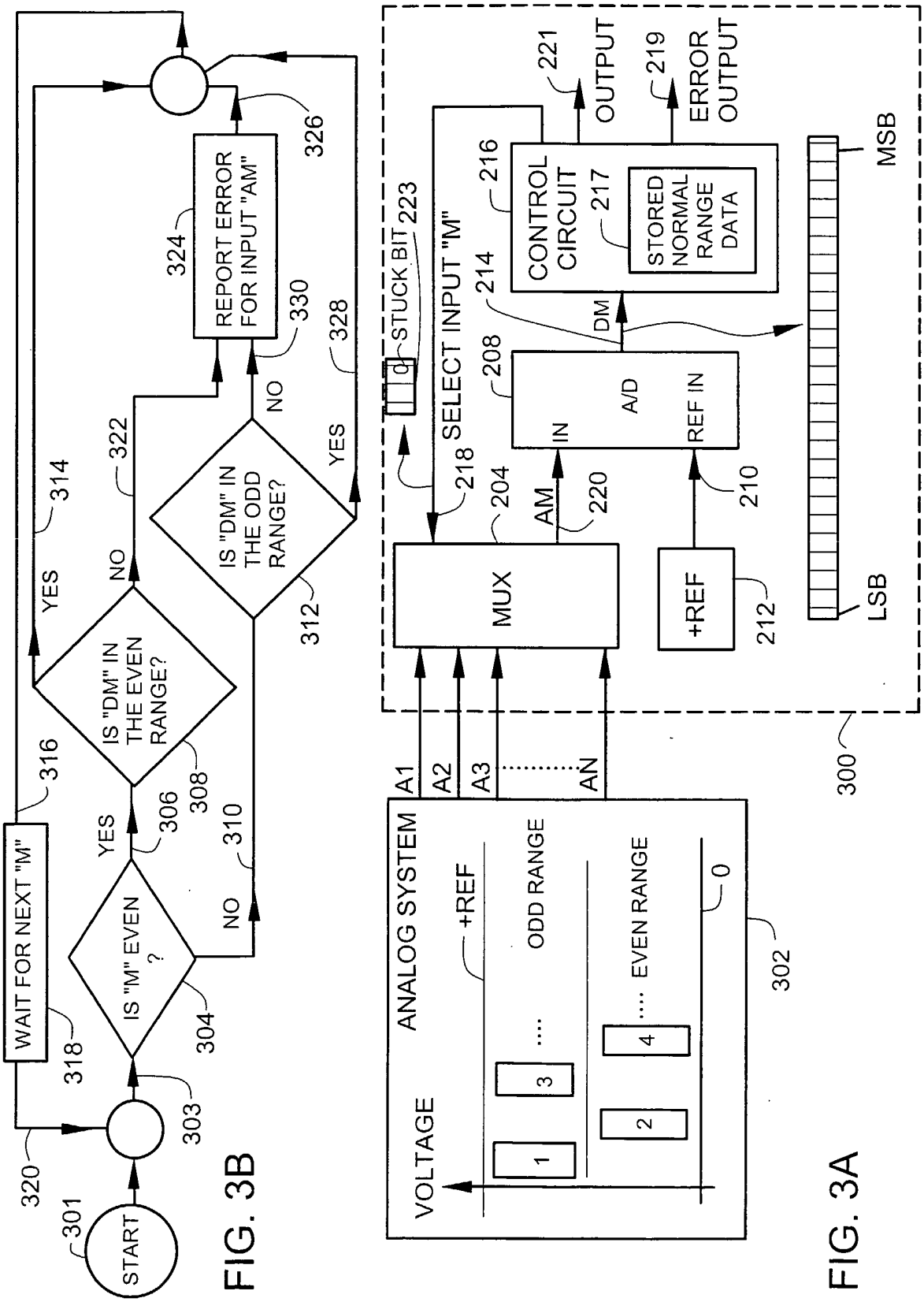
ANALOG SYSTEM
VOLTAGE
+REF
ODD RANGE
EVEN RANGE
0
A1
A2
A3
AN
MUX
AM
204
220
SELECT INPUT "M"
218
STUCK BIT
223
A/D
IN
REF IN
208
+REF
212
210
CONTROL CIRCUIT
216
217
STORED NORMAL RANGE DATA
214
DM
OUTPUT
221
ERROR OUTPUT
219
MSB
LSB
300
302
START
301
320
303
IS "M" EVEN ?
304
306
IS "DM" IN THE EVEN RANGE?
308
310
IS "DM" IN THE ODD RANGE?
312
314
316
WAIT FOR NEXT "M"
318
322
324
REPORT ERROR FOR INPUT "AM"
326
328
330
YES
NO

FIG. 3A

FIG. 3B

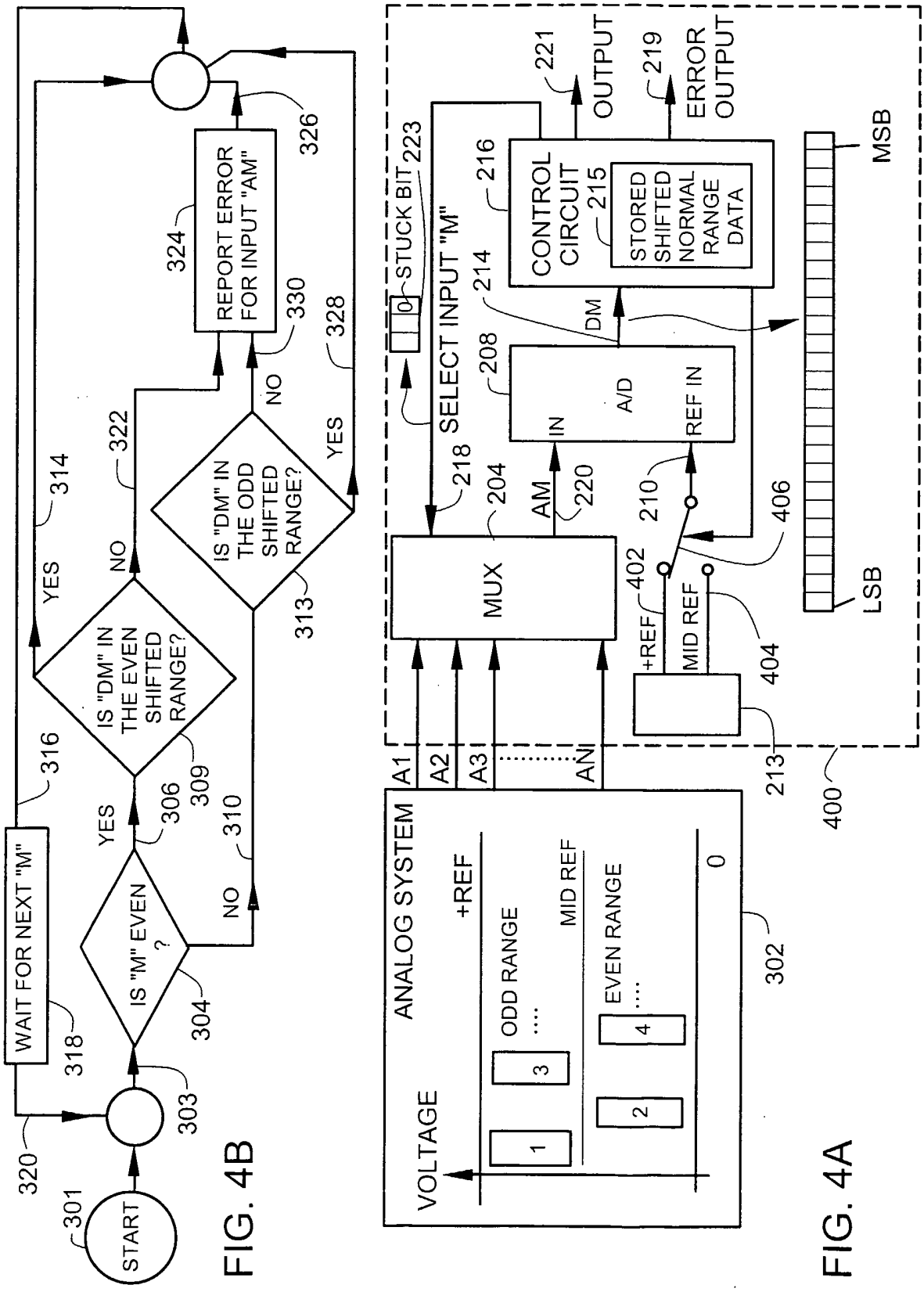
ANALOG SYSTEM
VOLTAGE
+REF
ODD RANGE
MID REF
EVEN RANGE
0
1
2
3
4
302
A1
A2
A3
AN
MUX
SELECT INPUT "M"
218
204
AM
220
IN
A/D
REF IN
208
210
406
402
+REF
MID REF
404
213
400
STUCK BIT
223
0
214
DM
CONTROL CIRCUIT
216
STORED SHIFTED NORMAL RANGE DATA
215
OUTPUT
221
ERROR OUTPUT
219
MSB
LSB
START
301
320
303
WAIT FOR NEXT "M"
318
316
IS "M" EVEN ?
304
306
NO
310
YES
IS "DM" IN THE EVEN SHIFTED RANGE?
309
NO
322
YES
314
IS "DM" IN THE ODD SHIFTED RANGE?
313
NO
330
YES
328
REPORT ERROR FOR INPUT "AM"
324
326

FIG. 4A

FIG. 4B

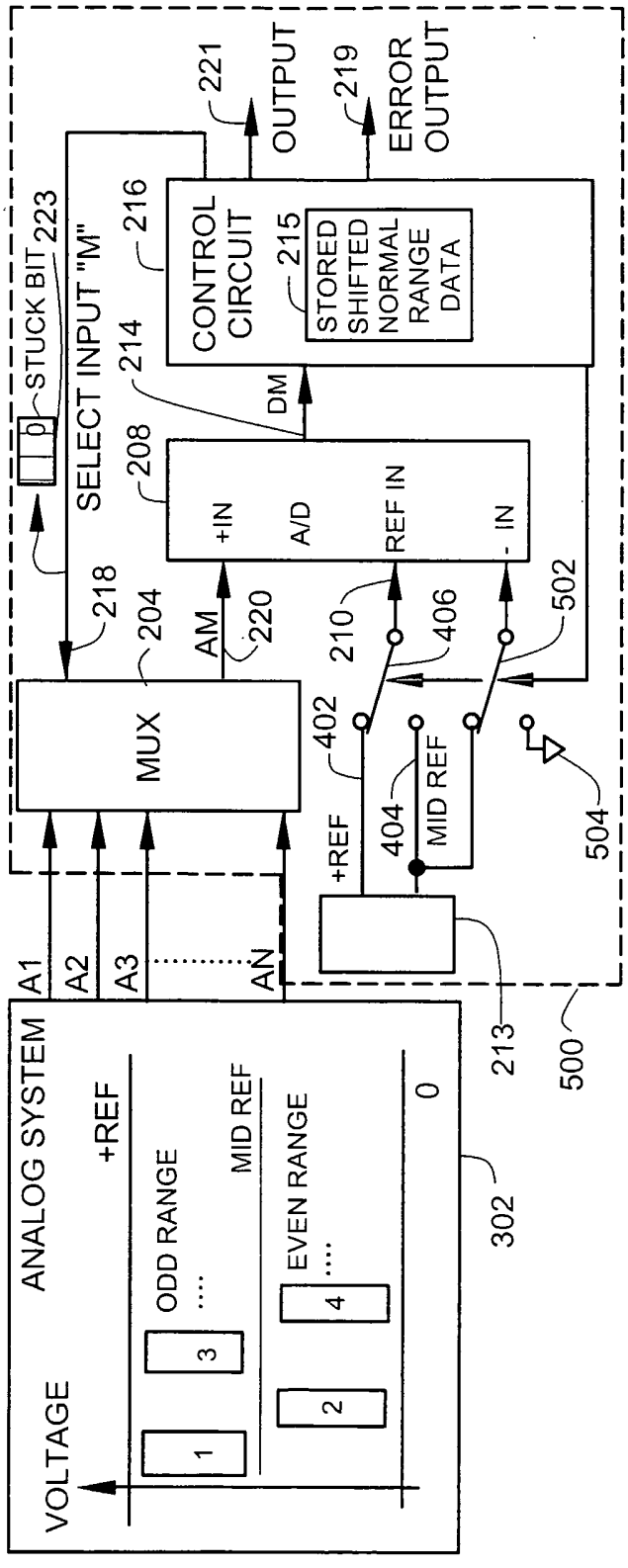
ANALOG SYSTEM
VOLTAGE
+REF
ODD RANGE
MID REF
EVEN RANGE
0
1
2
3
4
302
A1
A2
A3
AN
213
500
MUX
204
218
SELECT INPUT "M"
STUCK BIT
0
223
+REF
402
404
MID REF
210
406
502
504
AM
220
+IN
A/D
REF IN
- IN
208
DM
214
CONTROL CIRCUIT
216
STORED SHIFTED NORMAL RANGE DATA
215
OUTPUT
221
ERROR OUTPUT
219

FIG. 5

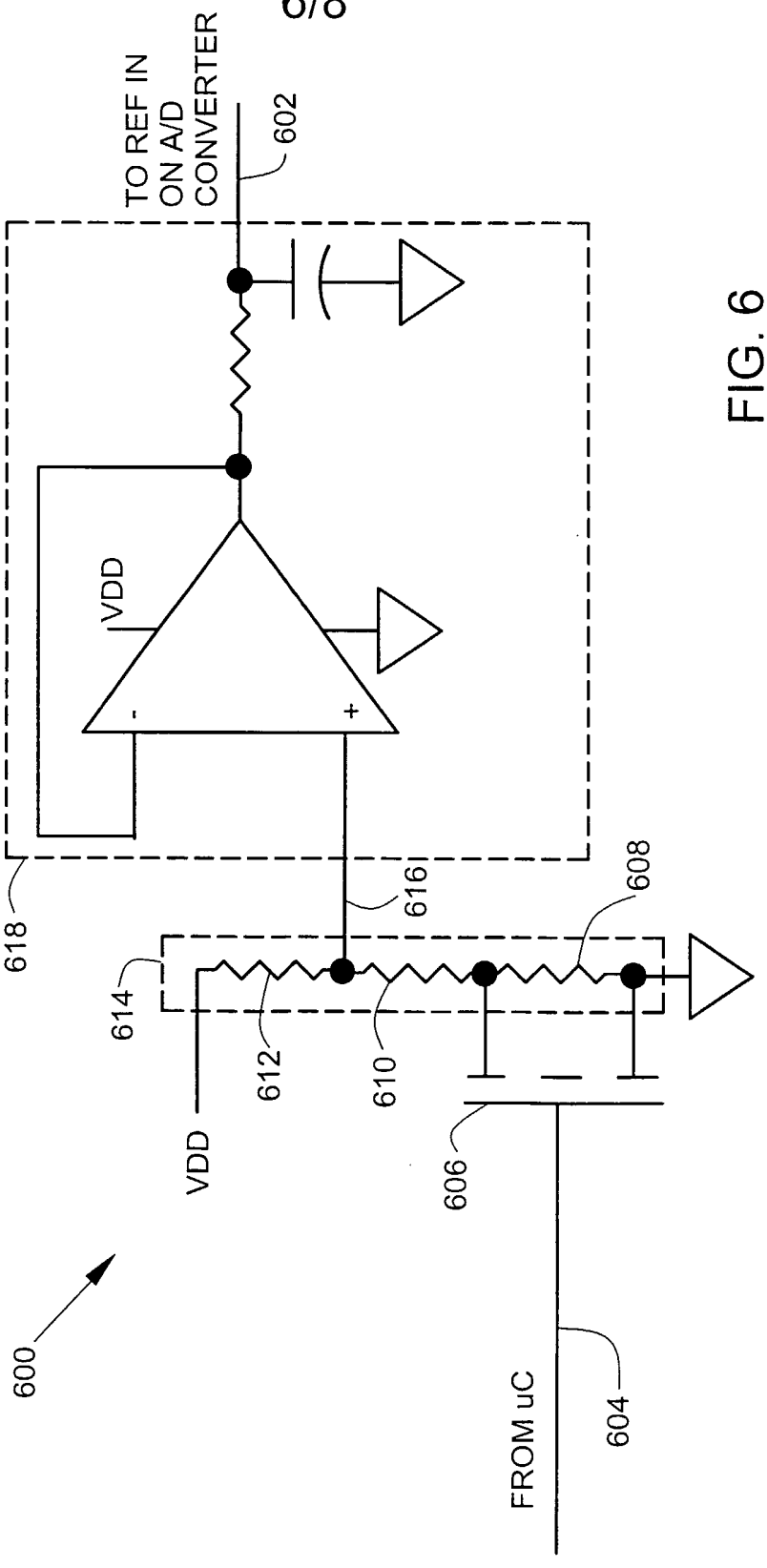
TO REF IN
ON A/D
CONVERTER
602
VDD
-
+
618
616
608
614
612
610
VDD
606
600
FROM uC
604

FIG. 6

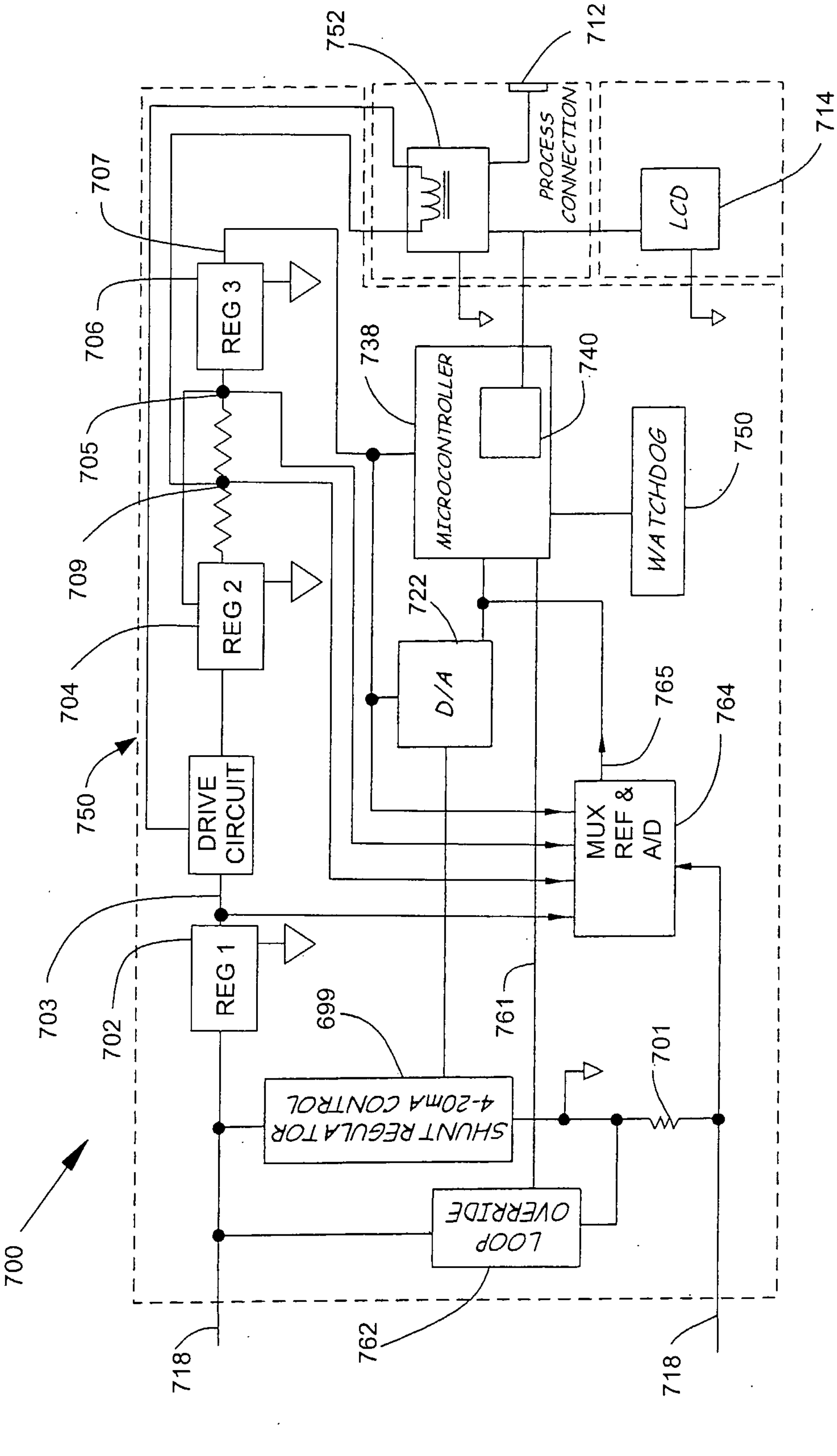
REG 1
REG 2
REG 3
DRIVE CIRCUIT
MICROCONTROLLER
D/A
WATCHDOG
MUX REF & A/D
LCD
PROCESS CONNECTION
SHUNT REGULATOR 4-20mA CONTROL
LOOP OVERRIDE
700
699
701
702
703
704
705
706
707
709
712
714
718
718
722
738
740
750
750
752
761
762
764
765

FIG. 7

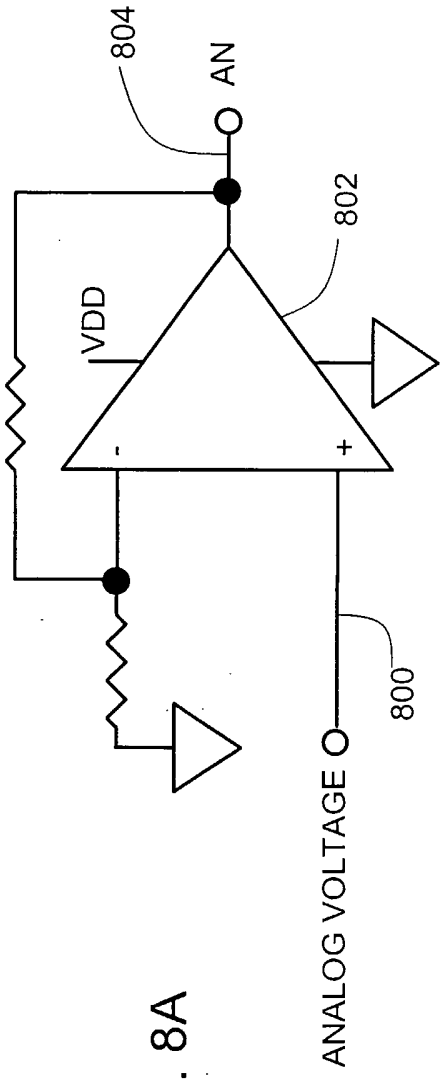

FIG. 8A

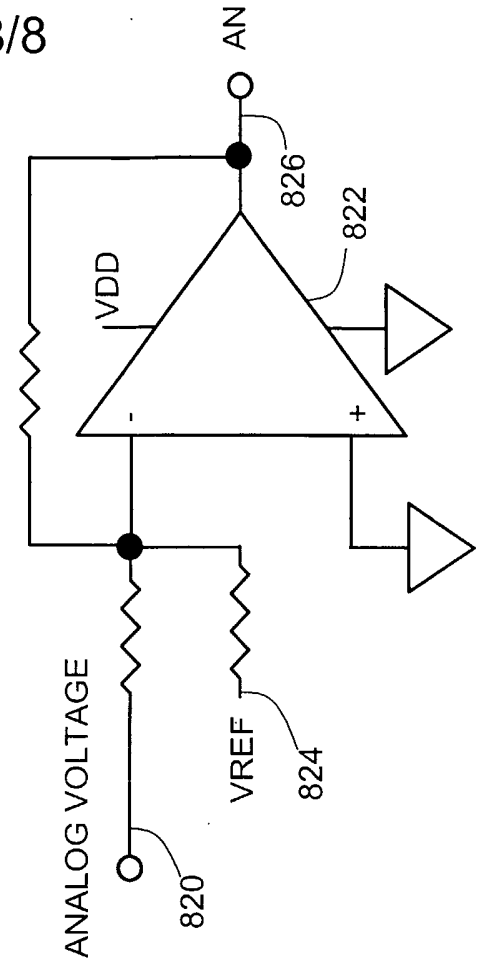

FIG. 8C

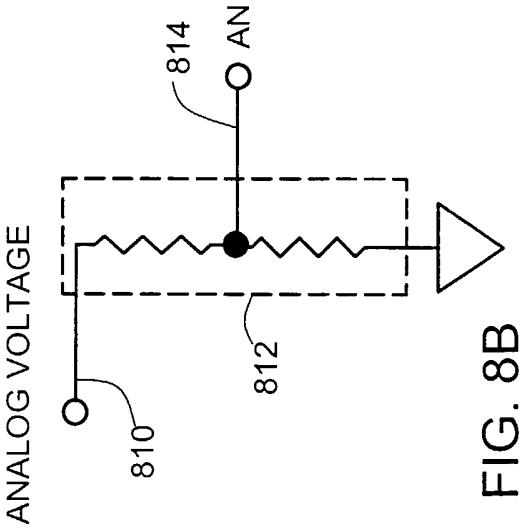

FIG. 8B

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/011385

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03M1/10 H03M1/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 492 921 B1 (KUNITANI HISAO ET AL) 10 December 2002 (2002-12-10) column 7, line 49 - column 8, line 65; figure 4	1,10,19
A		2-9, 11-18, 20,22

A	PATENT ABSTRACTS OF JAPAN vol. 007, no. 045 (E-160), 23 February 1983 (1983-02-23) -& JP 57 196619 A (HITACHI SEISAKUSHO KK), 2 December 1982 (1982-12-02) abstract	1-22

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 June 2005	04/07/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Nicolaucig, A

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/011385

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 396 426 B1 (BALARD ERIC ET AL) 28 May 2002 (2002-05-28) column 4, line 38 - column 7, line 38; claims 1,5; figure 2	1-22
A	GB 2 317 969 A (* ROBERT BOSCH GMBH) 8 April 1998 (1998-04-08) page 5, line 14 - page 9, line 9; figure 1	1-22

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US2005/011385

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 6492921	B1	10-12-2002	JP	2000278132 A	06-10-2000
			WO	0057556 A1	28-09-2000
JP 57196619	A	02-12-1982	NONE		
US 6396426	B1	28-05-2002	FR	2784193 A1	07-04-2000
GB 2317969	A	08-04-1998	DE	19640937 A1	09-04-1998
			FR	2754312 A1	10-04-1998
			IT	MI972192 A1	26-03-1999
			JP	10115247 A	06-05-1998