



- (51) **International Patent Classification:**
H04N 3/14 (2006.01)
- (21) **International Application Number:**
PCT/US2009/057587
- (22) **International Filing Date:**
18 September 2009 (18.09.2009)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
12/284,491 22 September 2008 (22.09.2008) US
- (71) **Applicant** (*for all designated States except US*): **CY-
PRESS SEMICONDUCTOR CORPORATION**
[US/US]; 198 Champion Court, San Jose, California
95134 (US).
- (72) **Inventors; and**
- (75) **Inventors/Applicants** (*for US only*): **DE WIT, Yannick**
[BE/BE]; Sneeuwbaslaan 21, B-2610 Wilrijk (BE).
WALSCHAP, Tom [BE/BE]; Dilkstraat 28, B-2880
Bornem (BE).
- (81) **Designated States** (*unless otherwise indicated, for every
kind of national protection available*): AE, AG, AL, AM,

AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO,
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP,
KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD,
ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI,
NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD,
SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT,
TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

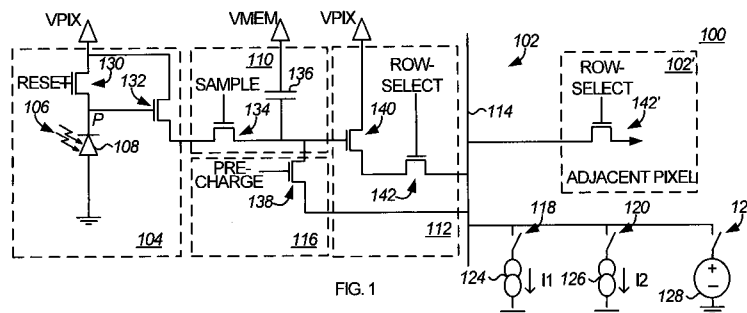
Declarations under Rule 4.17:

- as to the identity of the inventor (Rule 4.17(i))

Published:

- with international search report (Art. 21(3))

- (54) Title:** AN ACTIVE PIXEL WITH PRECHARGING CIRCUIT



- (57) Abstract:** An active pixel including a precharge circuit for a sample and hold (S/H) stage and methods of operating the same are provided. In addition to the precharge circuit and S/H stage, the pixel may include a sensor circuit to generate a signal in response to electromagnetic radiation received on a photodetector included therein, and a multiplexer circuit. The S/H stage may include a switching-element to couple the signal from the sensor circuit to a capacitor element in the S/H stage to read-out and store the signal. The multiplexer circuit may include a switching-element coupled to an output node of the capacitor element to couple the signal to a column. The precharge circuit may include a switching-element coupled between the output node of the capacitor element and the column to precharge the capacitor element to a fixed voltage applied to the column when the S/H stage is not reading-out the signal.

An Active Pixel with Precharging Circuit

TECHNICAL FIELD

[0001] The present disclosure relates generally to an active pixel including a precharge circuit.

BACKGROUND

[0002] Image sensors are widely used in digital cameras and other imaging devices to convert an optical image to an electric signal. Image sensors are fabricated as integrated circuit including a matrix or array of active picture elements or pixels.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] These and various other features of the interface device and methods for using the same will be apparent upon reading of the following detailed description in conjunction with the accompanying drawings and the appended claims provided below, where:

[0004] FIG. 1 is a simplified schematic diagram of a portion of an image sensor including an active pixel comprising an in-pixel precharge circuit and sample and hold (S/H) stage according to one embodiment;

[0005] FIG. 2 is a simplified schematic diagram of a portion of an image sensor including an active pixel comprising an in-pixel precharge circuit and S/H stage according to another embodiment;

[0006] FIG. 3 is a cross section diagram for the implants of an embodiment precharge transistor and row-select transistor having a shared source implant;

[0007] FIG. 4 is a timing chart of signals for an embodiment of a method for precharging the active pixel of FIG. 1;

[0008] FIG. 5 is a flowchart illustrating an embodiment of a method for precharging the active pixel of FIG. 1;

[0009] FIG. 6 is a simplified schematic diagram of a portion of an image sensor including an active pixel comprising an in-pixel precharge circuit and S/H stage according to another embodiment;

[0010] FIG. 7 is a timing chart of signals for an embodiment of a method for precharging the active pixel of FIG. 6; and

[0011] FIG. 8 is a flowchart illustrating an embodiment of a method for precharging the active pixel of FIG. 6.

DETAILED DESCRIPTION

[0012] For purposes of clarity, many of the details of image sensors in general and to image sensors including arrays of active pixels in particular, which are widely known and not relevant to the present control system and method have been omitted from the following description.

[0013] A simplified schematic diagram of a portion of an image sensor **100** including an embodiment of a single, active pixel **102** with an in-pixel sample and hold (S/H) stage and precharge circuit is shown in FIG. 1. Generally the active pixel **102** is one of a number of pixels in an array of pixels (not shown) arranged in multiple rows and multiple columns, each column shared by multiple pixel outputs from the multiple rows

of pixels to enable a pipelined or sequential readout of each row of pixels in the array through the shared columns coupled thereto. The array of pixels is formed in a layer of semiconductor material on a common, shared wafer or substrate (not shown), which may include other elements and circuits of the image sensor. The semiconductor layer may include any known semiconductor material including silicon, germanium, and indium-gallium-arsenide.

Referring to FIG. 1, the active pixel **102** generally includes a sensor circuit **104** to generate a signal in response to electromagnetic radiation **106** (light) received on a photosensor or photodetector **108**. Signals from the sensor circuit **104** are electrically coupled to a sample and hold (S/H) stage **110**, which reads-out or samples and temporarily stores the signals. The pixel **102** further includes a multiplexer or buffer/multiplexer circuit **112** to couple an output node of the S/H stage **110** to a pixel output or column **114**. A precharge circuit **116** is also coupled to the output node of the S/H stage **110** to precharge a storage element therein to a precharge voltage prior to the S/H stage sampling the signal from the sensor circuit **104**. The image sensor **100** further includes a number of switching-elements **118**, **120** and **122** to sequentially couple the column **114** to an output load **124**, a column precharge source or current path (I2 **126**) and a column high voltage supply **128** respectively.

[0014] The photodetector **108** can include one or more photodiodes (PD), phototransistors, photoresistors or a charge-coupled device (CCD), which generates distinct changes in current, or voltage or a charge on photodetector in response to incident electromagnetic radiation. In the embodiment shown in FIG. 1 the photodetector **108** is a reverse-biased photodiode coupled between a positive pixel voltage supply

(Vpix) and ground. When exposed to electromagnetic radiation (light) **106**, the semiconductor material of which the photodiode is fabricated photogenerates charge carriers, e.g. electrons, in proportion to the energy of electromagnetic radiation **106** received and to the time or integration period over which the PD is exposed and to the photocurrent or current through the PD. A reset switching-element or transistor **130** periodically resets the photodetector **108** to a fixed bias, clearing all accumulated charge on the photodetector **108** at the beginning of every integration period. The sensor circuit **104** further includes a readout transistor, such as a source follower (SF) amplifier **132**, having a drain connected or coupled to Vpix and a source coupled to an input of the S/H stage **110**. The SF **132** generates a voltage signal corresponding to the charge accumulated on the photodetector **108**, and acts as a buffer to enable the charge on the photodetector to be sampled or observed without removing the accumulated charge.

[0015] The S/H stage **110** samples and holds or stores the voltage signal from the sensor circuit **104**. The S/H stage **110** includes a sample switching-element or transistor **134** electrically connected or coupled to the SF **132** at the output of the sensor circuit **104** to couple the voltage signal to a memory or capacitor element, such as a capacitor **136** in FIG. 1. More specifically, after a predetermined integration period, a sample signal (SAMPLE) is applied to a gate of the sampling transistor **134** for a predetermined sample period causing the transistor to conduct storing a voltage signal on the capacitor **136**. The magnitude of the voltage signal stored on the capacitor **136** depends on the charge accumulated in the PD depletion capacitance and a transfer function of the SF **132** and sampling transistor **134**.

[0016] To provide an accurate measurement or sample of the voltage signal from the sensor circuit **104**, the capacitor **136** in the S/H stage **110** is precharged to delete any previous sampled value. The S/H stage **110** is driven by a simple source follower (SF **132**) and, if a previous sampled value is higher or within a threshold voltage (V_T) of the SF **132** of the next sampled value, the SF may cut off and no sampling will take place. Thus, without precharging or clearing the capacitor element, the image sensed by the image sensor **100** may rise to a black or blank image over time.

[0017] Referring to FIG. 1, in the implementation of the S/H stage **110** shown, the capacitor **136** is coupled to a positive memory voltage supply (V_{mem}) and through a precharge switching element or transistor **138** in the precharge circuit **116** to the column **114**. The column **114** is in turn coupled through the column precharge switch **120**, to a column precharge current supply **126** to simultaneously precharge the capacitor and the column to a predetermined voltage before the sampling occurs. It will be appreciated that coupling the capacitor **136** to the column **114** for precharging, rather than to an in-pixel ground tap or a separate precharge line, as is done in other precharge circuits, decreases a surface area of the pixel taken up with non-light sensitive elements substantially increasing the fill factor of the pixels and the array, thereby increasing the sensitivity of the image sensor **100**. By fill factor it is meant a ratio of the area of photosensitive elements in a pixel **102** or an array to a total area of the pixel or array. It will further be appreciated that increasing the fill factor also significantly increases the signal-to-noise (SNR) of the image sensor **100**, as the SNR is directly related to the product of fill factor and quantum efficiency.

[0018] In certain embodiments, columns **114** of image sensors **100** are also precharged prior to reading the signal on capacitor **136** to clear or erase any previous voltage thereon which could lead to ghosting. In other active pixels and image sensors column precharging is accomplished during or after sampling of the voltage signal from the sensor circuit **104** in a separate step or event from that of precharging the capacitor **136**. In contrast, the precharging circuit **116** of the active pixel **102** of FIG. 1 enables simultaneous precharging of the capacitor **136** and the column **114** to speed up precharging of the pixel.

[0019] In the embodiment shown in FIG. 1 and described above, the precharge transistor **138** is coupled to the precharge current supply **126** through the same column **114** to which the buffer/multiplexer circuit **112** is coupled to readout the sampled signal from the pixel **102**. The precharge transistor may alternatively be coupled to any column in the array located near the pixel in which it is included. Referring to FIG. 2 it is seen that in other embodiments the precharge transistor **238** of the precharge circuit **216** can be coupled to a column **214'** different from the column **214** to which the buffer/multiplexer circuit **212** of the pixel **202** is coupled. The column **214'** to which the precharge transistor **238** is coupled can include, for example, the column to which an adjacent pixel **202'** located in a different column and possibly a different row in the array is coupled. In addition to the precharge circuit **216** and buffer multiplexer circuit **212**, the pixel **202** includes a S/H stage **210** and a sensor circuit **204**, all of which function as in the pixel **102** of FIG. 1 described above.

[0020] Optionally as in the embodiment shown in FIG. 1, the image sensor **100** further includes a column high voltage switching-element **122** and a column high voltage

supply 128 to apply a fixed high voltage to the column 114 after precharging to reduce or eliminate loss of voltage stored on the capacitor 136 through drain-to-source leakage of the precharge transistor 138 by providing a negative gate to source voltage (V_{gs}) on the precharge transistor. In the embodiment shown in FIG. 1, this fixed high voltage can be applied during and after sampling of the sensor circuit 104 by the S/H stage 110 but may be removed prior to reading out the voltage signal on capacitor 136.

[0021] After precharging the capacitor 136 and sampling the voltage signal from the sensor circuit 104, the voltage signal on capacitor 136 is readout by the buffer/multiplexer circuit 112. In the embodiment shown in FIG. 1 the buffer/multiplexer circuit 112 includes a source follower (SF) amplifier 140 that acts as a buffer and has a drain connected or coupled to V_{pix} and a source coupled to the column 114 through a row-select switching-element or transistor 142. For reading, a row-select signal is applied to a gate of the row-select transistor causing it to conduct and to transfer the voltage at the source of the SF amplifier 140 to the column 114. Switch 118 is also closed, coupling the column 114 to the column load 124.

[0022] Although the sensor circuit 104 and buffer/multiplexer circuit 112 are shown as including source follower (SF) amplifiers 132, 140, respectively, which serve as buffers, it will be appreciated that other amplifier configurations can also be used to serve as buffers. It will further be appreciated that the SF amplifiers 132, 140, can be included in separate buffer stages (not shown) located between the sensor circuit 104 and S/H stage 110, and between the S/H stage and buffer/multiplexer circuit 112.

[0023] In another aspect, shown in FIG. 3, in certain embodiments the precharge switching element comprises a metal-oxide-semiconductor field-effect transistor

(MOSFET) 338 sharing a common source implant 344 with that of a row-select, MOSFET transistor 342 to further increase the fill factor of the pixel by reducing the area occupied by non-light sensitive transistors, thereby reducing the pitch or spacing between centers of the pixels. The precharge transistor 338 and the row-select transistor 342 are coupled through the shared source implant 344 to a column 314. The precharge transistor 338 further includes a drain implant 346 coupled to an output node of the capacitor in the S/H stage (not shown in this figure) and a gate stack or electrode 348 overlying a channel region 350 formed in the underlying substrate 352. The row-select transistor 342 further includes a drain implant 354 coupled to an output of a buffer (not shown), such as SF amplifier 140 in FIG. 1, and a gate electrode 356 overlying a channel region 358 joining the source implant 344 and the drain implant. The row-select transistor 342 with which the precharge transistor 338 shares the source implant 344 may be part of the same pixel as the precharge transistor, or may be a row-select transistor in an adjacent pixel in an array of pixels and the shared source implant may couple to a column 314 different from the column of the pixel comprising the precharge transistor.

[0024] In one embodiment, shown in FIG. 1, the precharge transistor 138 in a pixel 102 can share a source implant (not shown) with a row-select transistor 142' of an adjacent pixel 102' located in a different row in an array of pixels but coupling to the same column 114.

[0025] In an alternative embodiment, shown in FIG. 2, the precharge transistor 238 in one pixel 202 can share a source implant with a row-select transistor 242' of an adjacent pixel 202' located in a different column and possibly a different row in an array of pixels.

[0026] In the embodiment shown in FIG. 3, the precharge transistor **338** and row-select transistor **342** are NMOS transistors with n-type channels and n++ doped source and drain implants fabricated in a p-type substrate. However, it will be appreciated that this is not necessarily the case and the precharge transistor and row-select transistor can instead comprise PMOS transistors with appropriating biasing and selection of the control signals (PRECHARGE and ROW-SELECT) to the gates thereof.

[0027] A method of operating the image sensor **100** to precharge and read-out the pixel **102** of FIG. 1 will now be described with reference to the timing diagram of FIG. 4 and the flowchart of FIG. 5. Referring to FIGs. 4 and 5, in first block (block **502**) a reset signal or voltage (Vreset **402**) is applied for a brief, predetermined period of time to the gate of the reset transistor **120** to clear any charge accumulated on the photodetector (PD **108**). Thereafter, charge photogenerated by electromagnetic radiation **106** (light) received on the photodetector **108** is allowed to accumulate at output node **P** during subsequent precharging, sampling and read out steps. Next, the capacitor **136** in the S/H stage **110** is precharged (Block **504**).

[0028] In one embodiment, the precharging of the capacitor **136** is accomplished by briefly applying a column precharge signal (column precharge **408**) to close column precharge switching element **120** and a precharge signal (precharge **406**) to the precharge transistor **138**.

[0029] After the capacitor **136** has been precharged, the charge accumulated at photodiode node **P** in the sensor circuit **104** is then sampled by applying a sampling signal (Vsample **404**) to the sampling transistor **134**, causing it to conduct and transfer the voltage at the source of the SF **132** to the capacitor (Block **506**). While the sampling

continues a second column precharge signal (column precharge 410) can be applied to the precharge switching element 120 to precharge or maintain a complete precharge on column 114 in preparation for reading out the pixel 102 (Block 508).

[0030] After the sensor circuit 104 has been sampled and the column 114 precharged, switching-element 118 is closed to couple the column 114 to the output load 124, and a row-select signal (select 412) is applied to the row-select transistor 142, causing it to conduct and transfer the voltage at a source of the SF 140 to the column (Block 510). The multiple row-select signals (select 412) with the dashed line in between are meant to illustrate a sequential read of pixels in different rows in a single column, as row after row is read out. Switching-element 118 may be closed in response to the row-select signal (select 412)

[0031] Optionally, in embodiments in which the precharge transistor is coupled to a column of an adjacent pixel, such as that shown in FIG. 2 and described above, reading out the pixel (Block 510) can further include applying a select column high voltage signal 414 to switching-element 122 to apply a fixed high voltage to the column 214 after precharging to reduce or eliminate loss of voltage stored on the capacitor 136 through drain-to-source leakage of the precharge transistor 138.

In yet another aspect, shown in FIG. 6, in certain embodiments the precharge circuit 616 or transistor 638 can be coupled to a capacitor 636 in an S/H stage 610 through a sampling transistor 634 in the S/H stage. This embodiment further reduces a loss of charge stored on the capacitor 636 through drain-to-source leakage of the precharge transistor 638.

Referring to FIG. 6, the pixel **602** includes a sensor circuit **604** having a photodetector **608** to generate a signal in response to light received thereon, a reset transistor **630**, and a SF **632** buffer through which the sensor circuit is coupled to an S/H stage **610**. The output of the S/H stage **610** is coupled to a column **614** through a buffer/multiplexer circuit **612** including an SF amplifier **640** which serves as buffer and a row select transistor **642**. As in the embodiment of FIG. 1 described above, the image sensor **600** further includes a number of switching-elements **618**, **620** and **622** to sequentially couple the column **614** to an output load **624**, a column precharge source or current path (I2 **626**) and a column high voltage supply **628**, respectively.

[0032] It will be appreciated that since the sampling transistor **634** is on during pixel precharging, the timing or sequence of signal for operating the pixel **602** of FIG. 6 is slightly different than that described above with reference to FIG. 1.

[0033] A method of operating the image sensor **600** to precharge and read-out the pixel **602** of FIG. 6 will now be described with reference to the timing diagram of FIG. 7 and the flowchart of FIG. 8. Referring to FIGs. 7 and 8, in first block (block **802**) a reset signal or voltage (Vreset **702**) is applied for a brief, predetermined period of time to the gate of the reset transistor **620** to clear any charge accumulated on the photodetector **608**. Thereafter, charge photogenerated by light received on the photodetector **608** is allowed to accumulate at output node **P**.

[0034] Next, the capacitor **636** in the S/H stage **610** is precharged (Block **804**) by applying a sampling signal (Vsample **704**) to the sampling transistor **634**, briefly applying a column precharge signal (column precharge **708**) to close column precharge

switching element **620** and, briefly, applying a precharge signal (precharge **706**) to the precharge transistor **638**.

[0035] After the capacitor **636** has been precharged, the column precharge signal **708** and precharge signal **706** are removed while the sampling signal **704** is maintained to sample the charge accumulated in the sensor circuit **604** (Block **806**). While the sampling continues, a second column precharge signal (column precharge **710**) can be applied to the precharge switching element **620** to precharge or maintain a complete precharge on column **614** in preparation for reading out the pixel **102** (Block **808**).

[0036] After the sensor circuit **604** has been sampled and the column **614** precharged, switching-element **618** is closed to couple the column **614** to the output load **624**, and a row-select signal (select **712**) is applied to the row-select transistor **642**, causing it to conduct and transfer the voltage at a source of the SF **640** to the column (Block **810**).

[0037] Thus, embodiments of a precharging circuit and a method for precharging an in-pixel S/H stage of an active pixel that increases fill factor and SNR while decreasing precharge time have been described. Although the present disclosure has been described with reference to specific exemplary embodiments, it will be evident that various modifications and changes may be made to these embodiments without departing from the broader spirit and scope of the invention. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

[0038] The Abstract of the Disclosure is provided to comply with 37 C.F.R. §1.72(b), requiring an abstract that will allow the reader to quickly ascertain the nature of the technical disclosure. It is submitted with the understanding that it will not be used to

interpret or limit the scope or meaning of the claims. In addition, in the foregoing Detailed Description, it can be seen that various features are grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the claimed embodiments require more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter lies in less than all features of a single disclosed embodiment. Thus the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment.

[0039] In the forgoing description, for purposes of explanation, numerous specific details have been set forth in order to provide a thorough understanding of the control system and method of the present disclosure. It will be evident however to one skilled in the art that the present interface device and method may be practiced without these specific details. In other instances, well-known structures, and techniques are not shown in detail or are shown in block diagram form in order to avoid unnecessarily obscuring an understanding of this description.

[0040] Reference in the description to “one embodiment” or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the control system or method. The appearances of the phrase “one embodiment” in various places in the specification do not necessarily all refer to the same embodiment. The term “to couple” as used herein may include both to directly electrically connect two or more components or elements and to indirectly connect through one or more intervening components.

IN THE CLAIMS

1. An active pixel comprising:
 - a sensor circuit to generate a signal in response to electromagnetic radiation received on a photodetector included therein;
 - a sample and hold (S/H) stage coupled to an output of the sensor circuit to read-out and store the signal, the S/H stage including a sample switching-element to couple the signal from the sensor circuit to a capacitor element in the S/H stage to store the signal;
 - a buffer/multiplexer circuit including a row-select switching-element coupled to an output node of the capacitor element to couple the signal to a column; and
 - a precharge circuit including a precharge switching-element coupled between the output node of the capacitor element and the column to precharge the capacitor element to a precharge voltage applied to the column when the S/H stage is not reading-out the signal from the sensor circuit.
2. An active pixel according to claim 1, wherein the precharge switching-element comprises a precharge transistor having a drain coupled to the output node of the capacitor element and a source coupled to the column.
3. An active pixel according to claim 2, wherein the row-select switching-element comprises a row-select transistor having a drain coupled to the output node of the capacitor element through a buffer and a source coupled to the column, and wherein the source of the row-select transistor and the source of the precharge transistor comprise a shared source implant.

4. An active pixel according to claim 2, wherein the active pixel is one of a plurality of pixels in an array of pixels, and wherein the precharge transistor shares a source implant with a row-select transistor in an adjacent pixel in the array of pixels.

5. An active pixel according to claim 1, wherein the sample switching-element comprises an input node coupled to the output of the sensor circuit and a second output node coupled to the output node of the capacitor element, wherein the precharge switching-element couples to the output node of the capacitor element through the sample switching-element, wherein the sensor circuit further includes a reset switching-element and a source follower amplifier (SF) through which the sensor circuit is coupled to the S/H stage, and wherein the SF decouples the sensor circuit from the S/H stage when a reset signal is applied to the reset switching-element to enable the capacitor-element to be precharged through the sample switching-element and the precharge switching-element.

6. An active pixel according to claim 5, wherein the precharge switching-element does not couple to the output node of the capacitor element through the sample switching-element, and wherein the sample switching-element decouples the capacitor element from the sensor circuit to enable the capacitor-element to be precharged through the precharge switching-element.

7. A method for precharging a capacitor element in an in-pixel sample and hold (S/H) stage of an active pixel, the method comprising:

electrically decoupling a sensor circuit in the active pixel from the S/H stage;

electrically coupling an output node of the capacitor element to a column through a precharge transistor, the precharge transistor having a drain coupled to the output node of the capacitor element and a source coupled to the column; and

applying a precharge voltage to the column to precharge the capacitor element and the column.

8. A method according to claim 7, wherein the active pixel further comprises a row-select transistor having a drain coupled to the output node of the capacitor element through a buffer and a source coupled to the column, and wherein the source of the row-select transistor comprises a source implant shared with the source of the precharge transistor.

9. A method according to claim 7, wherein the S/H stage further comprises a sample transistor through which the sensor circuit is coupled to the output node of the capacitor element, and wherein the precharge transistor couples to the output of the capacitor element through the sample transistor.

10. A method according to claim 7, further comprising applying a fixed high voltage to the column after precharging the capacitor element to decrease leakage through the precharge transistor during readout of the sensor circuit by the S/H stage.

1/5

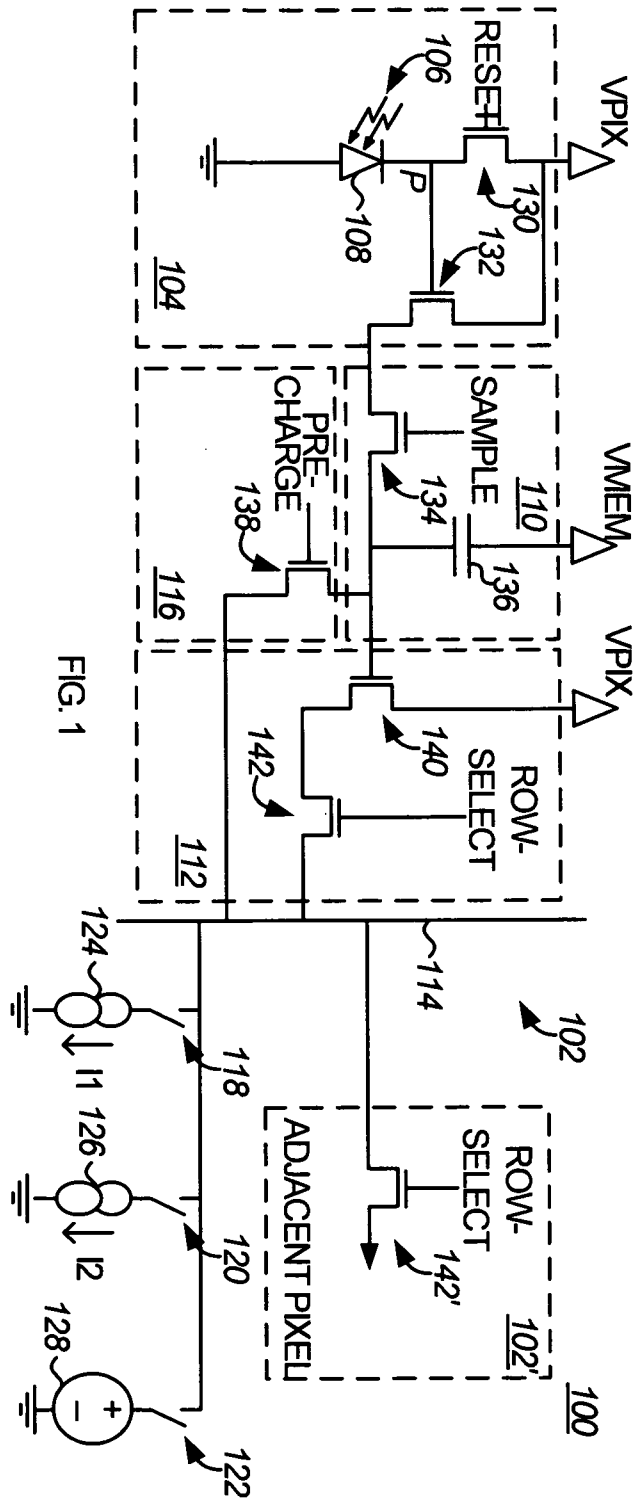


FIG. 1

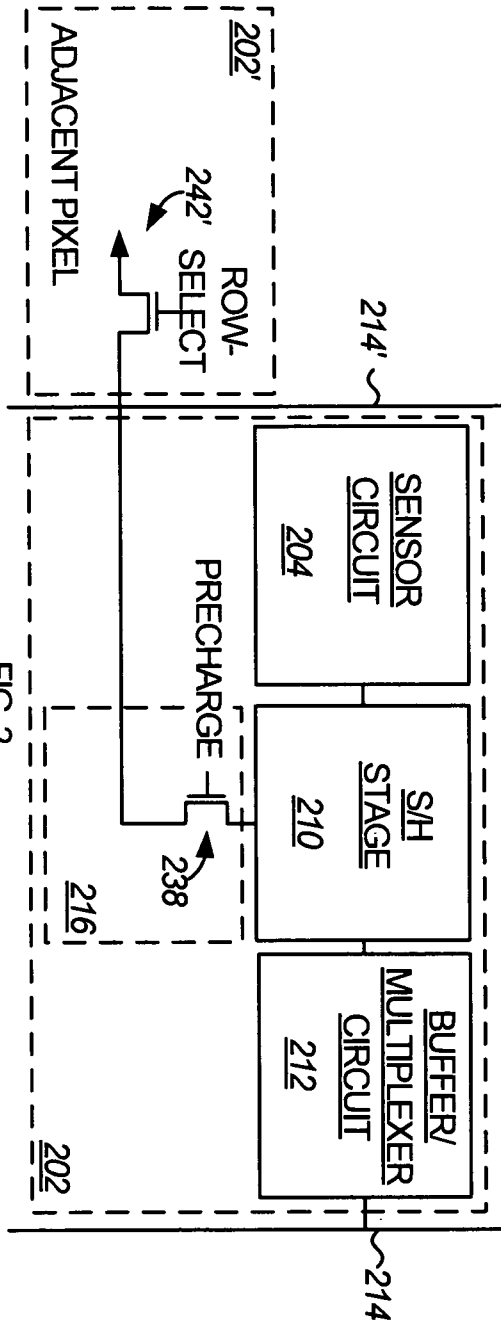


FIG. 2

2/5

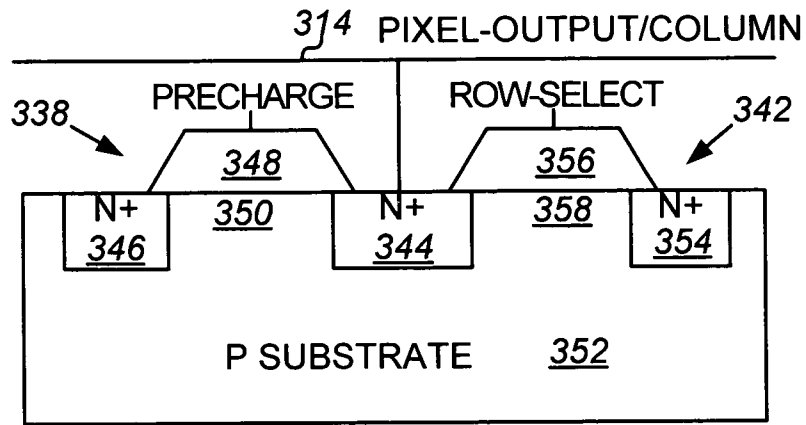


FIG. 3

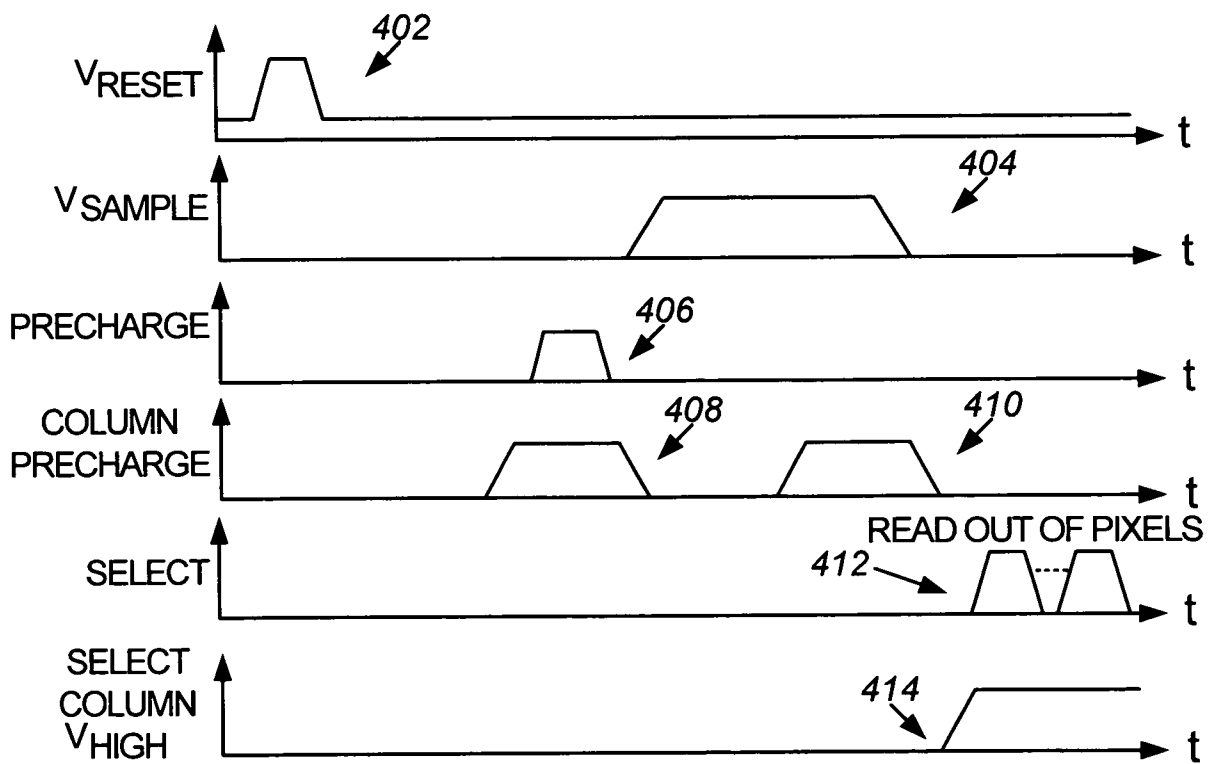


FIG. 4

3/5

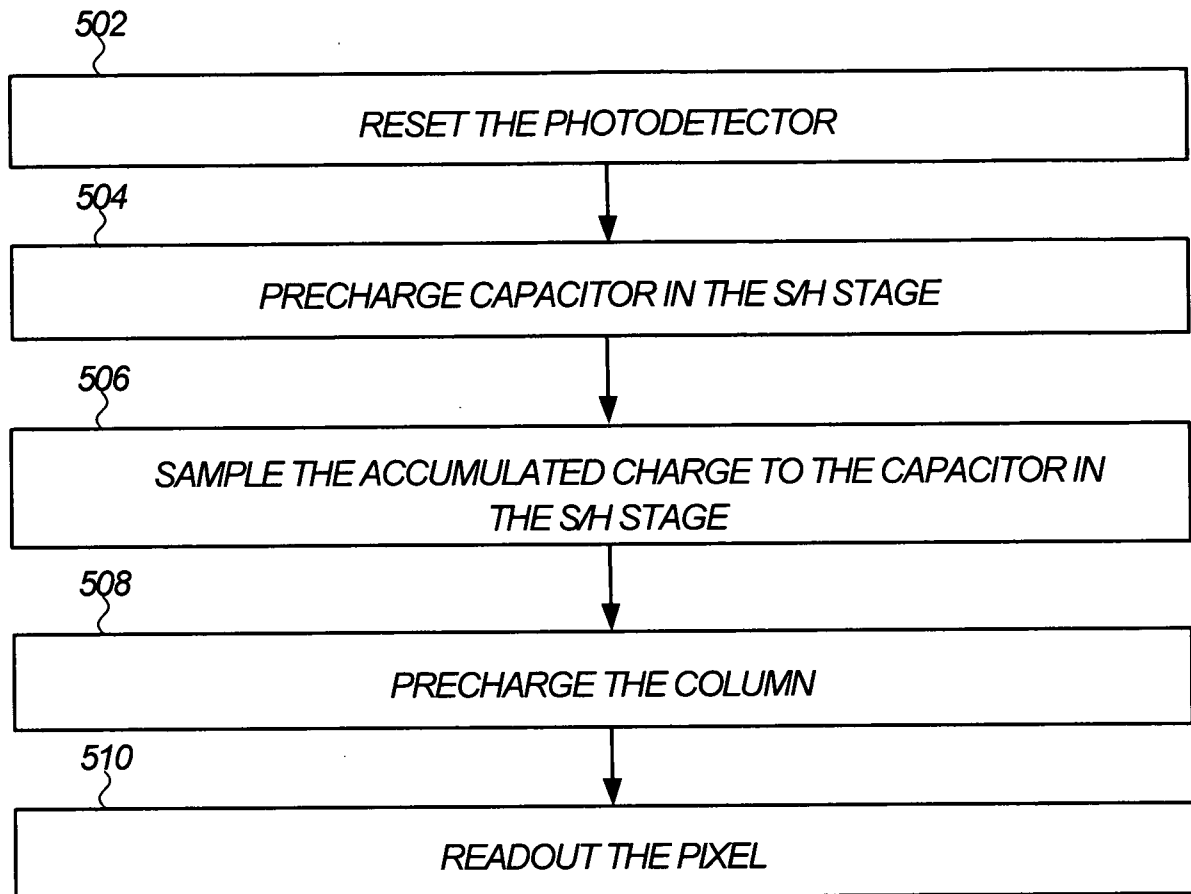


FIG. 5

4/5

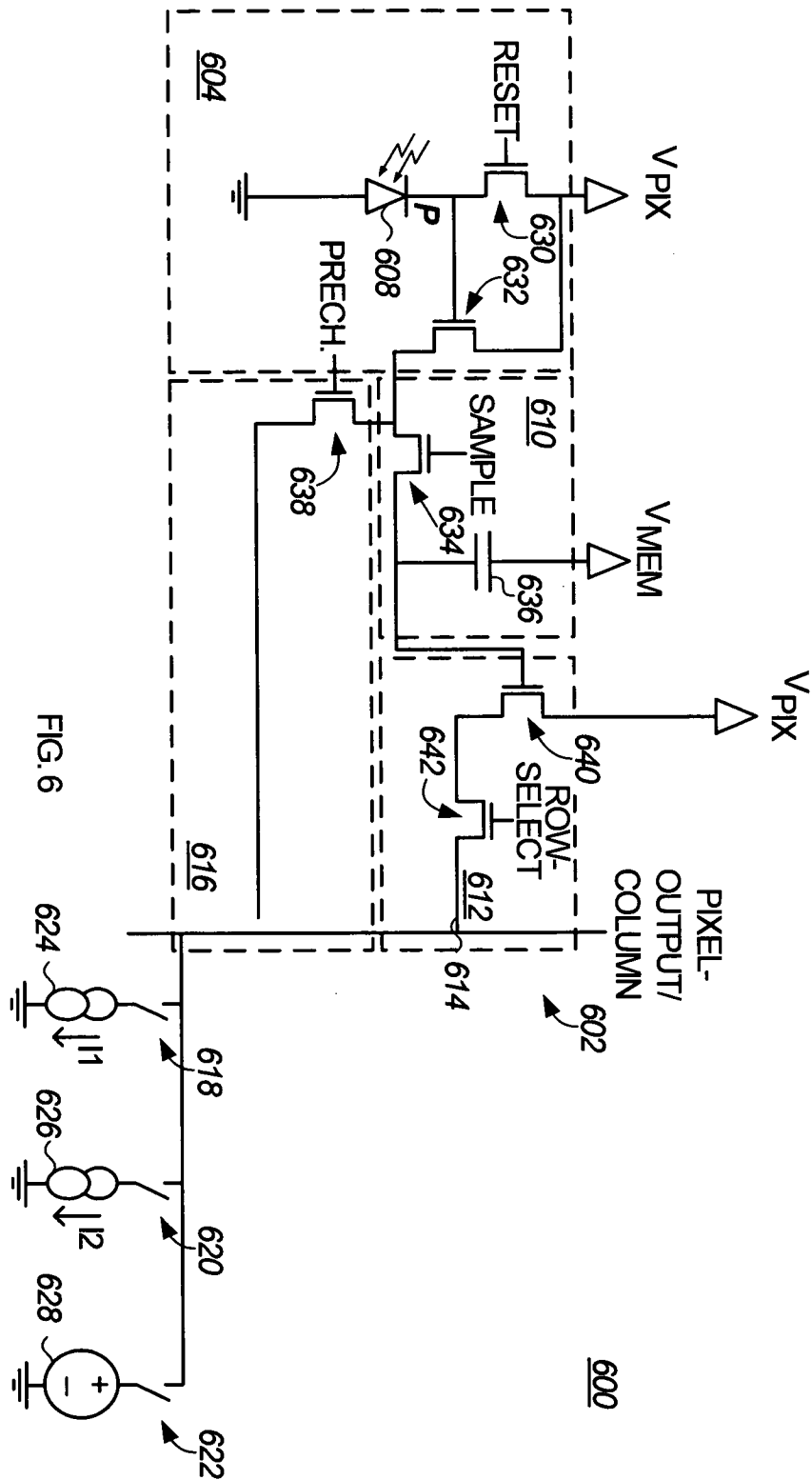


FIG. 6

5/5

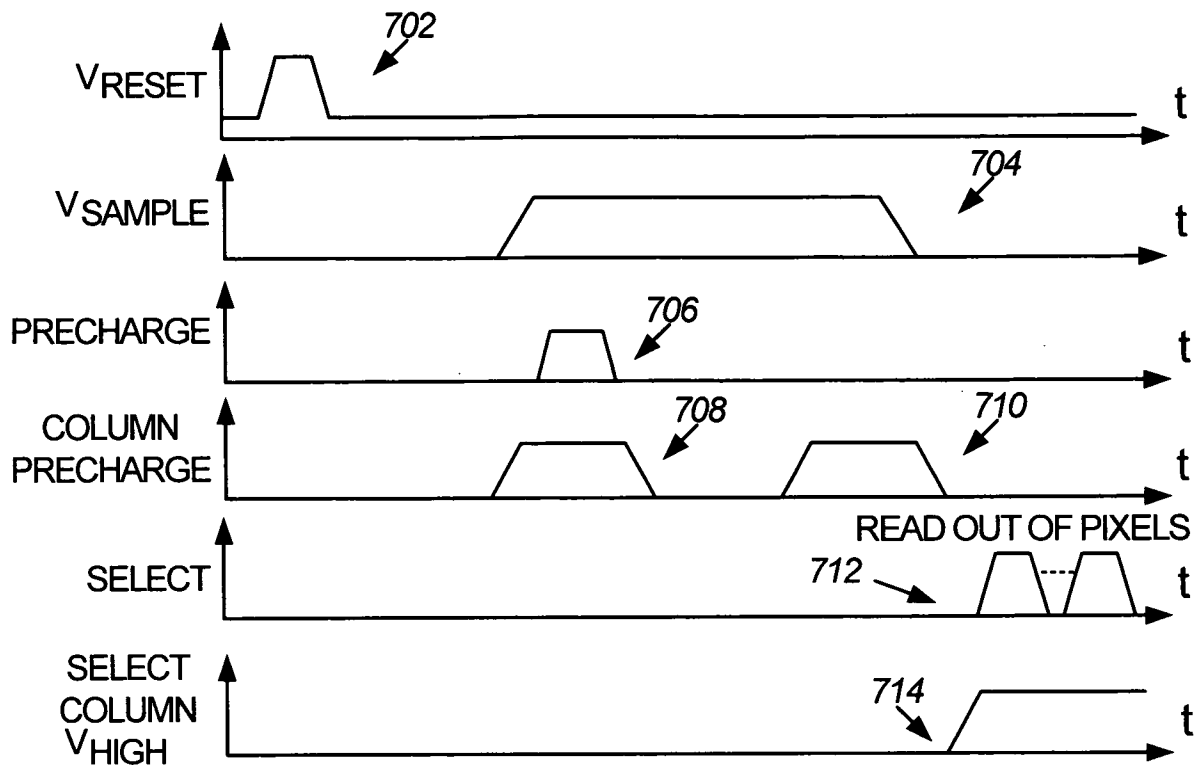


FIG. 7

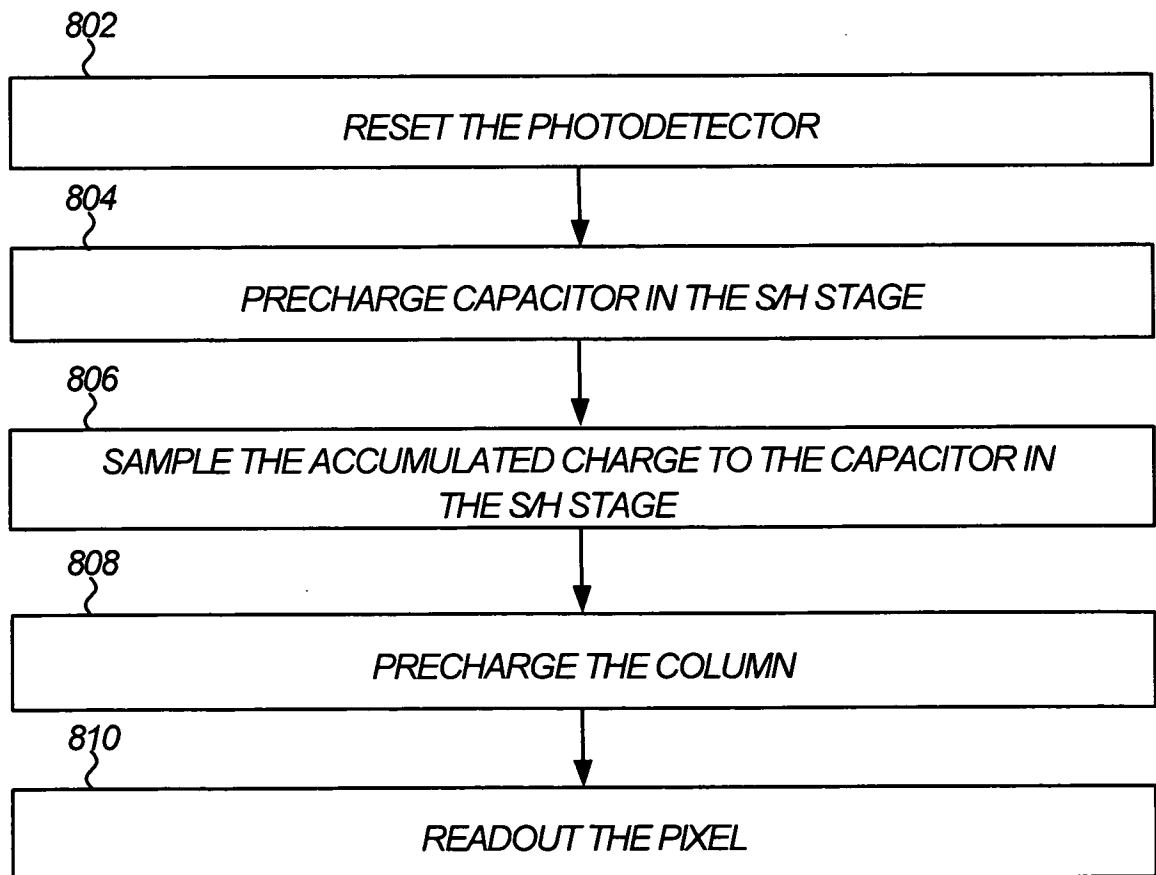


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 09/57587

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H04N 3/14 (2009.01)

USPC - 348/308

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

USPC: 348/308

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

USPC: 348/303, 304, 308

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PubWEST(USPT,PGPB,EPAB,JPAB); Google Patents; Google Scholar

Search Terms: active, pixel, sample, hold, precharge, transistor, row, select, array

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003/0011694 A1 (Dierickx) 16 January 2003 (16.01.2003), para [0007], [0009], [0011], [0013], [0019], [0025], [0035], [0039], [0041], [0042], [0043]	1-10
A	US 2008/0074524 A1 (Panicacci) 27 March 2008 (27.03.2008), entire document	1-10

☐ Further documents are listed in the continuation of Box C.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

15 November 2009 (15.11.2009)

Date of mailing of the international search report

30 NOV 2009

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US, Commissioner for Patents

P.O. Box 1450, Alexandria, Virginia 22313-1450

Facsimile No. 571-273-3201

Authorized officer:

Lee W. Young

PCT Helpdesk: 571-272-4300

PCT OSP: 571-272-7774