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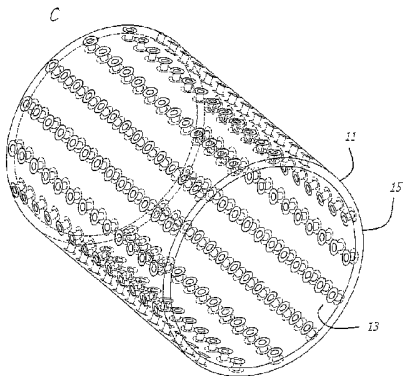
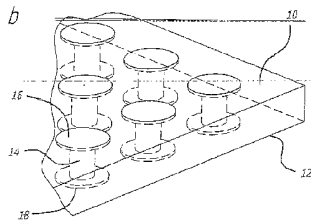
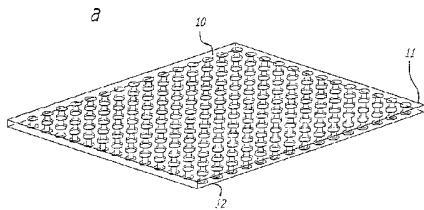
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[Continued on next page]

(54) Title: DIGITAL SEMICONDUCTOR BASED PRINTING SYSTEM AND METHOD



(57) Abstract: A digital printing system uses individual memory cells within memory dies mounted on a substrate to attract or repel ink in order to produce an image. There is a dead space between adjacent individual memory cells and also between adjacent memory dies. By staggering the location of the memory dies on two or more substrates the dead spaces may be eliminated or minimized. In addition, staggering the location of the memory dies on the substrates allows for backup operations in the event that a primary memory cell fails and for resolution stepping of the printed image.



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DIGITAL SEMICONDUCTOR BASED PRINTING SYSTEM AND METHOD

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This application claims priority to the prior patent application entitled, DIGITAL SEMICONDUCTOR BASED PRINTING SYSTEM AND METHOD, having a serial number of 10/759,765 and that was filed in the United States Patent and Trademark Office on January 16, 2004, to the prior patent application entitled, DIGITAL SEMICONDUCTOR BASED PRINTING SYSTEM AND METHOD, having a serial number of 10/956,416 and that was filed in the United States Patent and Trademark Office on October 1, 2004, and prior provisional patent application entitled DIGITAL PRINTING TECHNOLOGIES filed March 24, 2005.

BACKGROUND

[0001] 1. *Field of the Invention*

[0002] The present invention generally relates to semiconductor techniques for printing.

[0003] 2. *General Background and State of the Art*

[0004] There are currently several dominant techniques used in computer based and commercial printing (non-impact printing).

[0005] A large portion of Personal Computer (PC) based printing is based on Ink Jet technology, or "Drop on Demand" methods where the image to be printed is constructed on an appropriate printing medium such as paper, plastic, textiles, printing plates and even silicon based substrates using print heads which eject drops of ink at the appropriate location on the printing medium. Since the ejection of ink occurs at the time the image is being printed this is often called "Drop on Demand" printing. The ink ejection mechanism may be controlled using piezo electric mechanisms or thermal mechanisms (ink jet or bubble jet). These printing methods rely on electronics that reside on the computer and on the printing equipment to deposit the ink on the printing

medium. Since the entire image is constructed on a drop-by-drop basis, this can be a rather slow process.

[0006] Another kind of commercial printing that is carried out using the ink-jetting technique is called the Continuous Ink-Jetting Method. In this method, a continuous jet of ink is squirted through space, and using electrostatic deflector plates, the ink is selectively directed at the appropriate medium through a mesh, leading to deposition of dots to create patterns. The unused ink is directed through another channel and is recycled. This is the basis of the Continuous Ink Jetting technique and this process uses both charged and uncharged inks.

[0007] Another popular PC based printing method is "Laser Jet" or "Laser Writing" which is based on electrophotography. This method originated from Xerographic techniques for replication of images. In the original xerographic technique, a charged drum (photoconductive drum) is optically exposed to the image to be duplicated. Based on the image, charges are removed on the photoconductive drum using either a laser beam, or any other light source of appropriate spectral content and energy such as light emitting diodes (LED's). Specially charged ink, called toners, which could be either a fine powder or a liquid, are attracted to the locations on the photoconductive drum, which have the opposite electrical polarity. From the photoconductive drum, these charged particles are then transferred to the printing medium. In this method of printing, the contents of the entire image can be transferred to a photoconductive drum, and then the transfer effected to the printing media in a single step. This method of image transfer is therefore faster than the "Drop on Demand" technique previously described.

[0008] Another printing technology used in the commercial printing world, called magnetography, is similar to electrophotography, but uses magnetic fields instead of electrostatic fields to propel charges.

[0009] Perhaps the most dominant technology in the commercial printing world is based on lithography. Lithography involves a plate or an intermediate medium, on which the image to be printed is either exposed or engraved using a variety of techniques such as photography, laser ablation, thermal ablation and more recently ink jet based techniques. The areas of the printing plate have areas which accept ink

(olephilic – oil loving) and areas, which accept water (hydrophilic). In general, the oil loving areas of the image do not accept water and the water loving areas do not accept ink. As the lithographic printing ink is an emulsion of pigments and water, the ink and water selectively migrate to their respective locations on the printing plates. Once the ink and water have migrated to their respective locations, it is then transferred to the medium being printed or to an intermediate cylinder called an offset cylinder and from the offset cylinder the image is deposited on the final medium.

[0010] There are four other processes, namely flexography, gravure, letterpress and screen printing.

[0011] The above-mentioned technologies are fairly well established. They have great advantages in their respective niches. However, there are significant disadvantages with each of the methods.

[0012] For example, as previously mentioned, ink jet based printers are quite slow. There are high costs associated with electrostatic printing processes for commercial printing, due to low throughput and inability to provide more than a certain number of copies (40,000 copies with current technology) on an electro-photography based machine, before the photoconductor drum is rendered useless for any other more reproduction. In lithographic printing, primary costs include use of expensive printing plates or spools, and high costs for recycling and disposal of environmentally unfriendly chemicals. Furthermore, the imaging or pre-imaging equipment used in the commercial printing world can be quite large and bulky.

[0013] Most commercial printing technology also involves disposable pieces. For example, lithographic printing involves using a new printing plate for every image printed. There are also inks that need to be poured and replenished, if one wants to make a large number (many thousands) of copies. With xerography, a new printing plate is not used each time. However, the same large number of copies cannot be made because the charges wear off and need to be replenished. In addition, the photoconductive drums lose sensitivity to spectral content after multiple usage.

[0014] Finally, personal printers such as inkjet and laser printers utilize ink cartridges, which need to be replaced on a regular basis. Much of the money made in the personal printing market is by consumables such as ink cartridges, toner, drums, and printing plates.

[0015] Summary

[0016] A digital printing system uses individual memory cells within memory dies mounted on a substrate to attract or repel ink in order to produce an image. There is a dead space between adjacent individual memory cells and also between adjacent memory dies. By staggering the location of the memory dies on two or more substrates the dead spaces may be eliminated or minimized. In addition, staggering the location of the memory dies on the substrates allows for backup operations in the event that a primary memory cell fails and for resolution stepping of the printed image. The staggering of the location of the memory dies may be accomplished by an offset mapping of the locations of the memory dies between the two or more substrates. The offset mapping may be a translational mapping, a rotational mapping, or a combination of translation and rotational mappings.

[0017] Additional features and advantages will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the disclosed printing system. The objectives and other advantages of the printing system will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The accompanying drawings, which are included to provide a further understanding of the printing system and are incorporated in and constitute a part of this specification, illustrate embodiments of the system and together with the description serve to explain the principles of at least one embodiment of the invention.

[0019] FIGS. 1a-1b show an insulated conductive layer or medium in a flat configuration. FIGS. 1c-1d show an insulated conductive layer or medium in a cylindrical configuration.

[0020] FIGS. 2a-2b show how the memory layer is superimposed on the insulated conductive layer.

[0021] FIG. 3 shows an enlarged view of a memory cell.

[0022] FIGS. 4a-4b show memory cells overlaid on the insulated conductive layer for a cylindrical configuration of the print engine.

[0023] FIG. 5 shows an exploded view of how the different layers of the Print Engine are assembled.

[0024] FIG. 6 shows the cross sectional view of a single memory cell coupled to a single conductive pad.

[0025] FIGS. 7a-7b show a cutaway and top views of an insulated conductive layer (and memory layer)/ the print engine.

[0026] FIGS. 8a-8b show an insulated conductive layer in a flat geometric configuration.

[0027] FIGS. 9a-9b show an alternative embodiment of the present invention utilizing organic polymers to form memory.

[0028] FIG. 10 shows how an image can be mapped onto memory locations.

[0029] FIG. 11a is a block diagram of an exemplary semiconductor memory. FIGS. 11b-11c show one storage location of the memory.

[0030] FIGS. 12a-12b illustrate various embodiments of how individual memory cells may be laid out.

[0031] FIG. 13 shows an exemplary single ended storage cell.

[0032] FIG. 14 is a cross sectional view of a semiconductor layout showing how a micro-via may be used to connect the transistors of a memory element to the surface of the chip.

[0033] FIG. 15 shows how an array of chips can be connected to create a large array.

[0034] FIG. 16 is a block diagram of how each chip can be designed to have an interface element.

[0035] FIG. 17 illustrates an embodiment wherein each chip has a wireless link.

- [0036] FIGS. 18a-18b illustrate an exemplary embodiment of a printing system.
- [0037] FIGS. 19a-19b illustrate methods of adapting a traditionally flat chip onto a curved printing surface.
- [0038] FIG. 20 shows how a single-ended, thin film print element can be used.
- [0039] FIG. 21 shows the connection of a storage array to a thin film substrate.
- [0040] Figs. 22a and 22b depict the top and bottom, respectively, of a plurality of memory chips disposed on a substrate.
- [0041] Figs. 23a and 23b depict the distribution of memory chips on a substrate formed into a cylindrical print drum.
- [0042] Fig. 24 depicts a flat substrate that includes an array of memory dies that are positioned in a staggered configuration.
- [0043] Figs. 25a and 25b depict a translational mapping in the printel space among a plurality of substrates and the composite printel space, respectively.
- [0044] Figs. 26a and 26b depict a rotational mapping in the printel space among a plurality of substrates and the composite printel space, respectively.
- [0045] Fig. 27 depicts an image that is de-composed and spatially mapped into printel space and re-composed in the media space.

DETAILED DESCRIPTION

- [0046] Reference will now be made in detail to the preferred embodiments of the printing system, examples of which are illustrated in the accompanying drawings.
- [0047] An electronic stored image based scheme is proposed which permits the digital printing elements to print a digitally stored image onto any medium. This is accomplished by using a semiconductor memory-based scheme in which an image is stored in an electronic memory with each digital printing element occupying one memory location. Since information is stored in memory as a voltage, by directly coupling the memory location to a conductive element, the stored voltage can be used to directly control whether or not conductive toner based inks are attracted to that conductive element.

[0048] The system provides for a printing drum comprising a semiconductor memory. The semiconductor memory uses decoding elements to allow access to each of many storage locations without requiring an individual connection to each location. The system therefore utilizes the semiconductor memory structure to spatially map a digitally stored bit of data (e.g., 0 or 1) to a physical location.

[0049] In another embodiment, the semiconductor printing system can also be composed of a flat semiconductor memory panel, over which a system of charged and uncharged rollers can translate successively, and selectively transfer charged ink (toner) to and from the semiconductor memory panel to a printing medium.

[0050] As all printed images are generally composed of dots of ink at a specific location on a medium, it is possible to translate the specific location to where the ink can be transferred to a memory cell in a chip, and from the memory cell to the final printing medium. It is therefore possible to "load" an image efficiently over a bus or communication channel. Once the image is loaded into the memory, the conductive locations associated with each printing element receive the appropriate voltage and the image can be formed on any printing media. After a desired number of images have been printed, a new image can be downloaded and a new image can be printed. This is the basic principle of the print engine in accordance with the present invention.

[0051] The digital printing engine uses low voltage electrostatics to direct toners or other conductive printing inks to its surface. This print engine does not have any intervening consumable media such as a printing plate.

[0052] Print Engine Construction

[0053] The print engine of the disclosed embodiment comprises an insulated conductive layer and a semiconductor memory layer.

[0054] FIG. 1a shows an insulated conductive layer in a flat configuration. FIG. 1b is an enlarged view of the insulated conductive layer of FIG. 1a.

[0055] The insulated conductive layer comprises an insulating medium 11 having a top surface 10 and a bottom surface 12, a plurality of micro-vias 14 that connect the top

and bottom surfaces of the insulator, conductive pads 16 on the top, and conductive pads 18 on the bottom surfaces of the insulator.

[0056] The insulating medium can be either flexible or rigid. Typical choices for the insulating medium include, but are not limited to: plastics such as nylon, delrin, ABS, ceramics or even metals such as aluminum or steel that can be clad by a polymeric or ceramic insulating layer. The choice of the insulator depends on the application. The insulating medium has very small holes (approximately 20 microns in diameter) drilled through its thickness. The number of micro holes are determined by the dots per inch of printing that is required from the specific printing application.

[0057] The micro-vias 14 are through holes filled with a conductor. These holes can be drilled using excimer lasers or by chemical means. As future technologies become available, other machining methods can be used to drill these through holes, or micro vias 14. The micro-vias 14 are filled with an appropriate conductor such as copper or silver or gold, or any appropriately solidifying conductive paste, and they terminate at both the top 10 and bottom 12 surfaces with contact pads 16 and 18.

[0058] The contact pads 16 and 18 can be circular or rectangular in shape. Thus the contact pads 16 and 18 help electrically connect the top and the bottom surface of the insulated conductor. The thickness of the insulating medium is determined by whether the insulator is used as a rigid medium or as a flexible medium. In some cases, the insulating conducting pad can be made flexible and can be superimposed on a rigid flat plate and thus have a higher flexural rigidity. Typical thickness of the insulated medium can range from a few thousand micro inches to a few inches. The insulated medium can be either flexible or rigid. Both flat and cylindrical geometries are possible in the flexible or rigid configuration. The type of application, namely flexible or rigid configuration, determines the thickness of the insulated conductive layer.

[0059] FIGS. 1c-1d illustrate an insulated conductive layer in a cylindrical configuration. The cylindrical configuration has an inner surface 13 and an outer surface 15, with micro-vias 14 and contact pads 16 and 18 at the end of each micro-via, at the inner 13 and outer 15 surface.

[0060] Semiconductor Memory Structure

[0061] The semiconductor memory layer contains the “brains” of the printing engine. Memory can be manufactured using several different technologies, such as conventional silicon based semiconductors, organic semiconductors that use organic materials for semi-conducting purposes, or magneto-electronic materials that can be fashioned into memory cells. The print engine construction based on conventional silicon based semiconductors and organic semiconductors are now described.

[0062] FIGS. 2a-2b illustrate a typical memory layer 20 as it is superimposed on the insulated conductive layer 22. The memory layer 20 is generally made up of an array of individual memory cells 24. Memory is made of transistors and can be directly patterned over the insulated conducting layer as shown in FIGS. 1a and 1c, using different techniques. Memory can be made using traditional silicon wafer based semiconductors or organic semiconductors which have recently been developed.

[0063] FIG. 3 shows an enlarged view of a memory cell. In FIG. 3, an asymmetrically conductive adhesive (also known as anisotropic conductive adhesive) is used to couple the memory cell layer to the conductive pads on the insulated conductive layer.

[0064] FIGS. 4a-4b show memory cells overlaid on the insulated conductive layer for a cylindrical configuration of the print engine. The inner contact pads are in conformal contact with the asymmetrically conductive adhesive and are not visible in this picture. FIG. 4b is an enlarged view of the cylindrical configuration of the print engine.

[0065] FIG. 5 shows an exploded view of how the different layers of the Print Engine are assembled. The anisotropic conductive adhesive (ACA) binds the based memory layer to the insulated conductive layer, and using alignment marks during the assembly process, the individual memory cells are coupled to the contact pads on the insulated conductive layer, thus forming a single monolithic semiconductor based structure that can receive and store printing information.

[0066] FIG. 6 shows the cross sectional view of a single memory cell coupled to a single conductive pad. The insulated conductive layer 61 is shown with micro-via 14 and top and bottom conductive pads 16 and 18. The insulated conductive layer is

coupled to memory layer 20 using an asymmetrically conductive adhesive 52. FIGS. 2a through 6 show a flexible memory structure coupled to an insulated conductive layer with conductive pads.

[0067] FIG. 7a shows a cutaway view of an insulated conductive layer containing micro-vias in a cylindrical configuration, coupled to packaged integrated memory chips. Part of the insulated conductive layer has been removed to show the asymmetrically conductive adhesive layer, and the location of the integrated memory chips. In this embodiment, the memory locations in the packaged integrated memory chips are directly coupled to the conductive pads on the cylinder using asymmetrically conductive adhesives.

[0068] FIG. 7b illustrates the top view of an insulated conductive layer coupled to a packaged integrated memory chip. The dead space that exists between individual memory chips is also visible. These "dead spaces", do not contain any printing elements. By staggering the chip locations between two or more cylinders, it is possible to eliminate all dead space and evenly provide memory locations to print continuously in a linear fashion.

[0069] FIGS. 8a-8b show an insulated conductive layer in a flat geometric configuration. In FIG. 8a, the top surface is shown, and in figure 8a the bottom surface is shown. The integrated memory chip is attached to the bottom surface using different methods. One method is to use an asymmetrically conductive adhesive to bond the chip to the conductive micro-vias.

[0070] In FIGS. 1a through 6, the top surface generally represents the surface that will attract the ink. The bottom surface is generally where the memory chips or memory circuits are attached. The insulating layer isolates and provides mechanical isolation and electrical isolation between the chips and the ink receiving layers.

[0071] In both the packaged integrated memory chip and the flexible memory chip, the functionality of the memory elements is the same. The individual memory cells carry a voltage, and the voltage, when coupled to the conductive pads, is capable of attracting

charged toner. What the memory circuits help avoid is the need to wire each conductive pad individually by an independent wire, which carries a voltage through it.

[0072] Using an asymmetrically conductive adhesive layer (ACA) is just one way to couple the insulated conductive layer to the memory cells. Other means can be used to couple the insulated conductive layer to the memory cells.

[0073] The memory structures identified in the preceding paragraphs, i.e. flexible and non-flexible, are some of the many possible configurations which spatially map an image stored in computer memory to a physical printing conductive point.

[0074] Is it also contemplated that digital printing elements using non-silicon based memory may be used. For example, in another embodiment of the present invention, a new method using organic semiconductor polymers to form memory is composed of a grid of intersecting electrodes which sandwich a polymeric layer can be used in the digital printing element construction. The intersection between the word (horizontal electrodes) and the bit lines (vertical electrodes) in these cases forms the point that connects to the physical printing conductive point. FIG. 9a shows one such potential structure, in a flat format. This is based on memory developed by Thinfilms, Inc. of Sweden. FIG. 9b shows an enlarged view of the structure described in FIG. 9a. This memory structure overlaid on the insulated conductive layer is also possible in a cylindrical configuration.

[0075] Details of Individual Memory Elements

[0076] FIG. 11a is a block diagram of an exemplary semiconductor memory, which can be on a single integrated chip (IC). The address bus is used to access each memory location. Since the address is specified using a binary code, the number of connections to the chip needed to access many locations is $\log_2(n)$ where n is the number of memory locations. For example, for a standard 8'5" by 11" page at 300 dpi, which has 8,415,000 print locations, only 24 address bits are required to access all locations.

[0077] The integrated chip has row (105) and column (110) decoding circuits, along with global decoding and timing circuits (120). The storage locations are grouped in

arrays (100), with channels (125) in between the arrays. The channels carry power, ground, and un-decoded or partially decoded address lines and other signals.

[0078] In a typical semiconductor memory, there is an array of storage elements 100 surrounded by peripheral circuitry. The array of storage elements, typically in the middle, is made up of areas of storage elements with areas in between which contain channels for power, ground and other signals. FIGS. 12a and 12b illustrate an exemplary single storage location in the memory.

[0079] Unlike a typical semiconductor memory, in which each element is designed to be as small as possible in order to increase density, these elements can be larger. This is because the pitch required for printing is much larger than the pitch achievable by semiconductor memories. A 300 dpi (dots per inch) image requires a dot pitch of approximately 85 micrometers (μm), which is much larger than the pitch of storage elements or memory cells in a memory made in a modern semiconductor process. As a result, the pitch of the conductive elements at the surface is coarse, while the pitch at which the transistor elements, which form the memory in the semiconductor substrate, is fine. The transistor elements can therefore be larger, which makes them more robust and increases reliability and manufacturing yield. Furthermore the unused spacing can be used to perform local decoding which increases the uniformity of the memory array by moving some of the peripheral circuitry within the array itself, and also by making room for power, ground, and signal channels in between the elements.

[0080] FIG. 11b is a storage element used in a semiconductor memory. This element is generally optimized to be as small as possible in order to maximize the storage density. FIG. 11b shows a diagram of a typical 6-transistor static memory (SRAM) cell. Inverters 200 and 201 are cross-coupled and connected to bit lines 241 and 241 via access gates 210 and 211. The nodes 221 and 222 at the outputs of the inverters are the charge storage nodes. The access gates are driven by the word line 230. In a typical semiconductor memory used for mass storage, the access gates 210 and 211 are usually single NMOS transistors.

[0081] In the digital printing element application, since area density is allowed to be less, the access gates 210 and 211 may be transmission gates rather than single NMOS transistors, which can improve noise immunity and cell robustness.

[0082] In FIG. 11c, the charge stored on a typical SRAM storage node (221 and 222) is small and so the node cannot be connected directly to the printing surface. In order to decouple the storage node from the printing surface, an additional inverter 250 is used to isolate the storage node 222 from the printing surface. The output 251 of the inverter 250 is coupled using the metal via to the printing surface.

[0083] FIGS. 12a-12b shows how the relaxed pitch can be used to make the array more uniform; FIG. 12a shows the layout of a conventional semiconductor memory. The array consists of a grid of word lines (305 and 310) and bit line pairs (315, 320). Memory cells 325 are placed at the intersections of the word lines and bit line pairs. Since the aim is to maximize storage by optimizing density, the cells are made as small as possible and packed as close to each other as possible. Therefore, the spacing between word lines 305 & 310 is minimized, as is the spacing between the bit line pairs 315 & 320, and these are generally just as much as is needed to fit the storage cell at the intersection. So, all decoding circuits which decode the incoming address to provide signals for the word and bit lines are placed at the periphery of the array, as shown in FIG. 11a.

[0084] FIG. 12b illustrates an embodiment whereby the decoding circuits are located with each memory cell, as opposed to outside of the array of memory cells. FIG. 12b shows how wires and decoding circuits can be interspersed with the storage elements of the array when the pitch is relaxed. Since the digital printing element does not have to be as densely packed as a semiconductor memory and does not have to operate as fast as a conventional memory, two modifications can be made. One, the cell (375) can be made single ended (i.e. it can use only one bit line (365, 370) instead of a pair of complementary bit lines), and two, the spacing between word lines (355, 360) and bit lines (365, 370) can be larger than in a conventional memory. Therefore additional decoding and buffering circuits 380 can be placed in the area available at the word and

bit line intersections, in order to reduce the non-uniformity caused by having to place all the decoding circuits at the edges of the array.

[0085] One example of a single ended storage cell is shown in the circuit of a conventional master slave latch shown in FIG. 13. Many such circuits are known to those well versed in the art and can be used for this purpose.

[0086] FIG. 14 is a cross sectional view of a semiconductor layout and shows how a micro-via may be used to connect the transistors of a memory element to the surface of the chip to drive a print element. FIG. 14 shows the typical via structure used to connect the transistors to the printing surface. Transistors 410 and 420 are shown in a silicon wafer 415. The p-type transistor 420 is shown in an n-well 425, as is typical in CMOS technology. The transistor 420 has a source 431 and a drain 432 and a gate 433. The source 431 is connected via the metal contact and metal layer 441 as appropriate for the circuit (details not shown here).

[0087] The n-type transistor is constructed directly in the substrate 415 and has a source 411 and a drain 412 and a gate 413. The source 411 is connected as appropriate using a contact and metal layer 442. The two transistors are connected using contacts and metal layer 443. A dielectric layer 450 insulates metal layer 1 (441 and 442) from higher metal layers. A via and metal 2 layer 460 are used to connect down to metal layer 1 and the connection between transistors 410 and 420. Other connections (not shown) may also exist on this metal layer. There may be more metal layers (layer 3, layer 4) etc as required by the technology used to fabricate the circuit. Finally, a via 475 is used to connect the highest layer to the surface 480 of the chip. Dielectric layers 470, 465, etc are used to insulate the circuit at the lower levels from the surface. The topmost via 475 is finally connected to the printing surface using various means as discussed elsewhere in the document.

[0088] As is well known to those well versed in the art, this is a very typical configuration of transistors used to construct circuits in silicon. With reference to FIG. 11c, the transistors 410 and 420 together constitute the inverter 250, and the output 251 of the inverter is formed by the contact and metal layer 443 in FIG. 14. The

other transistors used to form the memory cell are not shown, but their formation and connection is similar and can be understood by a person well versed in the art.

[0089] The yield of semiconductor chips reduces as their area increases. Therefore, it is not practical to make a single memory chip that covers the area of an entire page, but it is necessary to use many chips to cover an entire page or image area. FIG. 15 shows how an array of chips 500 can be connected to create a large array. In order to maintain a simple and efficient communication channel to the entire array, a communication bus scheme is proposed in which a bus 500/505 is used to connect all the chips 500. An arbitration and communication protocol will be used to allow each chip to be loaded with its portion of the image. Since image loading time is not a constraint in this application, it is possible to optimize the protocol for ease of communication and low wire-count by using a low bandwidth protocol.

[0090] Busses 500 and 505 are used to connect the cells. These busses carry address, data, power, ground, and other signals, and are designed to reduce the wiring needed between the chips.

[0091] FIG. 16 is a block diagram of how each chip can be designed to have an interface element that handles the protocol, coupled with the image storage function described earlier.

[0092] The digital printing element array 600 is connected to conventional decoding circuits 610 that may be used in one chip. A communications controller 605 listens to the narrow bus 620 that connects the chips in an array. Communications controller 605 listens to the protocol on the bus 620 and recreates address and data information for the chip, which it passes to the decoding circuit 610 along a bus which is wider than 620. In turn, the decoding circuit 610 finishes the decoding and drives the array 600 along a bus of appropriate (as much as needed) width, as shown in the diagram.

[0093] In order to reduce the number of wires and therefore increase ease and reliability, a low-bandwidth wireless link can be built into each array as shown in FIG. 17. Thus each array can be made into a sealed module with a unique address and only power and ground connections made externally. This can be used to control

access to each module, and provide tracking and access control by including encryption and authentication in the communication protocol. In place of a wireless link, it is also possible to use some other physical connection that is made temporarily to download the image into the module, after which the connection is broken.

[0094] In addition to being a protocol engine as shown in FIG. 16, the block 705 can be a wireless communications processor, which uses an antenna 720 as its input bus for data, address, and other information. The antenna 720 can be built on to the chip 715, or can be an external metal trace that is connected to the chip. In this case, the bus 725 would only carry power and ground to the chips 715 in an array.

[0095] Working of the Print Engine

[0100] The print engine is composed of the semiconductor memory layer overlaid on the insulated conductive layer with a one to one correspondence of each memory cell with the conductive pad on the insulated layer. This combination of the memory cell with a conductive location is called a digital printing element. Once the overlaying of the memory cell with the conductive element is accomplished, then the entire structure can be fashioned into either a planar structure or a cylindrical structure with the insulated conductive pads providing protection to the sensitive semiconductor memory from impact loading that occurs during the printing process.

[0101] As pointed out earlier, the memory storage array is not contiguous even within a chip. When an array of chips is put together, there will be spaces (dead space) between the image element arrays due to the peripheral circuitry on each chip as well as the edge space required on each chip in which active circuitry cannot be placed. Therefore we propose a scheme of using two consecutive elements, in two cylinders or two plates, in which the stored memory arrays are spatially overlapped such that the print locations of one cover the areas of the other in which print locations are absent. This will give continuous coverage of the printing surface by print locations. This scheme will also provide a built-in redundancy mechanism by which failed print locations on one cylinder or surface can be compensated by a corresponding location on the other surface. This scheme can be extended to more than two surfaces in order to improve coverage and reduce the impact of failed print locations on any one surface.

[0102] The image to be printed is first stored in a computer as a binary bit pattern, physically corresponding to a 1 or a 0 depending upon the presence or absence of a dot. From the computer, the memory can be directly downloaded to the memory location on a bit by bit basis, corresponding to the pixel value of the image stored. Thus there is a spatial map of the data corresponding to the image and the physical memory cell location. See FIG. 11a for a pictorial representation of the memory map. Thus each memory cell location will contain a digitally stored "1" or a "0" depending on whether the pixel in the original image is turned on or off.

[0103] Because the print image is stored electronically and there is an electronic map of how each image digital printing element maps on to a physical location, the print image can be aligned very easily by adjusting the specific locations in which individual image bits are stored. Physical alignment of the paper to the cylinder is not needed, and alignment can be done electronically by shifting or rotating the image, as it is stored in the print array. This problem overcomes alignment and registration of images and colors that are found in traditional lithography based printing presses.

[0104] By adding a scanner to the output of the printer, it is also possible to align the print elements. An image or images with a fixed pattern can be printed and then scanned. The scanned output can be examined either manually or using computer algorithms which can detect registration errors between the multiple print cylinders, and the images stored in the cylinders can be adjusted until the final image is free from registration errors. This process can be either fully automatic, or may be used to minimize the amount of human intervention required to align the images.

[0105] FIG. 18a shows how the print engine can be configured with an offset cylinder and inking cylinders to transfer charged ink from a source to the final medium (Paper or plastic or metal) in sheet or continuous web form. For sake of clarity, the electrical connections, and mechanical support structures have been omitted. The ink is transferred from the inking cylinders via electrostatic attraction to the print engine. The ink cylinder will carry a charge that is opposite to the charge carried by the locations on the print engine, which have a digitally stored charge on them. Thus the toner ink will have the same charge as the ink cylinder. This causes the ink to travel from the surface

of the ink cylinder to the surface of the print engine, which has an opposite polarity of charge at the locations corresponding to the stored image. A multitude of print engines (3) are shown, as the image to be printed has to be spatialized without any dead space. From the print engine, the ink, which is only attracted to locations that have the pixels turned on the entire digitally stored image, is transferred to the offset cylinder. This offset image is transferred to the upper transport cylinder and from there it will be transferred finally to the printing medium. This process goes on continuously, until all the ink is depleted or the image is changed. FIG. 18a shows a perspective view from a different viewing angle with more details of the internal structure of the print engine. FIG. 18b shows another perspective viewing angle of the print engine and the associated components. In this perspective viewing angle the contact pads on the print engine are also visible.

[0106] In FIGS. 18a-18b the inking cylinders can all carry black ink, in which case the printer will be configured to print in monochrome. To print in color, four stations, each identical to the one configured in FIG. 18a can be arranged in series such that the medium such as paper or plastic or metal can successively pass through each station and acquire the component of color from each station. A subtractive color printing scheme employing cyan, magenta yellow and black colors could be used in each of the stations respectively to generate the composite color density required by the final image. A software based color separation scheme that will separate the color pixels from each image to be printed will be used to download the pixels into each of the print engines. In addition to the subtractive colors and black, additional colors can also be used for highlighting and other glossy effects. An extra print engine configuration in series with the four colors would be necessary in such a situation.

[0107] In FIG. 19a, some methods of adapting the flat integrated chip 805 to a curved printing surface 800 are shown. The chip has vias 810 that are connected to the storage elements and bring the stored voltage to the surface as discussed earlier. In FIG. 19a, a directionally conductive adhesive 815 is used to connect the vias at the chip surface to the curved printing surface. This adhesive serves as a vertical connection as well as a strain relief layer. FIG. 19b shows a grid of columns 820 which are used to

connect the chip surface to the printing layer. These columns are typically made of metal, though other materials may be used. An insulating material 825 can be used to fill in the gaps between the columns, and this material also acts as a support and strain relief layer.

[0108] FIG. 20 shows how a single-ended, larger-area thin-film print element 925 can be used. The inset shows the element 925, which takes in decoded row and column signals, a clock signal, and Vdd and ground. The arrangement of these elements into an array is also shown, and is similar to the conventional memory layout. The grid consists of coarse row and column decoding circuits 950 and 960, which decode the incoming addresses into rows (955) and columns (970). In addition, a global clock connection 975 is sent to all the storage elements 925. The storage elements 925 are placed at the intersection of the decoded row and column lines, and additional decoding circuits may also be placed there as discussed earlier. The address and data information for the chip is brought in on a bus 980.

[0109] FIG. 13 shows the circuit of a conventional latch circuit, which is traditionally used in IC design. It consists of a transmission gate 905, an inverter 910, a clocked inverter 915, and these are connected to form a storage element. Such an element may be more easily created using thin-film-transistor technology, since it is more robust because it can be made using larger transistors.

[0110] FIG. 21 shows the connection of a storage array on a thin-film substrate 1010 to a conventional silicon chip 1020 using a flexible bus 1015. The flexible thin-film substrate can be made conformal to the printing surface 1005.

[0111] Figs. 22a and 22b depict top and bottom views of a plurality of memory chips assembled on a substrate. In particular, a substrate 2202 has mounted thereon a plurality of memory dies 2204 having conductive interconnections 2206 therebetween. In the illustrative embodiment, the memory dies 2204 include a plurality of printing locations 2210 that correspond to individual memory cells within the die. As explained above, each memory cell is coupled to a first conductive pad that is electrically coupled to a second conductive pad disposed on the printing surface of the print engine. The second conductive pad takes on the charge or voltage of the first conductive pad and

attracts or repels ink depending upon the type of ink being used. In the embodiment illustrated in Figs. 22a and 22b, the memory dies 2204 are arranged in a rectilinear manner such that between each row and column of memory dies dead space 2208 exists between each adjacent memory die that, at least for the corresponding substrate is not printable. In addition, as illustrated in Fig. 22b, the memory cells on each die are also configured in a rectilinear fashion. Accordingly, there is also dead space 2212 between adjacent memory cells that, at least for the individual memory die is not printable.

[0112] Figs. 23a and 23b depict an assembly of memory dies formed on a substrate that is shaped to form a cylindrical print drum. In particular, the substrate 2302 is formed into a cylindrical print drum that includes a plurality of memory dies 2304 that are interconnected via conductive interconnects 2306. As with the flat substrate of Figs. 22a and 22b dead space 2308 between adjacent memory dies 2304 disposed on the surface of the cylindrical print drum 2302. As with the flat substrate, dead space 2312 exists between adjacent memory cells in each memory die 2304.

[0113] In one embodiment the dead space 2208 and 2308 in flat or curved substrates, respectively, is not an issue and the memory dies can be placed in the rectilinear configuration and provide adequate printing resolution. However, in other embodiments, the die layout on a substrate is not a regular rectilinear configuration and the positions of the various memory dies are varied in order to reduce the the number of dead spaces within the substrated and to reduce the size of any dead spaces that may remain. Fig. 24 depicts a flat substrate 2402 that includes an array of memory dies 2404 that are positioned in a staggered configuration such that the dead spaces 2406 are limited in size to the areas between adjacent memory dies and do not extend for the entire row and columns between adjacent memory dies as in Figs. 22a-b and 23a-b. Thus, in this configuration, the size of the dead spaces has been reduced. It should be appreciated that the flat substrate 2402 could be formed into a cylindrical print drum or other printing surface and the dead spaces 2406 would also be limited in those configurations.

[0114] It is also feasible to provide multiple substrates each of which print a portion of the image in succession. In this embodiment, the memory die pattern can be repeated on multiple substrates. Each substrate may be flat or formed into a shape such as a cylindrical print drum or other desired shape. In this embodiment, whatever the shape of the substrates, the different memory locations on the different substrates all overlap with one another.

[0115] Fig. 25a depicts an offset mapping that is a translational mapping in the printel space among a plurality of substrates 2502a, 2502b, and 2502c on which a 4x4 array of memory dies are arranged in a regular rectilinear configuration. However, the memory dies 2504b on substrate 2502b are slightly offset by Δx and Δy when compared to the position of the corresponding memory dies 2504a on substrate 2502a. Similarly, the memory dies 2504c on substrate 2502c are slightly offset by Δx and Δy when compared to the position of the corresponding memory dies 2504b on substrate 2502b. Thus, the use of translational mapping for the three combination of the three substrates forms a printel image depicted in Fig. 25b that shows the overall coverage of the composite printel image. In this way, the combination of the three substrates 25a-c work together to provide contiguous spatial coverage of the area. In addition, it is possible to provide an increase in resolution such that the printel spacing can be lower than the resolution that is ultimately required. For example, in one illustrative embodiment in which 800 dpi cells are positioned in a staggered format, it is possible to increase the resolution by a factor of 2 or more. In this embodiment, no single substrate will have to have the ultimate printel density but, rather, each can have a much lower printel density. For example, a plurality of 800 dpi substrates may be formed to provide 1600 dpi or 2400 dpi printel densities.

[0116] Fig. 26, depicts an offset mapping that is a rotational mapping of three substrates 2602a, 2602b, and 2602c. As depicted, substrate 2602b is rotated when compared to substrate 2602a, and substrate 2602c is rotated with respect to substrate 2602b. The composite printel image is depicted in Fig 26b. Thus, the combination of the three substrates 26a-c work together to provide contiguous spatial coverage of the area. As with the translation mapping described above, it is also possible to provide an increase

in resolution using rotational mapping such that the printel spacing can be lower than the resolution that is ultimately required. It should be appreciated that a combination of translation and rotational mappings may be used to achieve a desired resolution depending on the system configuration.

[0117]In addition, the use of translational mapping, rotational mapping, or a combination of both may be used to provide redundant memory cell locations that can be used to provide backup operations in the event that a primary memory cell fails.

[0118]Furthermore, the use of translational mapping, rotational mapping, or a combination of both may be used to provide resolution stepping of an image. As discussed above, an image is composed of individual dots and with the use of resolution stepping, the image may be printed at various levels of resolution. For example, depending on the configurations of each printing substrate and the number of substrates, an image that was originally 1000 dpi may be able to be printed from 100 dpi to over 2000 dpi in varying steps of resolution. Thus, depending on the system requirements, the printing time and cost required for an image to be printed may be reduced via the resolution stepping.

[0119]Fig. 27 depicts an original image that is de-composed and spatially mapped into printel space and re-composed in the media space. In this embodiment, the printel space refers to the plurality of substrates and memory dies and cell locations on each substrate. The media space is the actual printed image. This de-composition of the image into the printel space allows the number of cells used to print the image to be determined based on the areal density of the image in terms of the number of dots per inch and the die size. When using the resolution stepping described above, a minimum resolution value of one-half the final resolution on each printel bank or substrate allows for the doubling of the resolution when a plurality of such printel banks are used to form the printel space.

[0120]While the printing system has been described in detail and with reference to specific embodiments thereof, it will be apparent to those skilled in the art that various changes and modifications can be made therein without departing from the spirit and

scope thereof. Thus, it is intended that the appended claims, and their equivalents, define the invention.

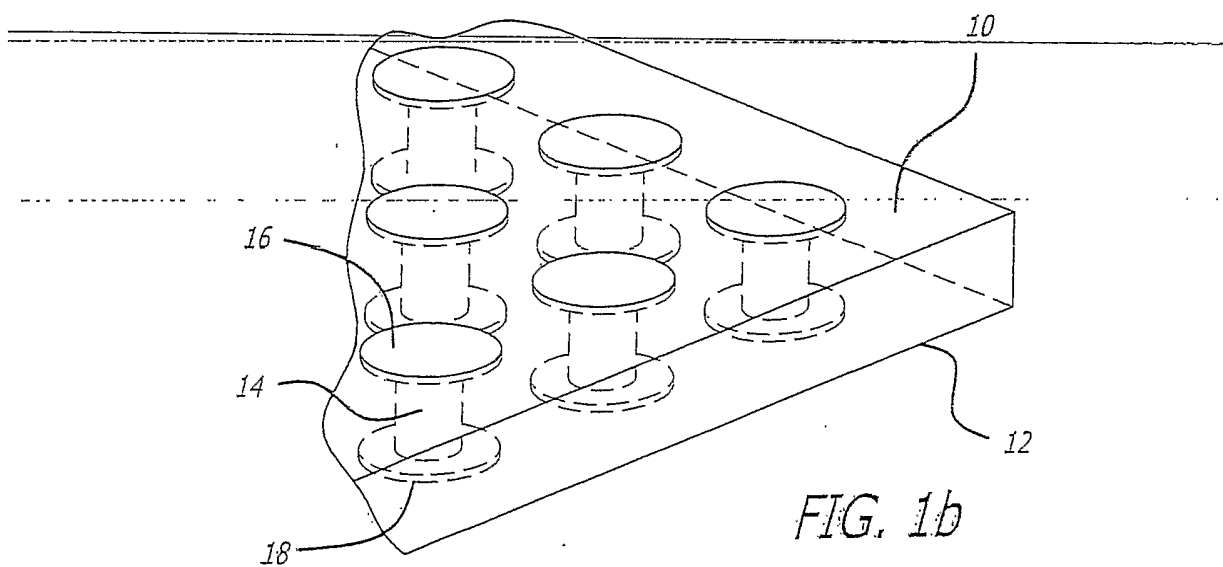
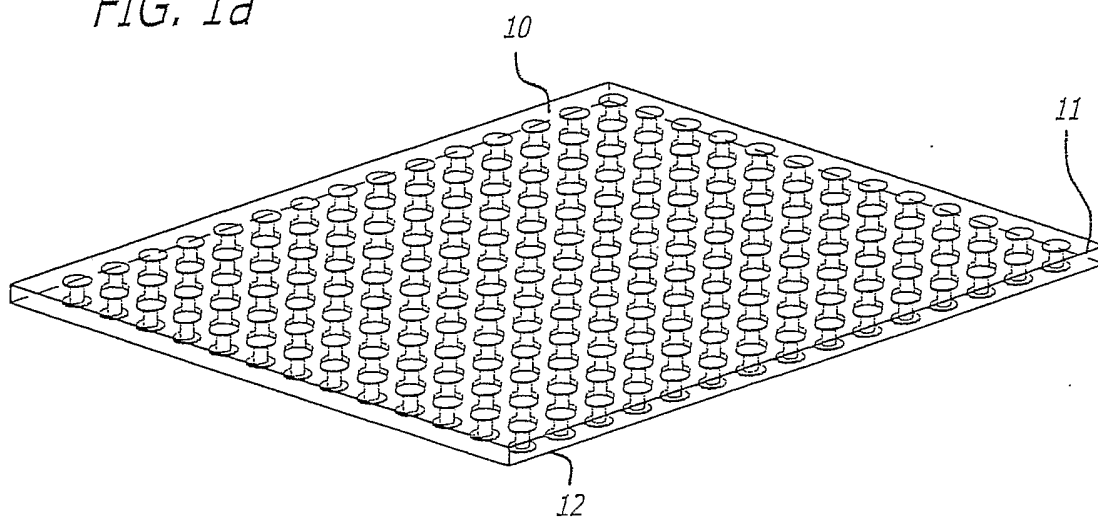
WE CLAIM:

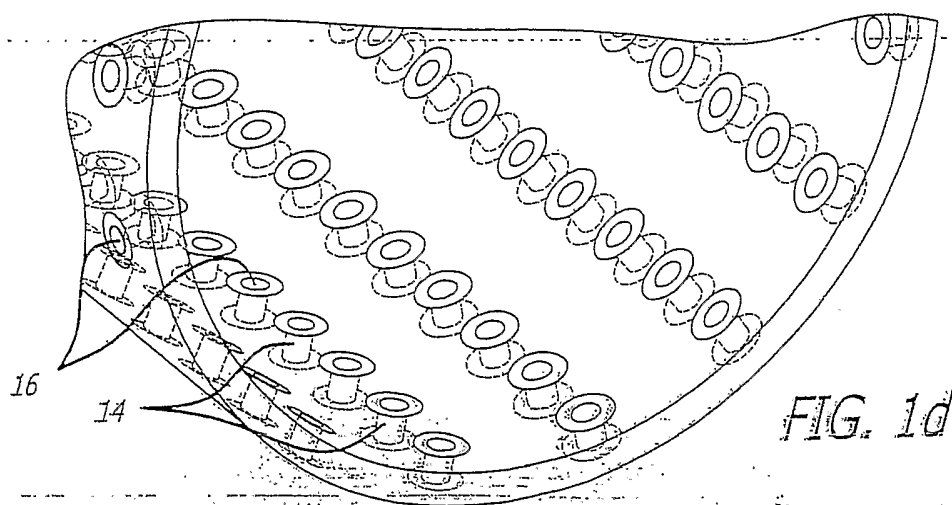
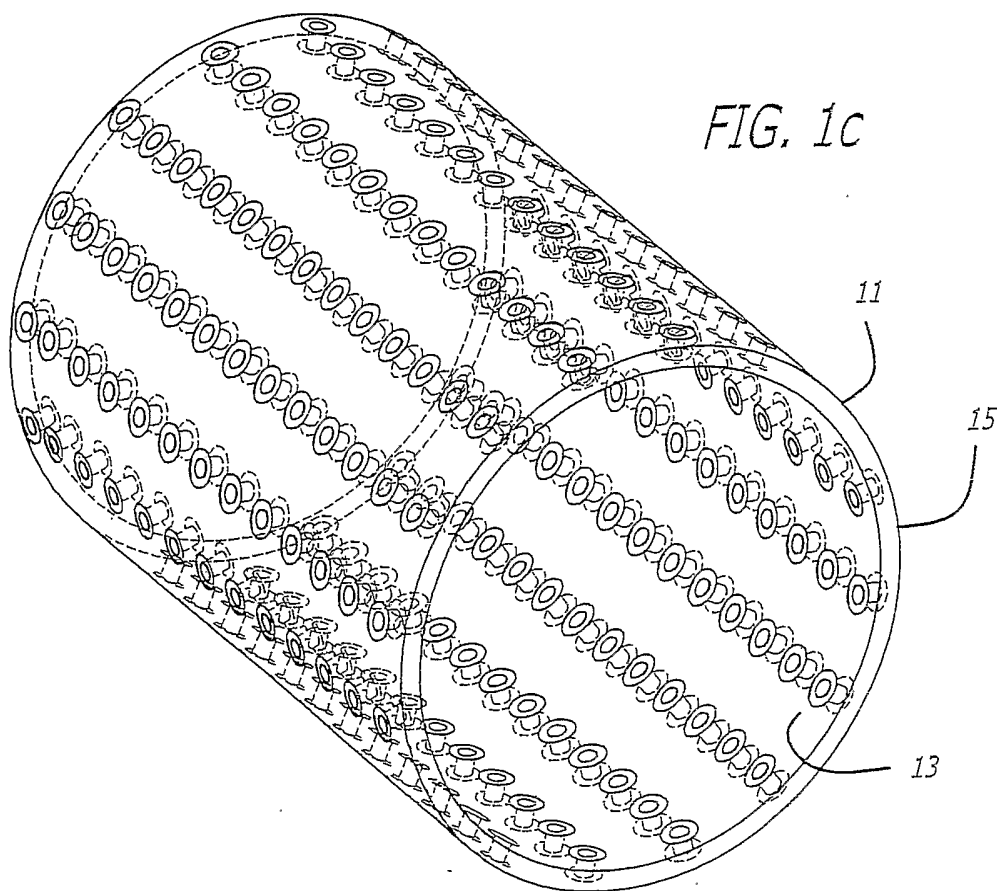
1. A digital printing system comprising:
 - a first substrate;
 - a first plurality of print elements disposed on said first substrate, each print element including at least one conductive element which is electrically coupled to a memory circuit that can switch between at least a first state and a second state, wherein the conductive element has a state that corresponds to the associated memory circuit, and wherein when in the first state the conductive element attracts the charged ink and when in the second state the conductive element does not attract the charged ink;
 - a second substrate
 - a second plurality of print elements disposed on said second substrate, each print element including at least one conductive element which is electrically coupled to a memory circuit that can switch between at least a first state and a second state, wherein the conductive element has a state that corresponds to the associated memory circuit, and wherein when in the first state the conductive element attracts the charged ink and when in the second state the conductive element does not attract the charged ink;
 - said first plurality of print elements disposed on said first substrate in a first pattern;
 - said second plurality of print elements disposed on said second substrate in a second pattern that is an offset mapping of the first pattern.
2. The digital print system of claim 1 wherein the offset mapping is a translational mapping.
3. The digital print system of claim 1 wherein the offset mapping is a rotational mapping.
4. The digital system of claim 1 wherein the offset mapping is both a translational and a rotational mapping.

5. The digital print system of claim 1 wherein the first and second substrates are flat.

6. The digital print system of claim 1 wherein the first and second substrates are formed into a cylindrical print drum.

FIG. 1a





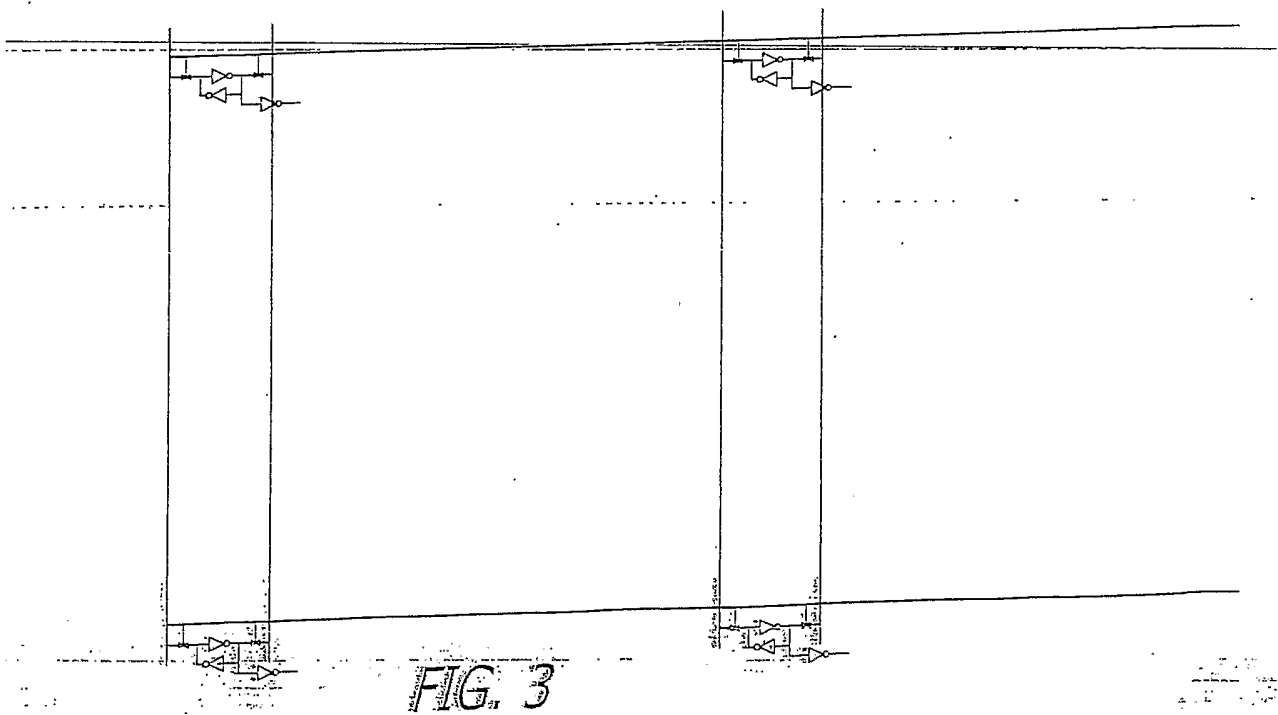
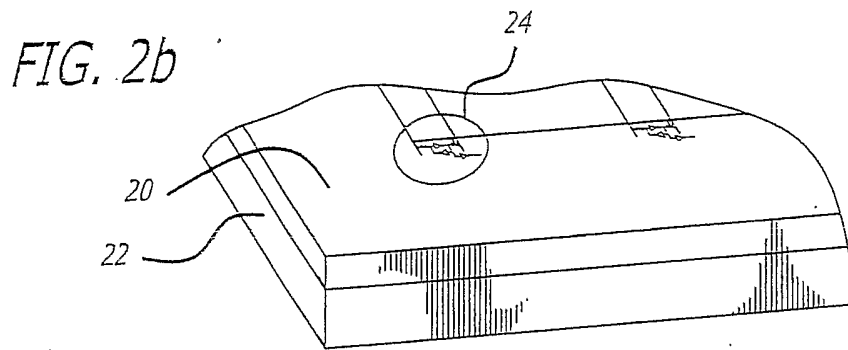
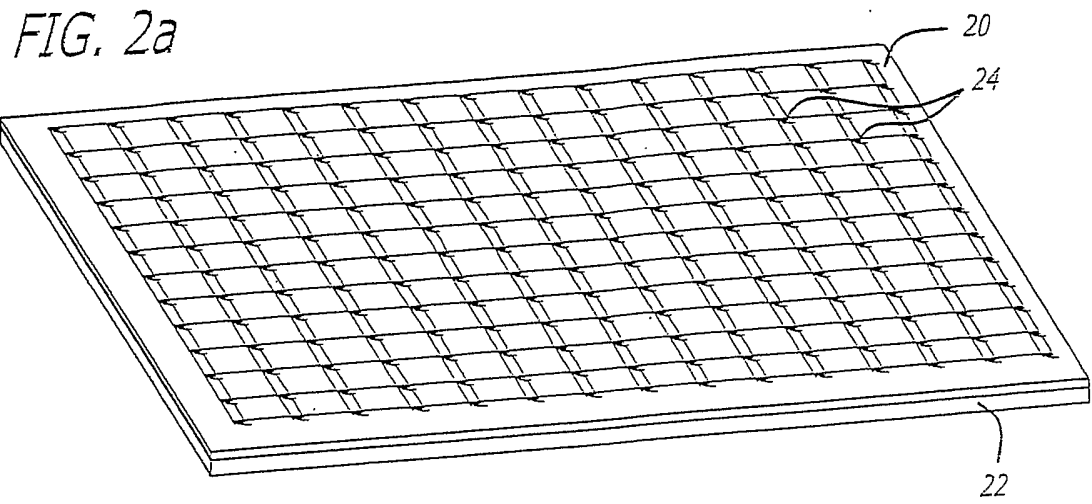


FIG. 4a

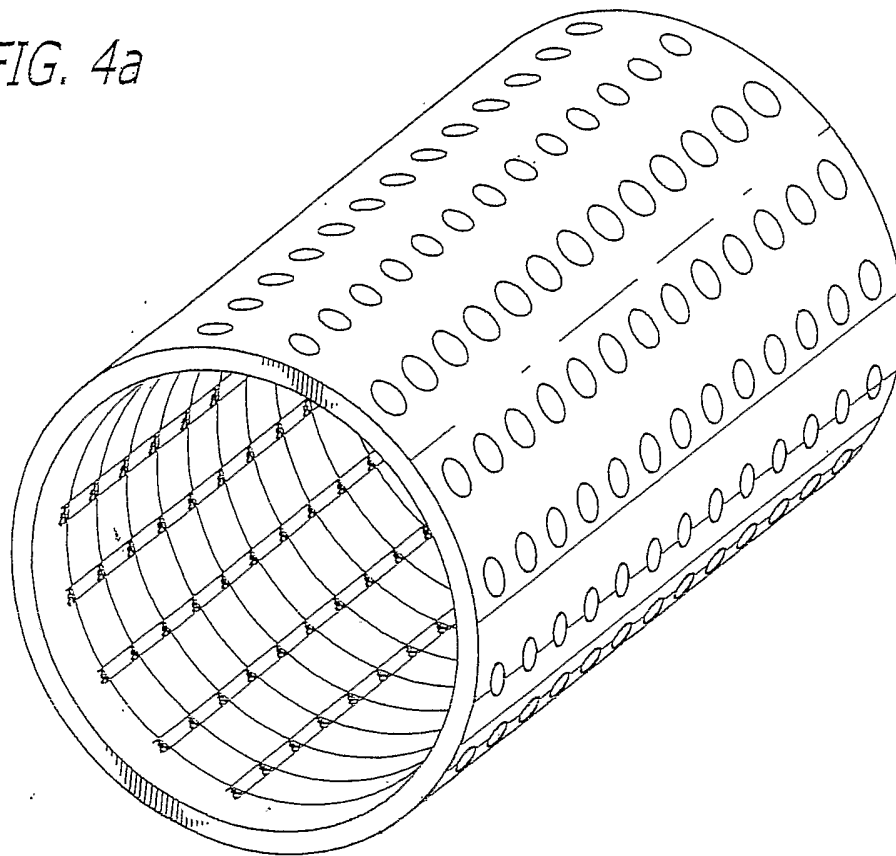
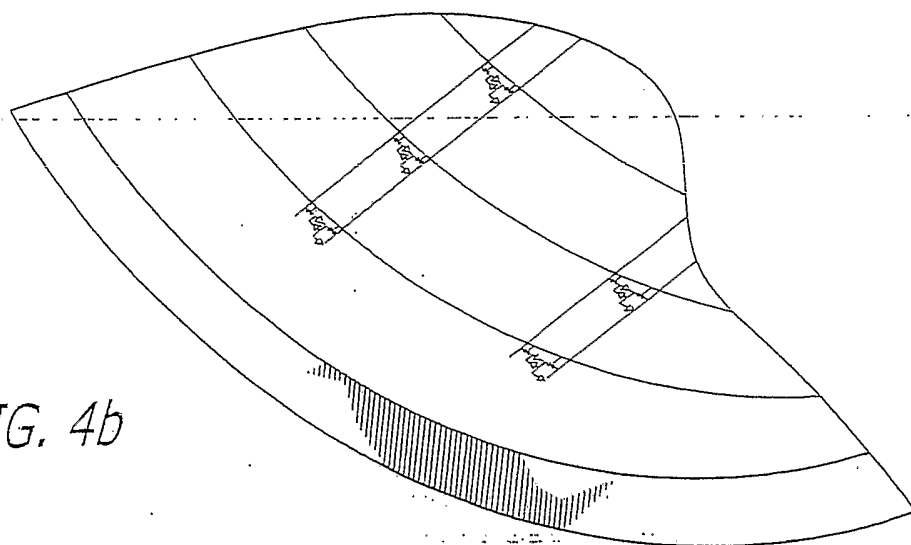


FIG. 4b



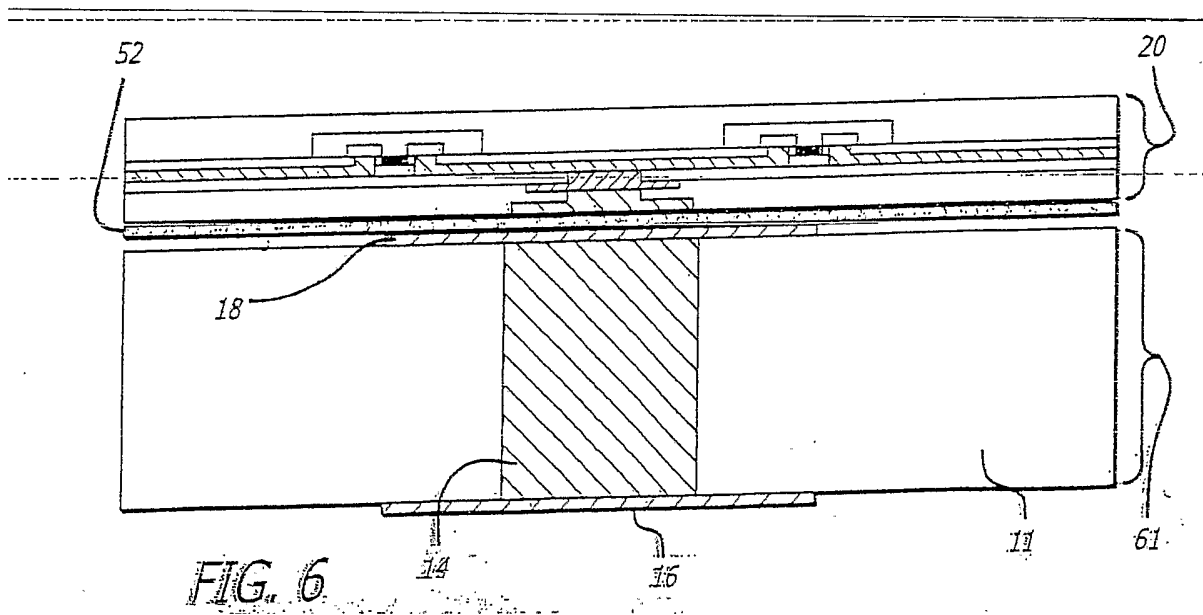
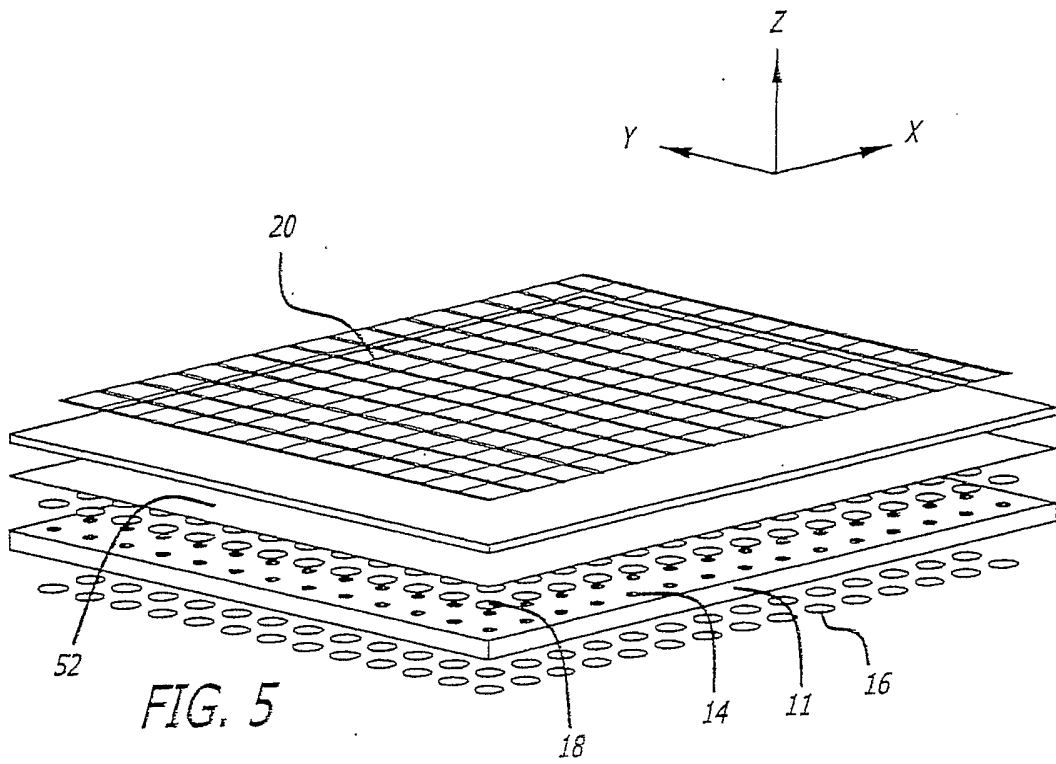


FIG. 7a

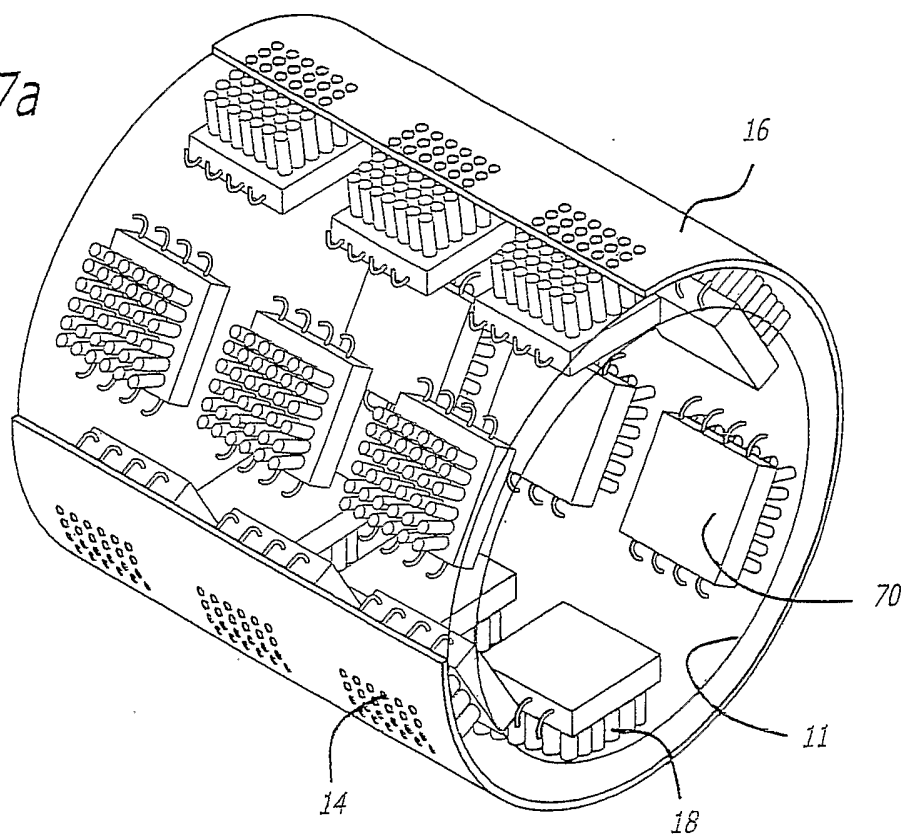


FIG. 7b

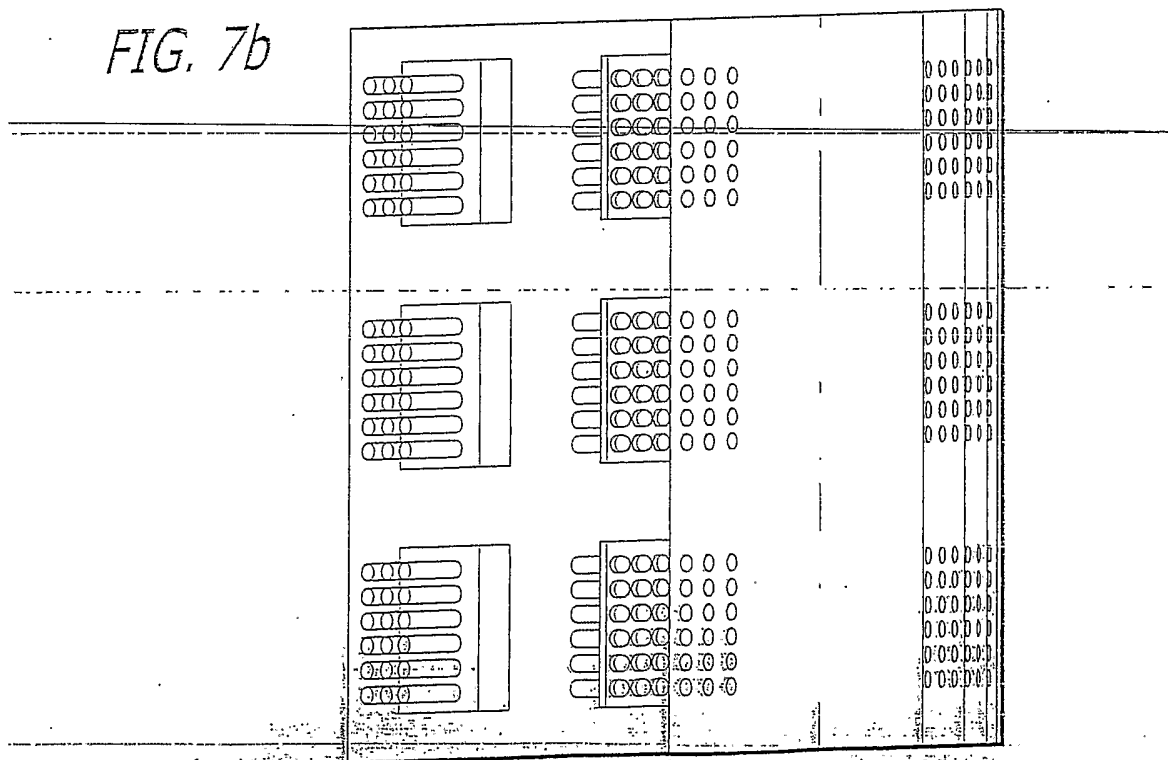


FIG. 8a

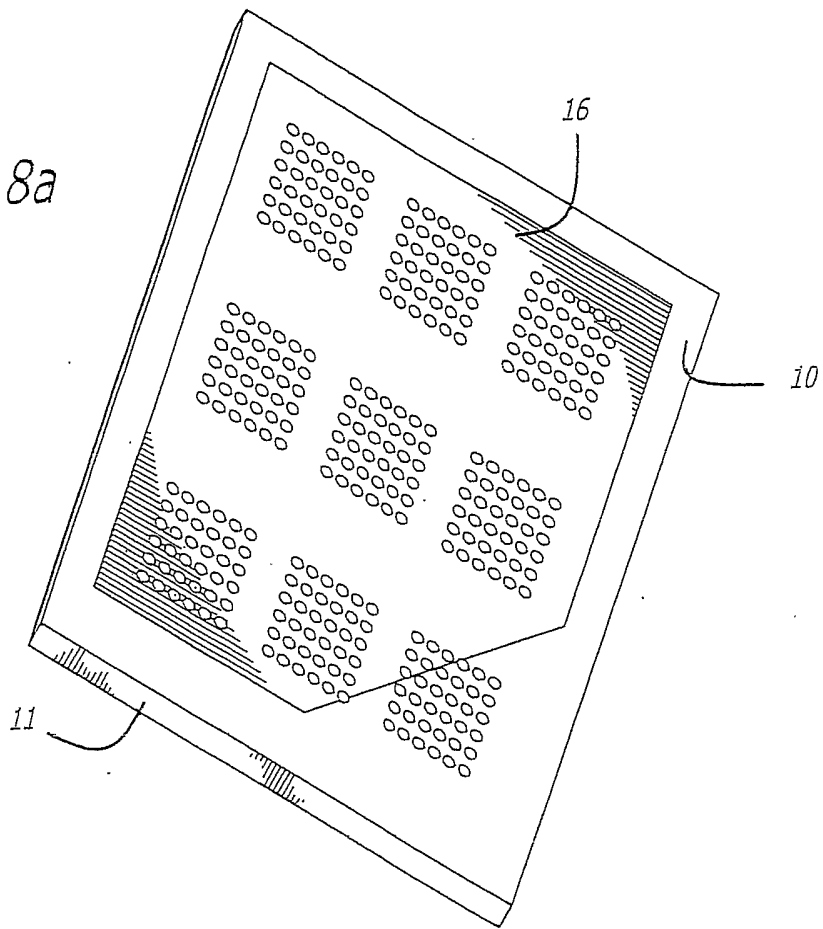


FIG. 8b

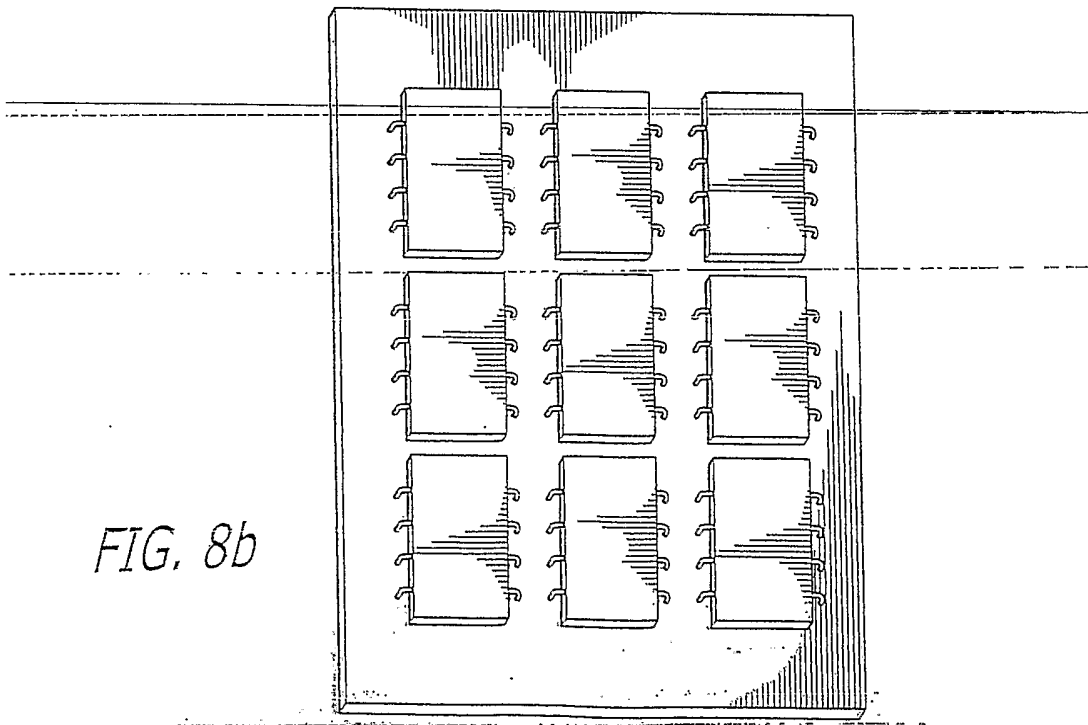


FIG. 9a

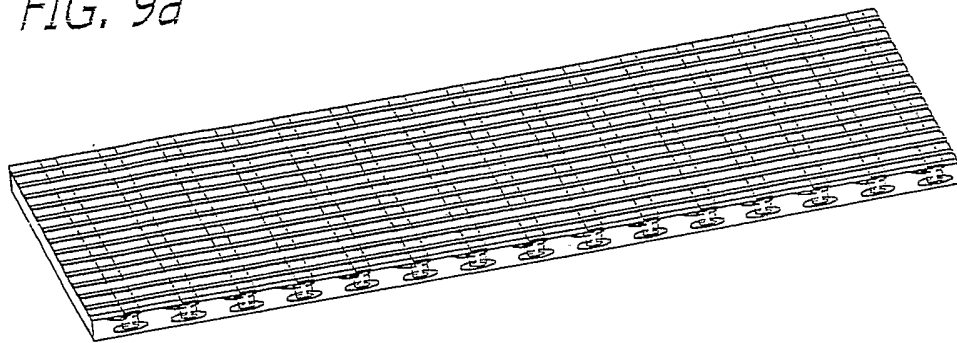


FIG. 9b

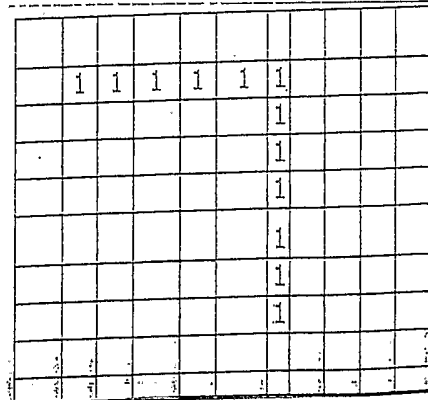
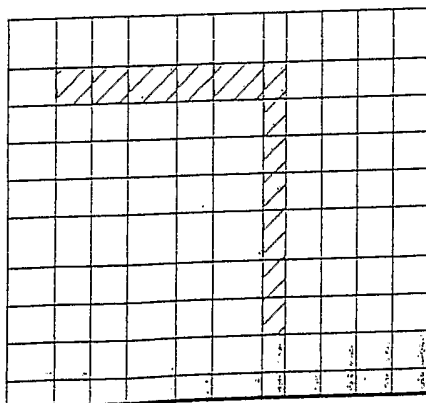
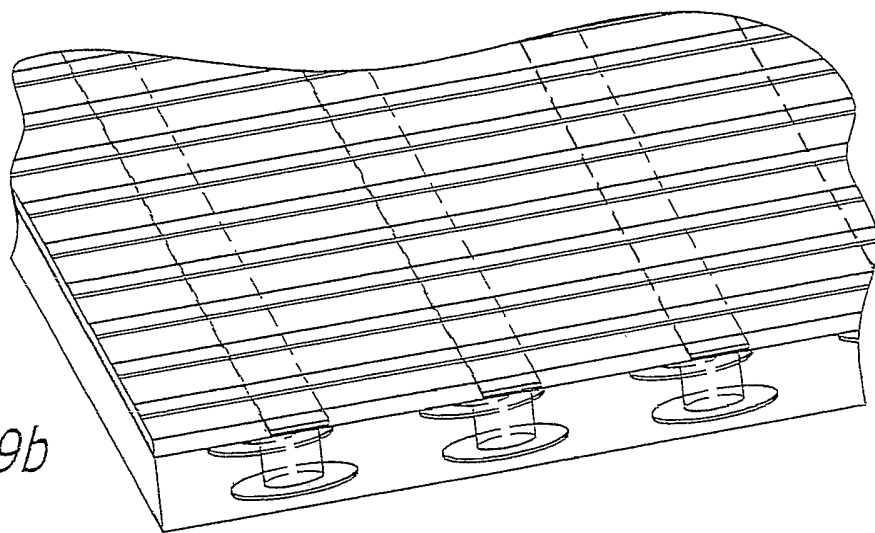


FIG. 10

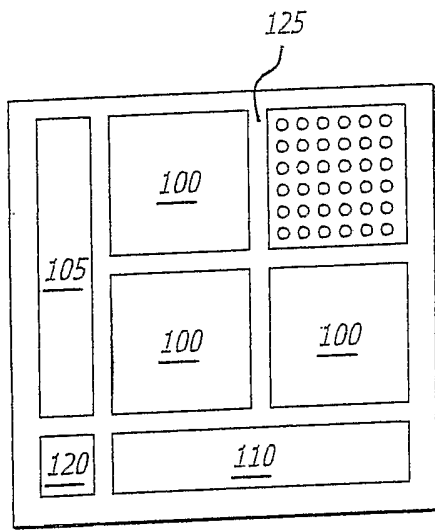


FIG. 11a

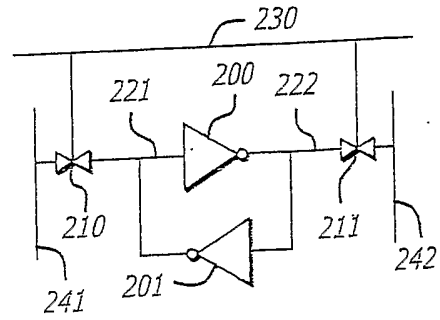


FIG. 11b

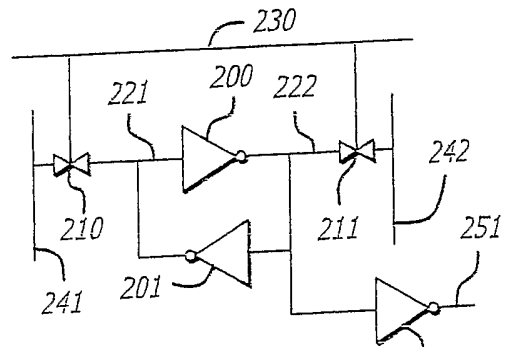


FIG. 11c

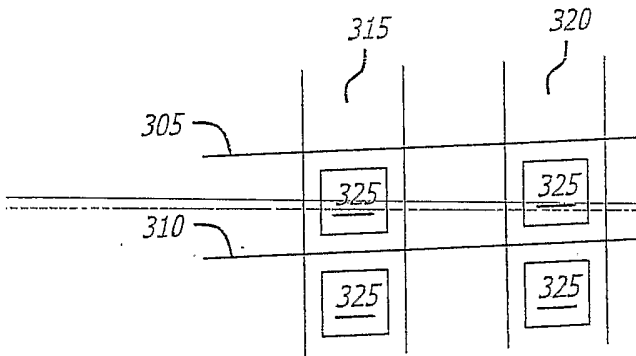


FIG. 12a

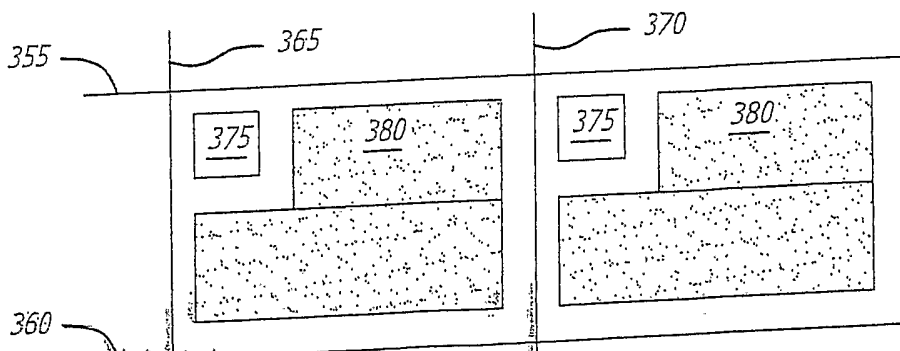


FIG. 12b

FIG. 13

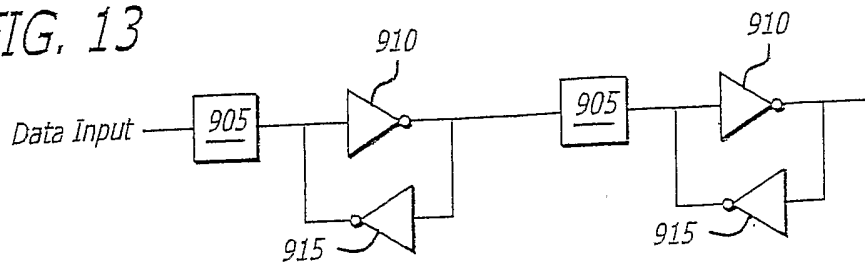


FIG. 14

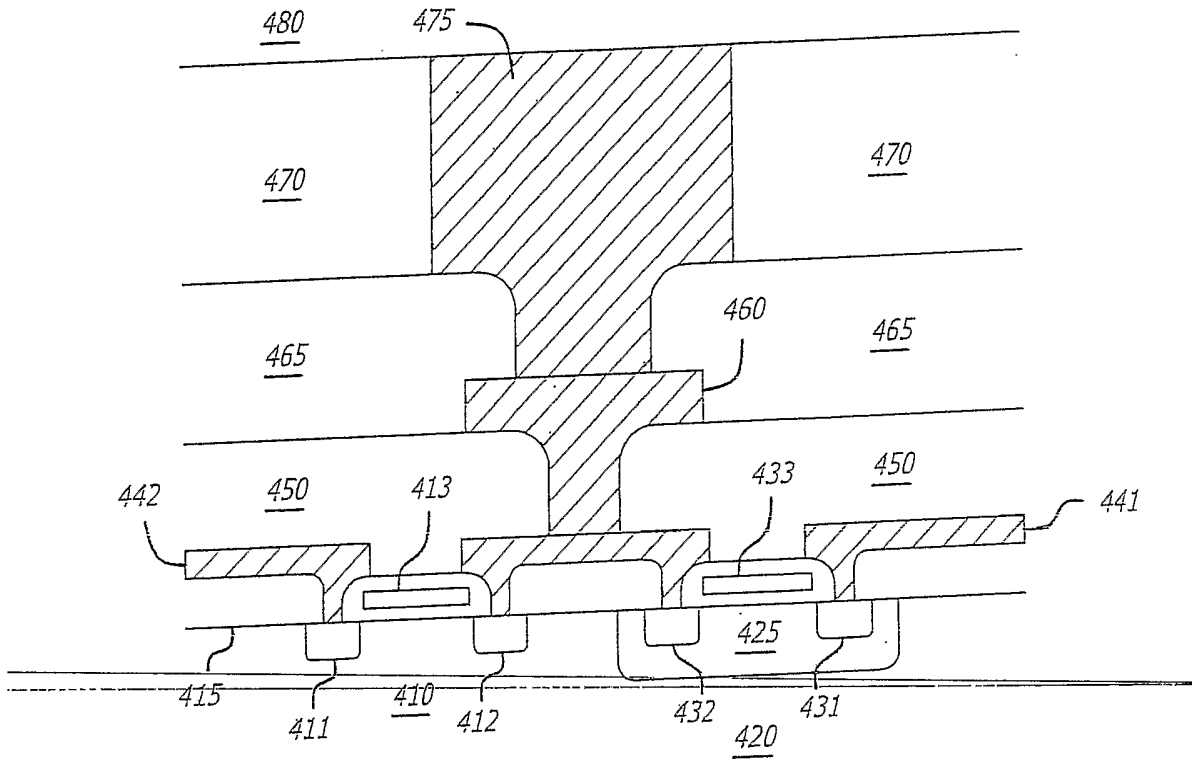
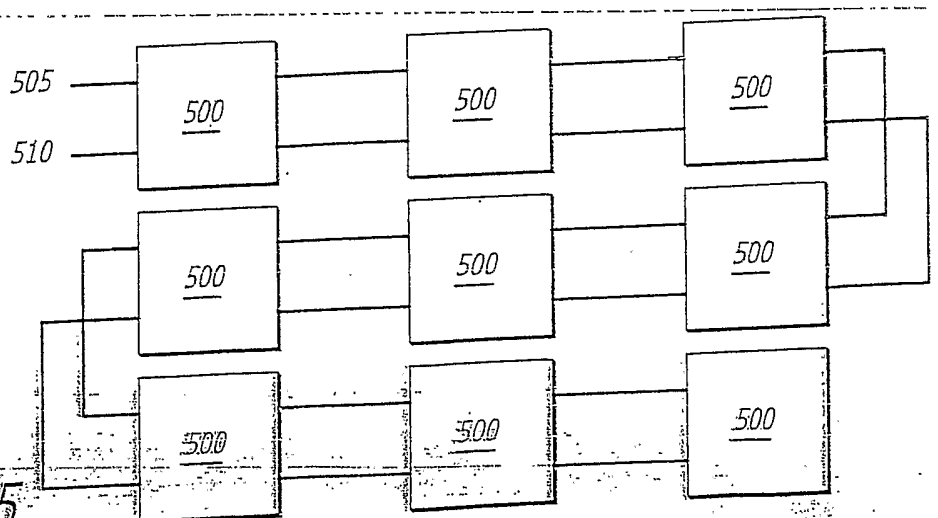


FIG. 15



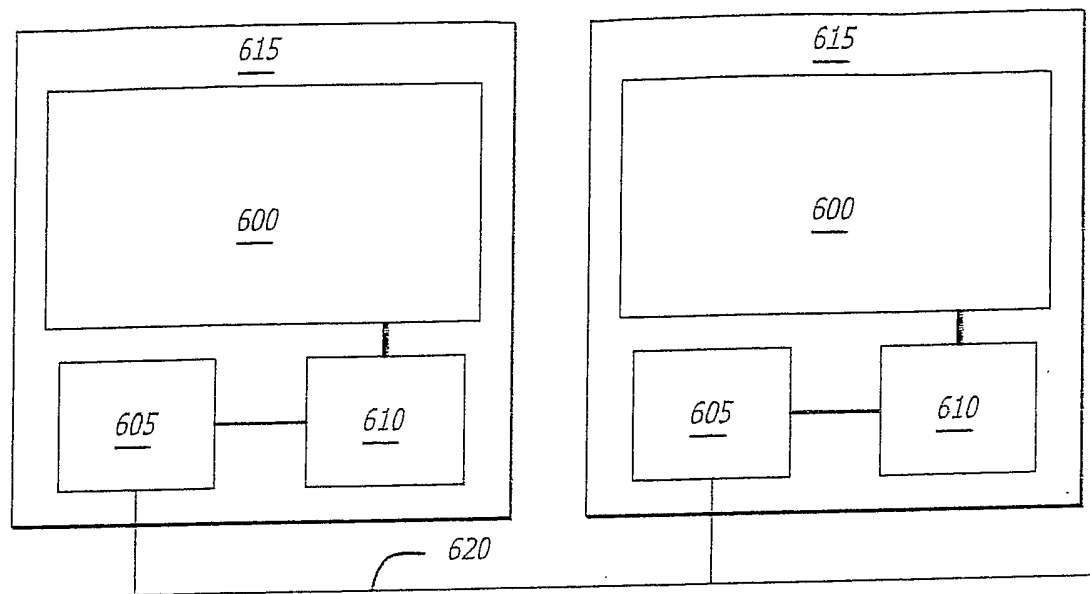


FIG. 16

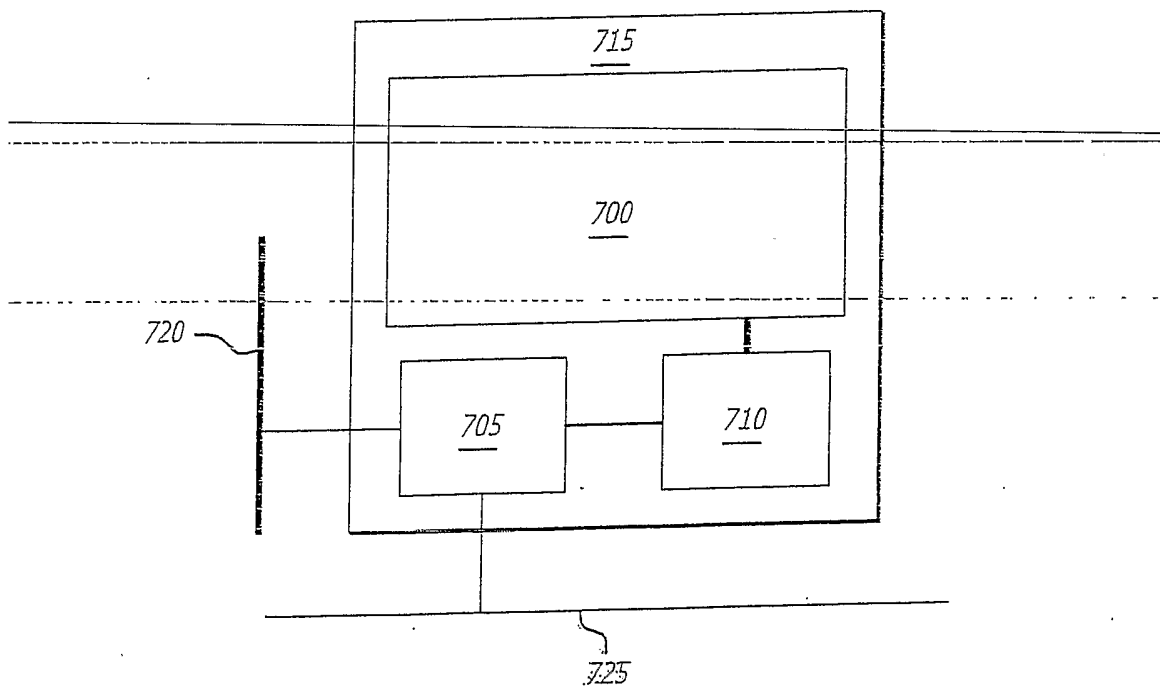


FIG. 17

FIG. 18a

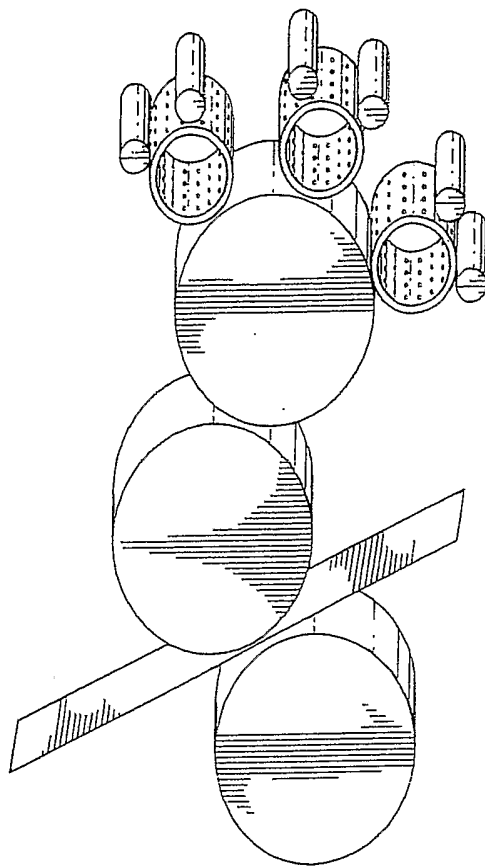
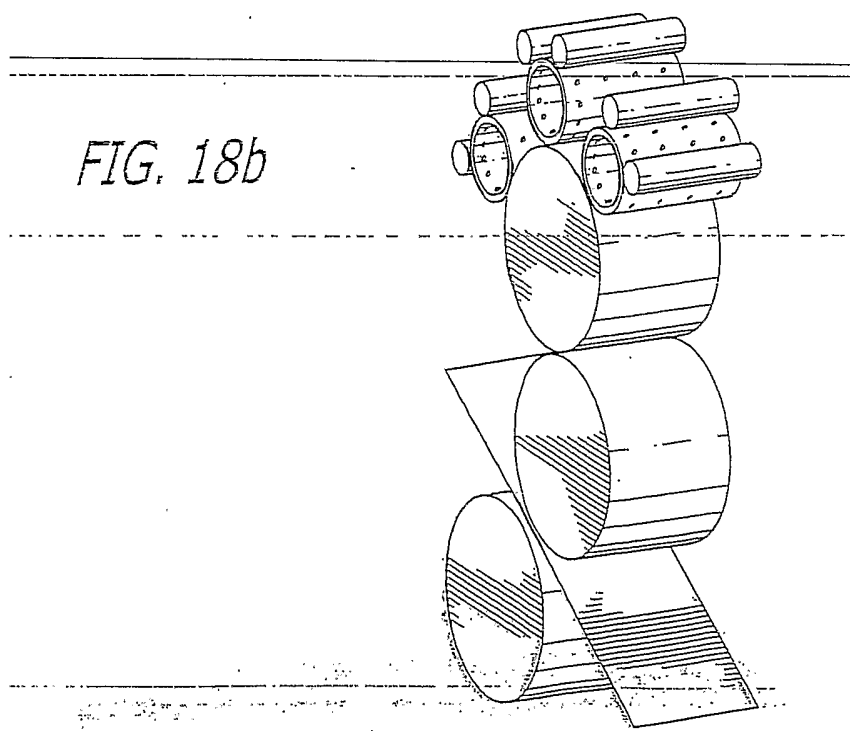
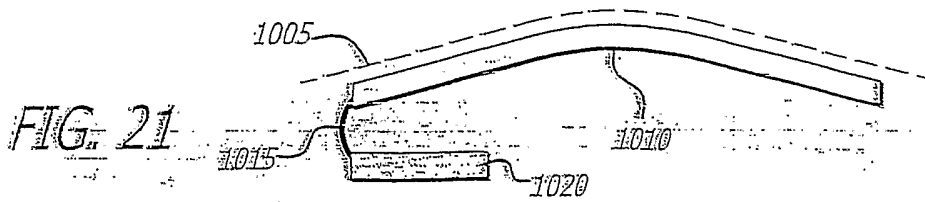
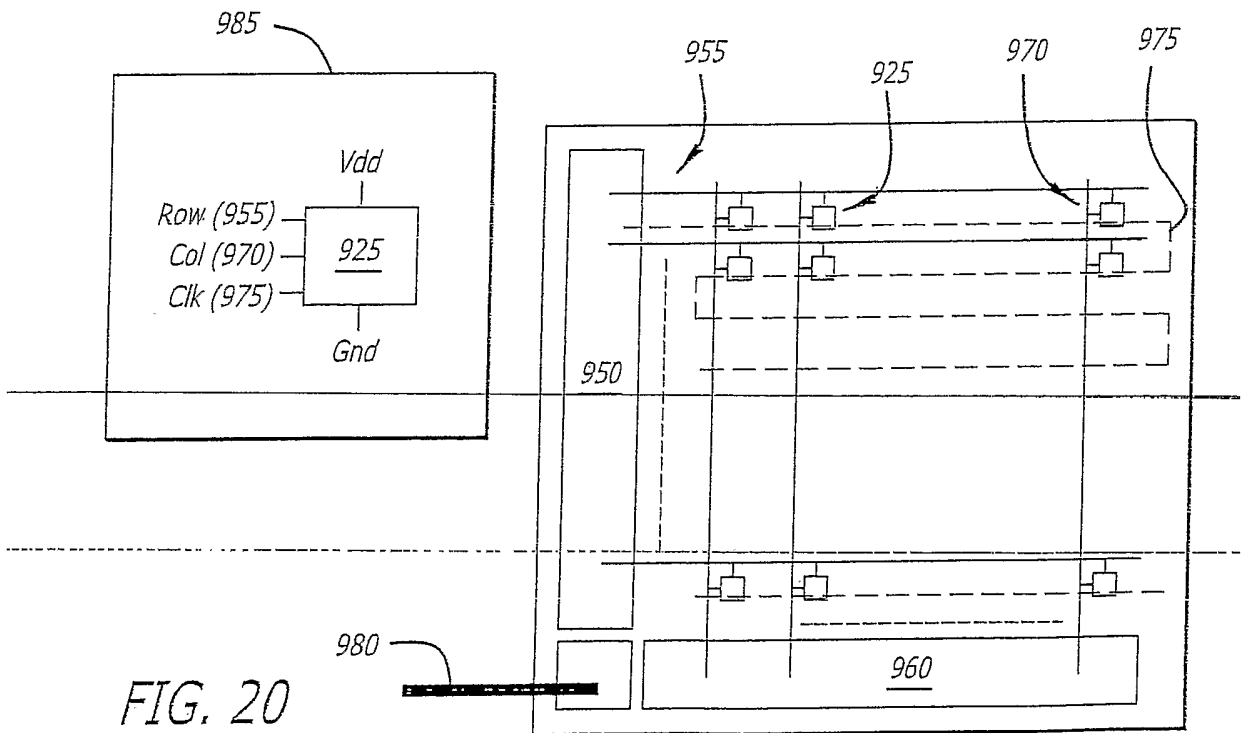
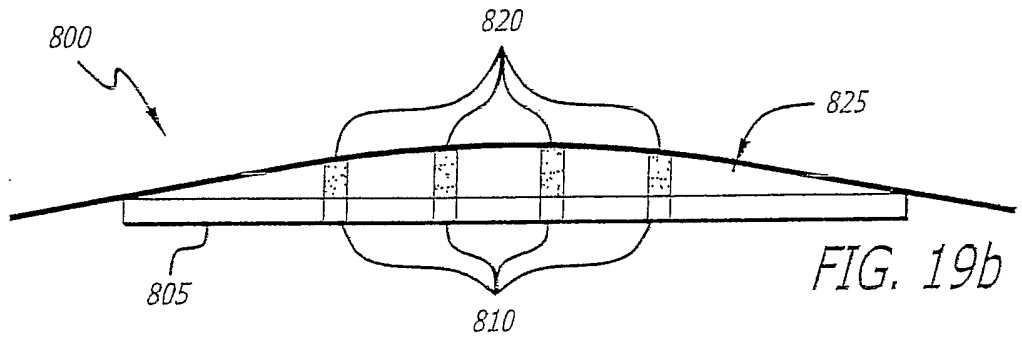
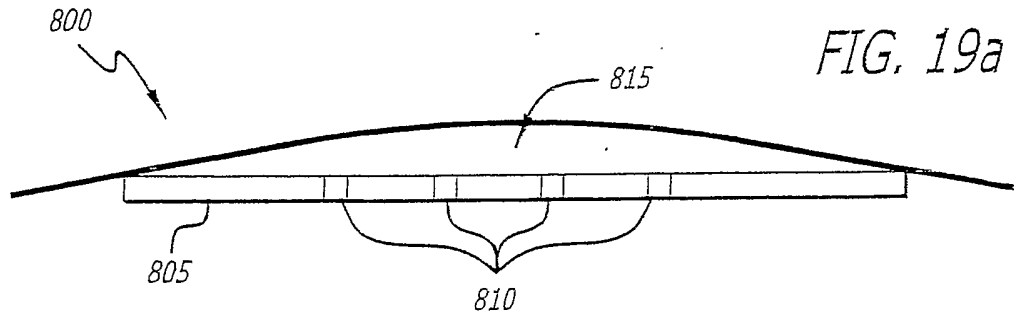
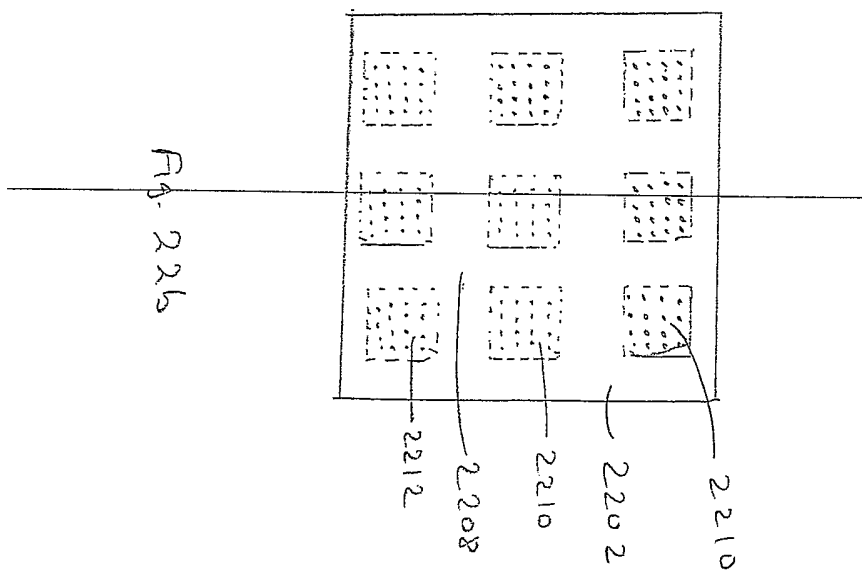
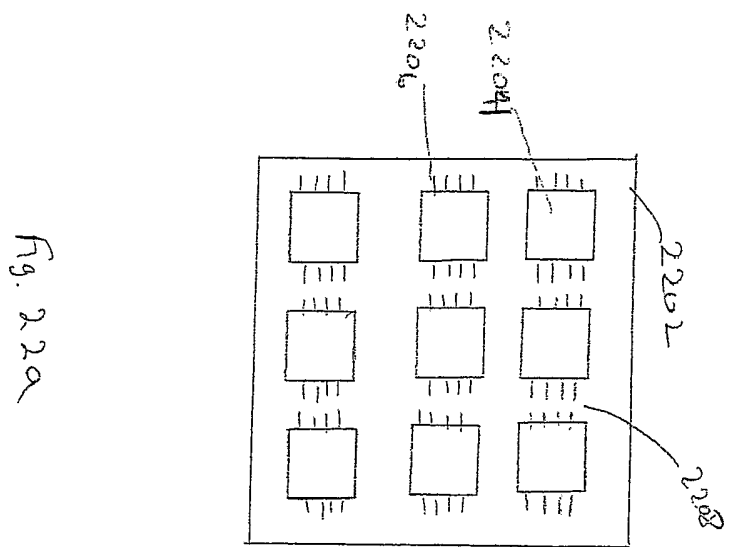


FIG. 18b







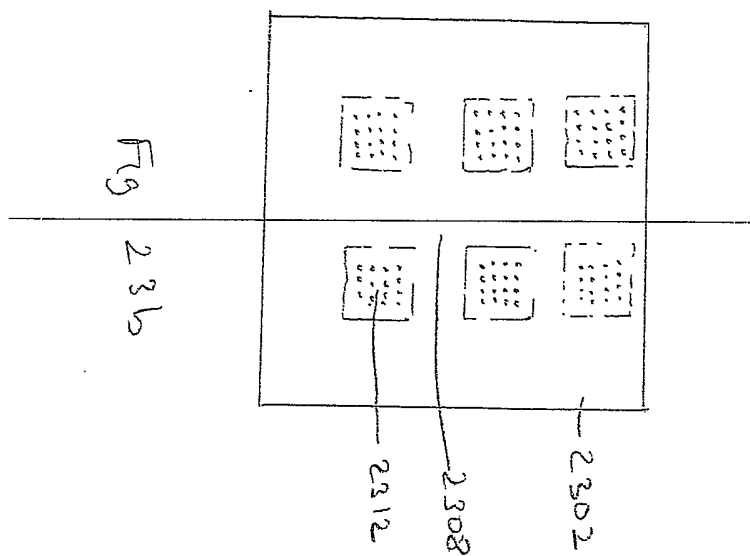
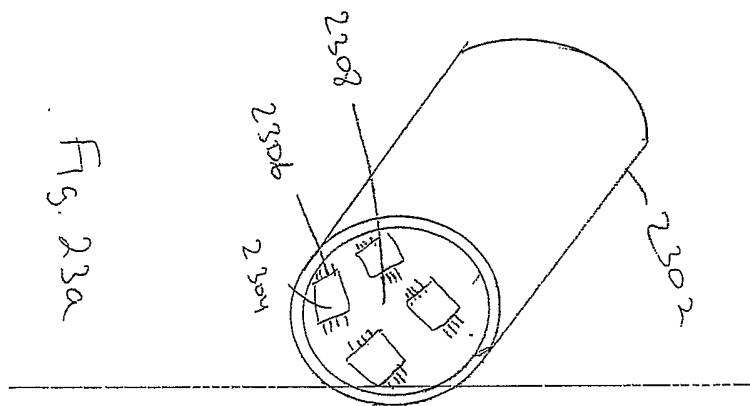
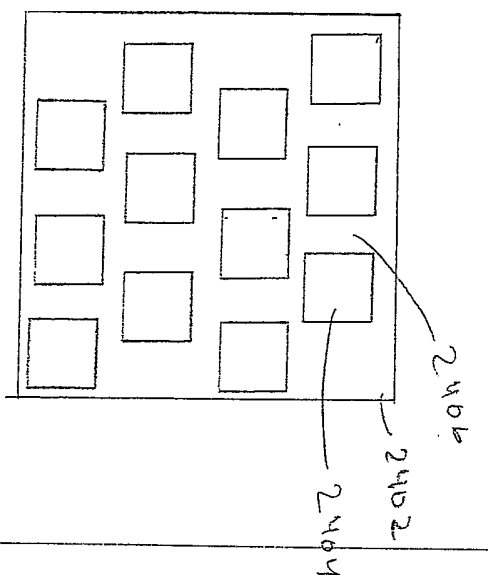
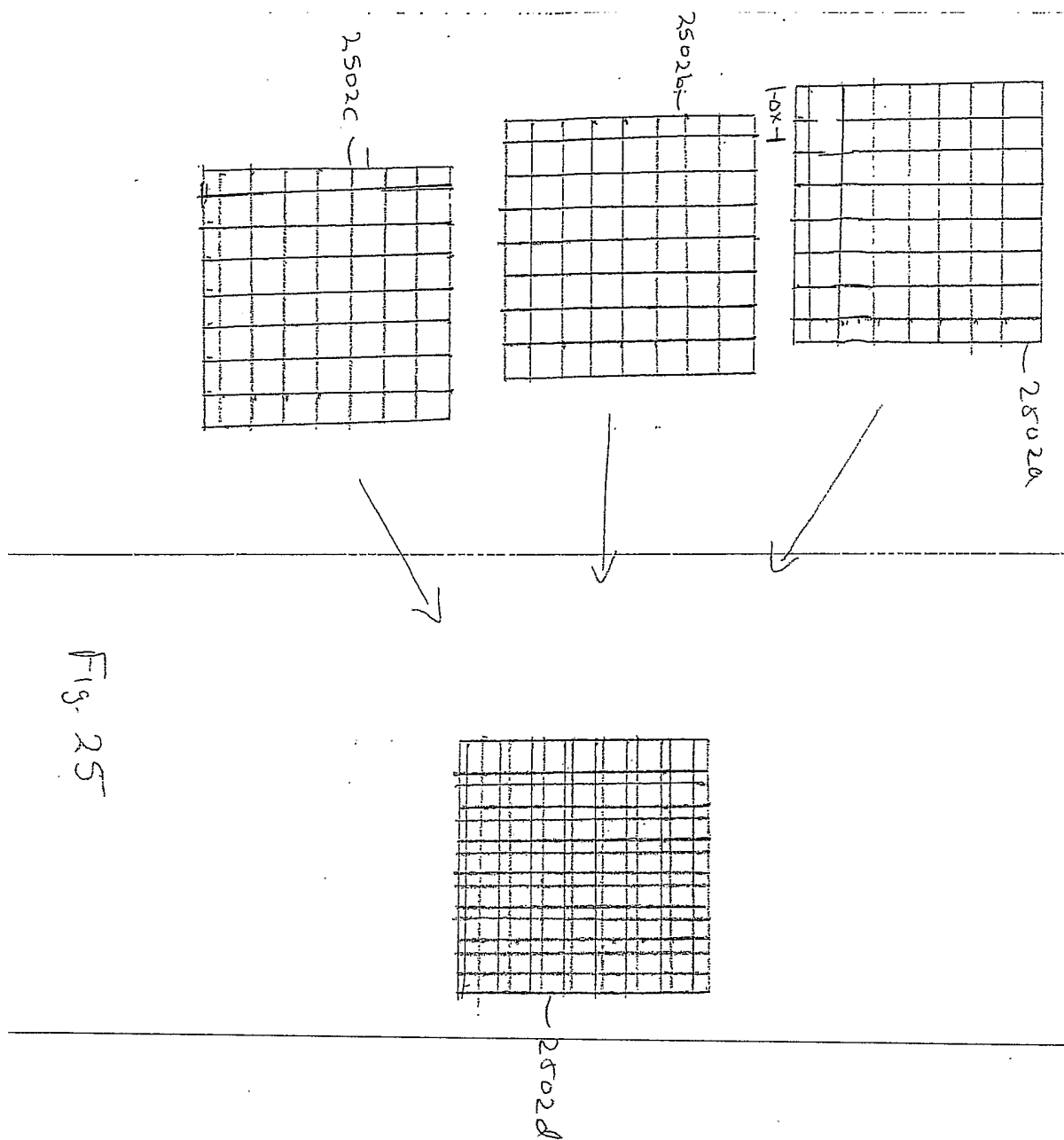
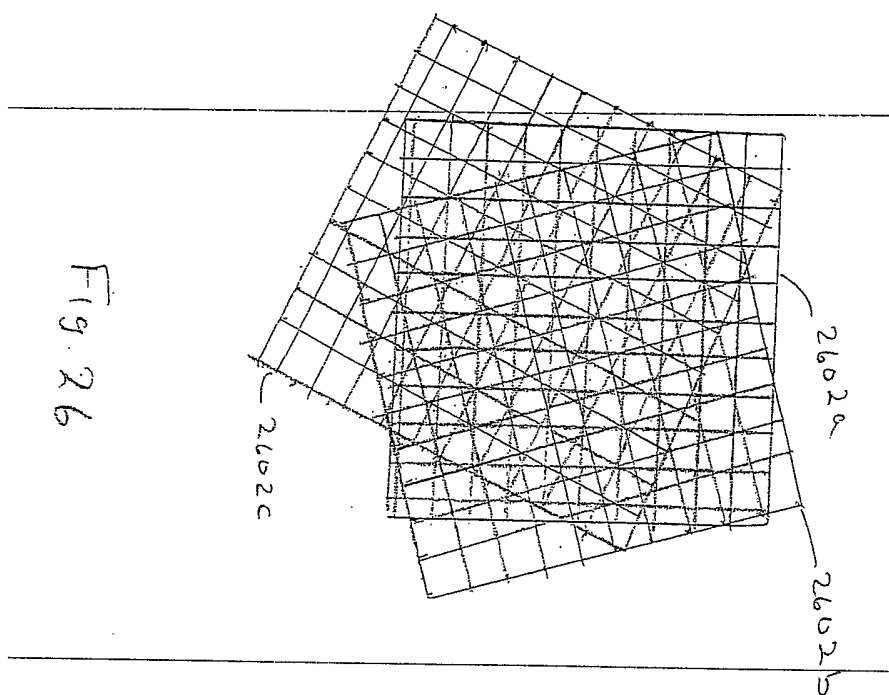


FIG. 24







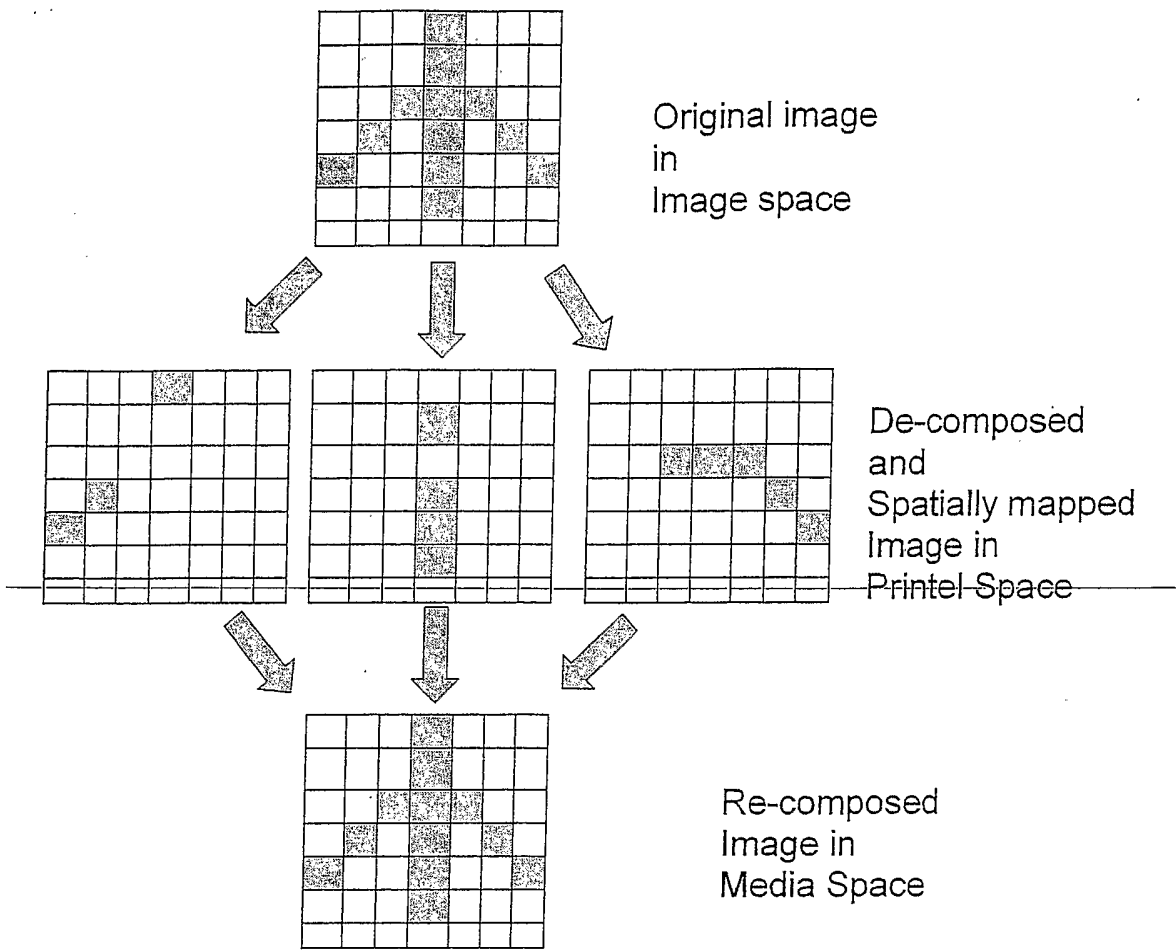


Fig. 27