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(54) Computing apparatus

(57) An apparatus for effecting transfers of data in a computer system:—

a) from one area of memory to another;

b) from an area of memory to an output device;

c) from an input device to an area of memory; or

d) from an input device to an output device;

has source and destination register address counters 3, 4 which are selectively, depending on the type of data transfer required, caused to count through the source and destination addresses in response to each data word transferred. The control of the application of word pulses to the counters is effected by the status of source and destination flags 8, 9. The apparatus may use the same data and address busses as a CPU of the system or different ones. The apparatus may be arranged to transfer data concurrently with the operation of the CPU on another function.

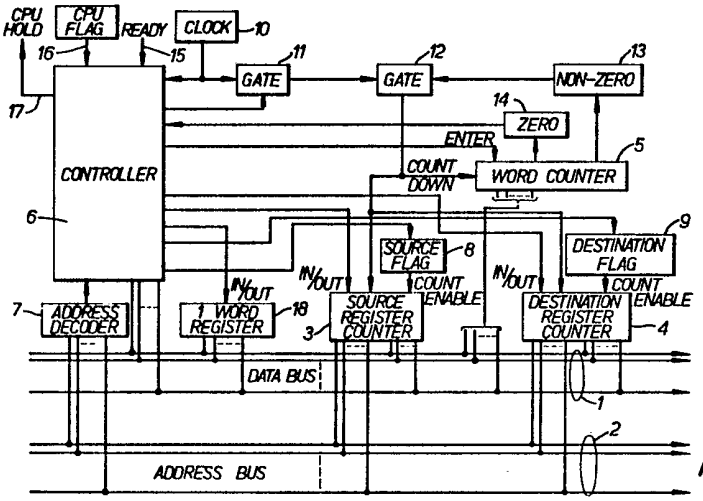

FIG.1.

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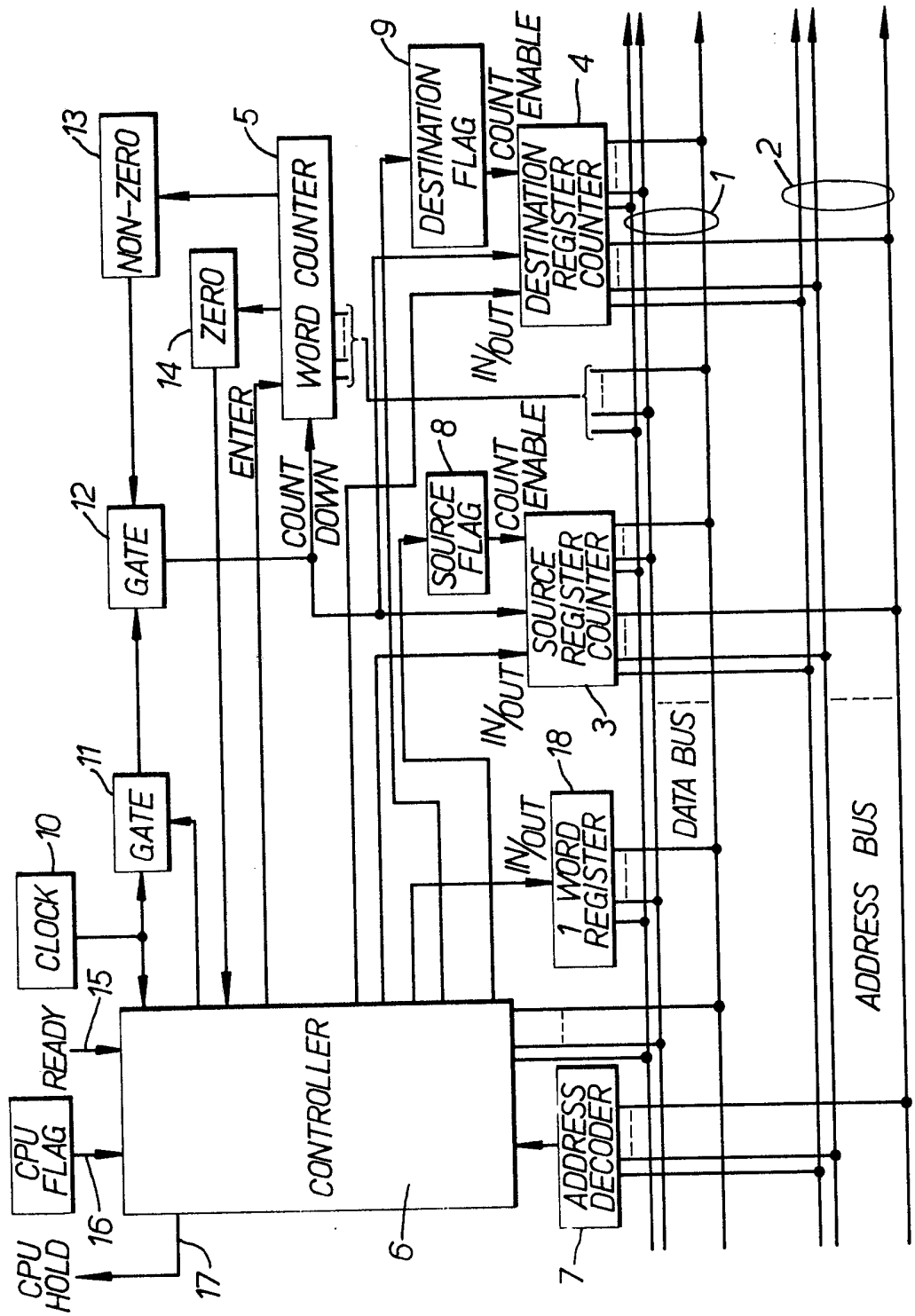
CPU HOLD
CPU FLAG
READY
CLOCK
GATE
GATE
NON-ZERO
ZERO
WORD COUNTER
ENTER
COUNT DOWN
CONTROLLER
ADDRESS DECODER
1 WORD REGISTER
SOURCE REGISTER COUNTER
SOURCE FLAG
COUNT ENABLE
DESTINATION REGISTER COUNTER
DESTINATION FLAG
COUNT ENABLE
IN/OUT
IN/OUT
IN/OUT
DATA BUS
ADDRESS BUS
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18

Fig.1.

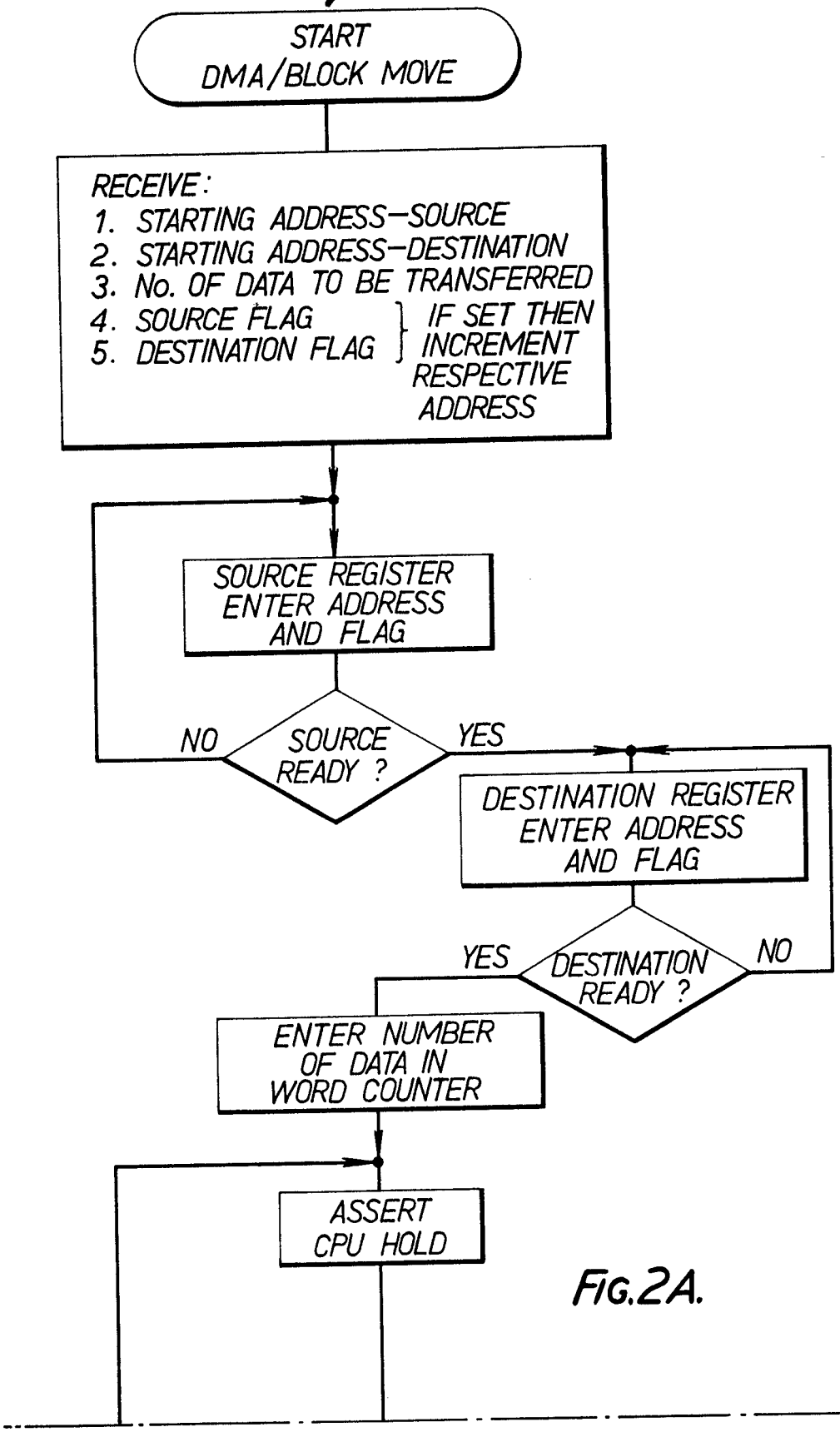
START
DMA/BLOCK MOVE
RECEIVE:
1. STARTING ADDRESS–SOURCE
2. STARTING ADDRESS–DESTINATION
3. No. OF DATA TO BE TRANSFERRED
4. SOURCE FLAG
5. DESTINATION FLAG
IF SET THEN INCREMENT RESPECTIVE ADDRESS
SOURCE REGISTER ENTER ADDRESS AND FLAG
SOURCE READY ?
NO
YES
DESTINATION REGISTER ENTER ADDRESS AND FLAG
DESTINATION READY ?
YES
NO
ENTER NUMBER OF DATA IN WORD COUNTER
ASSERT CPU HOLD

FIG. 2A.

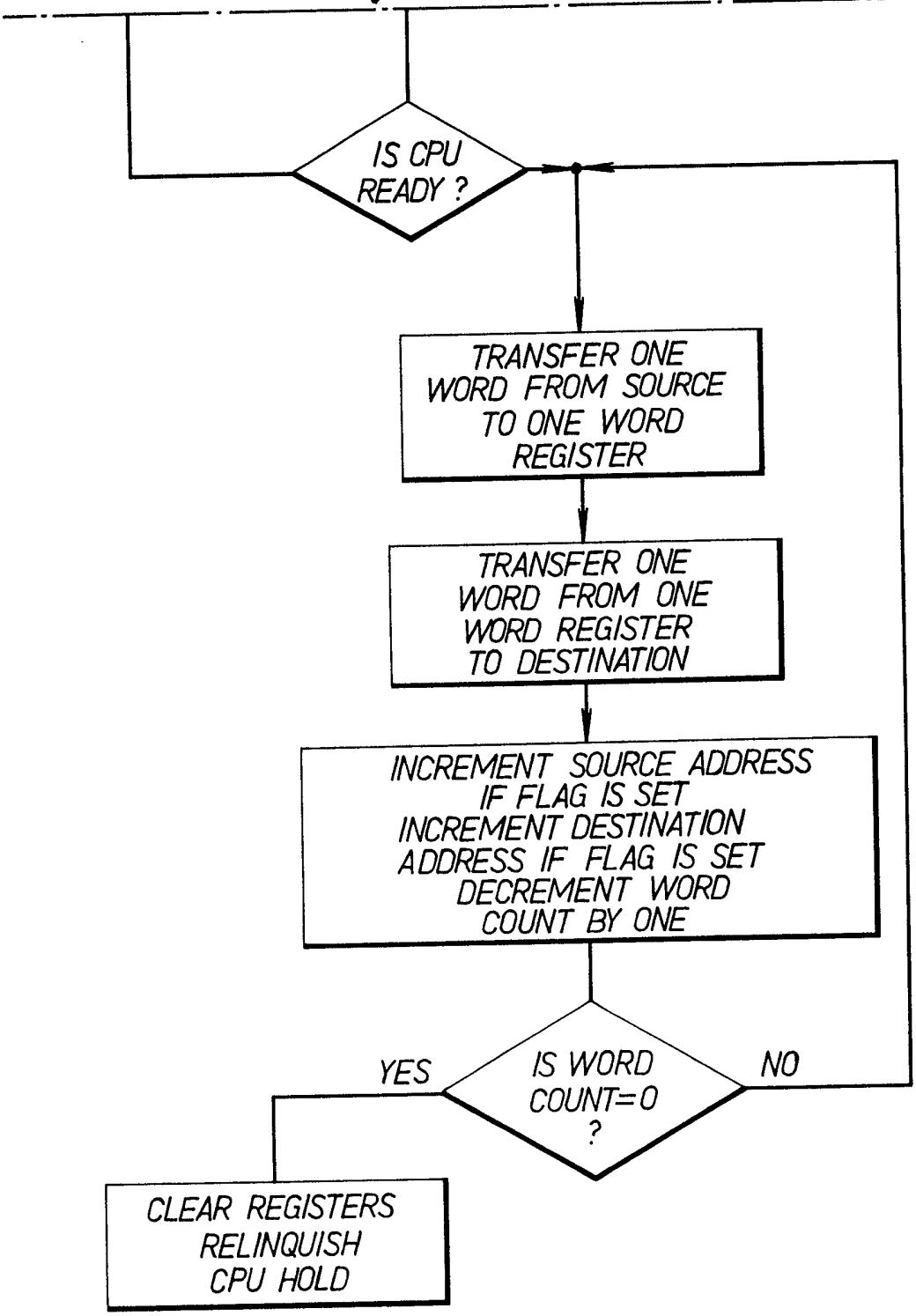
IS CPU READY ?
TRANSFER ONE WORD FROM SOURCE TO ONE WORD REGISTER
TRANSFER ONE WORD FROM ONE WORD REGISTER TO DESTINATION
INCREMENT SOURCE ADDRESS IF FLAG IS SET INCREMENT DESTINATION ADDRESS IF FLAG IS SET DECREMENT WORD COUNT BY ONE
IS WORD COUNT=0 ?
YES
NO
CLEAR REGISTERS RELINQUISH CPU HOLD

FIG.2B.

SPECIFICATION

Computing apparatus

This invention relates to computing apparatus and in particular to apparatus for effecting the transfer of large quantities of data between input devices, output devices and memory attached to computing apparatus.

In a computing apparatus, it is frequently required to move large quantities of data as quickly as possible from one place to another. For example, data may be stored in a long access time large capacity store such as a magnetic disc and in order to perform operations involving this data it is necessary for it to be transferred to rapid access semiconductor RAM. Likewise, data is required to be fed to an output device such as a display or a printer. Such transfers of data can be divided into four groups—(a) from one area of memory to another; (b) from an area of memory to an output device; (c) from an input device to an area of memory; (d) from an input device directly to an output device.

Certain types of microprocessors include firmware stored in their instruction ROM for performing one or more of the above functions. It is also known to provide a special component for carrying out one or more of the functions. Such a component is called a block move in case (a) and a direct memory access (DMA) in cases (b) and (c). A block move function is supported by many types of computing apparatus and is usually invoked by supplying it with a starting address for the source area of memory containing the data, a stirring address for the destination area of memory and a count of the number of data to be transferred. In operation, the component disables the central processing unit and takes control of the data and address buses. It then generates the appropriate addresses and memory control signals to organise the required data transfer. When the transfer has been completed, the component relinquishes control of the buses and reactivates the CPU.

The DMA component operates in a similar manner to the block move component and works through the addresses of the area of memory concerned until the required number of data have been transferred. It also supplies signals to the address bus to identify particular input or output device, assumed to be a memory mapped device in this instance. It may be that the selected input or output device is not ready for data transmission and the DMA component may be arranged to withhold its operation until it receives an indication from the device that it is ready.

The functions described above are usually performed by relatively simple devices using suitable software to control them or if the functions are performed by the microprocessor itself the components of the microprocessors are controlled by software stored in the ROM of the microprocessor.

It is an object of the present invention to provide a special hardware apparatus for performing all of the above functions as quickly as possible and therefore with the minimum of software control.

According to the present invention there is provided apparatus for use in a computer system for a plurality of words of data from a source to a destination via a data bus of the system, in which the source is a memory-shaped peripheral unit of the system or a group of consecutive addresses in a memory of the system and the destination is a memory-mapped peripheral unit of the system or a group of consecutive addresses in a memory of the system the addresses selected by the apparatus being applied via an address bus of the system, the apparatus comprising a source register counter, a destination register counter, a word counter, a generator of clock pulses, storage means for source and destination flags, and logic means responsive to the status of the source and destination flags selectively to cause the respective members in the source and destination register counters to be stepped progressively from initial values by the clock pulses as the number in the word counter is decremented from an initial value to zero, whereby if either of the flags is not set the respective register counter is not stepped by the clock pulses, the source and destination register counters respectively providing the addresses for the source and destination of the data to be transferred under the control of signals derived from the clock pulses.

In the transfer of data from or to a memory-mapped perpheral unit, the unit has a single address which is stored in the source or destination register counter, and is assumed to be able to transmit or receive the plurality of data words to be transferred.

It will be apparent that the four combinations of the two states of the two flags correspond to four different functions as follows:–

Source flag	Destination flag	Function
set	set	memory to memory block move
set	not set	memory to output peripheral unit
not set	set	input peripheral to memory
not set	not set	input peripheral unit to output peripheral unit

Apart from the fact that the apparatus employs the address and data busses of the system its operation is independent of that of the central processing unit and insofar as that unit can operate without using the data and address busses, for example, in carrying out a complex calculation, it may continue to do so whilst the apparatus is performing a data transfer. The apparatus may be used with non-memory-mapped peripheral units and therefore use data and/or busses not connected to the CPU; with such an arrangement the operation of the CPU may continue during a separate data transfer.

If the CPU relinquishes control during a data transfer to regain it at the end of the transfer, the apparatus may be arranged to restore control to the CPU temporarily whilst the peripheral unit is not ready to participate in an instructed data transfer.

The apparatus may be constructed as a unit, e.g. in integrated circuit form, or it may be embodied in a microprocessor or microcomputer.

In order that the invention may be fully understood and readily carried into effect, it will now be described with reference to the accompanying drawings of which:–

Figure 1 shows in diagrammatic form one example of the present invention; and

Figure 2 is a flow diagram of the operation of the example shown in Fig. 1.

The apparatus of Fig. 1 is connected to a data bus 1 having, for example, eight or sixteen parallel conductors and an address bus 2 having, for example, eight or sixteen parallel conductors. The apparatus includes a source register counter 3 and a destination register counter 4 together with a word counter 5. Control signals for these counters are generated by a controller 6 when activated by a signal from an address decoder 7 connected to the address bus 2. The controller 6 is also connected to receive signals from and apply signals to the data bys 1. Two bistables 8 and 9 are connected to outputs of the controller 6 and store respectively source and destination flags and are connected to "count enable" inputs of the source register counter 3 and the destination register counter 4 respectively. The word counter 5 is connected to receive signals from the data bus 1 which are stored in the counter 5 as an initial number in response to an enter signal from the controller 6. A clock 10 provides pulses which are applied to the controller 6 and through a gate 11 controlled by an output of the controller 6 to a gate 12 controlled by an output from a non-zero detector 13 responsive to the count stored in the counter 5. The clock pulses fed out from the gate 12 are applied to cause the count in the counter 5 to count downwards and also to the source and destination register counters 3 and 4. The counters 3 and 4 also receive in/out control signals from the controller 6 in response to which they receive an address from the data bus 1 or transmit an address to the address bus 2. The controller 6 has three further inputs, a signal indicating that the count in the counter 5 has reached zero from a zero detector 14, an input 15 for one or more ready signals from peripheral devices and an input 16 for a flag from a central processing unit indicating that this unit is ready to relinquish control of the data address busses 1 and 2. When the controller 6 takes control it applies a signal via a conductor 17 to hold the control processing unit. The controller 6 may be arranged to release the hold on the CPU for a short period if a ready signal is not received from a peripheral device involved in the data transfer and then reassert the hold when the peripheral device is ready.

A one-word register 18 is provided connected to the data bus 1 and is arranged to receive one word of data or transmit one word of data to the data bus 1 under the control of controller 6.

In the operation of the apparatus described, the controller receives an enabling signal from the address decoder 7 which activates it to receive data from the data bus 1. The data consists of the following elements:

(a) a starting address for the source of the data;

(b) a starting address for the destination of the data;

(c) a count of the number of data to be transferred;

(d) a flag, called the source flag, indicating whether or not to increment the start address with each item of data; and

(e) a flag, called the destination flag, indicating whether or not to increment the destination address with every item of data.

In addition, the controller 6 receives a CPU flag which is set by the CPU in response to a CPU hold signal applied to it via the conductor 17 when the CPU is ready for the data transfer to begin. The starting address for the source of the data is stored in the source register counter 3 having been entered therein from the data bus 1 in response to a signal from the controller 6 on the in/out connection of the counter 3. Similarly, the starting address for the destination of the data is stored in the destination register counter 4 from the data bus 1 in response to a signal from the controller 6 on the in/out connection of the counter 4. The count of the number of data to be transferred is entered in the word counter 5 from the data bus 1 in response to a signal on the enter input of the counter 5 from the controller 6. The source and destination flags are stored in the bistables 8 and 9 respectively in response to signals from the controller 6.

The following table shows the settings of the source and destination flags for the four functions of the apparatus:–

Source flag	Destination flag	Function
set	set	memory to memory block move
set	not set	memory to output peripheral unit
not set	set	input peripheral to memory
not set	not set	input peripheral unit to output peripheral unit

If the source flag is set to "on", the counter 3 is incremented after each transfer. If the destination flag is set to "on", the counter 4 is incremented after each transfer. Unless the particular flag is set to "on", the source and destination register counter do not respond to the clock pulses applied to them so that the address stored in them are unchanged.

When selecting a particular peripheral device, which may be an input device or an output device, the apparatus merely uses the appropriate address which is supplied to it by the CPU as part of its instructions, the address being stored in the counter 3 or the counter 4 depending on whether the device is to act as a source or destination for the data. It is of course necessary that the device be memory mapped, that is to say that it can be selected by the application of appropriate signals to the address bus 2. An address may consist of, for example, 2 bytes or 16 bits so that more than 64,000 addresses are available. Alternatively, 3 bytes may be used for the address in which case more than 16 million addresses are available.

In the operation of the apparatus, data from a source address is received along the data bus 1 and stored in the one-word register 17 and then that word of data is transferred from the register 17 via the data bus 1 again to the destination register as selected by the address in the counter 4. Thus the counters 3 and 4 use the address bus 2 to select in turn the source register and the destination register for each word to be transferred. When a transfer has been effected, the count in the word counter 5 is decremented by a clock pulse applied to it via the gate 12, which remains open as long as the count in the counter 5 is non-zero. When the count in the counter 5 reaches zero, the gate 12 is closed so that further pulses cannot be applied to the counter 5 or to either of the counters 3 and 4 and the detector 14 sends a signal to the controller 6 indicating that the number of words required has been transferred, so that the operation has been completed.

It will be apparent that the pulses from the clock 10 respectively correspond to the transfers of words from the source to the destination. The gate 11 is provided to control the transmission of pulses from the clock 10 to the gate 12 preventing pulses being applied to the gate 13 until the CPU and other devices are ready.

The operation described above is also shown in the flow diagram of Fig. 2.

It is intended that the whole of the apparatus be constructed as an integrated circuit and as such it may be incorporated in a microprocessor to handle the bulk data transfers on its behalf. By virtue of the fact that the apparatus includes dedicated items for particular operations, its speed of operation is inherently higher than would be the case, if, for example, a single counter

were provided in place of the counters 3, 4 and 5 and the apparatus were effectively formed by software control of the components normally provided in a data processing chip.

Although the invention has been described by reference to a memory-mapped peripheral unit or more than one such unit, it could equally well be used with units having data and/or address busses separate from those of the CPU (i.e. not memory-mapped units). If it is required that the operation of the CPU be disturbed as little as possible by the DMA/Block move operation, the CPU hold signal may be applied as a low priority interrupt.

CLAIMS

1. Apparatus for use in a computer system for transferring a plurality of words of data from a source to a destination via a data bus of the system, in which the source is a memory-mapped peripheral unit of the system or a group of consecutive addresses in a memory of the system and the destination is a memory-mapped peripheral unit of the system or a group of consecutive addresses in a memory of the system, the addresses selected by the apparatus being applied via an address bus of the system, the apparatus comprising a source register counter, a destination register counter, a word counter, a generator of clock pulses, storage means for source and destination flags, and logic means responsive to the status of the source and destination flags selectively to cause the respective members in the source and destination register counters to be stepped progressively from initial values by the clock pulses as the number in the word counter is decremented from an initial value to zero, whereby if either of the flags is not set the respective register counter is not stepped by the clock pulses, the source and destination register counters respectively providing the addresses for the source and destination of the data to be transferred under the control of signals derived from the clock pulses.

2. Apparatus according to claim 1, wherein the status of the source and destination flags determines the function of the apparatus as follows:–

Source flag	Destination flag	Function
set	set	memory to memory block move
set	not set	memory to output peripheral unit
not set	set	input peripheral unit to memory
not set	not set	input peripheral unit to output peripheral unit

3. Apparatus according to claim 1 or 2 including controller means for controlling the application of clock pulses to the word counter and the logic means and having a control input for a signal enabling a data transfer to start.

4. Apparatus according to claim 1, 2 or 3, connectible to address and data busses which are the address and data busses of a CPU of the computer system.

5. Apparatus according to claim 1, 2 or 3, connectible to address and data busses which are separate from the address and data busses of CPU of the computer system.

6. Apparatus according to claim 1 or 5, wherein it can be arranged to perform a transfer of data simultaneously with the CPU executing another operation.

7. Data transfer apparatus substantially as described herein with reference to the accompanying drawings.

8. Apparatus according to any of claims 1 to 7 constructed in integrated circuit form.

9. Apparatus according to claim 8 incorporated in a microprocessor or microcomputer.

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