(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
04 June 2020 (04.06.2020)

WIPO | PCT

(10) International Publication Number
WO 2020/108603 A1

(51) International Patent Classification:
H01L 23/522 (2006.01)

(21) International Application Number:
PCT/CN2019/121911

(22) International Filing Date:
29 November 2019 (29.11.2019)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
201811460134.6 30 November 2018 (30.11.2018) CN
201822028209.5 30 November 2018 (30.11.2018) CN

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME,

(54) Title: METHOD FOR FABRICATING SEMICONDUCTOR INTERCONNECT STRUCTURE AND SEMICONDUCTOR STRUCTURE THEREOF

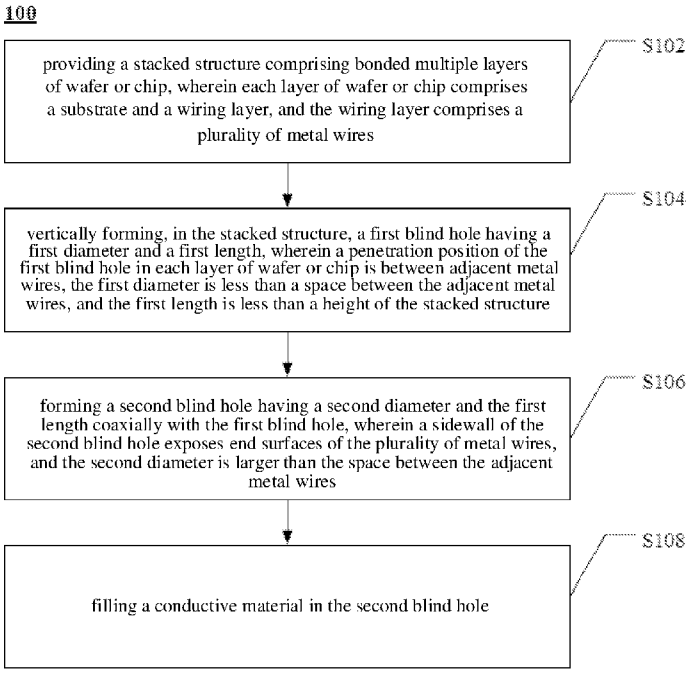

Fig. 1

(57) Abstract: A semiconductor interconnect structure and a fabricating method thereof are disclosed. The method comprises: providing a stacked structure comprising bonded multiple layers of wafer or die, each bonded layer comprises a substrate and a wiring layer, and the wiring layer comprises metal wires; vertically forming, in the stacked structure, a first blind hole having a first diameter and a first length and penetrating each bonded layer between adjacent metal wires, the first diameter is less than a space between the adjacent metal wires, and the first length is less than a height of the stacked structure; forming a second blind hole having a second diameter and the first length coaxially with the first blind hole, a sidewall of the second blind hole exposes the metal wires, and the second diameter is larger than the space between the adjacent metal wires; and filling a conductive material in the second blind hole.

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MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

METHOD FOR FABRICATING SEMICONDUCTOR INTERCONNECT STRUCTURE AND SEMICONDUCTOR STRUCTURE THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is based on and claims priority to and benefits of the Chinese Patent Application No. 201811460134.6, entitled "A METHOD FOR FABRICATING A SEMICONDUCTOR INTERCONNECT STRUCTURE AND SEMICONDUCTOR STRUCTURE THEREOF" filed with the China National Intellectual Property Administration (CNIPA) of the People's Republic of China on November 30, 2018. The entire content of the above-referenced application is incorporated herein by reference.

TECHNICAL FIELD

[0002] The present disclosure relates to the field of integrated circuit (IC) fabrication technology, and in particular to a method for fabricating a semiconductor interconnect structure and a semiconductor structure thereof.

BACKGROUND

[0003] In integrated circuit manufacturing, stacking multiple chips and establishing mechanical and electrical connections among them is an important way to reduce the size of integrated circuits. The current technology is fabricating Through Silicon Vias (TSVs) for each chip to be stacked, and then forming a bump (Micro-Bump) for each TSV. The chips then are bonded through a die-to-die or die-to-wafer approach, using the bumps and the TSVs for electrically connecting the stacked multiple chips.

[0004] First of all, the die-to-die or die-to-wafer bonding process has low efficiency and high cost. In addition, the TSVs for each chip need to be pre-fabricated, and the bumps need to be formed at the TSVs accordingly. As such, the bonding process has the high risks of alignment and connection errors, and the electrical connection paths between the upper and lower layers can be easily broken, resulting in low yield.

[0005] Therefore, there is a need for a solution of inter-layer electrical connections or interconnection that overcomes the above issues.

[0006] It is to be noted that the above information disclosed in this Background section is only for enhancement of understanding of the background of the invention, and therefore may contain information that does not form the prior art that is already known to a person of ordinary skill in the art.

SUMMARY OF THE INVENTION

[0007] The present disclosure provides a method for fabricating a semiconductor interconnection structure and a semiconductor structure thereof, to overcome the problems of complicated manufacturing process and the low yield of the semiconductor interconnect structure due to limitations and defects of related art.

[0008] A first aspect of embodiments of the present disclosure may direct to a method for a fabricating semiconductor interconnection structure. The method may include: providing a stacked structure comprising bonded multiple layers of wafer or die, wherein each layer of wafer or die comprises a substrate and a wiring layer, and the wiring layer comprises a plurality of metal wires; vertically forming, in the stacked structure, a first blind hole having a first diameter and a first length, wherein a penetration position of the first blind hole in each layer of wafer or die is between adjacent metal wires, the first diameter is less than a space between the adjacent metal wires, and

the first length is less than a height of the stacked structure; forming a second blind hole having a second diameter and the first length coaxially with the first blind hole, wherein a sidewall of the second blind hole exposes end surfaces of the plurality of metal wires, and the second diameter is larger than the space between the adjacent metal wires; and filling a conductive material in the second blind hole.

[0009] In an exemplary embodiment of the present disclosure, forming the second blind hole having the second diameter and the first length coaxially with the first blind hole may comprise widening a portion of the first blind hole in the substrate of each layer of wafer or die to the second diameter by a first wet etch process, and extending, by a second wet etching process, a portion of the first blind hole in the wiring layer of each layer of wafer or die to the second diameter to expose the end surfaces of the plurality of metal wires to form the second blind hole.

[0010] In an exemplary embodiment of the present disclosure, filling the conductive material in the second blind hole may comprise forming a dielectric isolation layer on an inner surface of the second blind hole, and etching the dielectric isolation layer to expose the end surfaces of the plurality of metal wires and a bottom of the second blind hole.

[0011] In an exemplary embodiment of the present disclosure, forming the dielectric isolation layer may comprise depositing SiCN on the inner surface of the second blind hole by a chemical vapor deposition process.

[0012] In an exemplary embodiment of the present disclosure, etching the dielectric isolation layer to expose the end surfaces of the plurality of metal wires and the bottom of the second blind hole may comprise by a plasma dry etch process, etching portions of the dielectric isolation layer on the end surfaces and upper surfaces of the plurality of metal wires to expose the plurality of metal wires, and etching a portion of the dielectric isolation layer at the bottom of the second blind hole to expose the bottom of the second blind hole.

[0013] In an exemplary embodiment of the present disclosure, filling the conductive material in the second blind hole may comprise sputtering a seed metal on the etched dielectric isolation layer and the exposed end surfaces of the plurality of metal wires and the bottom of the second blind hole, wherein the seed metal may comprise tantalum or copper, and growing the conductive metal in the second blind holes sputtered with the seed metal, the conductive metal may comprise copper.

[0014] In an exemplary embodiment of the present disclosure, the method may further include grinding a bottom layer of the stacked structure to expose a metal filled at a bottom of the second blind hole, and forming a bump on a surface of the exposed metal.

[0015] In an exemplary embodiment of the present disclosure, each of the first blind hole and the second blind hole may have a cross-sectional top view of a circle shape, a polygon shape, and an irregular shape.

[0016] In an exemplary embodiment of the present disclosure, the multiple layers of wafer or die may be directly bonded, wherein a substrate of a top layer is directly disposed on a wiring layer of a lower layer.

[0017] In an exemplary embodiment of the present disclosure, a difference between the first diameter and the space between the adjacent metal wires may be within a first preset safe range, and a difference between the second diameter and the space between the adjacent metal wires is within a second preset safe range.

[0018] A second aspect of the present disclosure may direct to a semiconductor structure. The semiconductor structure may include: a stacked structure comprising bonded multiple layers of wafer or die, each layer of wafer or die comprising a substrate and a wiring layer, and the wiring layer comprising a plurality of metal wires; and at least a through silicon via (TSV) penetrating the bonded multiple layers of wafer or die of the stacked structure, a center of a penetration position on each layer of wafer or die being located between adjacent metal wires, and a sidewall of the

through silicon via intersecting with the plurality of metal wires. The through silicon via penetrating the bonded multiple layers of wafer or die of the stacked structure may be fabricated by a method including one single etching process disclosed above.

[0019] In an exemplary embodiment of the present disclosure, the through silicon via may have a cross-sectional top view of a circle shape, a polygon shape, or an irregular shape.

[0020] In an exemplary embodiment of the present disclosure, the through silicon via penetrating the bonded multiple layers of wafer or die may be a one piece structure formed integrally.

[0021] In an exemplary embodiment of the present disclosure, the through silicon via penetrating the bonded multiple layers of wafer or die may comprise no bumps among the bonded multiple layers of wafer or die.

[0022] In an exemplary embodiment of the present disclosure, a difference between a diameter of the through silicon via and a space between the adjacent metal wires may be within a preset safe range.

[0023] In an exemplary embodiment of the present disclosure, the diameter of the through silicon via is consistent in each of the bonded plurality of layers of wafer or die.

[0024] In an exemplary embodiment of the present disclosure, a dielectric isolation layer may be disposed on an inner surface of the through silicon via, and the dielectric isolation layer may expose end surfaces of the plurality of metal wires.

[0025] In an exemplary embodiment of the present disclosure, a seed metal may be sputtered on the dielectric isolation layer and the exposed end surfaces of the plurality of metal wires, and the seed metal may comprise tantalum or copper.

[0026] In an exemplary embodiment of the present disclosure, the through silicon via may be filled with a conductive metal, and the conductive metal may comprise copper.

[0027] A third aspect of the present disclosure may direct to a semiconductor structure including the semiconductor interconnect structure disclosed above and fabricated by the method disclosed above.

[0028] A method for fabricating a semiconductor interconnect structure provided by an embodiment of the present disclosure forms a blind hole penetrating a stacked structure for a bonded wafer or die and expands the blind hole by wet etching to expose the end faces of the wires or chips in the stacked structure. Finally, the conductive material is filled in the blind hole to form the TSV connecting the leads, and the interconnect structure connecting the wires in each wafer or die can be fabricated by one etching process, thereby avoiding the use of bumps in the related art to realize the electrical connection between the chips. The process is complicated and the connection yield is low.

[0029] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive to this present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] The accompanying drawings, which are incorporated in and constitute a part of the present disclosure, illustrate embodiments consistent with the present disclosure and, together with the description, serve to explain the principles disclosed in the present disclosure. It is apparent that these drawings present only some embodiments of the present disclosure and those of ordinary skill in the art may obtain drawings of other embodiments from the accompanying drawings without exerting any creative effort.

[0031] FIG. 1 is a flow chart of a method for fabricating a semiconductor interconnection structure in an embodiment of the present disclosure.

[0032] FIG. 2 is a schematic diagram of the structure in step S102 in an embodiment of the present disclosure.

[0033] FIG. 3 is a schematic diagram of the structure in step S104 in an embodiment of the present disclosure.

[0034] FIGs. 4A, 4B, 4C, and 4D are schematic diagrams of the structures in step S106 in an embodiment of the present disclosure.

[0035] FIGs. 5A, 5B, 5C, 5D, 5E, 5F, and 5G are schematic diagrams of the structures in step S108 in an embodiment of the present disclosure.

[0036] FIGs. 6A and 6B are schematic diagrams of the structures in step S110 in an embodiment of the present disclosure.

[0037] FIG. 7 is a schematic diagram of a semiconductor interconnect structure according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0038] Exemplary embodiments will now be described more fully with reference to the accompanying drawings. However, these exemplary embodiments can be implemented in many forms and should not be construed as being limited to those set forth herein. Rather, these embodiments are presented to provide a full and thorough understanding of the present disclosure and to fully convey the concepts of the embodiments to others skilled in the art. In addition, the described features, structures, and characteristics may be combined in any suitable manner in one or more embodiments. In the following detailed description, many specific details are set forth to provide a more thorough understanding of the present disclosure. However, those skilled in the art will recognize that the various embodiments can be practiced without one or more of the specific details or with other methods, components, materials, or the like. In some instances, well-known

structures, materials, or operations are not shown or not described in detail to avoid obscuring aspects of the embodiments.

[0039] Further, the annexed drawings are merely illustrative to the present disclosure and are not necessarily drawn to scale. Throughout the figures, like reference numbers indicate identical or similar elements, so any duplicate description of them will be omitted. The represented blocks in the figures are purely functional entities, which do not necessarily correspond to physically separate entities. In other words, these functional entities may be implemented as software, or entirely or partially in one or more software-hardened modules, or in different networks and/or processor devices and/or microcontroller devices.

[0040] The embodiments of the present disclosure will be described in detail below with reference to the accompanying drawings.

[0041] FIG. 1 shows a flow chart of a method for fabricating a semiconductor interconnection structure in an embodiment of the present disclosure. Referring to FIG. 1, the method 100 can include the following steps.

[0042] In Step S102, a stacked structure including bonded multiple layers of wafer or die is provided. A wiring layer, such as a redistribution layer (RDL), may be disposed on an upper surface of each layer of the wafer or die, and the wiring layer may include a plurality of metal wires.

[0043] In Step S104, in the stacked structure, a first blind hole having a first diameter and a first length may be formed vertically, and the position for the first blind hole penetrating each layer of the wafer or die may be located between the metal wires. The first diameter is less than a space between the adjacent metal wires.

[0044] In Step S106, a second blind hole having a second diameter and the first length may be formed coaxially with the first blind hole, so that end surfaces of some of the plurality of metal

wires may be exposed from the sidewall of the second blind hole. The second diameter is greater than the space between the metal wires.

[0045] In Step S108, a conductive material may be filled in the second blind hole.

[0046] The method for fabricating a semiconductor interconnect structure provided by an embodiment of the present disclosure may form a blind hole penetrating the stacked structure having bonded layers of wafers or chips, and expand the blind hole by wet etching to expose the end surfaces of the metal wires in layers of wafer or the chip of the stacked structures. The blind hole then is filled with the conductive material to form the TSV connecting the metal wires of different layers. The interconnect structure connecting the metal wires in each layer of wafer or the chip can be fabricated by one single etching process, thereby avoiding bumps used in the inter-chip electrical connection in the related art. The problems of a complicated process and low connection yield caused by the inter-chip electrical connection with bumps can be prevented and the cost and time for manufacturing the 3D integrated circuit can be reduced.

[0047] Each step of the method 100 will be described in detail.

[0048] FIG. 2 is a schematic diagram of a stacked structure 200 provided in Step S102. It can be understood that the process of fabricating the stacked structure 200 (for example, bonding each wafer or die) may be conducted before Step S102, which is not described herein.

[0049] Referring to FIG. 2, the stacked structure 200 may include a wafer stacked structure or a chip stacked structure. A wafer stacked structure may be preferred in some of the embodiments of the present disclosure. Each layer of the wafer or die in the stacked structure 200 may include a substrate A and a wiring layer B. The wiring layer B includes a plurality of metal wires 21. In the embodiments of the present disclosure, a TSV may be formed for connecting the metal wires 21 at the corresponding positions of each layer, so as to electrically connect the layers of wafer or die.

As shown in FIG. 2, each wafer or die may be bonded directly, avoiding the cumbersome process of forming TSVs and bumps in the related art.

[0050] FIG. 3 is a schematic diagram of the first blind hole H1 having the first diameter D1 and the first length L1 vertically formed in the stacked structure 200 in step S104. Referring to FIG. 3, the penetration position of the first blind hole H1 in each layer of the wafer or die is located between the adjacent metal wires, and the first diameter D1 is smaller than the space DL between the adjacent metal wires. The first length L1 is shorter than the height L2 of the stacked structure. The first diameter D1 may be determined according to the space DL between the adjacent metal wires as long as the difference between D1 and DL is greater than a preset safety distance to avoid etching to the metal wires.

[0051] When a plurality of interconnect structures need to be fabricated, a plurality of first blind holes H1 can be fabricated in the stacked structure 200. The first blind hole can be formed by, for example, a process including gluing, photolithography, development, etching, etc., and the present disclosure is not particularly limited to.

[0052] As shown in FIG. 4A and FIG. 4B, in Step S106, a second blind hole H2 having a second diameter D2 and the first length L1 is formed coaxially with the first blind hole H1, such that the sidewall of the second blind hole H2 exposes the end surfaces of the metal wires 21. Wherein, the second diameter D2 is larger than the space DL of the metal wires.

[0053] Referring to FIG. 4A, first, the portion of the first blind hole H1 located in the substrate A of each layer of wafer or die may be widened to the second diameter D2 by a first wet etching process. The first wet etching process may be performed, for example, by injecting a first predetermined dose of the first etching solution into the first blind hole H1 to etch the substrate A by an etching width of D2-D1, and the type and the dose of the first etching solution may be determined according to the type of the substrate and the etching width.

[0054] Referring to FIG. 4B, on the basis of the process shown in FIG. 4A, the portion of the first blind hole located in the wiring layer B of each layer of wafer or die is expanded to the second diameter D2 by a second wet etching process to expose the end surfaces of the metal wires 21 to form the second blind hole H2. The second wet etching process is performed, for example, by injecting a second predetermined amount of the second etching solution into the first blind hole H1 to etch the dielectric portion of the wiring layer B by the etching width of D2-D1. The type and the dose of the second etching solution may be determined according to the type of the dielectric portion and the etching width, and the dielectric portion may be, for example, SiO2 or Si3N4.

[0055] As shown in FIGS. 4A and 4B, the second diameter D2 may be determined according to the space DL between the metal wires as long as the difference between D2 and DL is within a preset range and the end surfaces of the metal wires 21 are exposed.

[0056] FIGS. 4C and 4D are cross-sectional top views of the first blind hole H1 and the second blind hole H2 in the processes shown in FIGS. 4A and 4B. Referring to Fig. 4C, in the process shown in FIG. 4A, the diameter of the blind hole in the substrate A is increased from D1 to D2. Referring to FIG. 4D, in the process shown in FIG. 4B, after the blind hole diameter is enlarged, the dielectric portion of the wiring layer B is etched off to expose the end surfaces of the metal wires 21. Although FIG. 4C and FIG. 4D are examples in which the cross-sectional top views of the first blind hole H1 and the second blind hole H2 are in circular shapes, in other embodiments of the present disclosure, the cross-sectional top views of the first blind hole and the second blind hole may have other shapes including a polygon, an irregularity, a parallelogram (diamond or square), and rounded quadrilateral, etc., which are not particularly limited in the present disclosure.

[0057] FIGS. 5A, 5B, 5C, 5D, 5E, 5F, and 5G are schematic diagrams of the second blind hole filled with conductive materials in Step S108.

[0058] In Fig. 5A, a dielectric isolation layer 22 may be formed on the inner surface of the second blind hole before filling a conductive material in the second blind hole. The process of fabricating the dielectric isolation layer 22 may be, for example, depositing SiCN on the surface of the etched surfaces of the second blind hole by a chemical vapor deposition process, such that the dielectric isolation layer 22 covers the inner surfaces of the one or more second blind holes H2 and the top surface of the stacked structure 200. In some embodiments, the materials of the dielectric isolation layer may also include insulating materials of an outer layer, which include, but not limited to, tantalum, tantalum nitride, silicon oxycarbide, silicon carbide, silicon nitride, and the like.

[0059] In FIG. 5B, the dielectric isolation layer 22 of FIG. 5A is etched to expose the end surfaces of the metal wires 21 within the second blind hole and the bottom of the second blind hole.

[0060] FIG. 5C is an enlarged view of the structure shown in FIG. 5B. Referring to FIG. 5C, the dielectric isolation layer 22 on the metal wires can be etched by a plasma dry etching process to expose the end surfaces and/or partial upper surfaces of the metal wires 21 and the bottom of the second blind hole H1 (i.e., the portion of the bottom visible in the cross-sectional top view). At this time, the positions of the metal wires in the cross-sectional top view of the second blind hole are the same as those in FIG. 4B, such that the dielectric isolation layer on the lower surfaces of the metal wires cannot be seen.

[0061] FIG. 5D is an illustration of a seed metal 23 sputtered on the inner sidewall and bottom of the second blind hole. The seed metals may include, for example, copper. FIG. 5E is an enlarged view of the structure shown in FIG. 5D. Referring to FIG. 5E, the seed metal 23 may be sputtered on positions including the sidewall of the second blind hole, upper surfaces and side surfaces of the exposed metal wires, and the bottom of the second blind hole, so that the subsequently filled

copper may be connected with the metal wires via the tantalum or copper disposed on the metal wires.

[0062] FIG. 5F is an illustration of a conductive metal grown in the second blind hole. The second blind hole may be filled with the conductive metal on the surfaces of the seed metal 23, and the top surface of the conductive metal is aligned with the top surface of the wiring layer B to form the TSVs. The conductive metal may include, for example, copper or tungsten, and the process of growing the metal may be, for example, electroplating.

[0063] FIG. 5G is a cross-sectional top view of the structure shown in FIG. 5F.

[0064] FIG. 6A and 6B are schematic diagrams showing the structure in Step S110 of the method in one embodiment of the present disclosure.

[0065] As shown in FIG. 6A, Step S110 may include grinding the bottom layer of the stacked structure to expose the metal filled on the bottom of the second blind hole. A bump 24 is formed on the exposed surface of the metal as shown in Fig. 6B. The process disclosed in the present disclosure may fabricate the structures that can interconnect with other stacked structures.

[0066] Through the above process, the TSVs may be formed in a simple process and electrically connect the metal wires among layers of wafer or die. This can overcome the shortcomings of electrical connections through bumps in the related art, such as complicated process, high cost, and low yield, and can improve the manufacturing efficiency of the 3D integrated circuit.

[0067] FIG. 7 is a schematic diagram of a semiconductor interconnect structure according to an embodiment of the present disclosure.

[0068] Referring to FIG. 7, the semiconductor interconnect structure 700 may include a stacked structure 71. The stacked structure 71 may include bonded multiple layers of wafer or die. Each layer of wafer or die may include a substrate and a wiring layer, and the wiring layer may include a plurality of metal wires 72.

[0069] The semiconductor interconnect structure 700 may include TSVs penetrating through the stacked structure 71, and the centers of the penetrating positions on each layer of wafer or die may be located between the adjacent metal wires 72. The sidewalls of the TSVs may intersect with the metal wires 72, and the end surfaces of the metal wires 72 may extend into the TSVs. The TSVs may be fabricated by the method for fabricating a semiconductor interconnection structure disclosed above referring to FIGs. 2 to 5F. The main body of the TSV may include metals such as copper and tungsten, and the outer insulating material may include tantalum, tantalum nitride, silicon carbonitride, silicon oxycarbide, silicon carbide, silicon nitride, etc. The cross-sectional top views of the TSVs may be, but not limited to, shapes of a circle, a quadrangle (square, rectangle, parallelogram, diamond), a polygon, and other irregular shapes including a jagged shape.

[0070] The semiconductor interconnect structure disclosed in the embodiments of the present disclosure does not have bumps between the layers of chip, and the structure among the multiple layers of chips can be fabricated by one single TSV process, thereby avoiding the problems caused by the inter-chip electrical connections with bumps in the related art, such as misalignments and connection defects, and improving the efficiency and yield of manufacturing 3D integrated circuits.

[0071] Further, the annexed figures are merely illustrative of a series of processes included in the method according to embodiments of the present disclosure and are not limiting. It will be appreciated that the way in which the processes are illustrated does not indicate any chronological order of them or limit them to a particular chronological order. Furthermore, it will also be appreciated that the processes may be performed, for example, synchronously or asynchronously in multiple modules.

[0072] Other embodiments of the present disclosure will be apparent to those skilled in the art from considering the specification and practicing the invention disclosed herein. Accordingly, this present disclosure covers all and any variations, uses, or adaptations of the present disclosure

which follow, in general, the principles thereof and include any departures from the present disclosure as come within common knowledge or customary practice within the art to which the present disclosure pertains. The specification and examples are exemplary only, and the true scope and spirit of the present disclosure are indicated by the appended claims.

CLAIMS

1. A method for fabricating a semiconductor interconnect structure, comprising:

providing a stacked structure comprising bonded a plurality of layers of wafer or die , wherein each layer of wafer or die comprises a substrate and a wiring layer, and the wiring layer comprises a plurality of metal wires;

vertically forming, in the stacked structure, a first blind hole having a first diameter and a first length, wherein a penetration position of the first blind hole in each layer of wafer or die is between adjacent metal wires, the first diameter is less than a space between the adjacent metal wires, and the first length is less than a height of the stacked structure;

forming a second blind hole having a second diameter and the first length coaxially with the first blind hole, wherein a sidewall of the second blind hole exposes end surfaces of the plurality of metal wires, and the second diameter is larger than the space between the adjacent metal wires; and

filling a conductive material in the second blind hole.

2. The method of claim 1, wherein forming the second blind hole having the second diameter and the first length coaxially with the first blind hole comprises:

widening a portion of the first blind hole in the substrate of each layer of wafer or die to the second diameter by a first wet etch process; and

extending, by a second wet etching process, a portion of the first blind hole in the wiring layer of each layer of wafer or die to the second diameter to expose the end surfaces of the plurality of metal wires to form the second blind hole.

3. The method of claim 2, wherein filling the conductive material in the second blind hole comprises:

forming a dielectric isolation layer on an inner surface of the second blind hole; and

etching the dielectric isolation layer to expose the end surfaces of the plurality of metal wires and a bottom of the second blind hole.

4. The method of claim 3, wherein forming the dielectric isolation layer comprises depositing SiCN on the inner surface of the second blind hole by a chemical vapor deposition process.

5. The method of claim 3, wherein etching the dielectric isolation layer to expose the end surfaces of the plurality of metal wires and the bottom of the second blind hole comprises:

etching, by a plasma dry etch process, portions of the dielectric isolation layer on the end surfaces and upper surfaces of the plurality of metal wires to expose the plurality of metal wires, and etching a portion of the dielectric isolation layer at the bottom of the second blind hole to expose the bottom of the second blind hole.

6. The method of claim 5, wherein filling the conductive material in the second blind hole comprises:

sputtering a seed metal on the etched dielectric isolation layer and the exposed end surfaces of the plurality of metal wires and the bottom of the second blind hole, wherein the seed metal comprises tantalum or copper; and

growing the conductive metal in the second blind holes sputtered with the seed metal, the conductive metal comprises copper.

7. The method of claim 1, further comprising:

grinding a bottom layer of the stacked structure to expose a metal filled at a bottom of the second blind hole; and

forming a bump on a surface of the exposed metal.

8. The method of claim 1, wherein each of the first blind hole and the second blind hole has a cross-sectional top view of a circle shape, a polygon shape, and an irregular shape.

9. The method of claim 1, wherein the plurality of layers of wafer or die are directly bonded, wherein a substrate of a top layer is directly disposed on a wiring layer of a lower layer.

10. The method of claim 1, wherein

a difference between the first diameter and the space between the adjacent metal wires is within a first preset safe range, and

a difference between the second diameter and the space between the adjacent metal wires is within a second preset safe range.

11. A semiconductor interconnect structure, comprising:

a stacked structure comprising bonded a plurality of layers of wafer or die, each layer of wafer or die comprising a substrate and a wiring layer, and the wiring layer comprising a plurality of metal wires; and

at least a through silicon via (TSV) penetrating the bonded plurality of layers of wafer or die of the stacked structure, a center of a penetration position on each layer of wafer or die being located between adjacent metal wires, and a sidewall of the through silicon via intersecting with the plurality of metal wires,

wherein the through silicon via penetrating the bonded plurality of layers of wafer or die of the stacked structure is fabricated by a process including one single etching process.

12. The semiconductor interconnect structure of claim 11, wherein the through silicon via has a cross-sectional top view of a circle shape, a polygon shape, or an irregular shape.

13. The semiconductor interconnect structure of claim 11, wherein the through silicon via penetrating the bonded plurality of layers of wafer or die is a one piece structure formed integrally.

14. The semiconductor interconnect structure of claim 11, wherein the through silicon via penetrating the bonded plurality of layers of wafer or die comprises no bumps among the bonded plurality of layers of wafer or die.

15. The semiconductor interconnect structure of claim 11, wherein a difference between a diameter of the through silicon via and a space between the adjacent metal wires is within a preset safe range.

16. The semiconductor interconnect structure of claim 15, wherein the diameter of the through silicon via is consistent in each of the bonded plurality of layers of wafer or die.

17. The semiconductor interconnect structure of claim 11, wherein a dielectric isolation layer is disposed on an inner surface of the through silicon via, and the dielectric isolation layer exposes end surfaces of the plurality of metal wires.

18. The semiconductor interconnect structure of claim 17, wherein a seed metal is sputtered on the dielectric isolation layer and the exposed end surfaces of the plurality of metal wires, and the seed metal comprises tantalum or copper.

19. The semiconductor interconnect structure of claim 18, wherein the through silicon via is filled with a conductive metal, and the conductive metal comprises copper.

20. A semiconductor structure, including a semiconductor interconnect structure fabricated by a method, wherein the method comprises:

providing a stacked structure comprising bonded a plurality of layers of wafer or die, wherein each layer of wafer or die comprises a substrate and a wiring layer, and the wiring layer comprises a plurality of metal wires;

vertically forming, in the stacked structure, a first blind hole having a first diameter and a first length, wherein a penetration position of the first blind hole in each layer of wafer or die is between adjacent metal wires, the first diameter is less than a space between the adjacent metal wires, and the first length is less than a height of the stacked structure;

forming a second blind hole having a second diameter and the first length coaxially with the first blind hole, wherein a sidewall of the second blind hole exposes end surfaces of the plurality of metal wires, and the second diameter is larger than the space between the adjacent metal wires; and

filling a conductive material in the second blind hole.

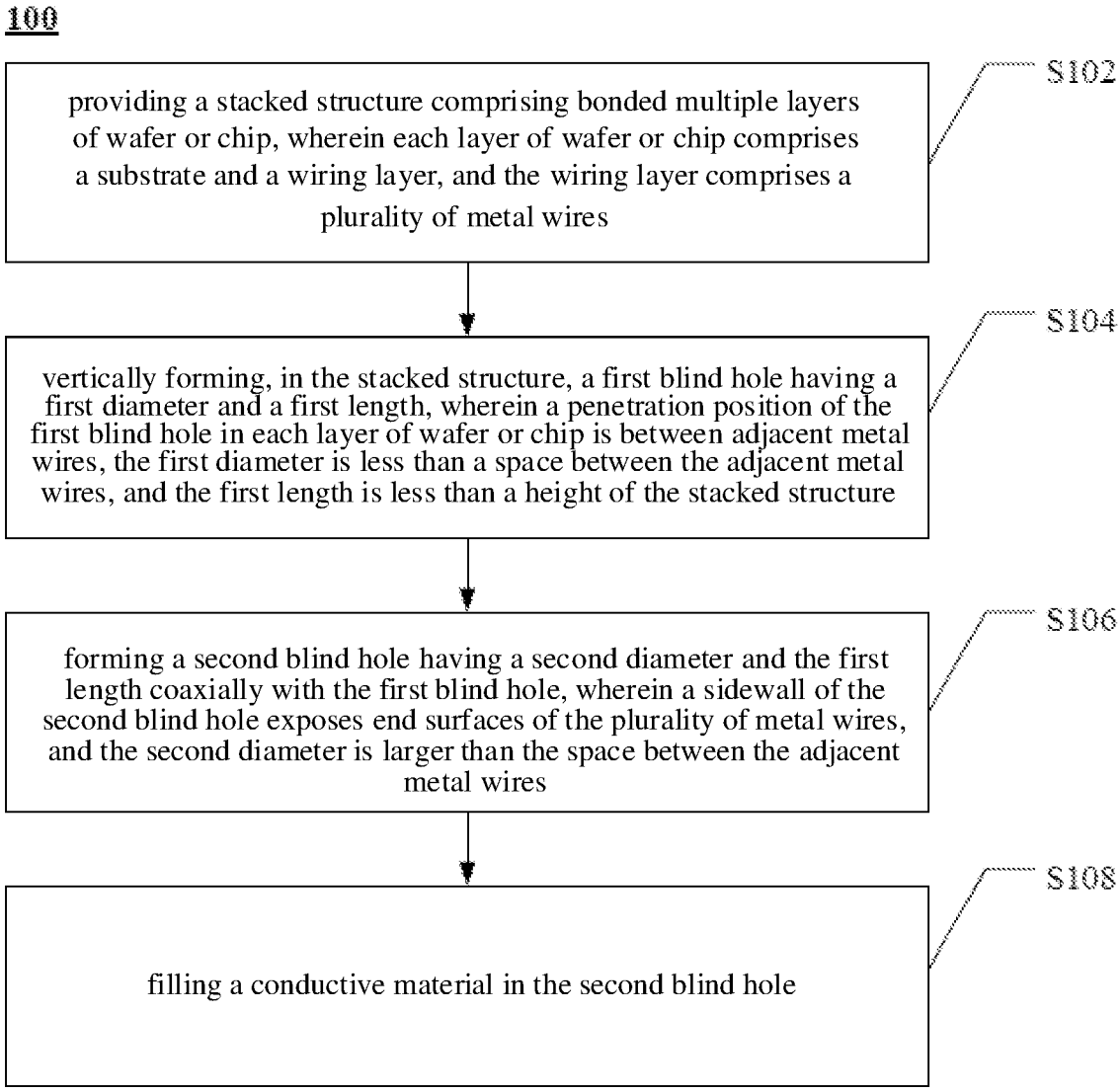
100
providing a stacked structure comprising bonded multiple layers of wafer or chip, wherein each layer of wafer or chip comprises a substrate and a wiring layer, and the wiring layer comprises a plurality of metal wires
S102
vertically forming, in the stacked structure, a first blind hole having a first diameter and a first length, wherein a penetration position of the first blind hole in each layer of wafer or chip is between adjacent metal wires, the first diameter is less than a space between the adjacent metal wires, and the first length is less than a height of the stacked structure
S104
forming a second blind hole having a second diameter and the first length coaxially with the first blind hole, wherein a sidewall of the second blind hole exposes end surfaces of the plurality of metal wires, and the second diameter is larger than the space between the adjacent metal wires
S106
filling a conductive material in the second blind hole
S108

Fig. 1

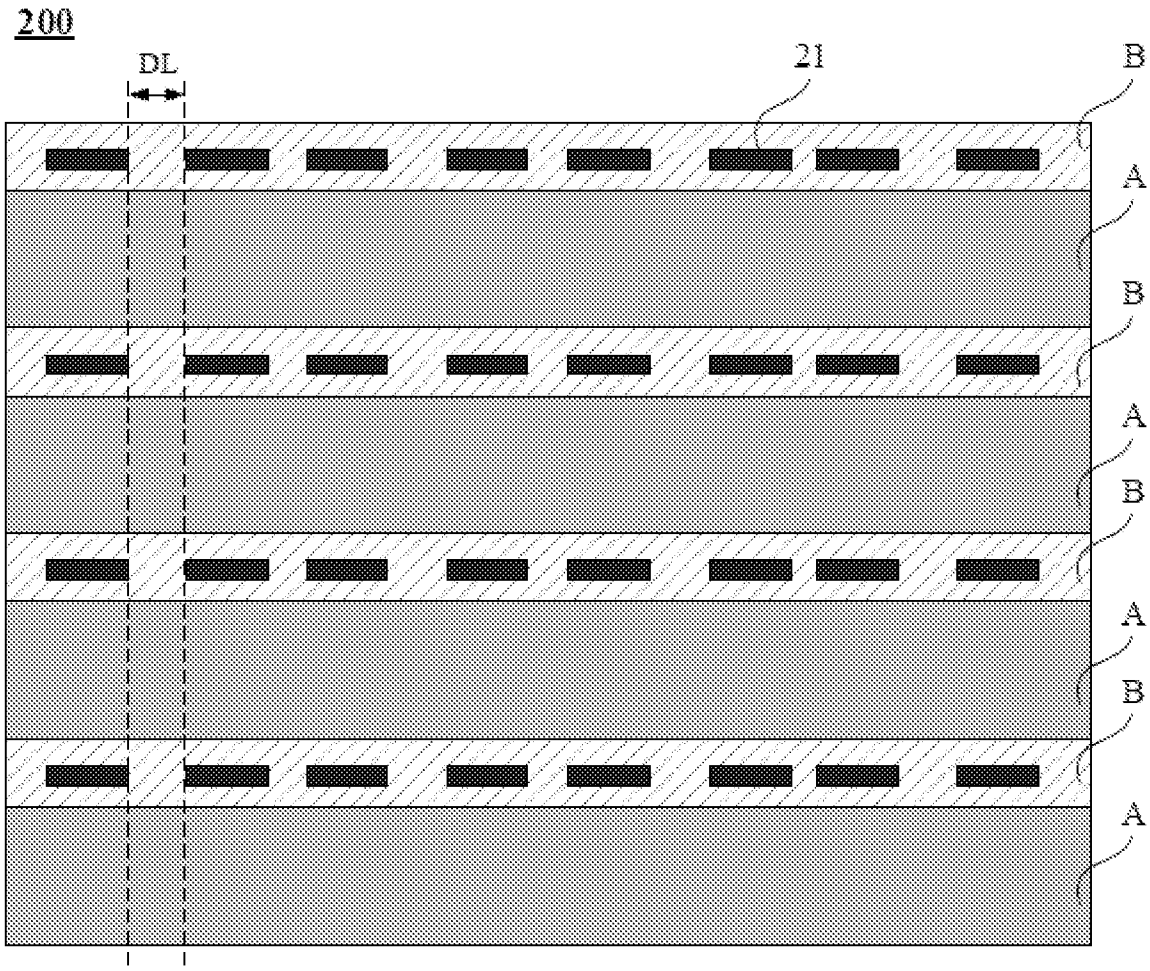

Fig. 2

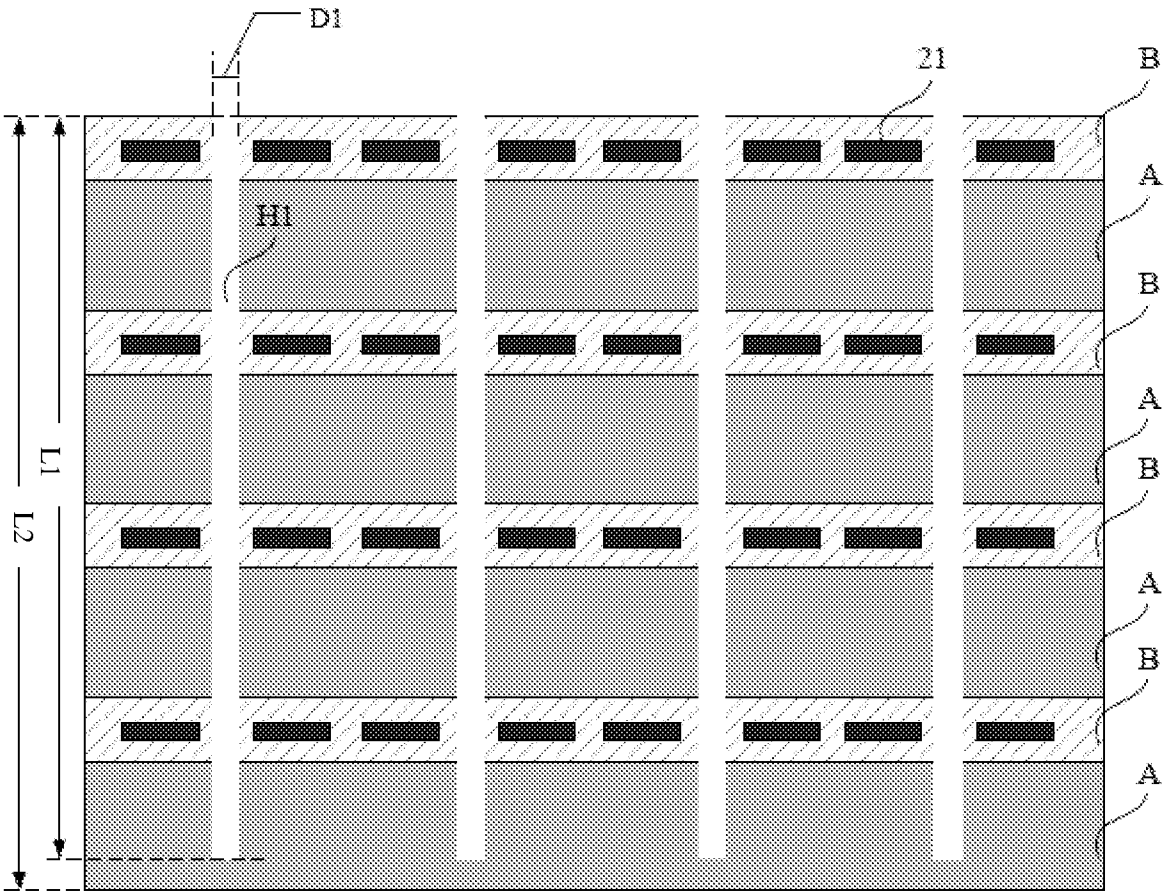

Fig. 3

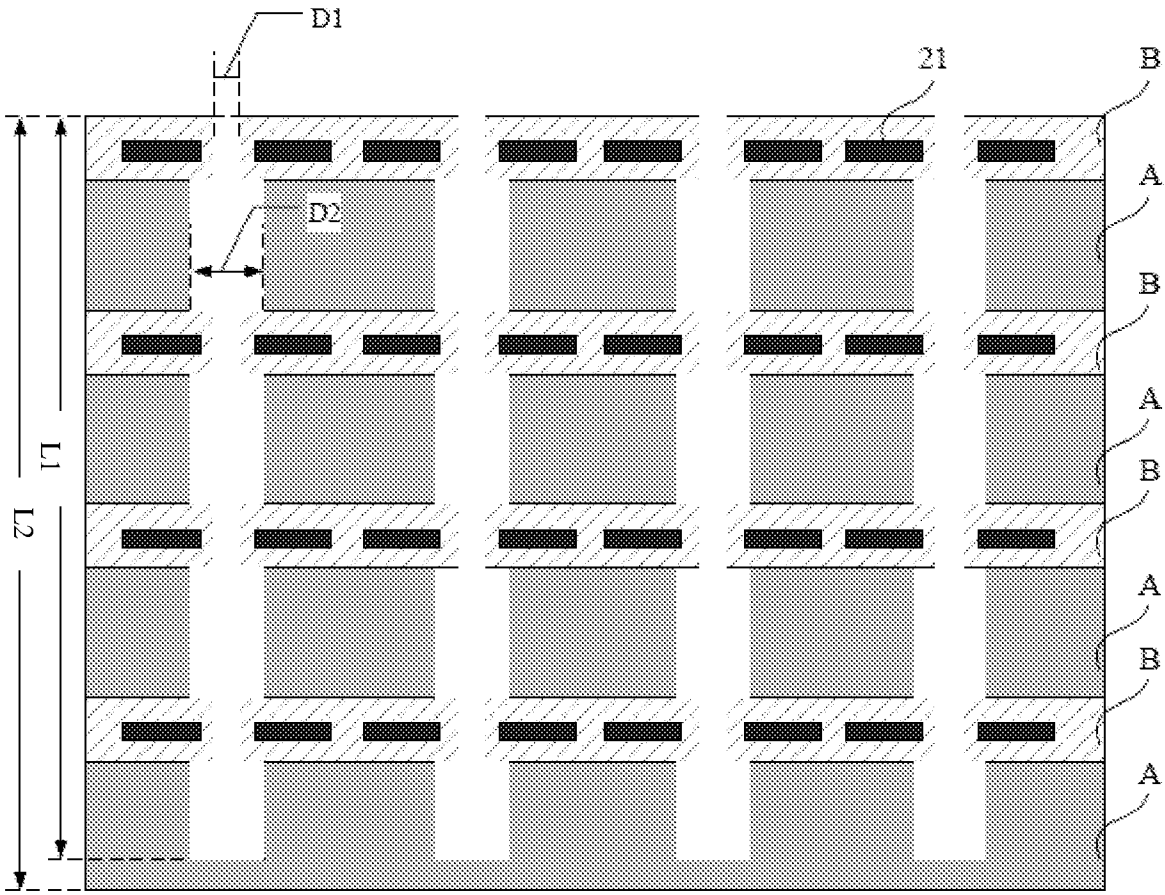

Fig. 4A

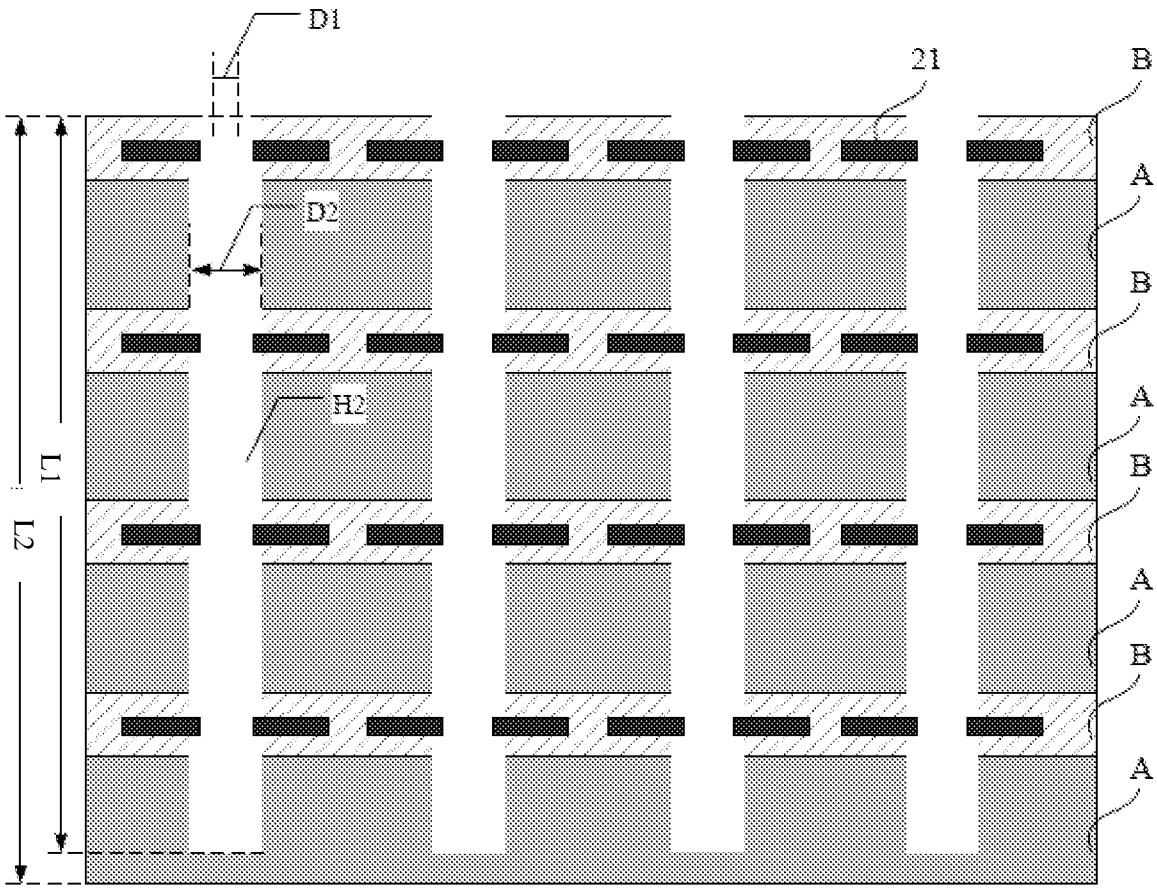

Fig. 4B

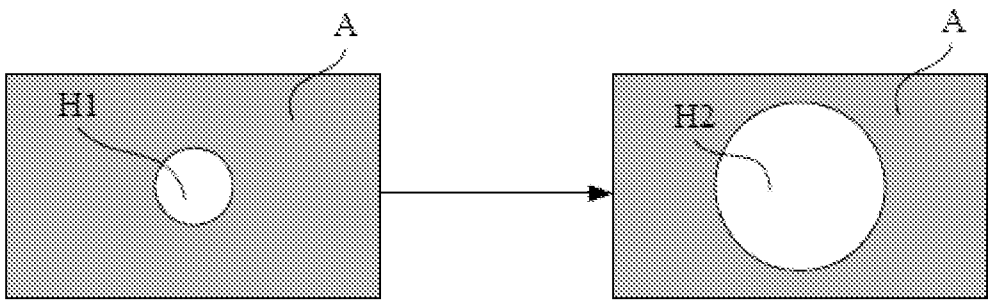

Fig. 4C

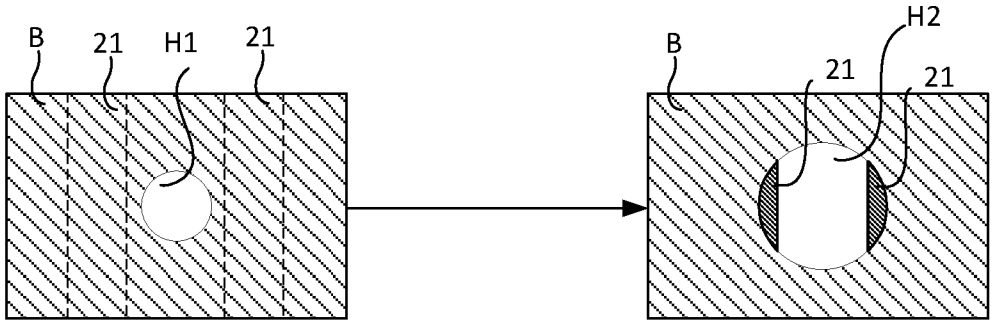

Fig. 4D

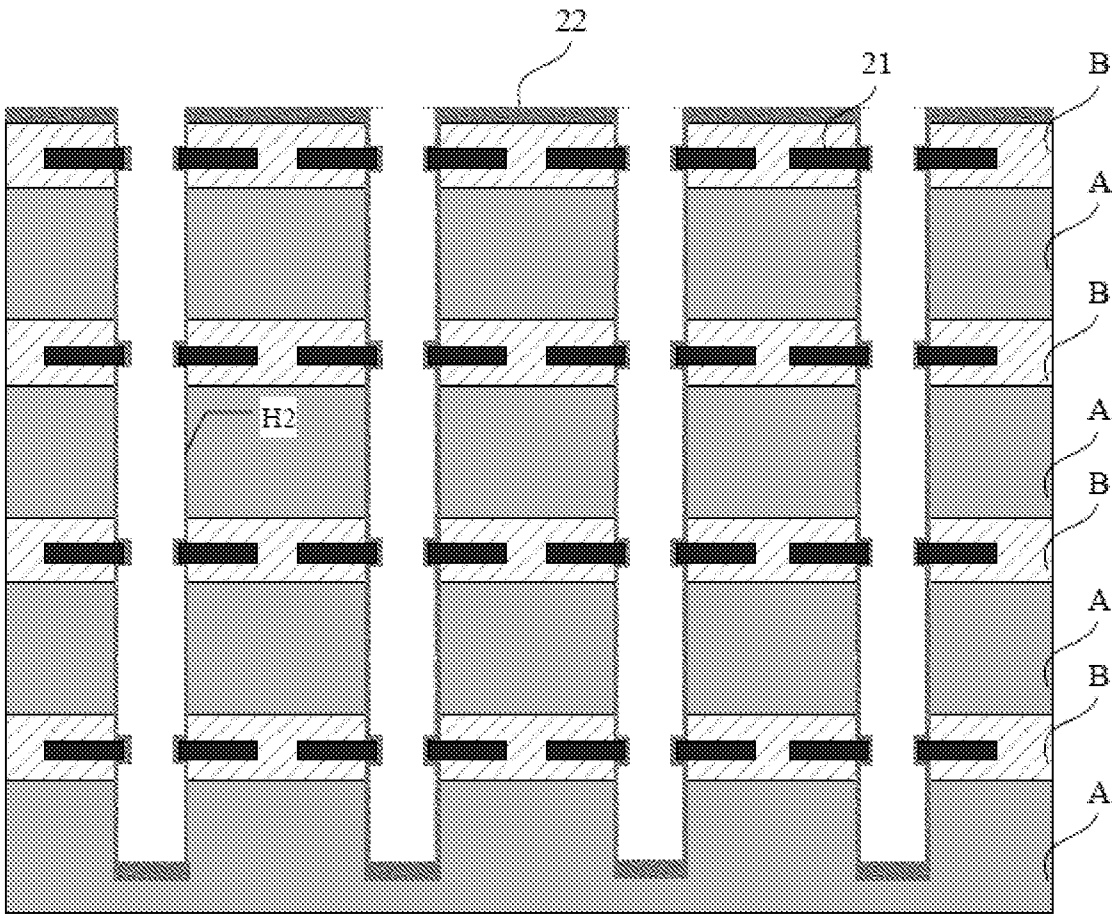

Fig. 5A

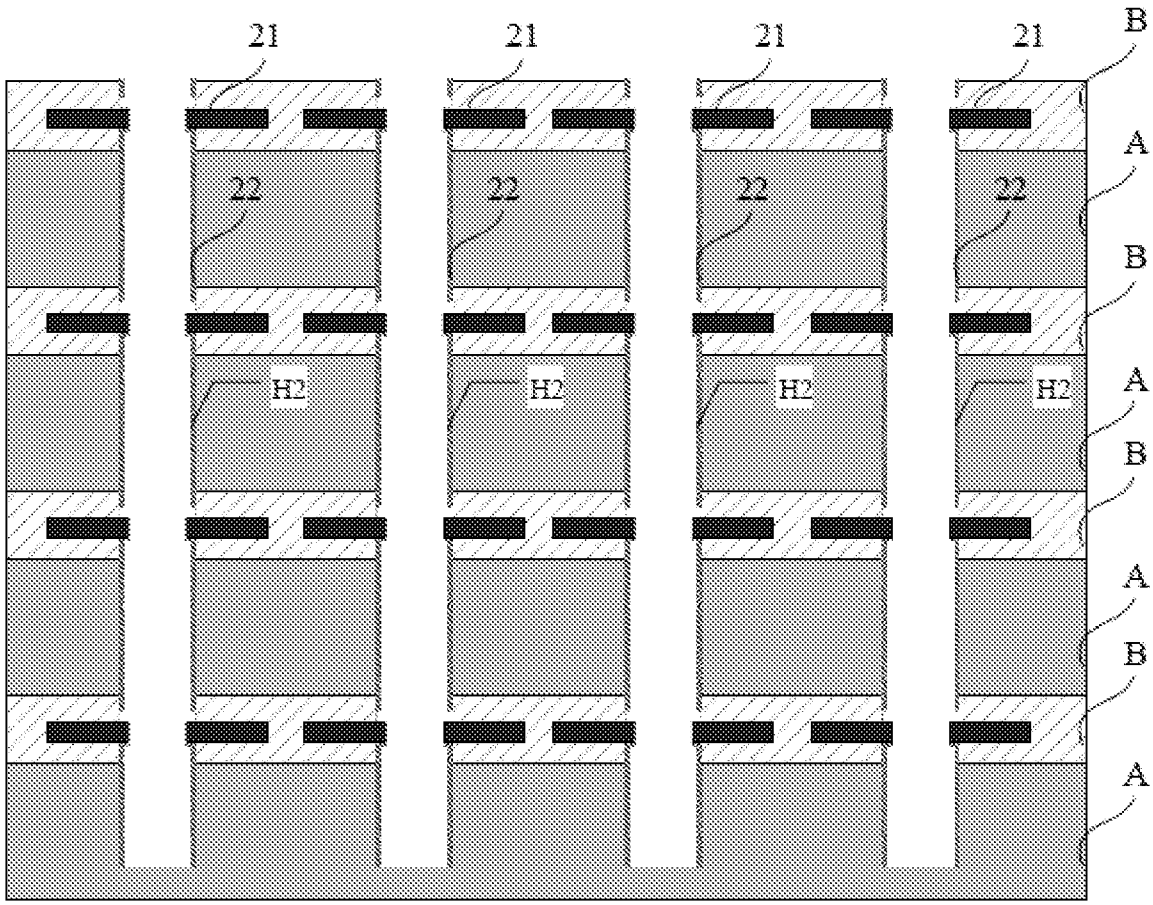

Fig. 5B

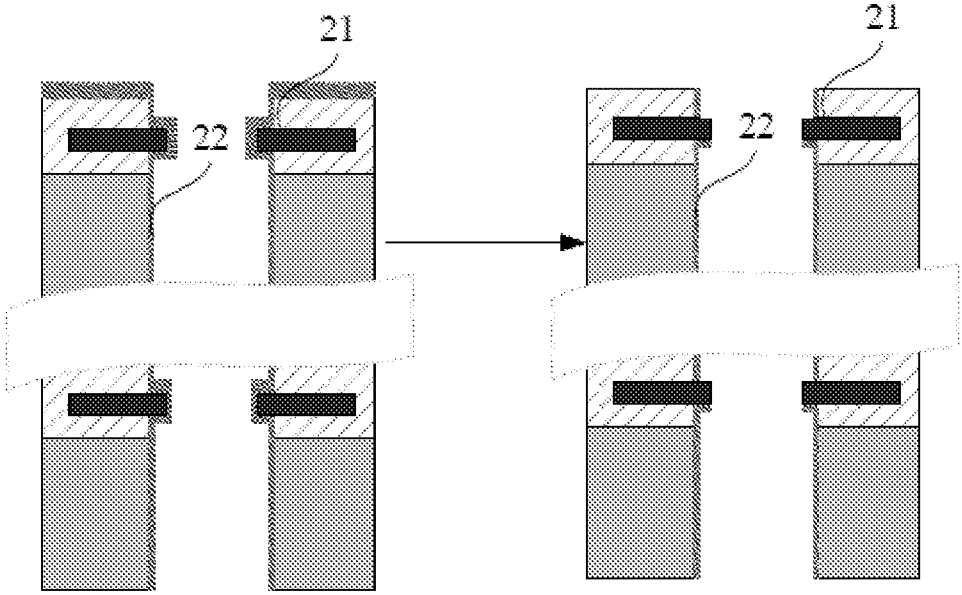

Fig. 5C

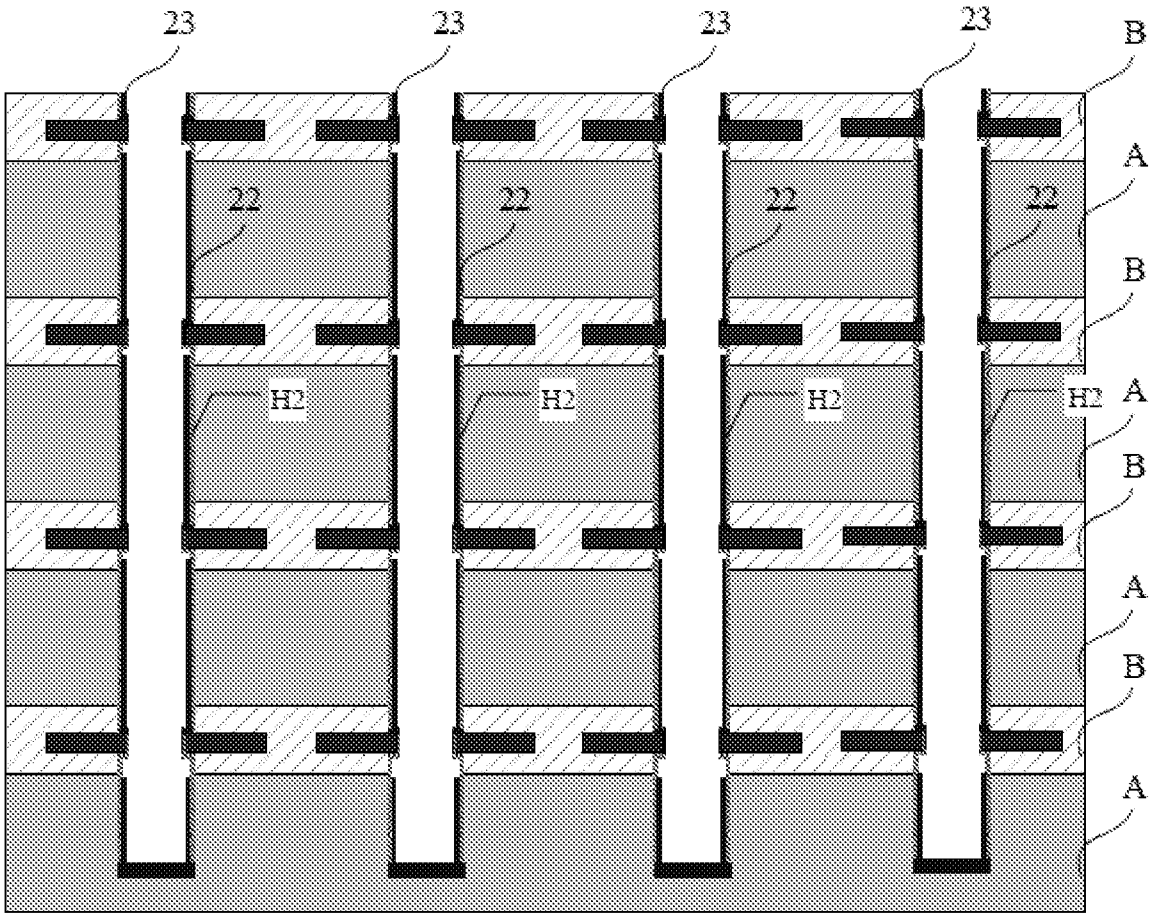

Fig. 5D

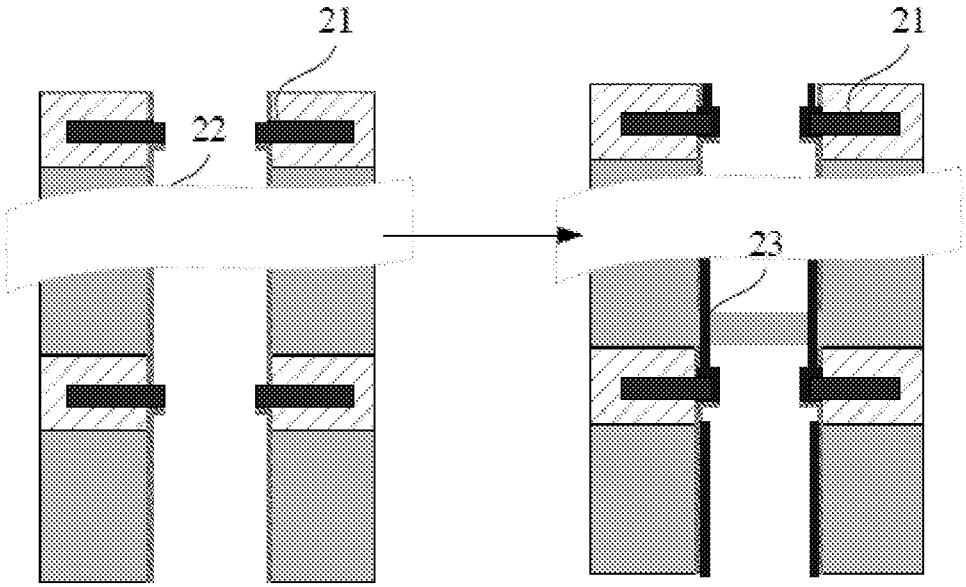

Fig. 5E

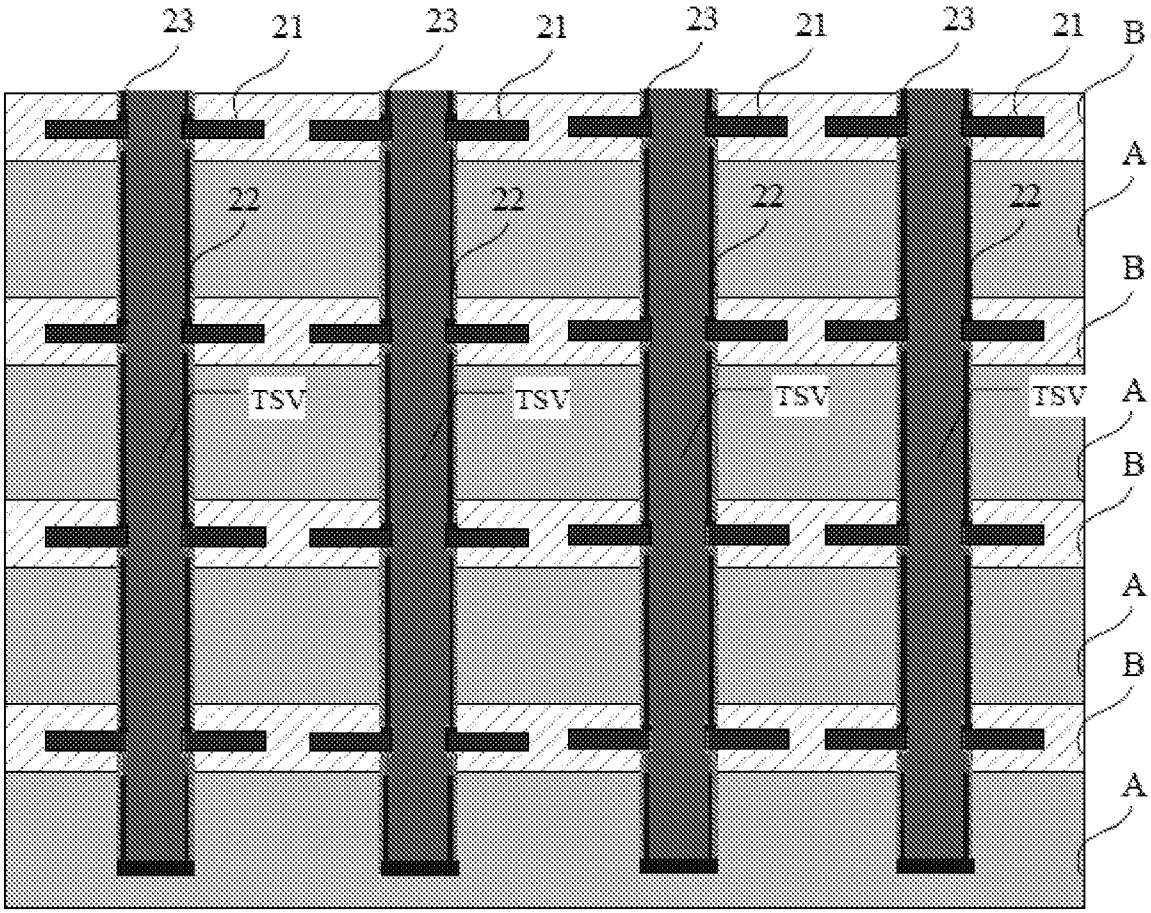
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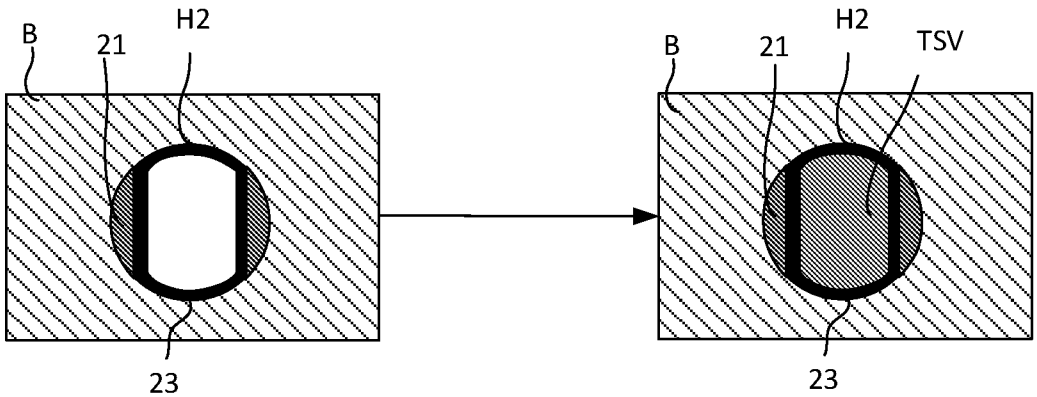
Fig. 5F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TSV
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Fig. 5G

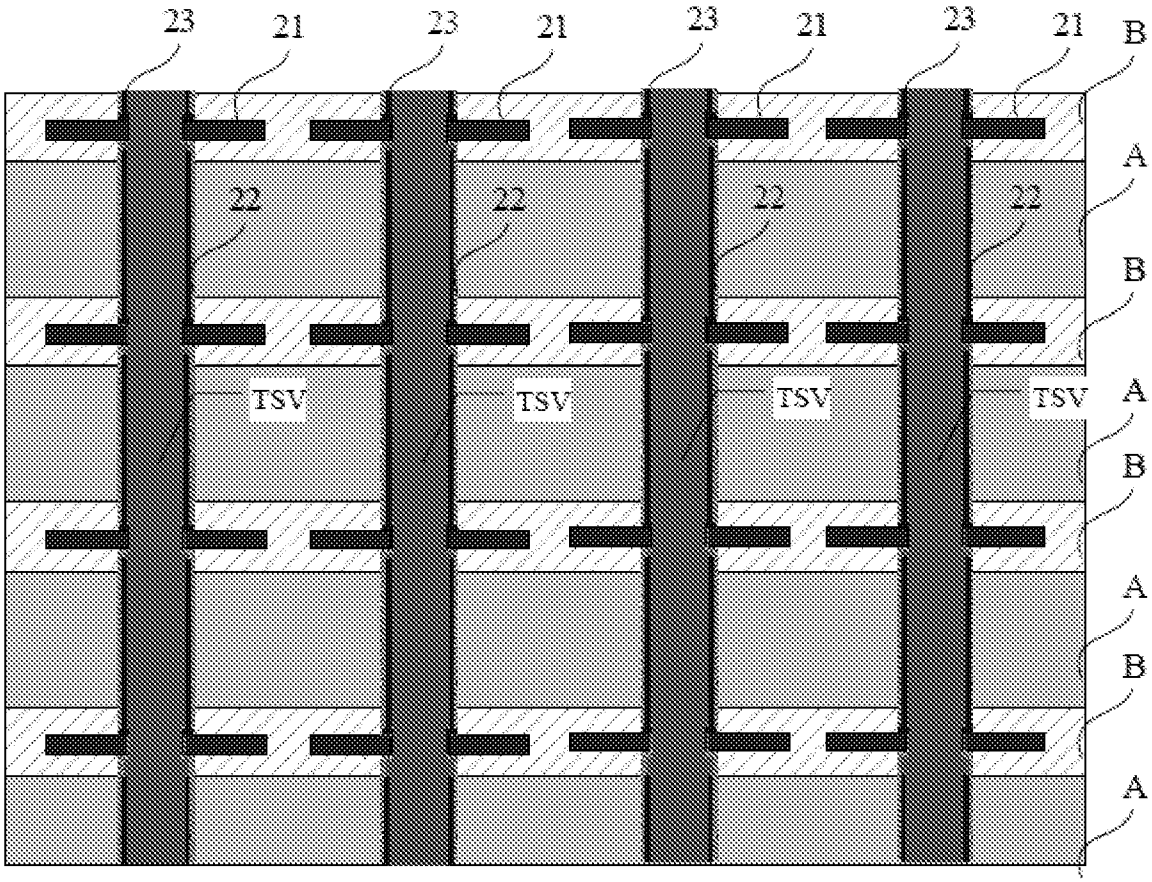

Fig. 6A

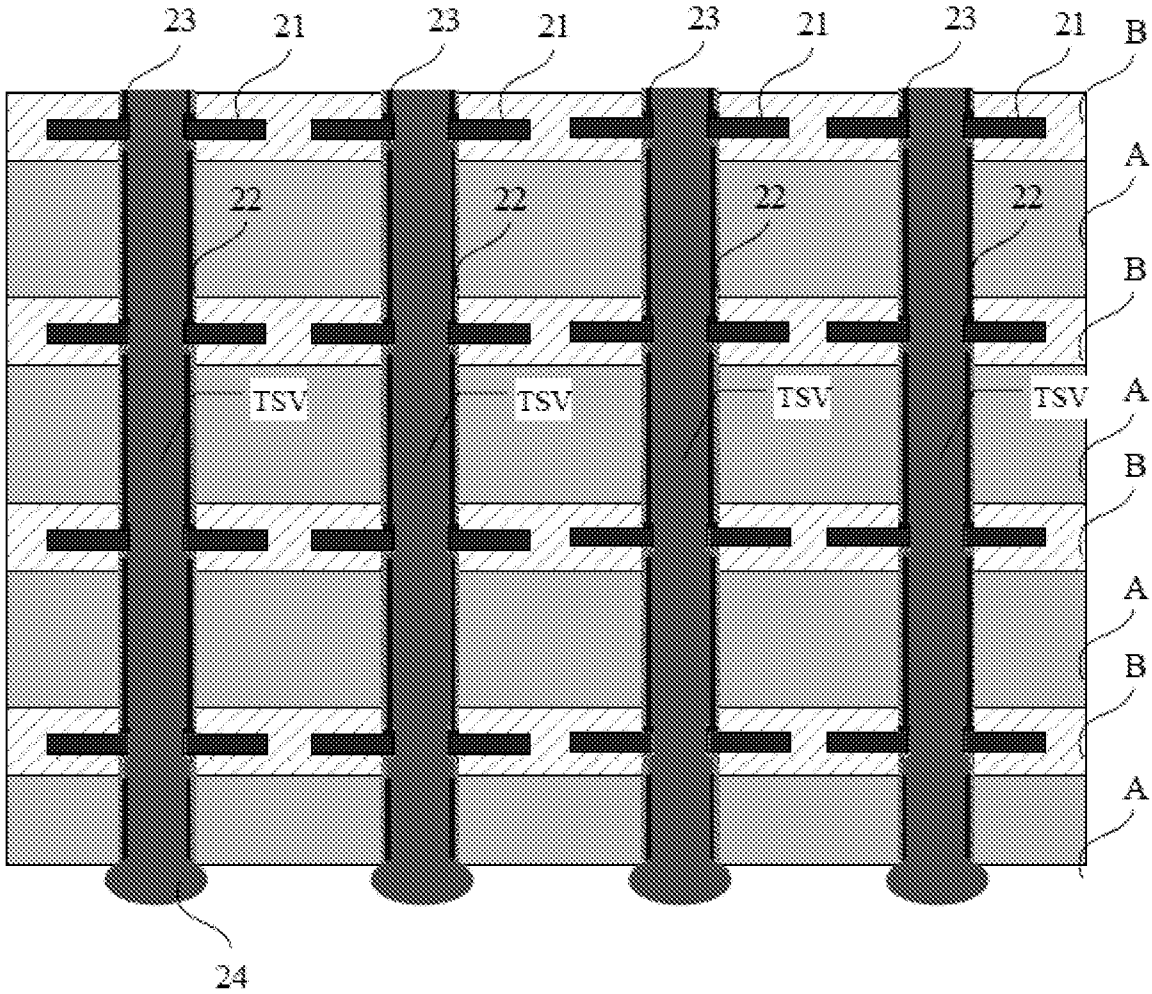

Fig. 6B

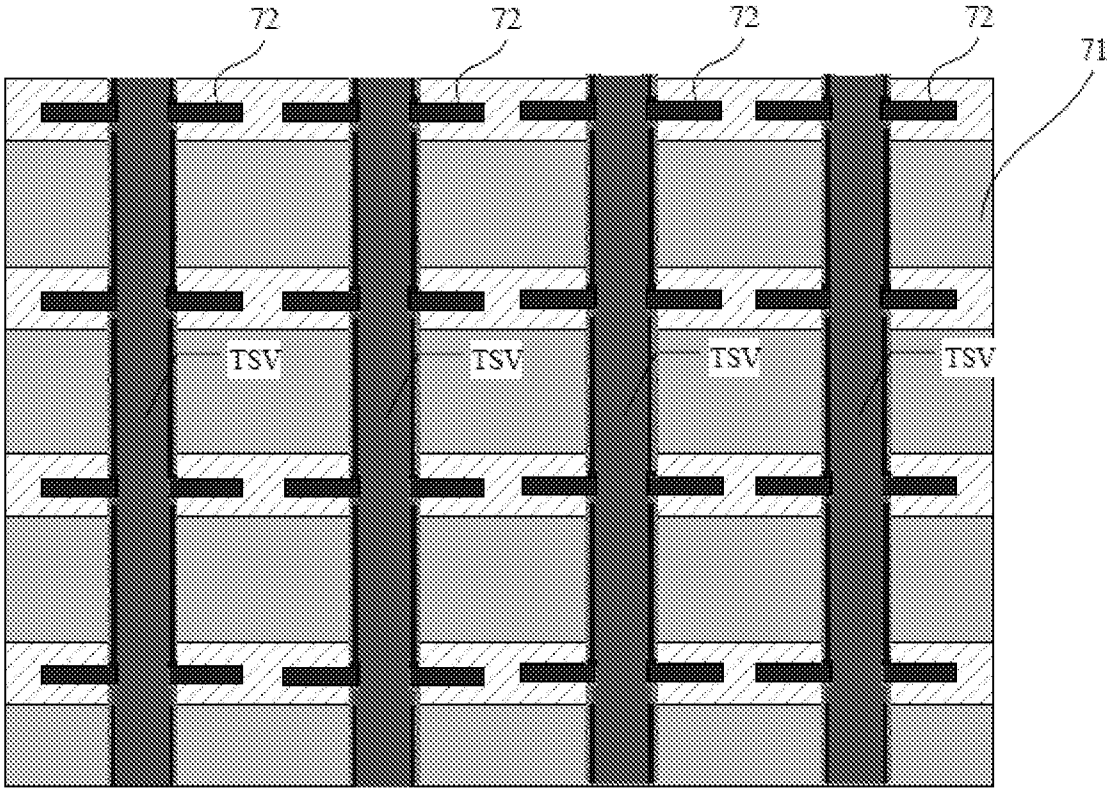

Fig. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2019/121911

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/522(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, EPODOC, CNPAT, CNKI, IEEE: via, bond, die, through silicon via, TSV, hole, throughhole, diameter, wafer, stack, wiring, wire, blind hole

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009065907 A1 (TESSERA, INC.) 12 March 2009 (2009-03-12) description, paragraphs [0043]-[0049], figures 5a and 6a	11-16
PX	CN 209045544 U (CHANGXIN MEMORY TECHNOLOGIES, INC.) 28 June 2019 (2019-06-28) description, paragraphs [0006]-[0029]	1-20
A	US 2015121693 A1 (UNIMICRON TECHNOLOGY CORP.) 07 May 2015 (2015-05-07) the whole document	1-20
A	US 9743526 B1 (INTERNATIONAL BUSINESS MACHINES CORPORATION et al.) 22 August 2017 (2017-08-22) the whole document	1-20
A	CN 101330076 A (HYNIX SEMICONDUCTOR INC.) 24 December 2008 (2008-12-24) the whole document	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 February 2020	**26 February 2020**
Name and mailing address of the ISA/CN **National Intellectual Property Administration, PRC** **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088** **China** Facsimile No. **(86-10)62019451**	Authorized officer **LI,Yong** Telephone No. **(86—10) 53961453**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
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