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(54) Title: LINE BASED IMAGE PROCESSING AND FLEXIBLE MEMORY SYSTEM

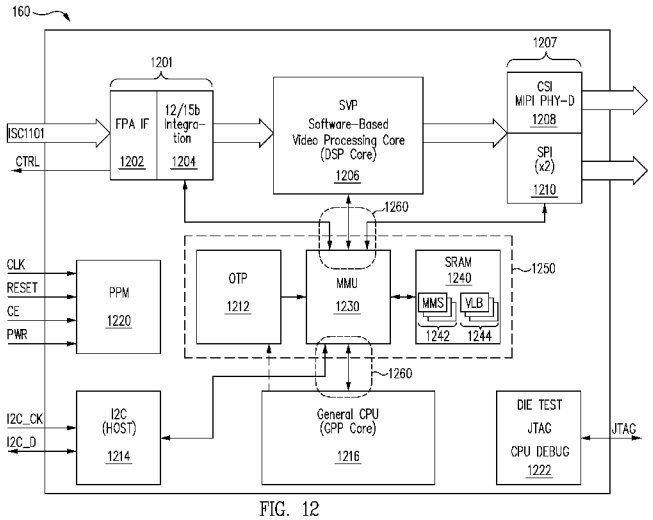

FIG. 12

(57) Abstract: Techniques are provided to implement line based processing of thermal images and a flexible memory system. In one example, individual lines of a thermal image frame may be provided to an image processing pipeline. Image processing operations may be performed on the individual lines in stages of the image processing pipeline. A memory system may be used to buffer the individual lines in the pipeline stages. In another example, a memory system may be used to send and receive data between various components without relying on a single shared bus. Data transfers may be performed between different components and different memories of the memory system using a switch fabric to route data over different buses. In another example, a memory system may support data transfers using different clocks of various components, without requiring the components and the memory system to all be synchronized to the same clock source.

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LINE BASED IMAGE PROCESSING AND FLEXIBLE MEMORY SYSTEM

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Patent Application No. 61/646,750 filed May 14, 2012 and entitled "LINE BASED IMAGE PROCESSING" which is hereby incorporated by reference in its entirety.

This application claims the benefit of U.S. Provisional Patent Application No. 61/646,732 filed May 14, 2012 and entitled "FLEXIBLE MEMORY SYSTEM" which is hereby incorporated by reference in its entirety.

This application claims the benefit of U.S. Provisional Patent Application No. 61/545,056 filed October 7, 2011 and entitled "NON-UNIFORMITY CORRECTION TECHNIQUES FOR INFRARED IMAGING DEVICES" which is hereby incorporated by reference in its entirety.

This application also claims the benefit of U.S. Provisional Patent Application No. 61/495,873 filed June 10, 2011 and entitled "INFRARED CAMERA PACKAGING SYSTEMS AND METHODS" which is hereby incorporated by reference in its entirety.

This application also claims the benefit of U.S. Provisional Patent Application No. 61/495,879 filed June 10, 2011 and entitled "INFRARED CAMERA SYSTEM ARCHITECTURES" which is hereby incorporated by reference in its entirety.

This application also claims the benefit of U.S. Provisional Patent Application No. 61/495,888 filed June 10, 2011 and entitled "INFRARED CAMERA CALIBRATION TECHNIQUES" which is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

One or more embodiments of the invention relate generally to thermal imaging devices and more particularly, for example, to the processing of thermal images.

BACKGROUND

Conventional image processing typically requires significant processing power and substantial memory resources. In this regard, a captured image (e.g., an image frame) may include a large number of pixels, each of which may have many bits or bytes of associated data. As a result, large amounts of memory may be required to store the captured image, and operations may be required to be performed on all of the many pixels to process even a single captured image. These difficulties are compounded in realtime applications where a

stream of images may need to be captured and processed without introducing significant latency or other delays.

Unfortunately, conventional frame based approaches to image processing are often problematic. For example, a powerful processor may be required to satisfactorily process an entire image. In addition, such a processor may rely on a centralized memory system to repeatedly read and write image data to a large memory block over a shared memory bus. Such approaches can lead to processing delays and bottlenecks in the use and operation of the processor and the memory system.

SUMMARY

In accordance with embodiments further described herein, various techniques are provided to implement line based processing of thermal images. In one embodiment, individual lines of a thermal image frame may be provided to an image processing pipeline. Image processing operations may be performed on the individual lines in stages of the image processing pipeline.

Various techniques are also provided to provide a flexible memory system. In one embodiment, the memory system may be used to buffer the individual lines in pipeline stages of the image processing pipeline. In another embodiment, the memory system may be used to send and receive data between various components (e.g., processing devices or other components) without relying on a single shared bus between the components. For example, data transfers may be performed between different components and different memories of the memory system using a switch fabric to route data over different buses simultaneously or substantially simultaneously.

In another embodiment, the memory system may be implemented to support data transfers using different clocks of the various components, without requiring the components and the memory system to all be synchronized to the same clock source.

In another embodiment, a method includes receiving a thermal image frame comprising a plurality of individual lines, wherein each individual line comprises substantially an entire row or column of thermal image data captured by a plurality of infrared sensors; providing each individual line of the thermal image frame to a line based image processing pipeline; performing image processing operations on the individual lines in stages of the image processing pipeline; and buffering the individual lines in the pipeline stages.

In another embodiment, an infrared imaging module includes a sensor input block adapted to receive a thermal image frame comprising a plurality of individual lines, wherein each individual line comprises substantially an entire row or column of thermal image data captured by a plurality of infrared sensors; a processing device comprising a line based image processing pipeline adapted to perform image processing operations on the individual lines in stages of the image processing pipeline; and a memory system adapted to buffer the individual lines in the pipeline stages.

In another embodiment, a device includes a plurality of components adapted to transfer thermal image data; a plurality of buses connected to the components; and a memory system connected to the components by the buses, the memory system comprising a plurality of memory buffers, each memory buffer comprising: a memory block comprising a single interface adapted to support a single read or write operation at a time, a plurality of ports, wherein each port is adapted to communicate with a corresponding one of the components over a corresponding one of the buses, and a switch fabric block adapted to selectively couple one of the ports with the memory block to permit transfer of at least a portion of the thermal image data between the corresponding one of the components and the memory block through the coupled port and the single interface.

In another embodiment, a method of operating a memory system and a plurality of components connected to the memory system by corresponding buses includes operating a switch fabric to couple a first port of a memory buffer with a memory block of the memory buffer, wherein the memory block comprises a single interface adapted to support a single read or write operation at a time, wherein the memory buffer is part of the memory system; transferring first thermal image data between a first one of the components and the memory block over a first one of the buses, through the first port, and through the single interface; subsequently operating the switch fabric to couple a second port of the memory buffer with the memory block; and transferring second thermal image data between a second one of the components and the memory block over a second one of the buses, through the second port, and through the single interface.

The scope of the invention is defined by the claims, which are incorporated into this section by reference. A more complete understanding of embodiments of the invention will be afforded to those skilled in the art, as well as a realization of additional advantages thereof, by a consideration of the following detailed description of one or more

embodiments. Reference will be made to the appended sheets of drawings that will first be described briefly.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates an infrared imaging module configured to be implemented in a host device in accordance with an embodiment of the disclosure.

Fig. 2 illustrates an assembled infrared imaging module in accordance with an embodiment of the disclosure.

Fig. 3 illustrates an exploded view of an infrared imaging module juxtaposed over a socket in accordance with an embodiment of the disclosure.

Fig. 4 illustrates a block diagram of an infrared sensor assembly including an array of infrared sensors in accordance with an embodiment of the disclosure.

Fig. 5 illustrates a flow diagram of various operations to determine non-uniformity correction (NUC) terms in accordance with an embodiment of the disclosure.

Fig. 6 illustrates differences between neighboring pixels in accordance with an embodiment of the disclosure.

Fig. 7 illustrates a flat field correction technique in accordance with an embodiment of the disclosure.

Fig. 8 illustrates various image processing techniques of Fig. 5 and other operations applied in an image processing pipeline in accordance with an embodiment of the disclosure.

Fig. 9 illustrates a temporal noise reduction process in accordance with an embodiment of the disclosure.

Fig. 10 illustrates particular implementation details of several processes of the image processing pipeline of Fig. 6 in accordance with an embodiment of the disclosure.

Fig. 11 illustrates spatially correlated FPN in a neighborhood of pixels in accordance with an embodiment of the disclosure.

Fig. 12 illustrates a block diagram of a processing module in accordance with an embodiment of the disclosure.

Fig. 13 illustrates a block diagram of a main memory slice (MMS) in accordance with an embodiment of the disclosure.

Fig. 14 illustrates a block diagram of a virtual line buffer (VLB) in accordance with an embodiment of the disclosure.

Fig. 15 illustrates a block diagram of a portion of a memory system in communication with various components in accordance with an embodiment of the disclosure.

Figs. 16A-E illustrate various operations performed by a memory system and a processing device in accordance with embodiments of the disclosure.

Embodiments of the invention and their advantages are best understood by referring to the detailed description that follows. It should be appreciated that like reference numerals are used to identify like elements illustrated in one or more of the figures.

DETAILED DESCRIPTION

Fig. 1 illustrates an infrared imaging module 100 (e.g., an infrared camera or an infrared imaging device) configured to be implemented in a host device 102 in accordance with an embodiment of the disclosure. Infrared imaging module 100 may be implemented, for one or more embodiments, with a small form factor and in accordance with wafer level packaging techniques or other packaging techniques.

In one embodiment, infrared imaging module 100 may be configured to be implemented in a small portable host device 102, such as a mobile telephone, a tablet computing device, a laptop computing device, a personal digital assistant, a visible light camera, a music player, or any other appropriate mobile device. In this regard, infrared imaging module 100 may be used to provide infrared imaging features to host device 102. For example, infrared imaging module 100 may be configured to capture, process, and/or otherwise manage infrared images and provide such infrared images to host device 102 for use in any desired fashion (e.g., for further processing, to store in memory, to display, to use by various applications running on host device 102, to export to other devices, or other uses).

In various embodiments, infrared imaging module 100 may be configured to operate at low voltage levels and over a wide temperature range. For example, in one embodiment, infrared imaging module 100 may operate using a power supply of approximately 2.4 volts, 2.5 volts, 2.8 volts, or lower voltages, and operate over a temperature range of approximately -20 degrees C to approximately +60 degrees C (e.g., providing a suitable dynamic range and performance over an environmental temperature range of approximately 80 degrees C). In one embodiment, by operating infrared imaging module 100 at low voltage levels, infrared imaging module 100 may experience reduced

amounts of self heating in comparison with other types of infrared imaging devices. As a result, infrared imaging module 100 may be operated with reduced measures to compensate for such self heating.

As shown in Fig. 1, host device 102 may include a socket 104, a shutter 105, motion sensors 194, a processor 195, a memory 196, a display 197, and/or other components 198. Socket 104 may be configured to receive infrared imaging module 100 as identified by arrow 101. In this regard, Fig. 2 illustrates infrared imaging module 100 assembled in socket 104 in accordance with an embodiment of the disclosure.

Motion sensors 194 may be implemented by one or more accelerometers, gyroscopes, or other appropriate devices that may be used to detect movement of host device 102. Motion sensors 194 may be monitored by and provide information to processing module 160 or processor 195 to detect motion. In various embodiments, motion sensors 194 may be implemented as part of host device 102 (as shown in Fig. 1), infrared imaging module 100, or other devices attached to or otherwise interfaced with host device 102.

Processor 195 may be implemented as any appropriate processing device (e.g., logic device, microcontroller, processor, application specific integrated circuit (ASIC), or other device) that may be used by host device 102 to execute appropriate instructions, such as software instructions provided in memory 196. Display 197 may be used to display captured and/or processed infrared images and/or other images, data, and information. Other components 198 may be used to implement any features of host device 102 as may be desired for various applications (e.g., clocks, temperature sensors, a visible light camera, or other components). In addition, a machine readable medium 193 may be provided for storing non-transitory instructions for loading into memory 196 and execution by processor 195.

In various embodiments, infrared imaging module 100 and socket 104 may be implemented for mass production to facilitate high volume applications, such as for implementation in mobile telephones or other devices (e.g., requiring small form factors). In one embodiment, the combination of infrared imaging module 100 and socket 104 may exhibit overall dimensions of approximately 8.5 mm by 8.5 mm by 5.9 mm while infrared imaging module 100 is installed in socket 104.

Fig. 3 illustrates an exploded view of infrared imaging module 100 juxtaposed over socket 104 in accordance with an embodiment of the disclosure. Infrared imaging module

100 may include a lens barrel 110, a housing 120, an infrared sensor assembly 128, a circuit board 170, a base 150, and a processing module 160.

Lens barrel 110 may at least partially enclose an optical element 180 (e.g., a lens) which is partially visible in Fig. 3 through an aperture 112 in lens barrel 110. Lens barrel 110 may include a substantially cylindrical extension 114 which may be used to interface lens barrel 110 with an aperture 122 in housing 120.

Infrared sensor assembly 128 may be implemented, for example, with a cap 130 (e.g., a lid) mounted on a substrate 140. Infrared sensor assembly 128 may include a plurality of infrared sensors 132 (e.g., infrared detectors) implemented in an array or other fashion on substrate 140 and covered by cap 130. For example, in one embodiment, infrared sensor assembly 128 may be implemented as a focal plane array (FPA). Such a focal plane array may be implemented, for example, as a vacuum package assembly (e.g., sealed by cap 130 and substrate 140). In one embodiment, infrared sensor assembly 128 may be implemented as a wafer level package (e.g., infrared sensor assembly 128 may be singulated from a set of vacuum package assemblies provided on a wafer). In one embodiment, infrared sensor assembly 128 may be implemented to operate using a power supply of approximately 2.4 volts, 2.5 volts, 2.8 volts, or similar voltages.

Infrared sensors 132 may be configured to detect infrared radiation (e.g., infrared energy) from a target scene including, for example, mid wave infrared wave bands (MWIR), long wave infrared wave bands (LWIR), and/or other thermal imaging bands as may be desired in particular implementations. In one embodiment, infrared sensor assembly 128 may be provided in accordance with wafer level packaging techniques.

Infrared sensors 132 may be implemented, for example, as microbolometers or other types of thermal imaging infrared sensors arranged in any desired array pattern to provide a plurality of pixels. In one embodiment, infrared sensors 132 may be implemented as vanadium oxide (VOx) detectors with a 17 μm pixel pitch. In various embodiments, arrays of approximately 32 by 32 infrared sensors 132, approximately 64 by 64 infrared sensors 132, approximately 80 by 64 infrared sensors 132, or other array sizes may be used.

Substrate 140 may include various circuitry including, for example, a read out integrated circuit (ROIC) with dimensions less than approximately 5.5 mm by 5.5 mm in one embodiment. Substrate 140 may also include bond pads 142 that may be used to contact complementary connections positioned on inside surfaces of housing 120 when

infrared imaging module 100 is assembled as shown in Figs. 5A, 5B, and 5C. In one embodiment, the ROIC may be implemented with low-dropout regulators (LDO) to perform voltage regulation to reduce power supply noise introduced to infrared sensor assembly 128 and thus provide an improved power supply rejection ratio (PSRR). Moreover, by implementing the LDO with the ROIC (e.g., within a wafer level package), less die area may be consumed and fewer discrete die (or chips) are needed.

Fig. 4 illustrates a block diagram of infrared sensor assembly 128 including an array of infrared sensors 132 in accordance with an embodiment of the disclosure. In the illustrated embodiment, infrared sensors 132 are provided as part of a unit cell array of a ROIC 402. ROIC 402 includes bias generation and timing control circuitry 404, column amplifiers 405, a column multiplexer 406, a row multiplexer 408, and an output amplifier 410. Image frames (e.g., thermal images) captured by infrared sensors 132 may be provided by output amplifier 410 to processing module 160, processor 195, and/or any other appropriate components to perform various processing techniques described herein. Although an 8 by 8 array is shown in Fig. 4, any desired array configuration may be used in other embodiments. Further descriptions of ROICs and infrared sensors (e.g., microbolometer circuits) may be found in U.S. Patent No. 6,028,309 issued February 22, 2000, which is incorporated herein by reference in its entirety.

Infrared sensor assembly 128 may capture images (e.g., image frames) and provide such images from its ROIC at various rates. Processing module 160 may be used to perform appropriate processing of captured infrared images and may be implemented in accordance with any appropriate architecture. In one embodiment, processing module 160 may be implemented as an ASIC. In this regard, such an ASIC may be configured to perform image processing with high performance and/or high efficiency. In another embodiment, processing module 160 may be implemented with a general purpose central processing unit (CPU) which may be configured to execute appropriate software instructions to perform image processing, coordinate and perform image processing with various image processing blocks, coordinate interfacing between processing module 160 and host device 102, and/or other operations. In yet another embodiment, processing module 160 may be implemented with a field programmable gate array (FPGA). Processing module 160 may be implemented with other types of processing and/or logic circuits in other embodiments as would be understood by one skilled in the art.

In these and other embodiments, processing module 160 may also be implemented with other components where appropriate, such as, volatile memory, non-volatile memory, and/or one or more interfaces (e.g., infrared detector interfaces, inter-integrated circuit (I2C) interfaces, mobile industry processor interfaces (MIPI), joint test action group (JTAG) interfaces (e.g., IEEE 1149.1 standard test access port and boundary-scan architecture), and/or other interfaces).

In some embodiments, infrared imaging module 100 may further include one or more actuators 199 which may be used to adjust the focus of infrared image frames captured by infrared sensor assembly 128. For example, actuators 199 may be used to move optical element 180, infrared sensors 132, and/or other components relative to each other to selectively focus and defocus infrared image frames in accordance with techniques described herein. Actuators 199 may be implemented in accordance with any type of motion-inducing apparatus or mechanism, and may positioned at any location within or external to infrared imaging module 100 as appropriate for different applications.

When infrared imaging module 100 is assembled, housing 120 may substantially enclose infrared sensor assembly 128, base 150, and processing module 160. Housing 120 may facilitate connection of various components of infrared imaging module 100. For example, in one embodiment, housing 120 may provide electrical connections 126 to connect various components as further described.

Electrical connections 126 (e.g., conductive electrical paths, traces, or other types of connections) may be electrically connected with bond pads 142 when infrared imaging module 100 is assembled. In various embodiments, electrical connections 126 may be embedded in housing 120, provided on inside surfaces of housing 120, and/or otherwise provided by housing 120. Electrical connections 126 may terminate in connections 124 protruding from the bottom surface of housing 120 as shown in Fig. 3. Connections 124 may connect with circuit board 170 when infrared imaging module 100 is assembled (e.g., housing 120 may rest atop circuit board 170 in various embodiments). Processing module 160 may be electrically connected with circuit board 170 through appropriate electrical connections. As a result, infrared sensor assembly 128 may be electrically connected with processing module 160 through, for example, conductive electrical paths provided by: bond pads 142, complementary connections on inside surfaces of housing 120, electrical connections 126 of housing 120, connections 124, and circuit board 170. Advantageously,

such an arrangement may be implemented without requiring wire bonds to be provided between infrared sensor assembly 128 and processing module 160.

In various embodiments, electrical connections 126 in housing 120 may be made from any desired material (e.g., copper or any other appropriate conductive material). In one embodiment, electrical connections 126 may aid in dissipating heat from infrared imaging module 100.

Other connections may be used in other embodiments. For example, in one embodiment, sensor assembly 128 may be attached to processing module 160 through a ceramic board that connects to sensor assembly 128 by wire bonds and to processing module 160 by a ball grid array (BGA). In another embodiment, sensor assembly 128 may be mounted directly on a rigid flexible board and electrically connected with wire bonds, and processing module 160 may be mounted and connected to the rigid flexible board with wire bonds or a BGA.

The various implementations of infrared imaging module 100 and host device 102 set forth herein are provided for purposes of example, rather than limitation. In this regard, any of the various techniques described herein may be applied to any infrared camera system, infrared imager, or other device for performing infrared/thermal imaging.

Substrate 140 of infrared sensor assembly 128 may be mounted on base 150. In various embodiments, base 150 (e.g., a pedestal) may be made, for example, of copper formed by metal injection molding (MIM) and provided with a black oxide or nickel-coated finish. In various embodiments, base 150 may be made of any desired material, such as for example zinc, aluminum, or magnesium, as desired for a given application and may be formed by any desired applicable process, such as for example aluminum casting, MIM, or zinc rapid casting, as may be desired for particular applications. In various embodiments, base 150 may be implemented to provide structural support, various circuit paths, thermal heat sink properties, and other features where appropriate. In one embodiment, base 150 may be a multi-layer structure implemented at least in part using ceramic material.

In various embodiments, circuit board 170 may receive housing 120 and thus may physically support the various components of infrared imaging module 100. In various embodiments, circuit board 170 may be implemented as a printed circuit board (e.g., an FR4 circuit board or other types of circuit boards), a rigid or flexible interconnect (e.g., tape or other type of interconnects), a flexible circuit substrate, a flexible plastic substrate,

or other appropriate structures. In various embodiments, base 150 may be implemented with the various features and attributes described for circuit board 170, and vice versa.

Socket 104 may include a cavity 106 configured to receive infrared imaging module 100 (e.g., as shown in the assembled view of Fig. 2). Infrared imaging module 100 and/or socket 104 may include appropriate tabs, arms, pins, fasteners, or any other appropriate engagement members which may be used to secure infrared imaging module 100 to or within socket 104 using friction, tension, adhesion, and/or any other appropriate manner. Socket 104 may include engagement members 107 that may engage surfaces 109 of housing 120 when infrared imaging module 100 is inserted into a cavity 106 of socket 104. Other types of engagement members may be used in other embodiments.

Infrared imaging module 100 may be electrically connected with socket 104 through appropriate electrical connections (e.g., contacts, pins, wires, or any other appropriate connections). For example, socket 104 may include electrical connections 108 which may contact corresponding electrical connections of infrared imaging module 100 (e.g., interconnect pads, contacts, or other electrical connections on side or bottom surfaces of circuit board 170, bond pads 142 or other electrical connections on base 150, or other connections). Electrical connections 108 may be made from any desired material (e.g., copper or any other appropriate conductive material). In one embodiment, electrical connections 108 may be mechanically biased to press against electrical connections of infrared imaging module 100 when infrared imaging module 100 is inserted into cavity 106 of socket 104. In one embodiment, electrical connections 108 may at least partially secure infrared imaging module 100 in socket 104. Other types of electrical connections may be used in other embodiments.

Socket 104 may be electrically connected with host device 102 through similar types of electrical connections. For example, in one embodiment, host device 102 may include electrical connections (e.g., soldered connections, snap-in connections, or other connections) that connect with electrical connections 108 passing through apertures 190. In various embodiments, such electrical connections may be made to the sides and/or bottom of socket 104.

Various components of infrared imaging module 100 may be implemented with flip chip technology which may be used to mount components directly to circuit boards without the additional clearances typically needed for wire bond connections. Flip chip connections may be used, as an example, to reduce the overall size of infrared imaging

module 100 for use in compact small form factor applications. For example, in one embodiment, processing module 160 may be mounted to circuit board 170 using flip chip connections. For example, infrared imaging module 100 may be implemented with such flip chip configurations.

In various embodiments, infrared imaging module 100 and/or associated components may be implemented in accordance with various techniques (e.g., wafer level packaging techniques) as set forth in U.S. Patent Application No. 12/844,124 filed July 27, 2010, and U.S. Provisional Patent Application No. 61/469,651 filed March 30, 2011, which are incorporated herein by reference in their entirety. Furthermore, in accordance with one or more embodiments, infrared imaging module 100 and/or associated components may be implemented, calibrated, tested, and/or used in accordance with various techniques, such as for example as set forth in U.S. Patent No. 7,470,902 issued December 30, 2008, U.S. Patent No. 6,028,309 issued February 22, 2000, U.S. Patent No. 6,812,465 issued November 2, 2004, U.S. Patent No. 7,034,301 issued April 25, 2006, U.S. Patent No. 7,679,048 issued March 16, 2010, U.S. Patent No. 7,470,904 issued December 30, 2008, U.S. Patent Application No. 12/202,880 filed September 2, 2008, and U.S. Patent Application No. 12/202,896 filed September 2, 2008, which are incorporated herein by reference in their entirety.

Referring again to Fig. 1, in various embodiments, host device 102 may include shutter 105. In this regard, shutter 105 may be selectively positioned over socket 104 (e.g., as identified by arrows 103) while infrared imaging module 100 is installed therein. In this regard, shutter 105 may be used, for example, to protect infrared imaging module 100 when not in use. Shutter 105 may also be used as a temperature reference as part of a calibration process (e.g., a NUC process or other calibration processes) for infrared imaging module 100 as would be understood by one skilled in the art.

In various embodiments, shutter 105 may be made from various materials such as, for example, polymers, glass, aluminum (e.g., painted or anodized) or other materials. In various embodiments, shutter 105 may include one or more coatings to selectively filter electromagnetic radiation and/or adjust various optical properties of shutter 105 (e.g., a uniform blackbody coating or a reflective gold coating).

In another embodiment, shutter 105 may be fixed in place to protect infrared imaging module 100 at all times. In this case, shutter 105 or a portion of shutter 105 may be made from appropriate materials (e.g., polymers or infrared transmitting materials such

as silicon, germanium, zinc selenide, or chalcogenide glasses) that do not substantially filter desired infrared wavelengths. In another embodiment, a shutter may be implemented as part of infrared imaging module 100 (e.g., within or as part of a lens barrel or other components of infrared imaging module 100), as would be understood by one skilled in the art.

Alternatively, in another embodiment, a shutter (e.g., shutter 105 or other type of external or internal shutter) need not be provided, but rather a NUC process or other type of calibration may be performed using shutterless techniques. In another embodiment, a NUC process or other type of calibration using shutterless techniques may be performed in combination with shutter-based techniques.

Infrared imaging module 100 and host device 102 may be implemented in accordance with any of the various techniques set forth in U.S. Provisional Patent Application No. 61/495,873 filed June 10, 2011, U.S. Provisional Patent Application No. 61/495,879 filed June 10, 2011, and U.S. Provisional Patent Application No. 61/495,888 filed June 10, 2011, which are incorporated herein by reference in their entirety.

In various embodiments, the components of host device 102 and/or infrared imaging module 100 may be implemented as a local or distributed system with components in communication with each other over wired and/or wireless networks. Accordingly, the various operations identified in this disclosure may be performed by local and/or remote components as may be desired in particular implementations.

Fig. 5 illustrates a flow diagram of various operations to determine NUC terms in accordance with an embodiment of the disclosure. In some embodiments, the operations of Fig. 5 may be performed by processing module 160 or processor 195 (both also generally referred to as a processor) operating on image frames captured by infrared sensors 132.

In block 505, infrared sensors 132 begin capturing image frames of a scene. Typically, the scene will be the real world environment in which host device 102 is currently located. In this regard, shutter 105 (if optionally provided) may be opened to permit infrared imaging module to receive infrared radiation from the scene. Infrared sensors 132 may continue capturing image frames during all operations shown in Fig. 5. In this regard, the continuously captured image frames may be used for various operations as further discussed. In one embodiment, the captured image frames may be temporally filtered (e.g., in accordance with the process of block 826 further described herein with regard to Fig. 8) and be processed by other terms (e.g., factory gain terms 812, factory

offset terms 816, previously determined NUC terms 817, column FPN terms 820, and row FPN terms 824 as further described herein with regard to Fig. 8) before they are used in the operations shown in Fig. 5.

In block 510, a NUC process initiating event is detected. In one embodiment, the NUC process may be initiated in response to physical movement of host device 102. Such movement may be detected, for example, by motion sensors 194 which may be polled by a processor. In one example, a user may move host device 102 in a particular manner, such as by intentionally waving host device 102 back and forth in an "erase" or "swipe" movement. In this regard, the user may move host device 102 in accordance with a predetermined speed and direction (velocity), such as in an up and down, side to side, or other pattern to initiate the NUC process. In this example, the use of such movements may permit the user to intuitively operate host device 102 to simulate the "erasing" of noise in captured image frames.

In another example, a NUC process may be initiated by host device 102 if motion exceeding a threshold value is exceeded (e.g., motion greater than expected for ordinary use). It is contemplated that any desired type of spatial translation of host device 102 may be used to initiate the NUC process.

In yet another example, a NUC process may be initiated by host device 102 if a minimum time has elapsed since a previously performed NUC process. In a further example, a NUC process may be initiated by host device 102 if infrared imaging module 100 has experienced a minimum temperature change since a previously performed NUC process. In a still further example, a NUC process may be continuously initiated and repeated.

In block 515, after a NUC process initiating event is detected, it is determined whether the NUC process should actually be performed. In this regard, the NUC process may be selectively initiated based on whether one or more additional conditions are met. For example, in one embodiment, the NUC process may not be performed unless a minimum time has elapsed since a previously performed NUC process. In another embodiment, the NUC process may not be performed unless infrared imaging module 100 has experienced a minimum temperature change since a previously performed NUC process. Other criteria or conditions may be used in other embodiments. If appropriate criteria or conditions have been met, then the flow diagram continues to block 520. Otherwise, the flow diagram returns to block 505.

In the NUC process, blurred image frames may be used to determine NUC terms which may be applied to captured image frames to correct for FPN. As discussed, in one embodiment, the blurred image frames may be obtained by accumulating multiple image frames of a moving scene (e.g., captured while the scene and/or the thermal imager is in motion). In another embodiment, the blurred image frames may be obtained by defocusing an optical element or other component of the thermal imager.

Accordingly, in block 520 a choice of either approach is provided. If the motion-based approach is used, then the flow diagram continues to block 525. If the defocus-based approach is used, then the flow diagram continues to block 530.

Referring now to the motion-based approach, in block 525 motion is detected. For example, in one embodiment, motion may be detected based on the image frames captured by infrared sensors 132. In this regard, an appropriate motion detection process (e.g., an image registration process, a frame-to-frame difference calculation, or other appropriate process) may be applied to captured image frames to determine whether motion is present (e.g., whether static or moving image frames have been captured). For example, in one embodiment, it can be determined whether pixels or regions around the pixels of consecutive image frames have changed more than a user defined amount (e.g., a percentage and/or threshold value). If at least a given percentage of pixels have changed by at least the user defined amount, then motion will be detected with sufficient certainty to proceed to block 535.

In another embodiment, motion may be determined on a per pixel basis, wherein only pixels that exhibit significant changes are accumulated to provide the blurred image frame. For example, counters may be provided for each pixel and used to ensure that the same number of pixel values are accumulated for each pixel, or used to average the pixel values based on the number of pixel values actually accumulated for each pixel. Other types of image-based motion detection may be performed such as performing a Radon transform.

In another embodiment, motion may be detected based on data provided by motion sensors 194. In one embodiment, such motion detection may include detecting whether host device 102 is moving along a relatively straight trajectory through space. For example, if host device 102 is moving along a relatively straight trajectory, then it is possible that certain objects appearing in the imaged scene may not be sufficiently blurred (e.g., objects in the scene that may be aligned with or moving substantially parallel to the

straight trajectory). Thus, in such an embodiment, the motion detected by motion sensors 194 may be conditioned on host device 102 exhibiting, or not exhibiting, particular trajectories.

In yet another embodiment, both a motion detection process and motion sensors 194 may be used. Thus, using any of these various embodiments, a determination can be made as to whether or not each image frame was captured while at least a portion of the scene and host device 102 were in motion relative to each other (e.g., which may be caused by host device 102 moving relative to the scene, at least a portion of the scene moving relative to host device 102, or both).

It is expected that the image frames for which motion was detected may exhibit some secondary blurring of the captured scene (e.g., blurred thermal image data associated with the scene) due to the thermal time constants of infrared sensors 132 (e.g., microbolometer thermal time constants) interacting with the scene movement.

In block 535, image frames for which motion was detected are accumulated. For example, if motion is detected for a continuous series of image frames, then the image frames of the series may be accumulated. As another example, if motion is detected for only some image frames, then the non-moving image frames may be skipped and not included in the accumulation. Thus, a continuous or discontinuous set of image frames may be selected to be accumulated based on the detected motion.

In block 540, the accumulated image frames are averaged to provide a blurred image frame. Because the accumulated image frames were captured during motion, it is expected that actual scene information will vary between the image frames and thus cause the scene information to be further blurred in the resulting blurred image frame (block 545).

In contrast, FPN (e.g., caused by one or more components of infrared imaging module 100) will remain fixed over at least short periods of time and over at least limited changes in scene irradiance during motion. As a result, image frames captured in close proximity in time and space during motion will suffer from identical or at least very similar FPN. Thus, although scene information may change in consecutive image frames, the FPN will stay essentially constant. By averaging, multiple image frames captured during motion will blur the scene information, but will not blur the FPN. As a result, FPN will remain more clearly defined in the blurred image frame provided in block 545 than the scene information.

In one embodiment, 32 or more image frames are accumulated and averaged in blocks 535 and 540. However, any desired number of image frames may be used in other embodiments, but with generally decreasing correction accuracy as frame count is decreased.

Referring now to the defocus-based approach, in block 530, a defocus operation may be performed to intentionally defocus the image frames captured by infrared sensors 132. For example, in one embodiment, one or more actuators 199 may be used to adjust, move, or otherwise translate optical element 180, infrared sensor assembly 128, and/or other components of infrared imaging module 100 to cause infrared sensors 132 to capture a blurred (e.g., unfocused) image frame of the scene. Other non-actuator based techniques are also contemplated for intentionally defocusing infrared image frames such as, for example, manual (e.g., user-initiated) defocusing.

Although the scene may appear blurred in the image frame, FPN (e.g., caused by one or more components of infrared imaging module 100) will remain unaffected by the defocusing operation. As a result, a blurred image frame of the scene will be provided (block 545) with FPN remaining more clearly defined in the blurred image than the scene information.

In the above discussion, the defocus-based approach has been described with regard to a single captured image frame. In another embodiment, the defocus-based approach may include accumulating multiple image frames while the infrared imaging module 100 has been defocused and averaging the defocused image frames to remove the effects of temporal noise and provide a blurred image frame in block 545.

Thus, it will be appreciated that a blurred image frame may be provided in block 545 by either the motion-based approach or the defocus-based approach. Because much of the scene information will be blurred by either motion, defocusing, or both, the blurred image frame may be effectively considered a low pass filtered version of the original captured image frames with respect to scene information.

In block 550, the blurred image frame is processed to determine updated row and column FPN terms (e.g., if row and column FPN terms have not been previously determined then the updated row and column FPN terms may be new row and column FPN terms in the first iteration of block 550). As used in this disclosure, the terms row and column may be used interchangeably depending on the orientation of infrared sensors 132 and/or other components of infrared imaging module 100.

In one embodiment, block 550 includes determining a spatial FPN correction term for each row of the blurred image frame (e.g., each row may have its own spatial FPN correction term), and also determining a spatial FPN correction term for each column of the blurred image frame (e.g., each column may have its own spatial FPN correction term). Such processing may be used to reduce the spatial and slowly varying (1/f) row and column FPN inherent in thermal imagers caused by, for example, 1/f noise characteristics of amplifiers in ROIC 402 which may manifest as vertical and horizontal stripes in image frames.

Advantageously, by determining spatial row and column FPN terms using the blurred image frame, there will be a reduced risk of vertical and horizontal objects in the actual imaged scene from being mistaken for row and column noise (e.g., real scene content will be blurred while FPN remains unblurred).

In one embodiment, row and column FPN terms may be determined by considering differences between neighboring pixels of the blurred image frame. For example, Fig. 6 illustrates differences between neighboring pixels in accordance with an embodiment of the disclosure. Specifically, in Fig. 6 a pixel 610 is compared to its 8 nearest horizontal neighbors: d0-d3 on one side and d4-d7 on the other side. Differences between the neighbor pixels can be averaged to obtain an estimate of the offset error of the illustrated group of pixels. An offset error may be calculated for each pixel in a row or column and the average result may be used to correct the entire row or column.

To prevent real scene data from being interpreted as noise, upper and lower threshold values may be used (thPix and –thPix). Pixel values falling outside these threshold values (pixels d1 and d4 in this example) are not used to obtain the offset error. In addition, the maximum amount of row and column FPN correction may be limited by these threshold values.

Further techniques for performing spatial row and column FPN correction processing are set forth in U.S. Patent Application No. 12/396,340 filed March 2, 2009 which is incorporated herein by reference in its entirety.

Referring again to Fig. 5, the updated row and column FPN terms determined in block 550 are stored (block 552) and applied (block 555, e.g., full terms and/or estimates may be applied) to the blurred image frame provided in block 545. After these terms are applied, some of the spatial row and column FPN in the blurred image frame may be reduced. However, because such terms are applied generally to rows and columns,

additional FPN may remain such as spatially uncorrelated FPN associated with pixel to pixel drift or other causes. Neighborhoods of spatially correlated FPN may also remain which may not be directly associated with individual rows and columns. Accordingly, further processing may be performed as discussed below to determine NUC terms.

In block 560, local contrast values (e.g., edges or absolute values of gradients between adjacent or small groups of pixels) in the blurred image frame are determined. If scene information in the blurred image frame includes contrasting areas that have not been significantly blurred (e.g., high contrast edges in the original scene data), then such features may be identified by a contrast determination process in block 560.

For example, local contrast values in the blurred image frame may be calculated, or any other desired type of edge detection process may be applied to identify certain pixels in the blurred image as being part of an area of local contrast. Pixels that are marked in this manner may be considered as containing excessive high spatial frequency scene information that would be interpreted as FPN (e.g., such regions may correspond to portions of the scene that have not been sufficiently blurred). As such, these pixels may be excluded from being used in the further determination of NUC terms. In one embodiment, such contrast detection processing may rely on a threshold that is higher than the expected contrast value associated with FPN (e.g., pixels exhibiting a contrast value higher than the threshold may be considered to be scene information, and those lower than the threshold may be considered to be exhibiting FPN).

In one embodiment, the contrast determination of block 560 may be performed on the blurred image frame after row and column FPN terms have been applied to the blurred image frame (e.g., as shown in Fig. 5). In another embodiment, block 560 may be performed prior to block 550 to determine contrast before row and column FPN terms are determined (e.g., to prevent scene based contrast from contributing to the determination of such terms).

Following block 560, it is expected that any high spatial frequency content remaining in the blurred image frame may be generally attributed to spatially uncorrelated FPN. In this regard, following block 560, much of the other noise or actual desired scene based information has been removed or excluded from the blurred image frame due to: intentional blurring of the image frame (e.g., by motion or defocusing in blocks 520 through 545), application of row and column FPN terms (block 555), and contrast determination (block 560).

Thus, it can be expected that following block 560, any remaining high spatial frequency content (e.g., exhibited as areas of contrast or differences in the blurred image frame) may be attributed to spatially uncorrelated FPN. Accordingly, in block 565, the blurred image frame is high pass filtered. In one embodiment, this may include applying a high pass filter to extract the high spatial frequency content from the blurred image frame. In another embodiment, this may include applying a low pass filter to the blurred image frame and taking a difference between the low pass filtered image frame and the unfiltered blurred image frame to obtain the high spatial frequency content. In accordance with various embodiments of the present disclosure, a high pass filter may be implemented by calculating a mean difference between a sensor signal (e.g., a pixel value) and its neighbors.

In block 570, a flat field correction process is performed on the high pass filtered blurred image frame to determine updated NUC terms (e.g., if a NUC process has not previously been performed then the updated NUC terms may be new NUC terms in the first iteration of block 570).

For example, Fig. 7 illustrates a flat field correction technique 700 in accordance with an embodiment of the disclosure. In Fig. 7, a NUC term may be determined for each pixel 710 of the blurred image frame using the values of its neighboring pixels 712 to 726. For each pixel 710, several gradients may be determined based on the absolute difference between the values of various adjacent pixels. For example, absolute value differences may be determined between: pixels 712 and 714 (a left to right diagonal gradient), pixels 716 and 718 (a top to bottom vertical gradient), pixels 720 and 722 (a right to left diagonal gradient), and pixels 724 and 726 (a left to right horizontal gradient).

These absolute differences may be summed to provide a summed gradient for pixel 710. A weight value may be determined for pixel 710 that is inversely proportional to the summed gradient. This process may be performed for all pixels 710 of the blurred image frame until a weight value is provided for each pixel 710. For areas with low gradients (e.g., areas that are blurry or have low contrast), the weight value will be close to one. Conversely, for areas with high gradients, the weight value will be zero or close to zero. The update to the NUC term as estimated by the high pass filter is multiplied with the weight value.

In one embodiment, the risk of introducing scene information into the NUC terms can be further reduced by applying some amount of temporal damping to the NUC term

determination process. For example, a temporal damping factor λ between 0 and 1 may be chosen such that the new NUC term (NUC_{NEW}) stored is a weighted average of the old NUC term (NUC_{OLD}) and the estimated updated NUC term (NUC_{UPDATE}). In one embodiment, this can be expressed as $NUC_{NEW} = \lambda \cdot NUC_{OLD} + (1-\lambda) \cdot (NUC_{OLD} + NUC_{UPDATE})$.

Although the determination of NUC terms has been described with regard to gradients, local contrast values may be used instead where appropriate. Other techniques may also be used such as, for example, standard deviation calculations. Other types flat field correction processes may be performed to determine NUC terms including, for example, various processes identified in U.S. Patent No. 6,028,309 issued February 22, 2000, U.S. Patent No. 6,812,465 issued November 2, 2004, and U.S. Patent Application No. 12/114,865 filed May 5, 2008, which are incorporated herein by reference in their entirety.

Referring again to Fig. 5, block 570 may include additional processing of the NUC terms. For example, in one embodiment, to preserve the scene signal mean, the sum of all NUC terms may be normalized to zero by subtracting the NUC term mean from each NUC term. Also in block 570, to avoid row and column noise from affecting the NUC terms, the mean value of each row and column may be subtracted from the NUC terms for each row and column. As a result, row and column FPN filters using the row and column FPN terms determined in block 550 may be better able to filter out row and column noise in further iterations (e.g., as further shown in Fig. 8) after the NUC terms are applied to captured images (e.g., in block 580 further discussed herein). In this regard, the row and column FPN filters may in general use more data to calculate the per row and per column offset coefficients (e.g., row and column FPN terms) and may thus provide a more robust alternative for reducing spatially correlated FPN than the NUC terms which are based on high pass filtering to capture spatially uncorrelated noise.

In blocks 571-573, additional high pass filtering and further determinations of updated NUC terms may be optionally performed to remove spatially correlated FPN with lower spatial frequency than previously removed by row and column FPN terms. In this regard, some variability in infrared sensors 132 or other components of infrared imaging module 100 may result in spatially correlated FPN noise that cannot be easily modeled as row or column noise. Such spatially correlated FPN may include, for example, window defects on a sensor package or a cluster of infrared sensors 132 that respond differently to

irradiance than neighboring infrared sensors 132. In one embodiment, such spatially correlated FPN may be mitigated with an offset correction. If the amount of such spatially correlated FPN is significant, then the noise may also be detectable in the blurred image frame. Since this type of noise may affect a neighborhood of pixels, a high pass filter with a small kernel may not detect the FPN in the neighborhood (e.g., all values used in high pass filter may be taken from the neighborhood of affected pixels and thus may be affected by the same offset error). For example, if the high pass filtering of block 565 is performed with a small kernel (e.g., considering only immediately adjacent pixels that fall within a neighborhood of pixels affected by spatially correlated FPN), then broadly distributed spatially correlated FPN may not be detected.

For example, Fig. 11 illustrates spatially correlated FPN in a neighborhood of pixels in accordance with an embodiment of the disclosure. As shown in a sample image frame 1100, a neighborhood of pixels 1110 may exhibit spatially correlated FPN that is not precisely correlated to individual rows and columns and is distributed over a neighborhood of several pixels (e.g., a neighborhood of approximately 4 by 4 pixels in this example). Sample image frame 1100 also includes a set of pixels 1120 exhibiting substantially uniform response that are not used in filtering calculations, and a set of pixels 1130 that are used to estimate a low pass value for the neighborhood of pixels 1110. In one embodiment, pixels 1130 may be a number of pixels divisible by two in order to facilitate efficient hardware or software calculations.

Referring again to Fig. 5, in blocks 571-573, additional high pass filtering and further determinations of updated NUC terms may be optionally performed to remove spatially correlated FPN such as exhibited by pixels 1110. In block 571, the updated NUC terms determined in block 570 are applied to the blurred image frame. Thus, at this time, the blurred image frame will have been initially corrected for spatially correlated FPN (e.g., by application of the updated row and column FPN terms in block 555), and also initially corrected for spatially uncorrelated FPN (e.g., by application of the updated NUC terms applied in block 571).

In block 572, a further high pass filter is applied with a larger kernel than was used in block 565, and further updated NUC terms may be determined in block 573. For example, to detect the spatially correlated FPN present in pixels 1110, the high pass filter applied in block 572 may include data from a sufficiently large enough neighborhood of pixels such that differences can be determined between unaffected pixels (e.g., pixels 1120)

and affected pixels (e.g., pixels 1110). For example, a low pass filter with a large kernel can be used (e.g., an N by N kernel that is much greater than 3 by 3 pixels) and the results may be subtracted to perform appropriate high pass filtering.

In one embodiment, for computational efficiency, a sparse kernel may be used such that only a small number of neighboring pixels inside an N by N neighborhood are used. For any given high pass filter operation using distant neighbors (e.g., a large kernel), there is a risk of modeling actual (potentially blurred) scene information as spatially correlated FPN. Accordingly, in one embodiment, the temporal damping factor λ may be set close to 1 for updated NUC terms determined in block 573.

In various embodiments, blocks 571-573 may be repeated (e.g., cascaded) to iteratively perform high pass filtering with increasing kernel sizes to provide further updated NUC terms further correct for spatially correlated FPN of desired neighborhood sizes. In one embodiment, the decision to perform such iterations may be determined by whether spatially correlated FPN has actually been removed by the updated NUC terms of the previous performance of blocks 571-573.

After blocks 571-573 are finished, a decision is made regarding whether to apply the updated NUC terms to captured image frames (block 574). For example, if an average of the absolute value of the NUC terms for the entire image frame is less than a minimum threshold value, or greater than a maximum threshold value, the NUC terms may be deemed spurious or unlikely to provide meaningful correction. Alternatively, thresholding criteria may be applied to individual pixels to determine which pixels receive updated NUC terms. In one embodiment, the threshold values may correspond to differences between the newly calculated NUC terms and previously calculated NUC terms. In another embodiment, the threshold values may be independent of previously calculated NUC terms. Other tests may be applied (e.g., spatial correlation tests) to determine whether the NUC terms should be applied.

If the NUC terms are deemed spurious or unlikely to provide meaningful correction, then the flow diagram returns to block 505. Otherwise, the newly determined NUC terms are stored (block 575) to replace previous NUC terms (e.g., determined by a previously performed iteration of Fig. 5) and applied (block 580) to captured image frames.

Fig. 8 illustrates various image processing techniques of Fig. 5 and other operations applied in an image processing pipeline 800 in accordance with an embodiment of the disclosure. In this regard, pipeline 800 identifies various operations of Fig. 5 in the context

of an overall iterative image processing scheme for correcting image frames provided by infrared imaging module 100. In some embodiments, pipeline 800 may be provided by processing module 160 or processor 195 (both also generally referred to as a processor) operating on image frames captured by infrared sensors 132.

Image frames captured by infrared sensors 132 may be provided to a frame averager 804 that integrates multiple image frames to provide image frames 802 with an improved signal to noise ratio. Frame averager 804 may be effectively provided by infrared sensors 132, ROIC 402, and other components of infrared sensor assembly 128 that are implemented to support high image capture rates. For example, in one embodiment, infrared sensor assembly 128 may capture infrared image frames at a frame rate of 240 Hz (e.g., 240 images per second). In this embodiment, such a high frame rate may be implemented, for example, by operating infrared sensor assembly 128 at relatively low voltages (e.g., compatible with mobile telephone voltages) and by using a relatively small array of infrared sensors 132 (e.g., an array of 64 by 64 infrared sensors in one embodiment).

In one embodiment, such infrared image frames may be provided from infrared sensor assembly 128 to processing module 160 at a high frame rate (e.g., 240 Hz or other frame rates). In another embodiment, infrared sensor assembly 128 may integrate over longer time periods, or multiple time periods, to provide integrated (e.g., averaged) infrared image frames to processing module 160 at a lower frame rate (e.g., 30 Hz, 9 Hz, or other frame rates). Further information regarding implementations that may be used to provide high image capture rates may be found in U.S. Provisional Patent Application No. 61/495,879 previously referenced herein.

Image frames 802 proceed through pipeline 800 where they are adjusted by various terms, temporally filtered, and additionally processed. In blocks 810 and 814, factory gain terms 812 (e.g., gain offsets/coefficients in one embodiment) and factory offset terms 816 (e.g., pixel offsets/coefficients and LaGrange offsets/coefficients in one embodiment) are applied to image frames 802 to compensate for gain and offset differences, respectively, between the various infrared sensors 132 and/or other components of infrared imaging module 100 determined during manufacturing and testing.

In block 580, NUC terms 817 are applied to image frames 802 to correct for FPN as discussed. In one embodiment, if NUC terms 817 have not yet been determined (e.g., before a NUC process has been initiated), then block 580 may not be performed or

initialization values may be used for NUC terms 817 that result in no alteration to the image data (e.g., offsets for every pixel would be equal to zero).

In blocks 818 and 822, column FPN terms 820 and row FPN terms 824, respectively, are applied to image frames 802. Column FPN terms 820 and row FPN terms 824 may be determined in accordance with block 550 as discussed. In one embodiment, if the column FPN terms 820 and row FPN terms 824 have not yet been determined (e.g., before a NUC process has been initiated), then blocks 818 and 822 may not be performed or initialization values may be used for the column FPN terms 820 and row FPN terms 824 that result in no alteration to the image data (e.g., offsets for every pixel would be equal to zero).

In block 826, temporal filtering is performed on image frames 802 in accordance with a temporal noise reduction (TNR) process. Fig. 9 illustrates a TNR process in accordance with an embodiment of the disclosure. In Fig. 9, a presently received image frame 802a and a previously temporally filtered image frame 802b are processed to determine a new temporally filtered image frame 802e. Image frames 802a and 802b include local neighborhoods of pixels 803a and 803b centered around pixels 805a and 805b, respectively. Neighborhoods 803a and 803b correspond to the same locations within image frames 802a and 802b and are subsets of the total pixels in image frames 802a and 802b. In the illustrated embodiment, neighborhoods 803a and 803b include areas of 5 by 5 pixels. Other neighborhood sizes may be used in other embodiments.

Differences between corresponding pixels of neighborhoods 803a and 803b are determined and averaged to provide an averaged delta value 805c for the location corresponding to pixels 805a and 805b. Averaged delta value 805c may be used to determine weight values in block 807 to be applied to pixels 805a and 805b of image frames 802a and 802b.

In one embodiment, as shown in graph 809, the weight values determined in block 807 may be inversely proportional to averaged delta value 805c such that weight values drop rapidly towards zero when there are large differences between neighborhoods 803a and 803b. In this regard, large differences between neighborhoods 803a and 803b may indicate that changes have occurred within the scene (e.g., due to motion) and pixels 802a and 802b may be appropriately weighted, in one embodiment, to avoid introducing blur across frame-to-frame scene changes. Other associations between weight values and averaged delta value 805c may be used in various embodiments.

The weight values determined in block 807 may be applied to pixels 805a and 805b to determine a value for corresponding pixel 805e of image frame 802e (block 811). In this regard, pixel 805e may have a value that is a weighted average (or other combination) of pixels 805a and 805b, depending on averaged delta value 805c and the weight values determined in block 807.

For example, pixel 805e of temporally filtered image frame 802e may be a weighted sum of pixels 805a and 805b of image frames 802a and 802b. If the average difference between pixels 805a and 805b is due to noise, then it may be expected that the average change between neighborhoods 805a and 805b will be close to zero (e.g., corresponding to the average of uncorrelated changes). Under such circumstances, it may be expected that the sum of the differences between neighborhoods 805a and 805b will be close to zero. In this case, pixel 805a of image frame 802a may both be appropriately weighted so as to contribute to the value of pixel 805e.

However, if the sum of such differences is not zero (e.g., even differing from zero by a small amount in one embodiment), then the changes may be interpreted as being attributed to motion instead of noise. Thus, motion may be detected based on the average change exhibited by neighborhoods 805a and 805b. Under these circumstances, pixel 805a of image frame 802a may be weighted heavily, while pixel 805b of image frame 802b may be weighted lightly.

Other embodiments are also contemplated. For example, although averaged delta value 805c has been described as being determined based on neighborhoods 805a and 805b, in other embodiments averaged delta value 805c may be determined based on any desired criteria (e.g., based on individual pixels or other types of groups of sets of pixels).

In the above embodiments, image frame 802a has been described as a presently received image frame and image frame 802b has been described as a previously temporally filtered image frame. In another embodiment, image frames 802a and 802b may be first and second image frames captured by infrared imaging module 100 that have not been temporally filtered.

Fig. 10 illustrates further implementation details in relation to the TNR process of block 826. As shown in Fig. 10, image frames 802a and 802b may be read into line buffers 1010a and 1010b, respectively, and image frame 802b (e.g., the previous image frame) may be stored in a frame buffer 1020 before being read into line buffer 1010b. In one embodiment, line buffers 1010a-b and frame buffer 1020 may be implemented by a block

of random access memory (RAM) provided by any appropriate component of infrared imaging module 100 and/or host device 102.

Referring again to Fig. 8, image frame 802e may be passed to additional blocks 827-832 for further processing to provide a result image frame 833 that may be used by host device 102 as desired. In one embodiment, such processing may include: bad pixel replacement processing in block 827 (e.g., to compensate for malfunctioning or inoperative pixels); distortion correction processing in block 828 (e.g., to compensate for possible lens distortion or other distortion); video polarity processing in block 829; gamma correction processing in block 830; automatic gain compensation processing in block 831; and pseudo-color processing in block 832 (e.g., using a look up table (LUT)).

Fig. 8 further illustrates various operations that may be performed to determine row and column FPN terms and NUC terms as discussed. In one embodiment, these operations may use image frames 802e as shown in Fig. 8. Because image frames 802e have already been temporally filtered, at least some temporal noise may be removed and thus will not inadvertently affect the determination of row and column FPN terms 824 and 820 and NUC terms 817. In another embodiment, non-temporally filtered image frames 802 may be used.

In Fig. 8, blocks 510, 515, and 520 of Fig. 5 are collectively represented together. As discussed, a NUC process may be selectively initiated and performed in response to various NUC process initiating events and based on various criteria or conditions. As also discussed, the NUC process may be performed in accordance with a motion-based approach (blocks 525, 535, and 540) or a defocus-based approach (block 530) to provide a blurred image frame (block 545). Fig. 8 further illustrates various additional blocks 550, 552, 555, 560, 565, 570, 571, 572, 573, and 575 previously discussed with regard to Fig. 5.

As shown in Fig. 8, row and column FPN terms 824 and 820 and NUC terms 817 may be determined and applied in an iterative fashion such that updated terms are determined using image frames 802 to which previous terms have already been applied. As a result, the overall process of Fig. 8 may repeatedly update and apply such terms to continuously reduce the noise in image frames 833 to be used by host device 102.

Referring again to Fig. 10, further implementation details are illustrated for various blocks of Figs. 5 and 8 in relation to pipeline 800. For example, blocks 525, 535, and 540 are shown as operating at the normal frame rate of image frames 802 received by pipeline 800. In the embodiment shown in Fig. 10, the determination made in block 525 is

represented as a decision diamond used to determine whether a given image frame 802 has sufficiently changed such that it may be considered an image frame that will enhance the blur if added to other image frames and is therefore accumulated (block 535 is represented by an arrow in this embodiment) and averaged (block 540).

Also in Fig. 10, the determination of column FPN terms 820 (block 550) is shown as operating at an update rate that in this example is 1/32 of the sensor frame rate (e.g., normal frame rate) due to the averaging performed in block 540. Other update rates may be used in other embodiments. Although only column FPN terms 820 are identified in Fig. 10, row FPN terms 824 may be implemented in a similar fashion at the reduced frame rate.

Fig. 10 also illustrates further implementation details in relation to the NUC determination process of block 570. In this regard, the blurred image frame may be read to a line buffer 1030 (e.g., implemented by a block of RAM provided by any appropriate component of infrared imaging module 100 and/or host device 102). The flat field correction technique 700 of Fig. 7 may be performed on the blurred image frame.

In view of the present disclosure, it will be appreciated that techniques described herein may be used to remove various types of FPN (e.g., including very high amplitude FPN) such as spatially correlated row and column FPN and spatially uncorrelated FPN.

Other embodiments are also contemplated. For example, in one embodiment, the rate at which row and column FPN terms and/or NUC terms are updated can be inversely proportional to the estimated amount of blur in the blurred image frame and/or inversely proportional to the magnitude of local contrast values (e.g., determined in block 560).

In various embodiments, the described techniques may provide advantages over conventional shutter-based noise correction techniques. For example, by using a shutterless process, a shutter (e.g., such as shutter 105) need not be provided, thus permitting reductions in size, weight, cost, and mechanical complexity. Power and maximum voltage supplied to, or generated by, infrared imaging module 100 may also be reduced if a shutter does not need to be mechanically operated. Reliability will be improved by removing the shutter as a potential point of failure. A shutterless process also eliminates potential image interruption caused by the temporary blockage of the imaged scene by a shutter.

Also, by correcting for noise using intentionally blurred image frames captured from a real world scene (not a uniform scene provided by a shutter), noise correction may be performed on image frames that have irradiance levels similar to those of the actual

scene desired to be imaged. This can improve the accuracy and effectiveness of noise correction terms determined in accordance with the various described techniques.

In accordance with additional embodiments, various techniques are provided to implement line based processing of thermal images. In one embodiment, individual lines of a thermal image frame may be provided to an image processing pipeline provided, for example, by one or more processing devices of infrared imaging module 100. Image processing operations may be performed on the individual lines in stages of the image processing pipeline.

In accordance with additional embodiments, techniques are provided to implement a flexible memory system to support one or more processing devices of infrared imaging module 100. For example, in some embodiments, the memory system may be used to support line based (e.g., row based or column based) processing of thermal images provided by infrared sensor assembly 128. In this regard, a line may generally refer to a row or a column, and the terms line, row, and column are used interchangeably herein.

Also in some embodiments, the memory system may be used to send and receive data between various components without relying on a single shared bus between the components. For example, in some embodiments, data transfers may be performed between different components and different memories of the memory system using a switch fabric to route data over different buses simultaneously or substantially simultaneously. In some embodiments, the memory system may be implemented to support data transfers using different clocks of the various components, without requiring the components and the memory system to all be synchronized to the same clock source.

These and other features of various embodiments of the memory system are further described with regard to Figs. 12-16E. Although the memory system will be primarily described with regard to processing module 160, it may be used with any processing device (e.g., processing module 160, processor 195, and/or other devices) and the various components of processing module 160 may be implemented as any type of processing device, logic, and/or circuitry as appropriate in various implementations.

Fig. 12 illustrates a block diagram of processing module 160 in accordance with an embodiment of the disclosure. In the illustrated embodiment, processing module includes a sensor input block 1201, a digital signal processing (DSP) core 1206, a video output block 1207, a one time programmable (OTP) memory 1212, an inter-integrated circuit (I2C)

interface 1214, a general purpose CPU 1216, a system control block 1220, a system support block 1222, a memory management unit (MMU) 1230, and memory blocks 1240.

Sensor input block 1201 receives thermal image frames from infrared sensor assembly 128 which correspond to thermal images captured by infrared sensors 132. In this regard, sensor input block 1201 includes an FPA interface 1202 to receive the thermal image frames and an integration block 1204 to integrate the thermal image frames (e.g., provided in form of analog or digital signals) over multiple thermal image frames to provide, for example, thermal image frames with improved signal to noise characteristics.

DSP core 1206 may be used to perform any of the various operations described herein to process thermal image data and/or related operations. For example, in some embodiments, DSP core 1206 may be used to implement pipeline 800 of Fig. 8. DSP core 1206 may be implemented as any appropriate processing device.

Video output block 1207 provides processed thermal image frames from processing module to other components of infrared imaging module 100, host device 102, and/or other devices through one or more mobile industry processor interfaces (MIPI) 1208 and/or one or more serial peripheral interfaces (SPI) 1210.

OTP memory 1212 (e.g., including one or more OTP memory blocks) may be implemented with appropriate control circuitry and non-volatile memory used to store various previously determined data for use in the various operations described herein. Such data may include, but need not be limited to, factory gain terms 812 and factory offset terms 816 (e.g., collectively and separately referred to as factory calibration terms), bad pixel maps/lists, pixel deltas and weights for distortion correction, look up tables (LUT) for color, polarity, and gamma corrections, and/or other data as appropriate. Although OTP memory 1212 is generally referred to herein, any type of volatile or non-volatile memory may be used in addition to and/or instead of OTP memory 1212 as may be appropriate in various implementations.

I2C interface 1214 may be used to support communications between processing module 160 and host device 102. General purpose CPU 1216 (e.g., also referred to as a GPP core) may be used to perform various operations to support the overall operation of processing module 160 including, for example, servicing communications and commands over I2C interface 1214, initializing data and DSP core 1206, power management, write sequencing for OTP memory block 1212, direct memory access (DMA) operations, memory mapping and configuration, configuration of DSP core 1206, configuration of

video output block 1207, calibration support, and/or other operations. GPP core 1216 may be implemented as any appropriate processing device.

System control block 1220 (e.g., also referred to as a PPM block) may be used to generate clocks and reset signals, and provide on-chip power control. System support block 1222 may be used to perform various die test and CPU debugging operations, and provide one or more joint test action group (JTAG) interfaces (e.g., IEEE 1149.1 standard test access port and boundary-scan architecture).

Memory management unit (MMU) 1230 (e.g., a memory controller) may be used to manage data communications between OTP memory 1212, memory blocks 1240, and other components of processing module 160. For example, in some embodiments, MMU 1230 may pass data over various buses 1260 connected to MMU 1230 as illustrated in Fig. 12. Thus, OTP memory 1212, MMU 1230, and memory blocks 1240 may effectively provide a memory system 1250 to support line based processing of thermal images and various operations described herein. In this regard, memory system 1250 may provide a switch fabric to selectively route data between components of processing module 160 and the various memories of memory system 1250. Such a switch fabric may be provided, for example, by MMU 1230 and/or additional circuitry of OTP memory 1212 and/or memory blocks 1240.

Memory blocks 1240 may be implemented, for example, as volatile static random access memory (SRAM) including main memory slices (MMSs) 1242 and virtual line buffers (VLBs) 1244 further described herein. In one embodiment, memory blocks 1240 may include 3 Mbits of SRAM, with approximately 2.5 Mbits allocated to MMSs 1242 (e.g., each MMS 1242 may include approximately 256 kbits of SRAM) and approximately 0.5 Mbits allocated to all of VLBs 1244 (e.g., each of 64 VLBs 1244 may include approximately 8 kbits of SRAM). Other implementations and configurations of volatile and/or non-volatile memory are also contemplated.

Fig. 13 illustrates a block diagram of an MMS 1242 of memory system 1250 in accordance with an embodiment of the disclosure. MMS 1242 includes a memory block 1302 and access circuitry 1304 providing a switch fabric for MMS 1242. In one embodiment, memory block 1302 may be implemented as a 256 kbit SRAM memory block having a single interface 1306 (e.g., also referred to as an SRAM access port) adapted to support a single read or write operation at a time. Access circuitry 1304 may be used to permit one or more components of processing module 160 to access memory block 1302

through multiple ports 1312 and 1314 (e.g., memory bus ports). Components of processing module 160 may also be referred to as owners of MMS 1242 when MMS 1242 is configured for access by such components. Access circuitry 1304 includes a multiplexer 1308, a port select input 1310, and ports 1312 and 1314 (e.g., each port providing read and write access in one embodiment). In some embodiments, access circuitry 1304 may be implemented with additional circuitry and/or logic as appropriate.

In one embodiment, MMU 1230 and access circuitry 1304 may be used to permit simultaneous or substantially simultaneous access to memory block 1302 by multiple components of processing module 160. In this regard, MMU 1230 may be connected to port select input 1310 and ports 1312 and 1314 to manage access to memory block 1302 by other components of processing module 160. For example, MMU 1230 may pass data between any of the various components of processing module 160 and memory block 1302 through ports 1312 and 1314.

Fig. 14 illustrates a block diagram of a VLB 1244 of memory system 1250 in accordance with an embodiment of the disclosure. VLB 1244 includes a memory block 1402 and a switch fabric 1404. In one embodiment, memory block 1402 may be implemented as an 8 kbit SRAM memory block having a single interface 1403 (e.g., also referred to as an SRAM access port and shown in Fig. 15 as interfaces 1403A-D for memory blocks 1402A-D of memory buffers 1244A-D) adapted to support a single read or write operation at a time. Switch fabric 1404 may be used to permit one or more components of processing module 160 to access memory block 1402 through multiple ports 1420 (e.g., memory bus ports labeled MB_0 through MB_3). Although four ports 1420 are shown in Fig. 14, any desired number of ports 1420 may be provided. Similar to MMS 1242, components of processing module 160 may also be referred to as owners of VLB 1244 when VLB 1244 is configured for access by such components.

In Fig. 14, switch fabric 1404 is represented by arrows and may also include one or more multiplexers 1431 used to select between ports 1420. VLB 1244 may also include one or more state machines 1430, clock switches 1432, and/or other circuits 1433, any of which may be provided as part of, or separate from, switch fabric 1404. VLB 1244 receives control signals 1408, for example, from MMU 1230 which cause VLB 1244 to be configured to permit various components of processing module 160 to access memory block 1402. In one embodiment, a state machine 1430 may operate multiplexers 1431 in response to control signals 1408 to selectively couple memory block 1402 with one or

more ports 1420. In this regard, in one embodiment, control signals 1408 may be used to: define the owner of VLB 1244 (signal Def_Owner); identify the next owner of VLB 1244 (signal New_Owner); switch to the next owner through a signal transition (signal Switch_Owner); and provide a clock for state machine 1430 (signal MMU_CLK). VLB 1244 also provides control signal 1410 (signal Cur_Owner) to identify the current owner of VLB 1244.

Each port 1420 may receive corresponding input signals 1412 from a particular component of processing module 160 in communication with VLB 1244 through buses 1260 and/or MMU 1230. In one embodiment, input signals 1412 may include: a clock signal (signal MBx_CLK); an address signal (signal MBx_ADDR); a read signal (signal MBx_RD); a write signal (signal MBx_WR); and one or more additional signals (signal MBx_).

Memory block 1402 may be synchronized by the particular clock signal MBx_CLK of the particular port 1420 to which memory block 1402 is currently connected. For example, while memory block 1402 is associated with port MB_0, memory block 1402 may be synchronized by clock signal MB0_CLK. If memory block is subsequently associated with port MB_1 (e.g., based on control signals 1408), then memory block 1402 may be synchronized by clock signal MB1_CLK. In this regard, one or more clock switches 1432 may be used to permit such changes in clock synchronization. For example, one or more clock switches 1432 may be used to provide glitchless transitions between different clock signals provided to memory block 1402. Accordingly, ownership of memory block 1402 may be rapidly switched between various components of processing module 160 running independent clocks and without requiring clock resampling or resynchronization across different clock domains (e.g., which could otherwise result in extra indeterminate latency clock cycles lost for each clock domain crossing). In one embodiment, if no clock signal is available for a selected port 1420, then memory block 1402 may be synchronized by clock signal MMU_CLK of control signals 1408.

Each port 1420 may exchange data signals 1414 (signals MBx_D) with its associated component of processing module 160 through buses 1260 and/or MMU 1230. In some embodiments, data signals 1414 of different ports 1420 may be used simultaneously. For example, in one embodiment, data may be passed from memory block 1402 to several components of processing module 160.

Fig. 15 illustrates a block diagram of a portion of memory system 1250 in communication with various components of processing module 160 in accordance with an embodiment of the disclosure. As shown, memory system 1250 is in communication with sensor interface 1201, DSP core 1206, video interface 1207, and GPP core 1216 over buses 1260. However, such communication may be provided with fewer or greater numbers of components of processing module 160 or other devices in other embodiments.

MMU 1230 manages the passing of input signals 1412 and data signals 1414 between buses 1260 and VLBs 1244 (e.g. labeled 1244A-D in Fig. 15) through one or more communication channels 1510 (e.g., hardware circuit paths, multiplexed communications, and/or other forms as appropriate), some of which are shown with specific paths and others are shown more generally as a cloud in Fig. 15. In this regard, MMU 1230 may be implemented, for example, with a memory controller 1502 and/or other circuitry as appropriate to generate control signals 1408 and to control communication channels 1510.

For example, in some embodiments, memory controller 1502 may be configured with a predetermined instruction sequence (e.g., provided on a non-transitory machine readable medium) that is optimized for pipeline 800 and/or the operations shown in Figs. 16A-E. In this regard, memory controller 1502 may generate control signals 1408 to independently operate each of switch fabric blocks 1404A-D to support data transfers between various components for thermal image processing and/or other operations.

As discussed, each VLB 1244 may be implemented with a memory block 1402 (e.g., labeled 1402A-D in Fig. 15) and a switch fabric 1404 (e.g., labeled 1404A-D in Fig. 15). Control signals 1408 provided by MMU 1230 may be used to control the switch fabric 1404 of each VLB 1244 to selectively pass input signals 1412 and data signals 1414 through particular ports 1420 (e.g., labeled 1420A-D for VLBs 1244A-D).

In the embodiment shown in Fig. 15, a corresponding communication channel 1510 is provided between each of sensor interface 1201, DSP core 1206, video interface 1207, and GPP core 1216 and one of the ports 1420 of each VLB 1244. As a result, such components may share and pass data (e.g., any desired type of information, messages, and/or other content) between each other using memory system 1250. For example, in one embodiment, sensor interface 1201 may be an owner of SRAM 1402A of VLB 1244A and may access SRAM 1402A through the first port of VLB 1244A. It may be desired to share the data in SRAM 1402A with DSP core 1206 (e.g., for further processing). In this case, memory controller 1502 of MMU 1230 may generate control signals 1408 to operate

switch fabric 1404A to select the second port of VLB 1244A. As a result, DSP core 1206 may now be the owner of SRAM 1402A and thus access SRAM 1402A to read or write data therewith.

In another embodiment, MMU 1230 and/or switch fabric 1404 may be configured to permit multiple components to receive data signals 1414 over multiple communication channels 1510 from a single SRAM 1402. Accordingly, such an embodiment provides another flexible approach for sharing data of SRAMs 1402.

In another embodiment, different components of processor module 160 may be connected to different combinations of VLBs 1244 (e.g., different subsets of VLBs 1244). For example, a first one of VLBs 1244 may be configured to communicate with a first subset of components over a first set of buses 1260, and a second one of VLBs 1244 may be configured to communicate with a second subset of components over a second set of buses 1260. In some embodiments, the first and second subsets of components and buses 1260 may be the same as each other. In other embodiments, the first and second subsets of components and buses 1260 may be different from each other (e.g., the subsets may have some or none of the same components and buses 1260 in common with each other).

Data may be passed between one or more intermediate components and/or SRAMS 1402. For example, if communication channels 1510 are provided: between sensor interface 1201 and only VLBs 1244A-B; between DSP core 1206 and only VLBs 1244B-C; between video interface 1207 and only VLBs 1244C-D; and between GPP core 1216 and only VLB 1244D, then intermediate data passing may be performed to share data from SRAM 1402A with GPP core 1216. In this case, data in SRAM 1402A could be provided to GPP core 1216, for example, by: sensor interface 1201 reading data from SRAM 1402A and writing the data into SRAM 1402B, DSP core 1206 reading the data from SRAM 1402B and writing the data into SRAM 1402C, and video interface 1207 reading the data from SRAM 1402C and writing the data into SRAM 1402D, and GPP core 1216 reading the data from SRAM 1402D. Other data sharing combinations are also contemplated.

Figs. 16A-E illustrate various operations performed by memory system 1250 and DSP core 1206 in accordance with embodiments of the disclosure. For example, in some embodiments, at least some of the operations of Figs. 16A-E may correspond to operations of pipeline 800 of Fig. 8.

In some embodiments, the operations of Figs. 16A-E may be performed in a line based manner. In this regard, individual lines (e.g., rows or columns) of an image frame

may be passed through different pipeline stages illustrated in Figs. 16A-E. Such an approach permits individual VLBs 1244 to be efficiently used to store data associated with a particular line of a thermal image frame. Thus, the processing of different lines of a thermal image frame may be distributed among different VLBs 1244 and different pipeline stages during the operations of Figs. 16A-E. Such data may also be shared by various components of processing module 160 as described. Although line based processing is described primarily with regard to Figs. 16A-E, such line based processing may be similarly implemented in any of the operations of the present disclosure as desired.

Figs. 16A-E identify various types of data passed between portions of memory system 1250 and DSP core 1206. In general, the various types of data identified in Figs. 16A-E, and similar data, may be referred to as thermal image data (e.g., data that includes at least a portion of a captured thermal image, data used in the processing of thermal images, and/or any data associated with such processing).

In one embodiment, various data identified as "OTP" may be stored by OTP memory 1212. In one embodiment, data that is less than approximately 8kbits may be stored by VLBs 1244. Such data may be referred to as rows, row buffers, line history, LUTs, and/or other terms. Such data may be of various sizes as set forth in Figs. 16A-E or other sizes (e.g., 60x1x8bits, 80x1x8bits, 80x1x16bits, 81x1x16bits, 1x256x8bits, and/or other sizes). In this regard, VLBs 1244 may be used primarily to store data for individual lines (e.g., individual rows or columns) for line based processing of thermal image frames.

In one embodiment, data that is greater than approximately 8kbits and less than approximately 256 kbits may be stored by MSSs 1242. Such data may be referred to as full frame buffers, double full frame buffers, histograms, and/or other terms. Such data may be of various sizes as set forth in Figs. 16A-E or other sizes (e.g., 80x60x8bits, 80x60x16bits, 80x60x32bits, 1x2048x8bits, and/or other sizes). In this regard, MSSs 1244 may be used primarily to store data for one or more thermal image frames (e.g., MMSs 1244 may be used as full frame buffers in some embodiments).

Referring now to Fig. 16A, data 1602 includes an image frame 802 (e.g., a thermal image frame) received from infrared sensor assembly 128 for processing in one or more pipeline stages corresponding to blocks 810, 814, 580, 818, and 822 of Fig. 8. As shown, data 1602 may be received as a full image frame 802 and provided on a line by line basis through a VLB 1244 for processing. In some embodiments, image frame 802 may be

approximately 80 by 60 pixels, and individual lines may be approximately 80 pixels or fewer, or approximately 60 pixels or fewer.

Data 1604 includes factory gain terms 812, factory offset terms 816 (e.g., including pixel offsets/coefficients and LaGrange offsets/coefficients in one embodiment), NUC terms 817, column FPN terms 820, and row FPN terms 824 received from various memories and/or provided in accordance with various processing as shown.

In some embodiments, a plurality of NUC terms 817 may be determined for an unblurred thermal image frame from an intentionally blurred thermal image frame. NUC terms 817 associated with a single one of the individual lines may be stored in a VLB 1244 and applied to the individual lines.

In some embodiments, a plurality of factory calibration terms 812/816 may be read from OTP memory block 1212. Factory calibration terms 812/816 associated with a single one of the individual lines may be stored in a VLB 1244 and applied to the individual lines.

An individually processed line is provided as data 1606 stored in a VLB 1244 operating as a pipeline register to be used for LaGrange calculations in one or more pipeline stages corresponding to block 814. Following block 814, processed line data (e.g., adjusted by offsets and coefficients) is passed to Fig. 16B.

Referring now to Fig. 16B, processed line data 1620 received from Fig. 16A is stored in a VLB 1244 operating as a pipeline register and is provided for temporal filtering operations in one or more pipeline stages corresponding to block 826. Block 826 uses data 1630 which includes various lines and image frames that have been buffered, accumulated, and/or otherwise stored as shown. In particular, data 1630 may include multiple image frames that are accumulated to provide a blurred image frame in an accumulation frame buffer, individual lines of the current and accumulated image frames, local (e.g., adjacent) lines, a previous image frame, temporary lines, lines from multiple previous frames, and local line changes from previous image frames. Accordingly, in some embodiments, at least some of data 1630 corresponds to various data referenced in Figs. 8-10.

In some embodiments, a current thermal image frame may be compared with a previous thermal image frame to determine whether a scene has changed in block 826. For example, a first set of individual lines may be buffered in a first set of corresponding memory buffers (e.g., local pixel history line buffers in one embodiment) that correspond to a subset of the current thermal image frame. A second set of individual lines may be buffered in a second set of corresponding memory buffers (e.g., previous frame line buffers

in one embodiment) that correspond to a subset of a previous thermal image frame. The first and second sets of buffered individual lines may be compared to determine if a scene has changed (e.g., changes between the buffered lines of the thermal image frames may be buffered using one or more local kernel line buffers in one embodiment). If the scene has changed, then the current and/or previous thermal image frames may be accumulated (e.g., in a blur-frame accumulation frame buffer in one embodiment).

Following block 826, processed line data 1638 (e.g., temporally filtered line data) is stored in a VLB 1244 operating as a pipeline register and is provided for bad pixel replacement operations in one or more pipeline stages corresponding to block 827. Data 1640 includes bad pixels maps/lists provided by OTP memory 1212 as well as various lines that have been buffered, accumulated, and/or otherwise stored for processing in block 827 as shown. In particular, data 1640 may include local lines, a bad pixel map provided as a full frame and temporary lines, and local lines containing the bad pixel map.

In some embodiments, one or more pixels of a thermal image frame may be replaced in block 827. For example, a first set of individual lines may be buffered in a first set of corresponding memory buffers (e.g., local kernel line buffers) that correspond to a subset of the thermal image frame. A second set of individual lines may be buffered in a second set of corresponding memory buffers (e.g., local line buffers) that correspond to a subset of a pixel map. One or more pixels of the first set of individual lines may be replaced based on the second set of individual lines. Following block 827, processed line data (e.g., with bad pixels replaced) is passed to Fig. 16C.

Referring now to Fig. 16C, processed line data 1650 received from Fig. 16B is stored in a VLB 1244 operating as a pipeline register and is provided for distortion processing operations (e.g., to compensate for warping or distortion effects caused by one or more optical elements and/or other sources) in one or more pipeline stages corresponding to block 828. Data 1655 includes various pixel deltas and weights, and bad pixel maps provided by OTP memory 1212 (e.g., collectively and separately referred to as distortion correction terms). In particular, data 1655 may include pixel deltas, pixel weights, and bad pixel maps buffered in full frames and in individual lines.

In some embodiments, individual lines of a thermal image frame may be corrected to compensate for distortion. For example, a plurality of distortion correction terms may be read from OTP memory block 1212. Distortion correction terms associated with a single one of the individual lines may be stored in a VLB 1244 and applied to the individual lines.

Following block 828, processed line data 1660 (e.g., de-warped line data) is stored in a VLB 1244 operating as a pipeline register and is provided for video polarity processing, gamma correction processing, automatic gain compensation processing, and pseudo-color processing in one or more pipeline stages corresponding to blocks 829, 830, 831, and 832. Data 1665 includes various LUT information provided by OTP memory 1212, histograms, and calculated values as shown.

In some embodiments, LUT data may be used in the processing performed in blocks 829, 830, 831, and 832. For example, LUT data may be read from OTP memory block 1212. LUT data associated with a single one of the individual lines may be stored in a VLB 1244 and applied to the individual lines. Following blocks 829, 830, 831, and 832, processed line data (e.g., processed by blocks 829, 830, 831, and 832) for a result image frame 833 (e.g., a result thermal image frame) is provided and stored in a VLB 1244 operating as a pipeline register.

Referring now to Fig. 16D, data 1670 includes accumulated thermal image frames (e.g., provided in accordance with block 535) received as full thermal image frames and provided as individual lines for processing in one or more pipeline stages corresponding to blocks 540 and 545. In particular, data 1670 may include multiple image frames that are accumulated to provide a blurred image frame in an accumulation frame buffer and individual lines of the accumulated image frames.

Following blocks 540/545, processed line data 1672 (e.g., blurred averaged accumulated lines) is stored in various VLBs 1244 operating as pipeline registers and multiple lines are buffered as a full image frame in an MMS 1242. Data 1672 is provided for processing in one or more pipeline stages corresponding to blocks 550 and 555.

Block 550 also uses data 1674 which includes previous line data. Block 550 also provides column FPN terms 820 and row FPN terms 824 as part of data 1674 which is provided to Fig. 16A as shown. Block 550 also provides column noise estimates 1676 and row noise estimates 1678 to block 555 which are stored in VLBs 1244 operating as pipeline registers.

In some embodiments, a previous thermal image frame may be used to determine column FPN terms 820 and row FPN terms 824. For example, a set of individual lines may be buffered in a set of corresponding memory buffers that correspond to a subset of the previous thermal image frame. The lines of the previous thermal image frame may be processed to determine row and column noise terms for the current thermal image frame.

Block 555 uses data 1672, 1676, and 1678 to provide processed line data 1680 (e.g., with column and row noise removed) which is stored in a VLB 1244 operating as a pipeline register. Blocks 560, 565, 570, 571, 572, 573, and 575 use data 1680 and 1682 (e.g., including buffered line data and NUC terms 817) and operate as one or more pipeline stages to provide NUC terms 817 to Fig. 16A as shown. In particular, data 1682 may include individual lines of NUC terms 817.

Referring now to Fig. 16E, further operations of block 831 are identified. In this regard, block 831 uses data 1690 that includes histogram and LUT information as shown for processing in one or more pipeline stages and to communicate such data with Fig. 16C as shown.

In view of the present disclosure, it will be appreciated that line based processing of thermal image frames may be performed in an efficient pipelined manner, thus distributing processing tasks into smaller tasks than conventional frame based processing. Such line based processing may be efficiently used with hardware and software optimized for fast and efficient processing, such as relatively small memory buffers with single interface memory blocks may be used with associated switch fabric circuitry to support efficient line based processing.

In this regard, memory system 1250 may be efficiently and flexibly utilized by processing module 160 to provide individual components with memory access through associated buses 1260, rather than a conventional main memory system shared system bus. In addition, by passing clock signals from individual components over buses 1260, individual memory blocks of memory system 1260 may be separately synchronized with their associated components (e.g., owners).

In addition, as discussed, memory system 1250 may be used to transfer (e.g., move, copy, and/or otherwise pass) and share data between individual components without requiring a centralized memory system to perform such transfers through conventional read and write commands and/or direct memory access (DMA) engines. For example, control signals 1408 may be used to change the particular port 1420 of a VLB 1244, thus effectively transferring the data of its associated memory block 1402 to be used by a different component associated with a different port 1420 of the same VLB 1244. As discussed, data may also be transferred to different memory blocks 1402 my individual components as desired.

Other embodiments are also contemplated. In some embodiments, various system implementations described herein may be scaled for increased capacity and/or performance as desired for various implementations. For example, it is contemplated that one or more additional components (e.g., local or remote to processing module 160) may be networked or otherwise interfaced with memory system 1260 and/or processing module 160 to use the various features thereof. It is also contemplated that the various components of memory system 1260 may be may be scaled to accommodate such additional components and/or to improve performance.

Where applicable, various embodiments provided by the present disclosure can be implemented using hardware, software, or combinations of hardware and software. Also where applicable, the various hardware components and/or software components set forth herein can be combined into composite components comprising software, hardware, and/or both without departing from the spirit of the present disclosure. Where applicable, the various hardware components and/or software components set forth herein can be separated into sub-components comprising software, hardware, or both without departing from the spirit of the present disclosure. In addition, where applicable, it is contemplated that software components can be implemented as hardware components, and vice-versa.

Software in accordance with the present disclosure, such as non-transitory instructions, program code, and/or data, can be stored on one or more non-transitory machine readable mediums. It is also contemplated that software identified herein can be implemented using one or more general purpose or specific purpose computers and/or computer systems, networked and/or otherwise. Where applicable, the ordering of various steps described herein can be changed, combined into composite steps, and/or separated into sub-steps to provide features described herein.

Embodiments described above illustrate but do not limit the invention. It should also be understood that numerous modifications and variations are possible in accordance with the principles of the invention. Accordingly, the scope of the invention is defined only by the following claims.

CLAIMS

What is claimed is:

1. A method comprising:

receiving a thermal image frame comprising a plurality of individual lines, wherein each individual line comprises substantially an entire row or column of thermal image data captured by a plurality of infrared sensors;

providing each individual line of the thermal image frame to a line based image processing pipeline;

performing image processing operations on the individual lines in stages of the image processing pipeline; and

buffering the individual lines in the pipeline stages.

2. The method of claim 1, wherein the image processing operations comprise:

storing a plurality of factory calibration terms associated with a single one of the individual lines in a memory buffer; and

applying the stored factory calibration terms to the one of the individual lines.

3. The method of claim 1, wherein the thermal image frame is a current thermal image frame, wherein the image processing operations comprise:

buffering a first set of the individual lines comprising a subset of the current image frame in a first set of corresponding memory buffers of a memory system;

buffering a second set of individual lines comprising a subset of a previous thermal image frame in a second set of corresponding memory buffers of the memory system;

comparing the first and second sets of individual lines to determine if a scene has changed; and

if the scene has changed, accumulating at least one of the image frames in an accumulation buffer of the memory system to provide a temporally filtered image frame.

4. The method of claim 1, wherein the image processing operations comprise:

buffering a set of the individual lines comprising a subset of the image frame in a first set of corresponding memory buffers;

buffering a subset of a pixel map in a second set of corresponding memory buffers; and

replacing one or more pixels of the individual lines based on the subset of the pixel map.

5. The method of claim 1, wherein the image processing operations comprise:

storing a plurality of distortion correction terms associated with a single one of the individual lines in a memory buffer; and

applying the distortion correction terms to the one of the individual lines.

6. The method of claim 1, wherein the image processing operations comprise:

storing look up table (LUT) data associated with a single one of the individual lines in a memory buffer; and

applying the LUT data to the one of the individual lines.

7. The method of claim 1, wherein the thermal image frame is a current thermal image frame, wherein the image processing operations comprise:

buffering a set of individual lines comprising a subset of a previous image frame in a set of corresponding memory buffers; and

processing the individual lines of the previous thermal image frame to determine row and column noise terms for the current thermal image frame.

8. The method of claim 1, wherein the thermal image frame is an unblurred thermal image frame, wherein the image processing operations comprise:

determining a plurality of non-uniform correction (NUC) terms for a single one of the individual lines of the unblurred thermal image frame from an intentionally blurred thermal image frame;

storing the NUC terms associated with a single one of the individual lines in a memory buffer; and

applying the stored NUC terms to the one of the individual lines.

9. The method of claim 1, wherein each individual line comprises approximately 80 pixels or fewer.

10. The method of claim 1, further comprising:

operating a switch fabric to couple a first port of a memory buffer with a memory block of the memory buffer, wherein the memory block comprises a single interface adapted to support a single read or write operation at a time;

transferring a first one of the individual lines between a first component and the memory block over a first bus, through the first port, and through the single interface;

subsequently operating the switch fabric to couple a second port of the memory buffer with the memory block; and

transferring a second one of the individual lines between a second component and the memory block over a second bus, through the second port, and through the single interface.

11. An infrared imaging module comprising:

a sensor input block adapted to receive a thermal image frame comprising a plurality of individual lines, wherein each individual line comprises substantially an entire row or column of thermal image data captured by a plurality of infrared sensors;

a processing device comprising a line based image processing pipeline adapted to perform image processing operations on the individual lines in stages of the image processing pipeline; and

a memory system adapted to buffer the individual lines in the pipeline stages.

12. The infrared imaging module of claim 11, wherein the processing device is adapted to:

store factory calibration terms associated with a single one of the individual lines in a memory buffer of the memory system; and

apply the stored factory calibration terms to the one of the individual lines.

13. The infrared imaging module of claim 11, wherein the thermal image frame is a current thermal image frame,

wherein the memory system is adapted to:

buffer a first set of the individual lines comprising a subset of the current image frame in a first set of corresponding memory buffers of the memory system, and

buffer a second set of individual lines comprising a subset of a previous thermal image frame in a second set of corresponding memory buffers of the memory system; and

wherein the processing device is adapted to:

compare the first and second sets of individual lines to determine if a scene has changed, and

if the scene has changed, accumulate at least one of the image frames in an accumulation buffer of the memory system to provide a temporally filtered image frame.

14. The infrared imaging module of claim 11,

wherein the memory system is adapted to:

buffer a set of the individual lines comprising a subset of the image frame in a first set of corresponding memory buffers of the memory system, and

buffer a subset of a pixel map in a second set of memory buffers of the memory system; and

wherein the processing device is adapted to replace one or more pixels of the first set of individual lines based on the subset of a pixel map.

15. The infrared imaging module of claim 11, wherein the processing device is adapted to:

store a plurality of distortion correction terms associated with a single one of the individual lines in a memory buffer of the memory system; and

apply the distortion correction terms to the one of the individual lines.

16. The infrared imaging module of claim 11, wherein the processing device is adapted to:

store look up table (LUT) data associated with a single one of the individual lines in a memory buffer of the memory system; and

apply the LUT data to the one of the individual lines.

17. The infrared imaging module of claim 11, wherein the thermal image frame is a current thermal image frame,

wherein the memory system is adapted to buffer a set of individual lines comprising a subset of a previous image frame in a set of corresponding memory buffers of the memory system; and

wherein the processing device is adapted to process the individual lines of the previous thermal image frame to determine row and column noise terms for the current thermal image frame.

18. The infrared imaging module of claim 11, wherein the thermal image frame is an unblurred thermal image frame, wherein the processing device is adapted to:

determine a plurality of non-uniform correction (NUC) terms for a single one of the individual lines of the unblurred thermal image frame from an intentionally blurred thermal image frame;

store the NUC terms in a memory buffer of the memory system; and

apply the stored NUC terms to the one of the individual lines.

19. The infrared imaging module of claim 11, wherein each individual line comprises approximately 80 pixels or fewer.

20. The infrared imaging module of claim 11,

wherein the memory system is adapted to:

operating a switch fabric to couple a first port of a memory buffer with a memory block of the memory buffer, wherein the memory block comprises a single interface adapted to support a single read or write operation at a time;

transfer a first one of the individual lines between a first component and the memory block over a first bus, through the first port, and through the single interface;

subsequently operate the switch fabric to couple a second port of the memory buffer with the memory block; and

transfer a second one of the individual lines between a second component and the memory block over a second bus, through the second port, and through the single interface.

21. A device comprising:

a plurality of components adapted to transfer thermal image data;

a plurality of buses connected to the components; and

a memory system connected to the components by the buses, the memory system comprising a plurality of memory buffers, each memory buffer comprising:

a memory block comprising a single interface adapted to support a single read or write operation at a time,

a plurality of ports, wherein each port is adapted to communicate with a corresponding one of the components over a corresponding one of the buses, and

a switch fabric block adapted to selectively couple one of the ports with the memory block to permit transfer of at least a portion of the thermal image data between the corresponding one of the components and the memory block through the coupled port and the single interface.

22. The device of claim 21, wherein each memory buffer is adapted to store a different single line of a thermal image frame included in the thermal image data.

23. The device of claim 22, wherein each memory buffer is a pipeline register for a line based image processing pipeline used to process the thermal image frame.

24. The device of claim 21, wherein each port is adapted to receive a clock signal from the corresponding one of the components over the corresponding one of the buses, wherein the memory block is adapted to be synchronized by the clock signal received by the coupled port.

25. The device of claim 24, further comprising a clock switch adapted to switch between the clock signals to synchronize the memory block in a glitchless manner.

26. The device of claim 21, wherein the switch fabric comprises a multiplexer adapted to select the ports based on control signals received by the memory buffer.

27. The device of claim 26, wherein the memory system further comprises a memory controller adapted to provide the control signals to select the ports in accordance with a predetermined instruction sequence to transfer the thermal image data.

28. The device of claim 21, wherein:

a first subset of the components is connected to a first subset of the memory buffers by the buses, but is not connected to a second subset of the memory buffers by the buses; and

a second subset of the components is connected to the second subset of the memory buffers by the buses, but is not connected to the first subset of the memory buffers by the buses.

29. The device of claim 21, wherein:

a first one of the components adapted to communicate with a first one of the memory buffers and a second one of the memory buffers;

a second one of the components is adapted to communicate with the first memory buffer but not the second memory buffer; and

the first component is adapted to read the thermal image data from the second memory buffer and write the thermal image data to the first memory buffer to share the thermal image data with the second component.

30. The device of claim 21, wherein:

a first one of the components is an application specific integrated circuit (ASIC);

a second one of the components is a general purpose processor;

a third one of the components is a non-volatile memory block of the memory system; and

the memory block is a static random access memory (SRAM) block.

31. A method of operating a memory system and a plurality of components connected to the memory system by corresponding buses, the method comprising:

operating a switch fabric to couple a first port of a memory buffer with a memory block of the memory buffer, wherein the memory block comprises a single interface adapted to support a single read or write operation at a time, wherein the memory buffer is part of the memory system;

transferring first thermal image data between a first one of the components and the memory block over a first one of the buses, through the first port, and through the single interface;

subsequently operating the switch fabric to couple a second port of the memory buffer with the memory block; and

transferring second thermal image data between a second one of the components and the memory block over a second one of the buses, through the second port, and through the single interface.

32. The method of claim 31, further comprising storing in the memory buffer a single line of a thermal image frame included in the thermal image data.

33. The method of claim 32, wherein the memory buffer is a pipeline register for a line based image processing pipeline used to process the thermal image frame.

34. The method of claim 31, further comprising:

receiving a first clock signal from the first component over the first bus and at the first port;

receiving a second clock signal from the second component over the second bus and at the second port;

synchronizing the memory block by the first clock signal while the first port is coupled with the memory block; and

synchronizing the memory block by the second clock signal while the second port is coupled with the memory block.

35. The method of claim 34, further comprising switching between the first and second clock signals to synchronize the memory block in a glitchless manner.

36. The method of claim 31, further comprising receiving control signals at the memory buffer, wherein the operating steps are performed by a multiplexer of the switch fabric to select the first or second ports.

37. The method of claim 36, further comprising providing the control signals from a memory controller of the memory system to select the first or second ports in accordance with a predetermined instruction sequence to transfer the thermal image data.

38. The method of claim 31, wherein:

the memory system comprises a plurality of memory buffers;

a first subset of the components is connected to a first subset of the memory buffers by the buses, but is not connected to a second subset of the memory buffers by the buses; and

a second subset of the components is connected to the second subset of the memory buffers by the buses, but is not connected to the first subset of the memory buffers by the buses.

39. The method of claim 31, wherein:

the memory buffer is a first memory buffer;

the first component is adapted to communicate with the first memory buffer and a second memory buffer;

the second component is adapted to communicate with the first memory buffer but not the second memory buffer; and

the method further comprises:

reading the thermal image data from the second memory buffer using the first component, and

writing the thermal image data to the first memory buffer using the first component to share the thermal image data with the second component.

40. The method of claim 31, wherein:

the first component is an application specific integrated circuit (ASIC);

the second component is a general purpose processor;

a third one of the components is a non-volatile memory block of the memory system; and

the memory block is a static random access memory (SRAM) block.

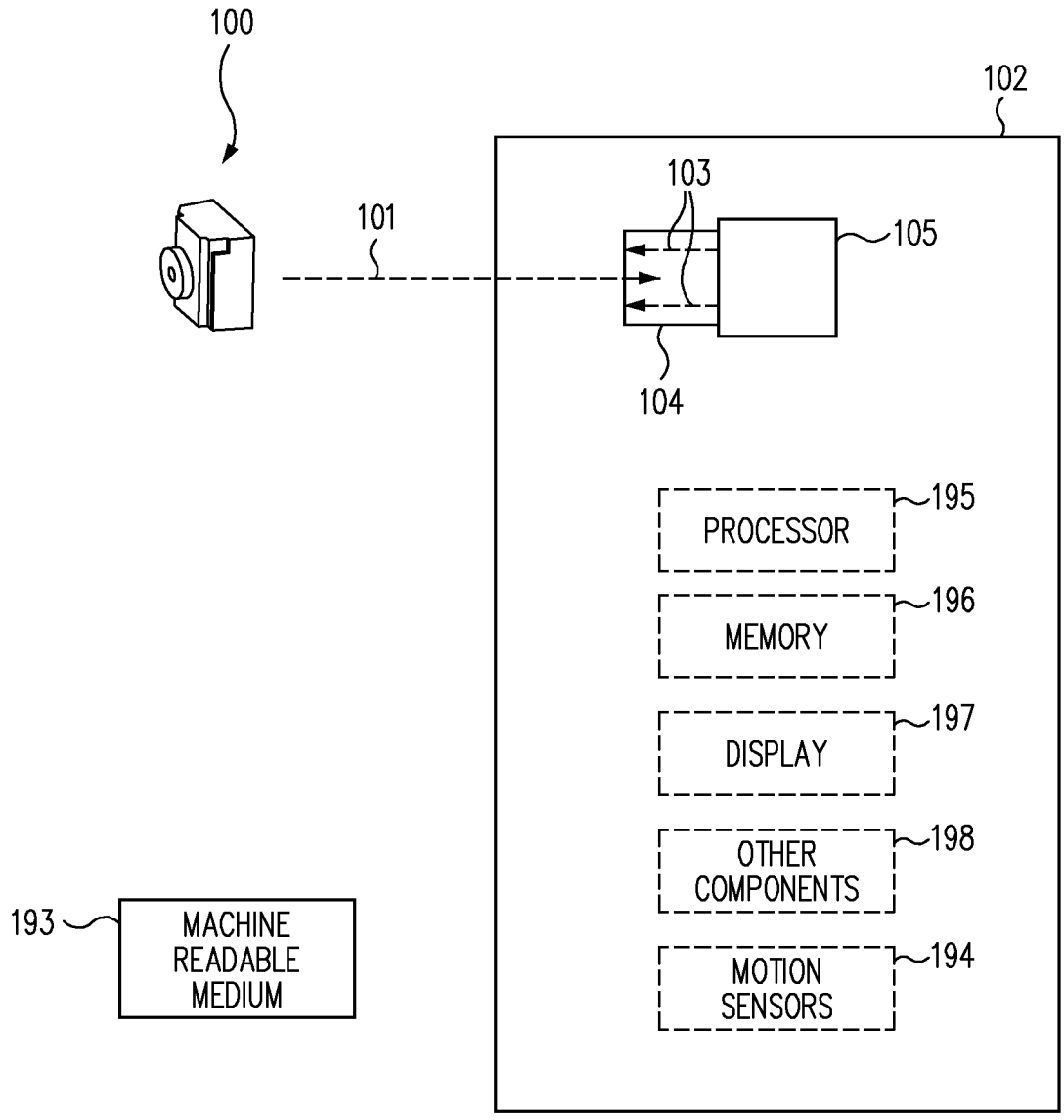

100
102
103
101
105
104
195
PROCESSOR
196
MEMORY
197
DISPLAY
198
OTHER COMPONENTS
194
MOTION SENSORS
193
MACHINE READABLE MEDIUM

FIG. 1

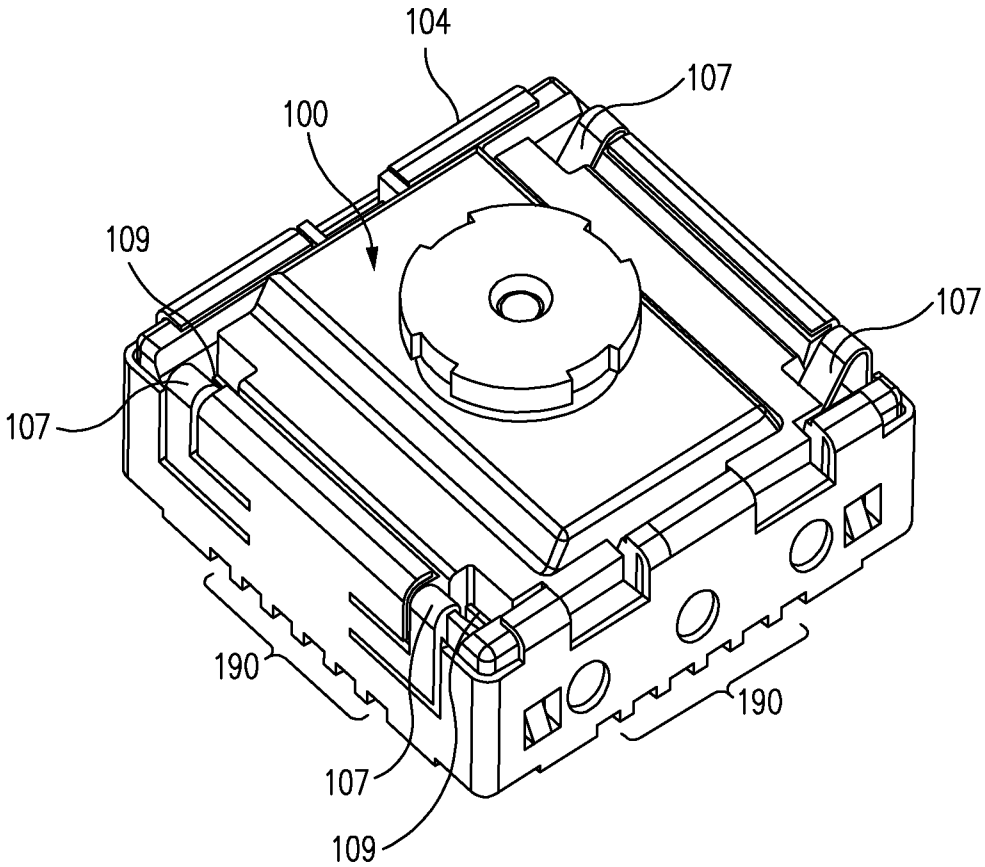


FIG. 2

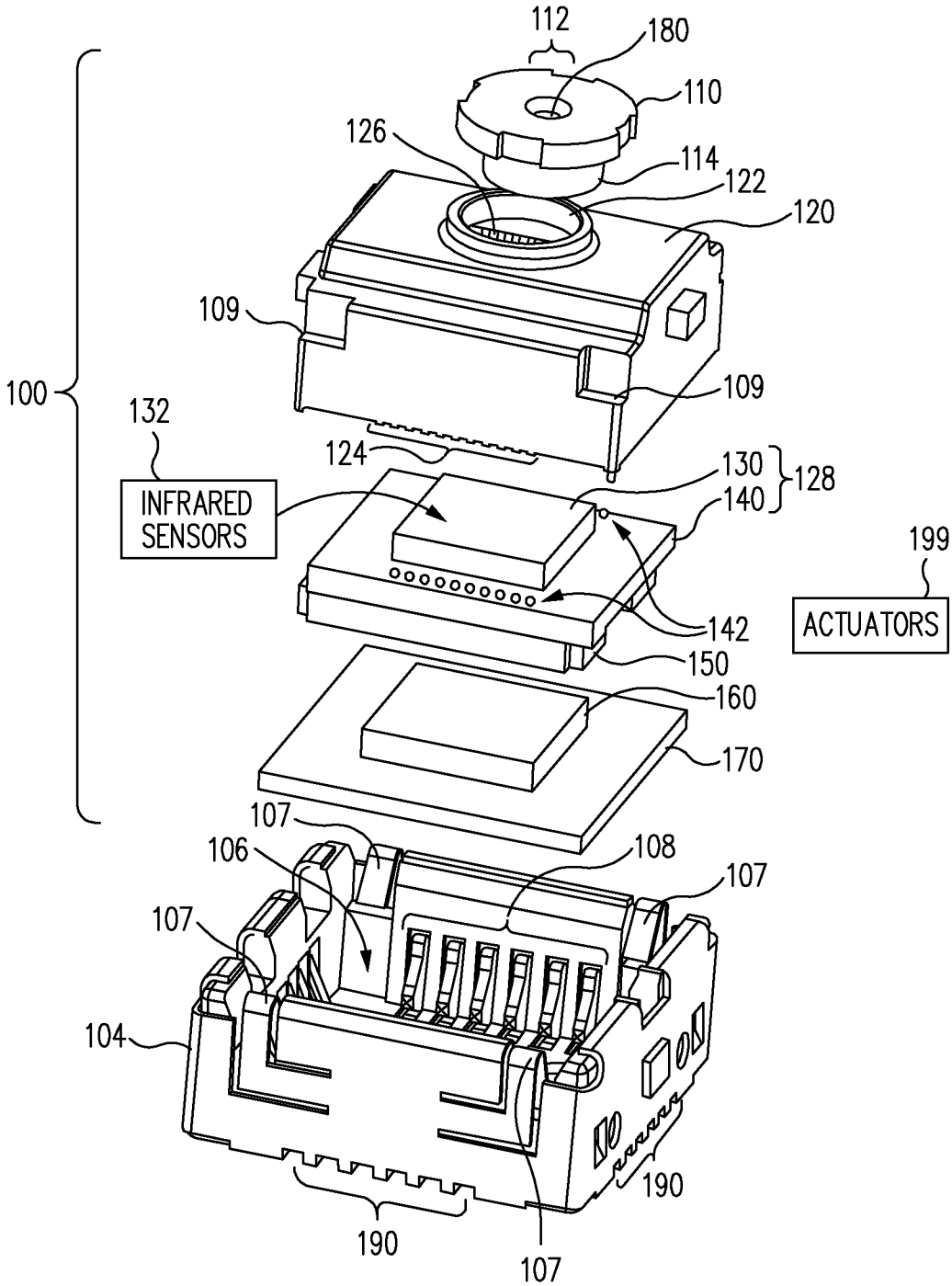

112
180
110
126
114
122
120
109
109
100
132
124
130
128
140
INFRARED SENSORS
199
ACTUATORS
142
150
160
170
107
106
108
107
107
104
190
190
107

FIG. 3

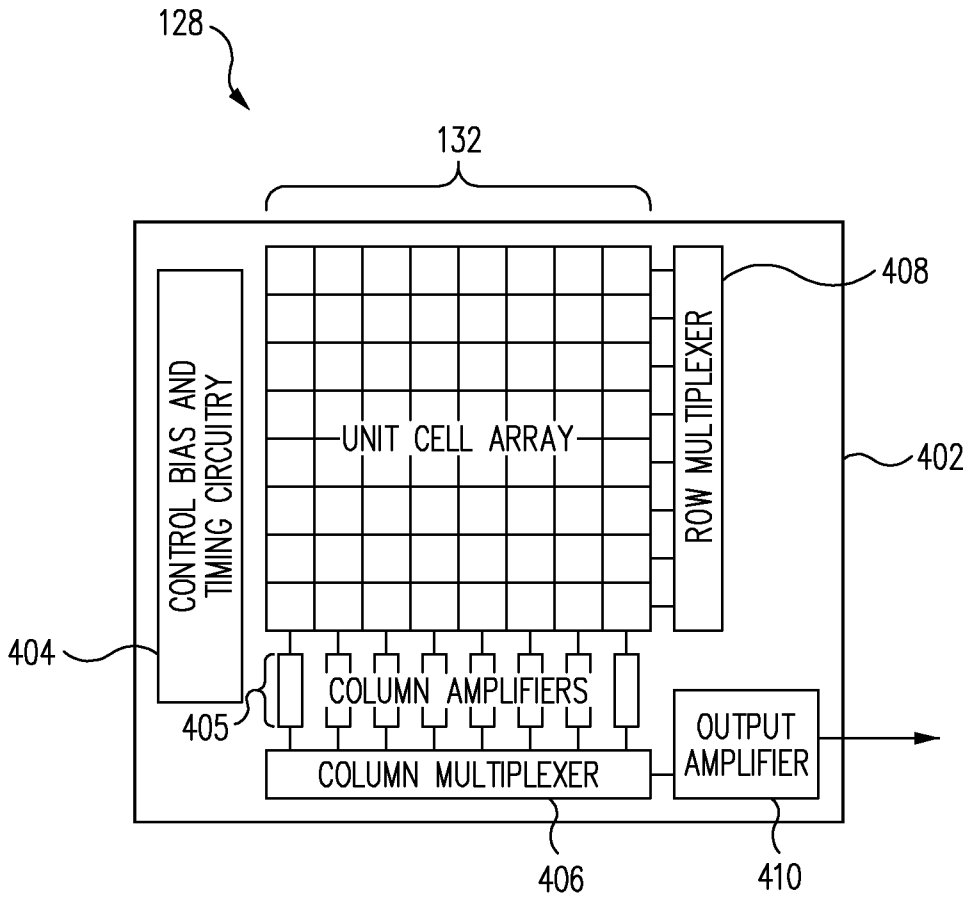

128
132
408
CONTROL BIAS AND TIMING CIRCUITRY
UNIT CELL ARRAY
ROW MULTIPLEXER
402
404
405
COLUMN AMPLIFIERS
OUTPUT AMPLIFIER
COLUMN MULTIPLEXER
406
410

FIG. 4

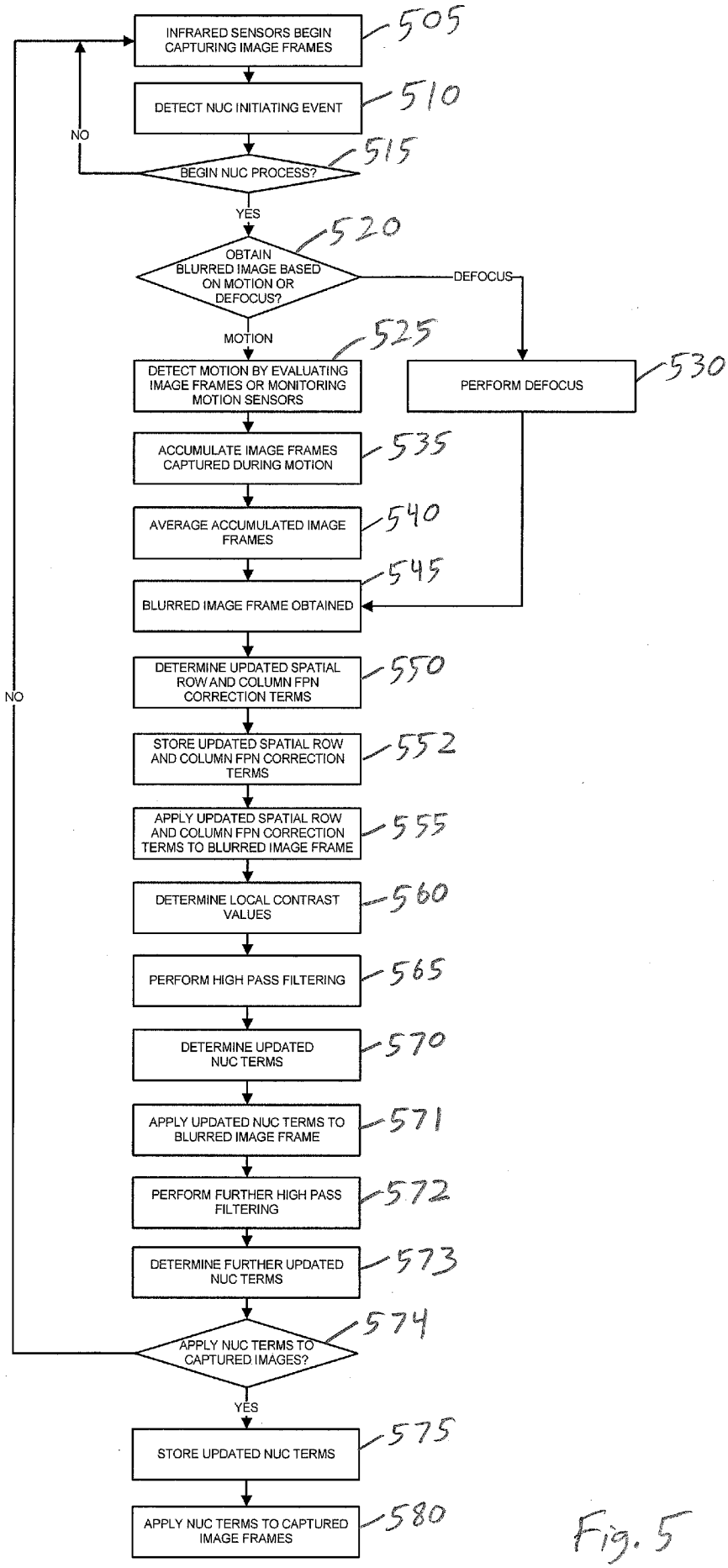

INFRARED SENSORS BEGIN CAPTURING IMAGE FRAMES
505
DETECT NUC INITIATING EVENT
510
NO
BEGIN NUC PROCESS?
515
YES
OBTAIN BLURRED IMAGE BASED ON MOTION OR DEFOCUS?
520
DEFOCUS
MOTION
DETECT MOTION BY EVALUATING IMAGE FRAMES OR MONITORING MOTION SENSORS
525
PERFORM DEFOCUS
530
ACCUMULATE IMAGE FRAMES CAPTURED DURING MOTION
535
AVERAGE ACCUMULATED IMAGE FRAMES
540
BLURRED IMAGE FRAME OBTAINED
545
DETERMINE UPDATED SPATIAL ROW AND COLUMN FPN CORRECTION TERMS
550
NO
STORE UPDATED SPATIAL ROW AND COLUMN FPN CORRECTION TERMS
552
APPLY UPDATED SPATIAL ROW AND COLUMN FPN CORRECTION TERMS TO BLURRED IMAGE FRAME
555
DETERMINE LOCAL CONTRAST VALUES
560
PERFORM HIGH PASS FILTERING
565
DETERMINE UPDATED NUC TERMS
570
APPLY UPDATED NUC TERMS TO BLURRED IMAGE FRAME
571
PERFORM FURTHER HIGH PASS FILTERING
572
DETERMINE FURTHER UPDATED NUC TERMS
573
APPLY NUC TERMS TO CAPTURED IMAGES?
574
YES
STORE UPDATED NUC TERMS
575
APPLY NUC TERMS TO CAPTURED IMAGE FRAMES
580

Fig. 5

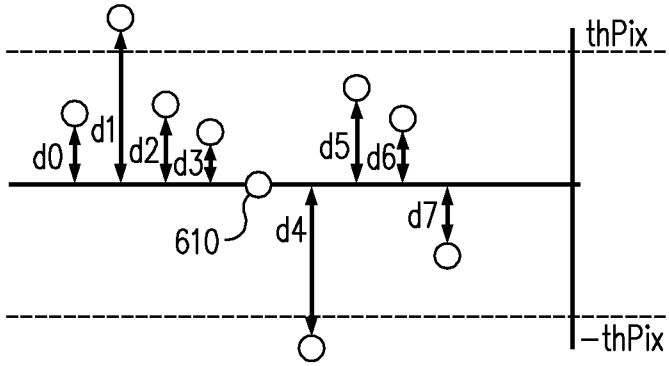

thPix
d0
d1
d2
d3
d5
d6
d7
610
d4
-thPix

FIG. 6

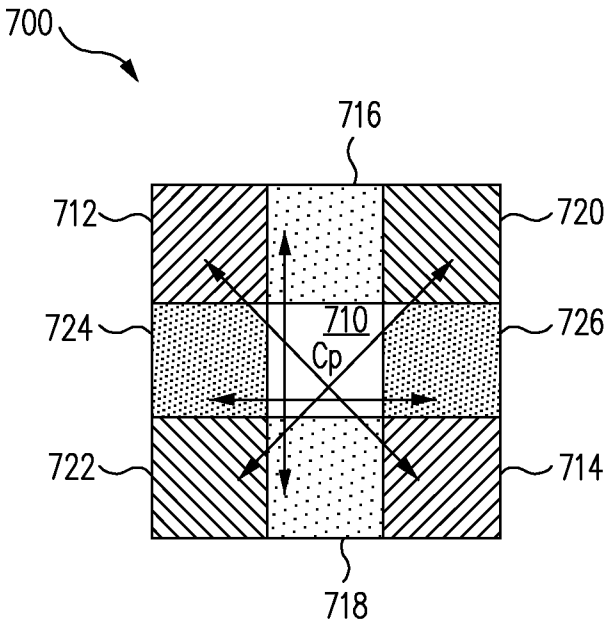
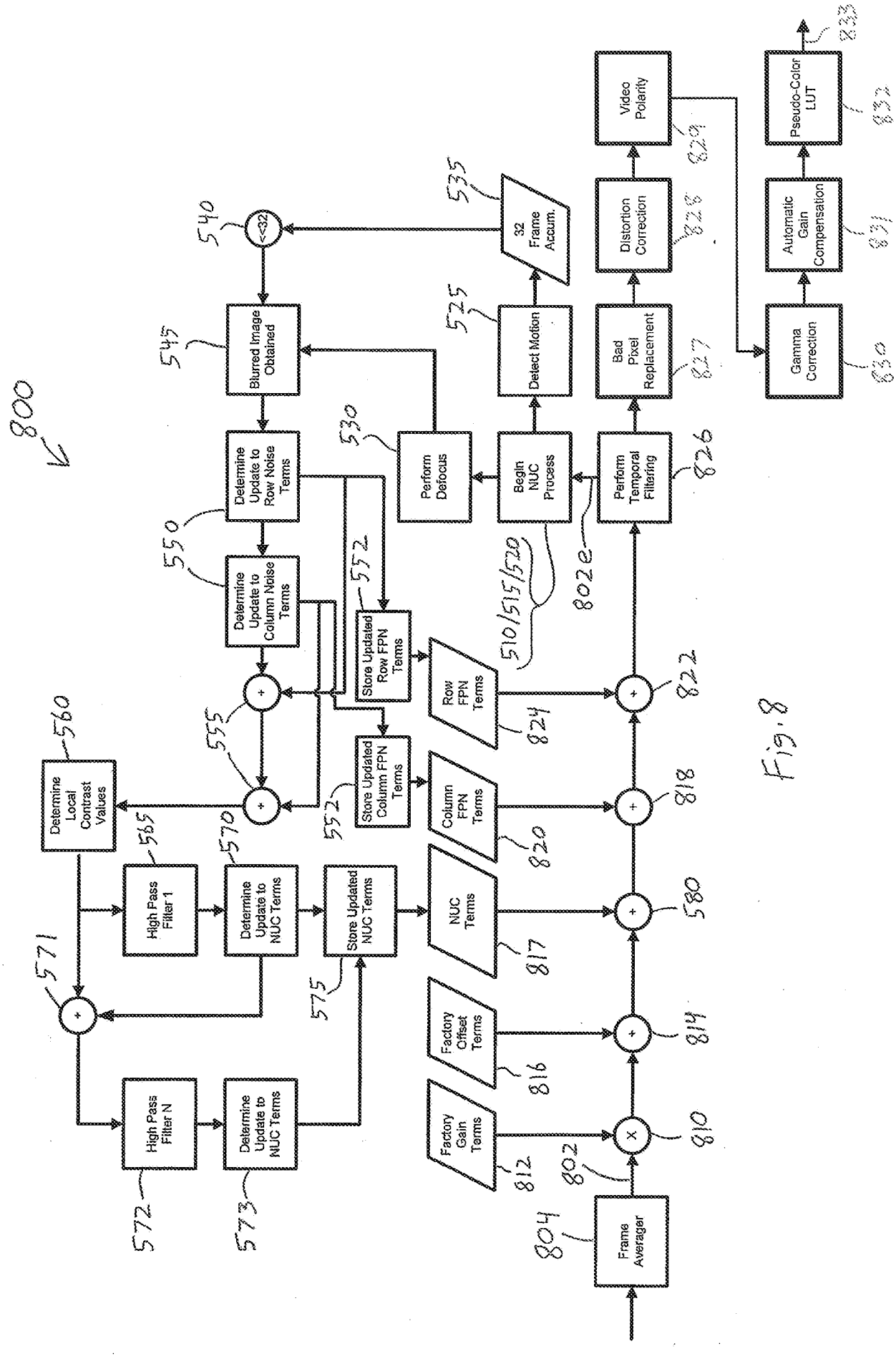

700
716
712
720
724
710
Cp
726
722
714
718

FIG. 7


800
Frame Averager
804
802
Factory Gain Terms
812
Factory Offset Terms
816
NUC Terms
817
Column FPN Terms
820
Row FPN Terms
824
Store Updated NUC Terms
Store Updated Column FPN Terms
Store Updated Row FPN Terms
552
572
573
575
High Pass Filter N
High Pass Filter 1
Determine Update to NUC Terms
Determine Update to Column Noise Terms
Determine Update to Row Noise Terms
550
Determine Local Contrast Values
560
565
570
571
555
Blurred Image Obtained
545
<<32
540
32 Frame Accum.
535
Detect Motion
525
Perform Defocus
530
Begin NUC Process
510/515/520
802e
Perform Temporal Filtering
826
Bad Pixel Replacement
827
Distortion Correction
828
Video Polarity
829
Gamma Correction
830
Automatic Gain Compensation
831
Pseudo-Color LUT
832
833
×
+
580
814
818
822
Fig. 8

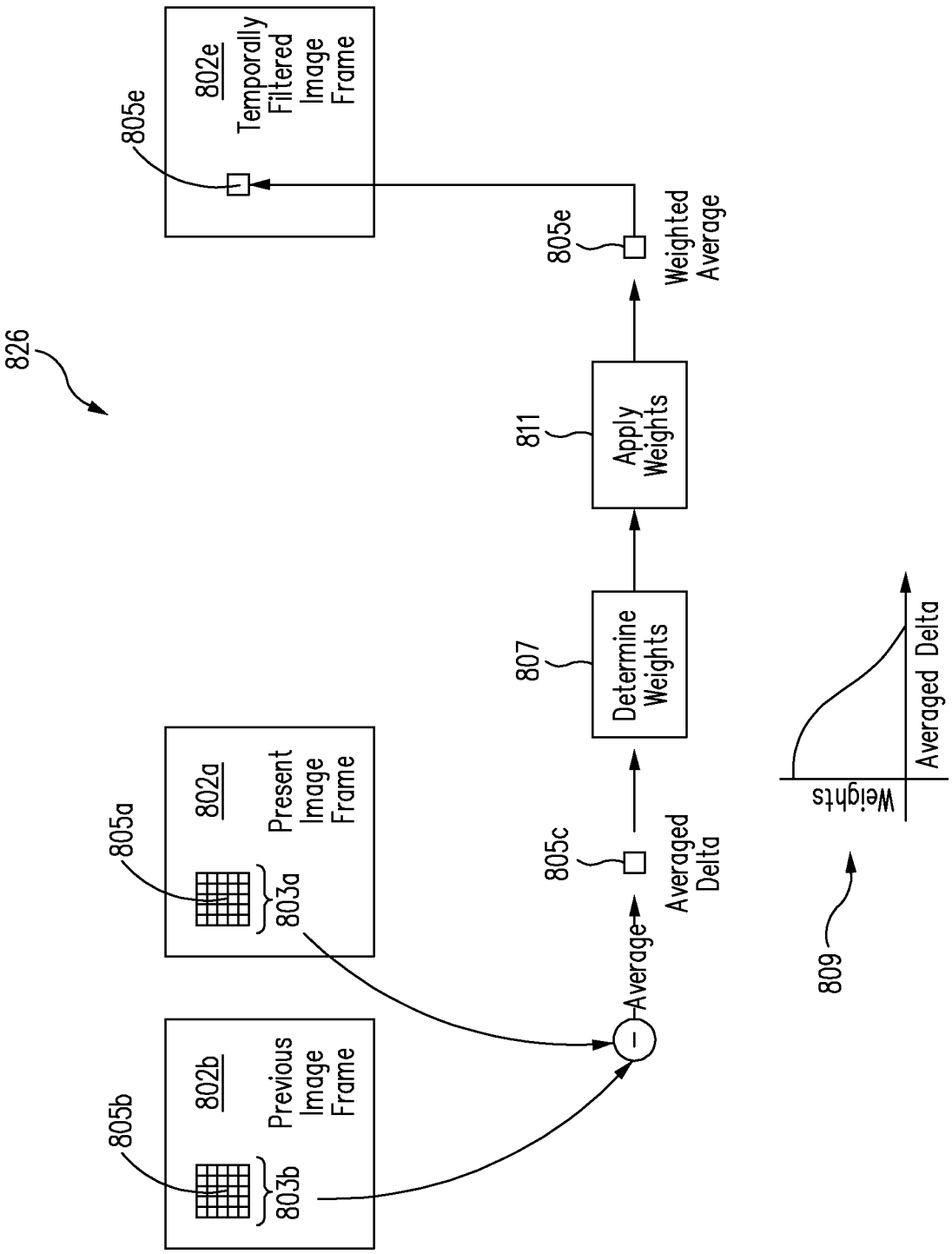

826
805e
802e
Temporally Filtered Image Frame
805e
Weighted Average
811
Apply Weights
807
Determine Weights
805a
802a
Present Image Frame
803a
805c
Averaged Delta
Average
805b
802b
Previous Image Frame
803b
Weights
Averaged Delta
809

FIG. 9

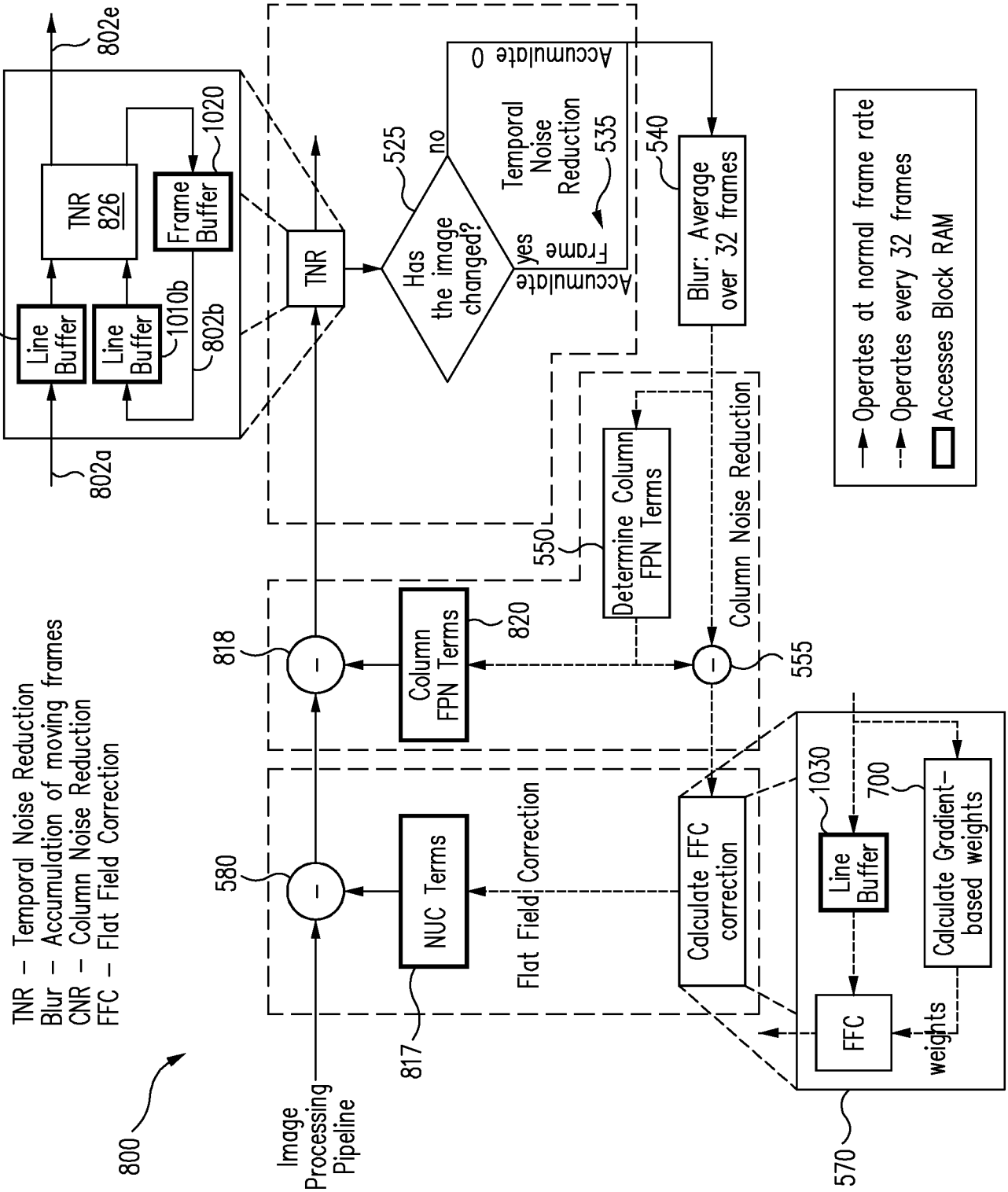

TNR – Temporal Noise Reduction
Blur – Accumulation of moving frames
CNR – Column Noise Reduction
FFC – Flat Field Correction
800
Image Processing Pipeline
802a
802b
802e
1010a
1010b
1020
Line Buffer
Line Buffer
TNR 826
Frame Buffer
TNR
525
Has the image changed?
no
yes
Accumulate 0
Accumulate Frame
Temporal Noise Reduction
535
540
Blur: Average over 32 frames
550
Determine Column FPN Terms
Column Noise Reduction
555
818
820
Column FPN Terms
580
817
NUC Terms
Flat Field Correction
Calculate FFC correction
570
1030
700
Line Buffer
FFC
Calculate Gradient-based weights
weights
Operates at normal frame rate
Operates every 32 frames
Accesses Block RAM

FIG. 10

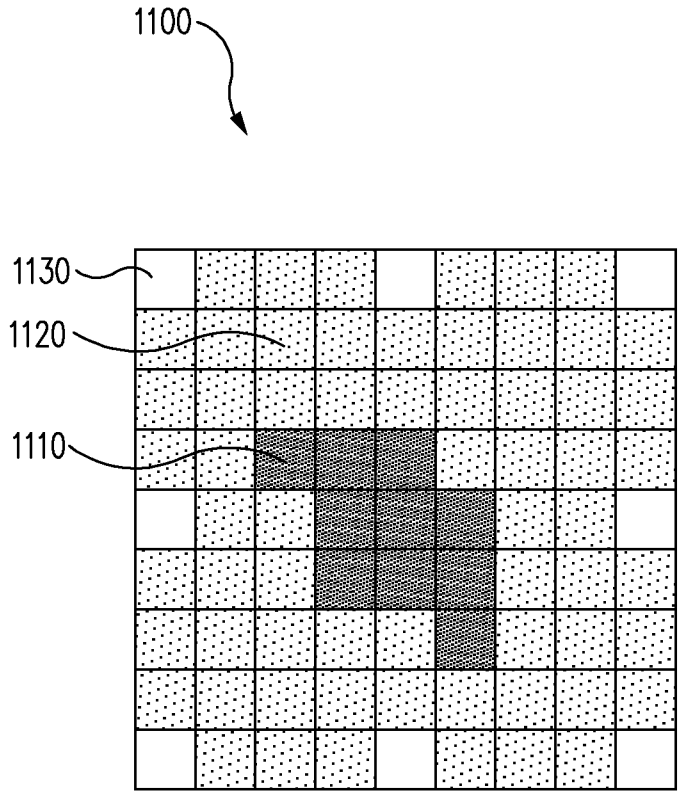


FIG. 11

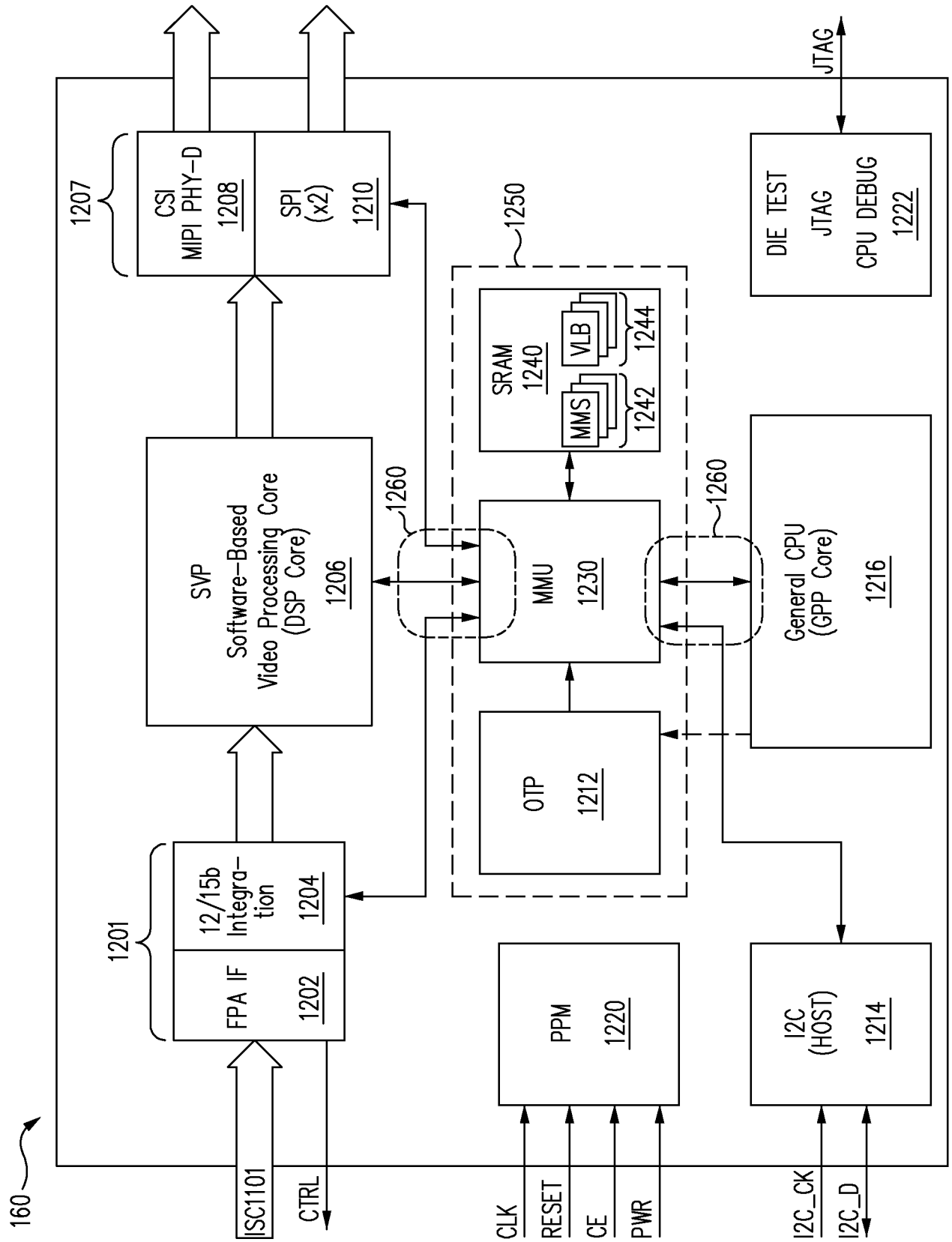

160
ISC1101
CTRL
CLK
RESET
CE
PWR
I2C_CK
I2C_D
JTAG
1207
CSI MIPI PHY-D 1208
SPI (x2) 1210
1250
DIE TEST JTAG CPU DEBUG 1222
SRAM 1240
VLB
MMS
1242
1244
SVP Software-Based Video Processing Core (DSP Core) 1206
1260
MMU 1230
1260
General CPU (GPP Core) 1216
OTP 1212
1201
12/15b Integra-tion 1204
FPA IF 1202
PPM 1220
I2C (HOST) 1214

FIG. 12

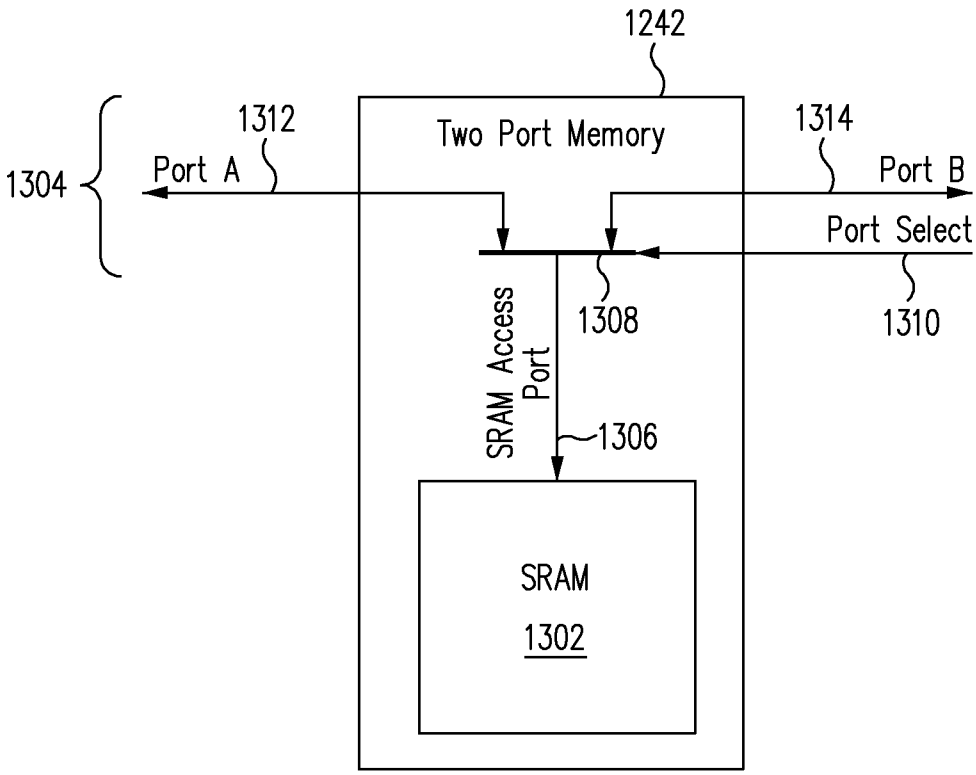

1242
1312
Two Port Memory
1314
1304
Port A
Port B
Port Select
1308
1310
SRAM Access Port
1306
SRAM
1302

FIG. 13

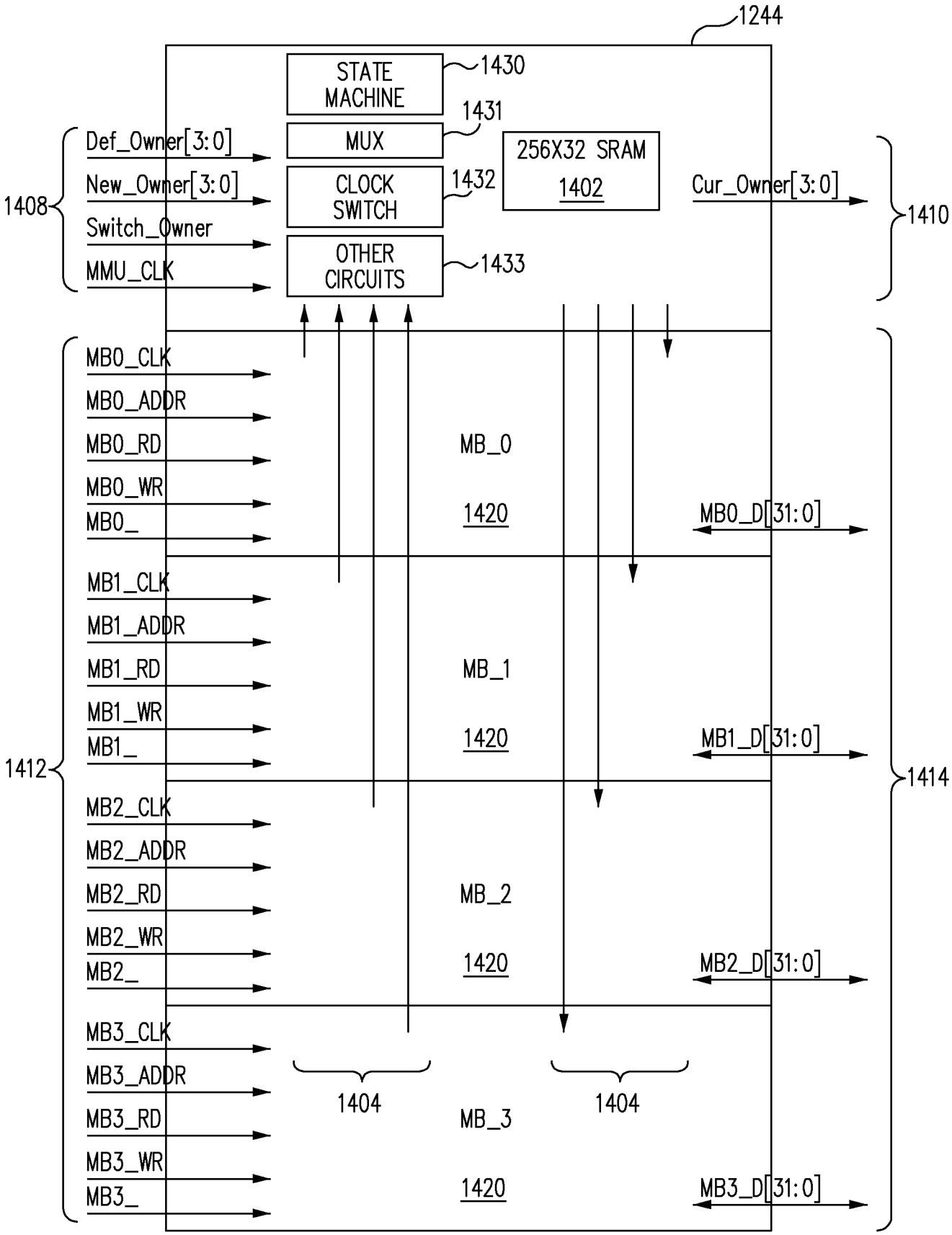

1244
STATE MACHINE
1430
1431
MUX
256X32 SRAM
1402
CLOCK SWITCH
1432
OTHER CIRCUITS
1433
Def_Owner[3:0]
New_Owner[3:0]
Switch_Owner
MMU_CLK
1408
Cur_Owner[3:0]
1410
MB0_CLK
MB0_ADDR
MB0_RD
MB0_WR
MB0_
MB_0
1420
MB0_D[31:0]
MB1_CLK
MB1_ADDR
MB1_RD
MB1_WR
MB1_
MB_1
1420
MB1_D[31:0]
1412
1414
MB2_CLK
MB2_ADDR
MB2_RD
MB2_WR
MB2_
MB_2
1420
MB2_D[31:0]
MB3_CLK
MB3_ADDR
MB3_RD
MB3_WR
MB3_
1404
1404
MB_3
1420
MB3_D[31:0]

FIG. 14

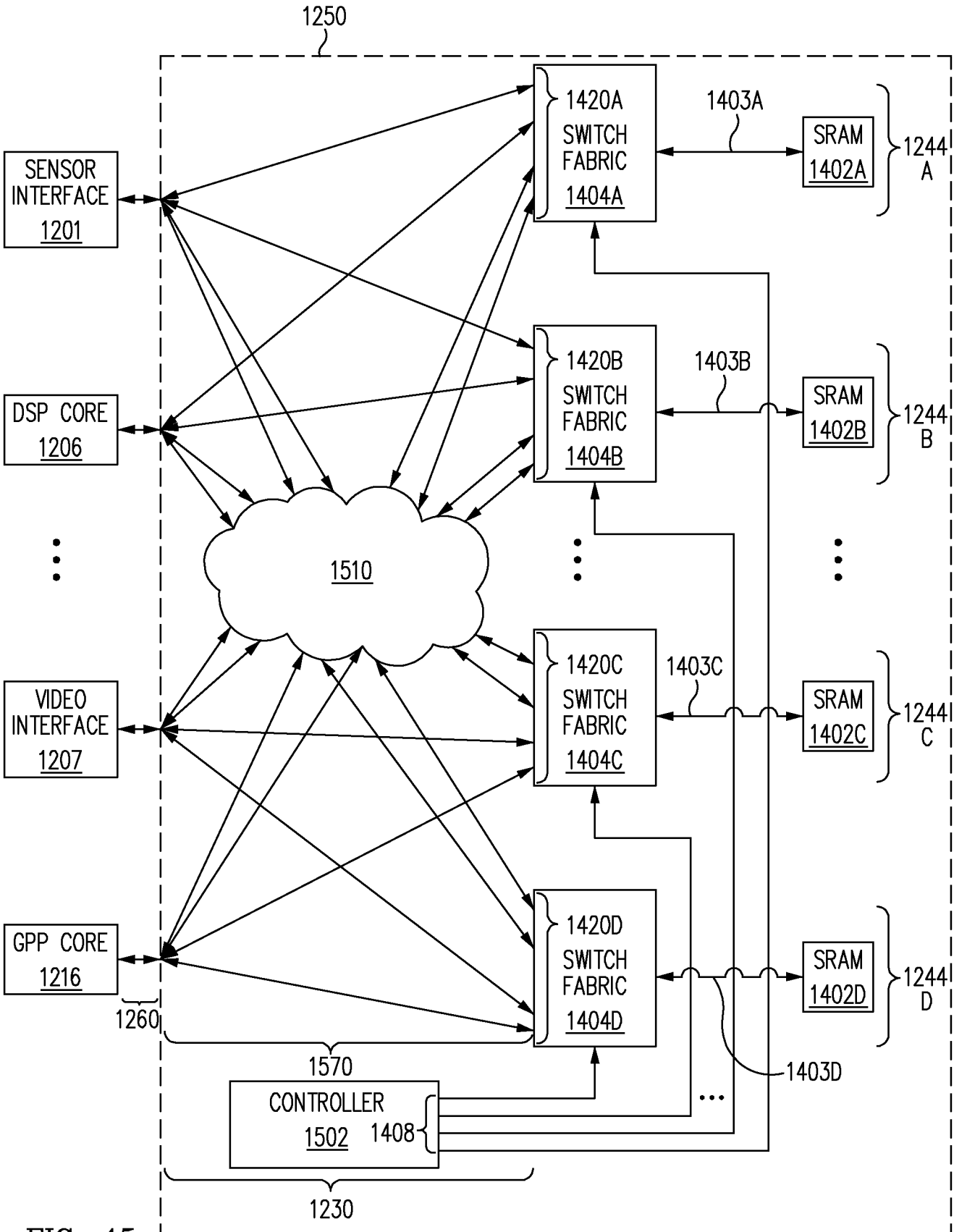

1250
SENSOR INTERFACE 1201
DSP CORE 1206
VIDEO INTERFACE 1207
GPP CORE 1216
1260
1510
1420A SWITCH FABRIC 1404A
1420B SWITCH FABRIC 1404B
1420C SWITCH FABRIC 1404C
1420D SWITCH FABRIC 1404D
1403A
1403B
1403C
1403D
SRAM 1402A
SRAM 1402B
SRAM 1402C
SRAM 1402D
1244 A
1244 B
1244 C
1244 D
1570
CONTROLLER 1502
1408
1230

FIG. 15

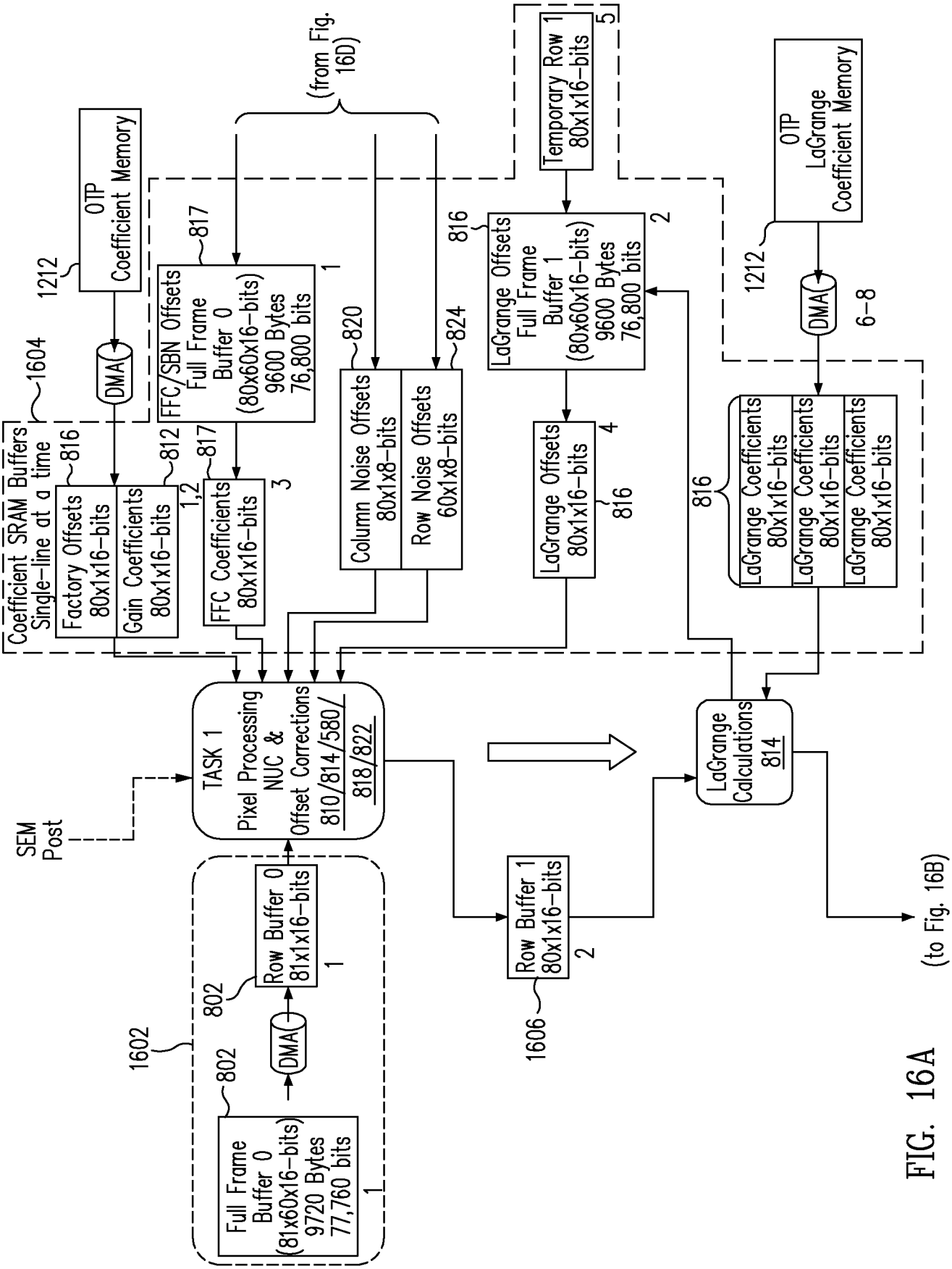

Coefficient SRAM Buffers Single-line at a time
1604
Factory Offsets 80x1x16-bits
816
Gain Coefficients 80x1x16-bits
812
1,2
FFC Coefficients 80x1x16-bits
817
3
DMA
1212
OTP Coefficient Memory
FFC/SBN Offsets Full Frame Buffer 0 (80x60x16-bits) 9600 Bytes 76,800 bits
817
1
(from Fig. 16D)
Column Noise Offsets 80x1x8-bits
820
Row Noise Offsets 60x1x8-bits
824
LaGrange Offsets 80x1x16-bits
816
4
LaGrange Offsets Full Frame Buffer 1 (80x60x16-bits) 9600 Bytes 76,800 bits
816
2
Temporary Row 1 80x1x16-bits
5
OTP LaGrange Coefficient Memory
1212
DMA
6-8
LaGrange Coefficients 80x1x16-bits
LaGrange Coefficients 80x1x16-bits
LaGrange Coefficients 80x1x16-bits
816
SEM Post
TASK 1 Pixel Processing NUC & Offset Corrections 810/814/580/ 818/822
LaGrange Calculations 814
Row Buffer 0 81x1x16-bits
802
1
DMA
802
Full Frame Buffer 0 (81x60x16-bits) 9720 Bytes 77,760 bits
1
1602
Row Buffer 1 80x1x16-bits
2
1606
(to Fig. 16B)

FIG. 16A

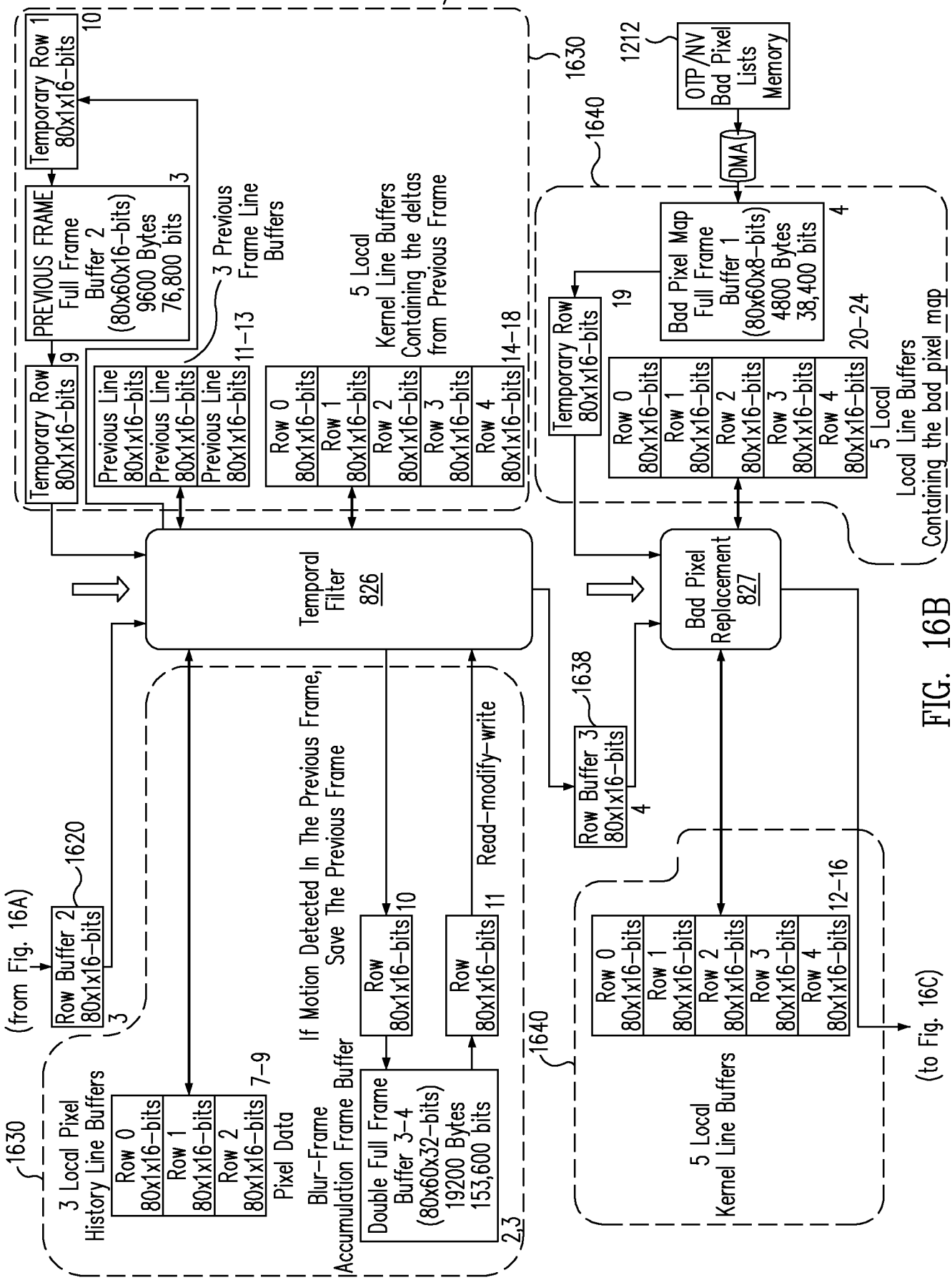

Temporary Row 1 80x1x16-bits 10
PREVIOUS FRAME Full Frame Buffer 2 (80x60x16-bits) 9600 Bytes 76,800 bits 3
3 Previous Frame Line Buffers
Temporary Row 80x1x16-bits 9
Previous Line 80x1x16-bits
Previous Line 80x1x16-bits
Previous Line 80x1x16-bits 11-13
5 Local Kernel Line Buffers Containing the deltas from Previous Frame
Row 0 80x1x16-bits
Row 1 80x1x16-bits
Row 2 80x1x16-bits
Row 3 80x1x16-bits
Row 4 80x1x16-bits 14-18
1630
1640
1212
OTP/NV Bad Pixel Lists Memory
DMA
Bad Pixel Map Full Frame Buffer 1 (80x60x8-bits) 4800 Bytes 38,400 bits 4
Temporary Row 80x1x16-bits 19
Row 0 80x1x16-bits
Row 1 80x1x16-bits
Row 2 80x1x16-bits
Row 3 80x1x16-bits
Row 4 80x1x16-bits 20-24
5 Local Local Line Buffers Containing the bad pixel map
Temporal Filter 826
Bad Pixel Replacement 827
(from Fig. 16A)
Row Buffer 2 80x1x16-bits 3
1620
If Motion Detected In The Previous Frame, Save The Previous Frame
Row 80x1x16-bits 10
Row 80x1x16-bits 11
Read-modify-write
Row Buffer 3 80x1x16-bits 4
1638
3 Local Pixel History Line Buffers
Row 0 80x1x16-bits
Row 1 80x1x16-bits
Row 2 80x1x16-bits 7-9
Pixel Data
Blur-Frame Accumulation Frame Buffer
Double Full Frame Buffer 3-4 (80x60x32-bits) 19200 Bytes 153,600 bits 2,3
Row 0 80x1x16-bits
Row 1 80x1x16-bits
Row 2 80x1x16-bits
Row 3 80x1x16-bits
Row 4 80x1x16-bits 12-16
5 Local Kernel Line Buffers
(to Fig. 16C)

FIG. 16B

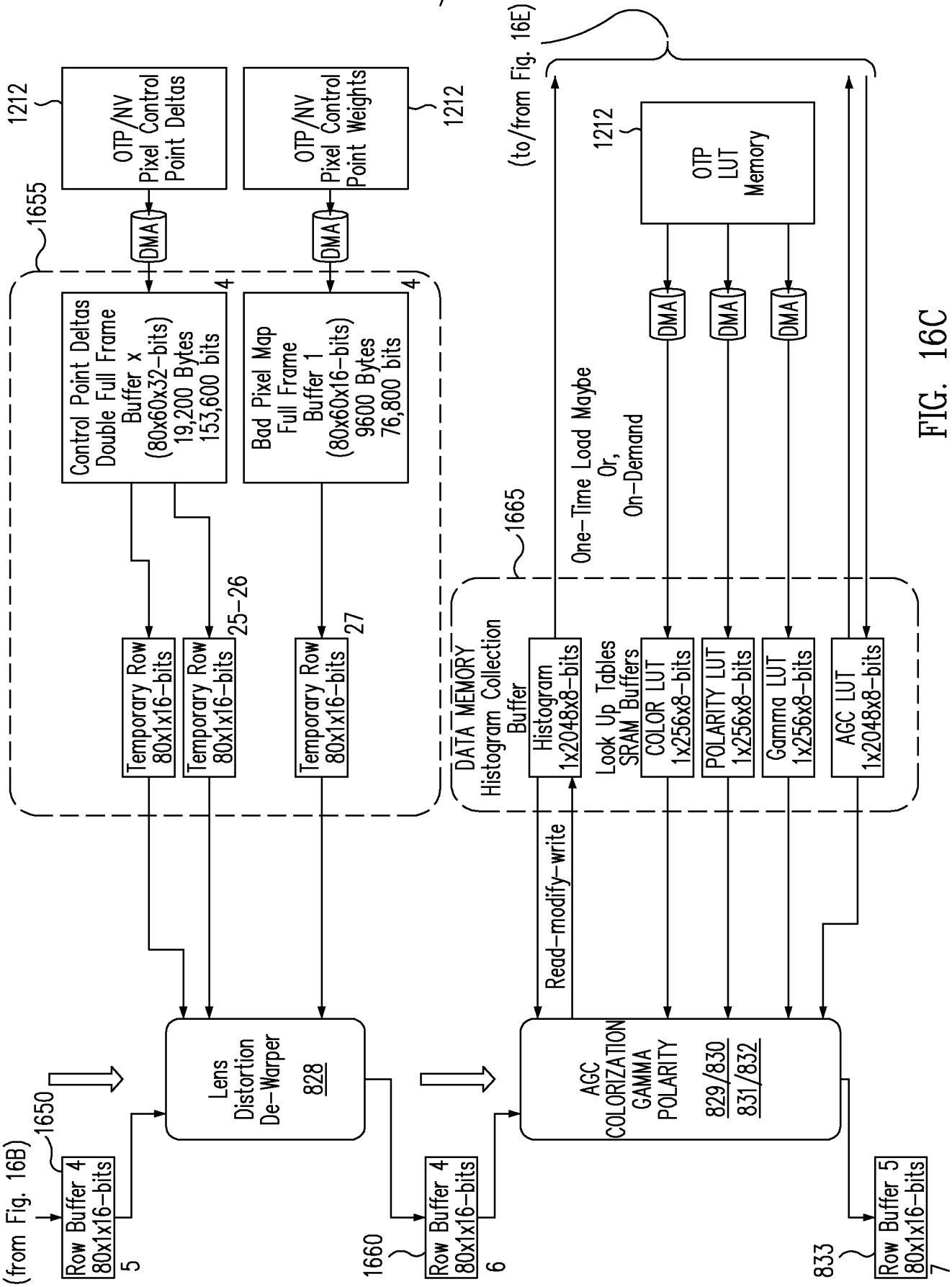

(from Fig. 16B)
1650
Row Buffer 4
80x1x16-bits
5
Lens
Distortion
De-Warper
828
1660
Row Buffer 4
80x1x16-bits
6
AGC
COLORIZATION
GAMMA
POLARITY
829/830
831/832
833
Row Buffer 5
80x1x16-bits
7
1655
1212
OTP/NV
Pixel Control
Point Deltas
DMA
Control Point Deltas
Double Full Frame
Buffer x
(80x60x32-bits)
19,200 Bytes
153,600 bits
4
Temporary Row
80x1x16-bits
25-26
Temporary Row
80x1x16-bits
1212
OTP/NV
Pixel Control
Point Weights
DMA
Bad Pixel Map
Full Frame
Buffer 1
(80x60x16-bits)
9600 Bytes
76,800 bits
4
Temporary Row
80x1x16-bits
27
(to/from Fig. 16E)
1212
OTP
LUT
Memory
DMA
DMA
DMA
1665
One-Time Load Maybe
Or,
On-Demand
DATA MEMORY
Histogram Collection
Buffer
Histogram
1x2048x8-bits
Read-modify-write
Look Up Tables
SRAM Buffers
COLOR LUT
1x256x8-bits
POLARITY LUT
1x256x8-bits
Gamma LUT
1x256x8-bits
AGC LUT
1x2048x8-bits

FIG. 16C

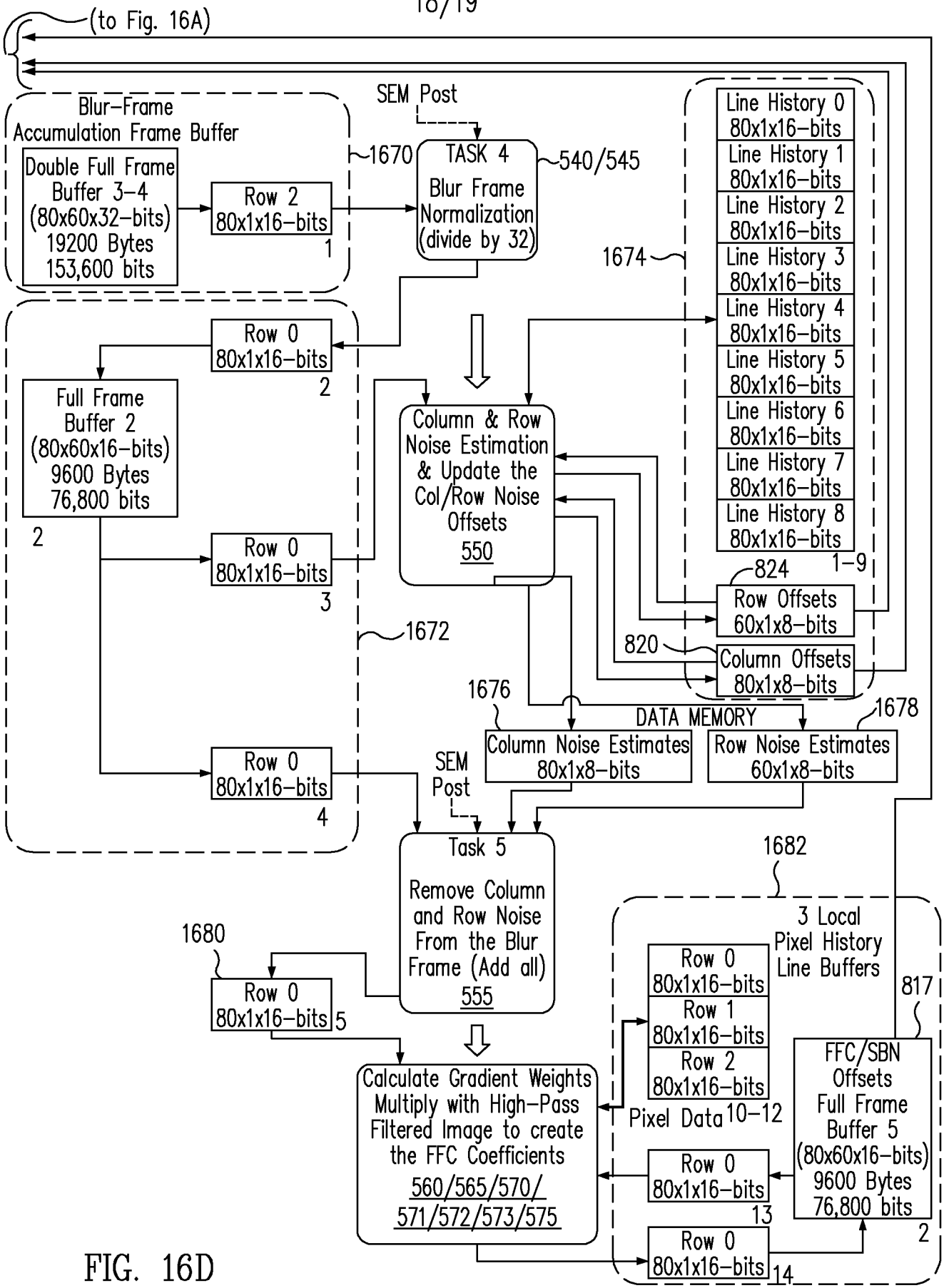

(to Fig. 16A)
Blur-Frame Accumulation Frame Buffer
Double Full Frame Buffer 3-4 (80x60x32-bits) 19200 Bytes 153,600 bits
Row 2 80x1x16-bits 1
SEM Post
1670
TASK 4
Blur Frame Normalization (divide by 32)
540/545
1674
Line History 0 80x1x16-bits
Line History 1 80x1x16-bits
Line History 2 80x1x16-bits
Line History 3 80x1x16-bits
Line History 4 80x1x16-bits
Line History 5 80x1x16-bits
Line History 6 80x1x16-bits
Line History 7 80x1x16-bits
Line History 8 80x1x16-bits
1-9
Row 0 80x1x16-bits 2
Full Frame Buffer 2 (80x60x16-bits) 9600 Bytes 76,800 bits
2
Column & Row Noise Estimation & Update the Col/Row Noise Offsets 550
824
Row Offsets 60x1x8-bits
820
Column Offsets 80x1x8-bits
Row 0 80x1x16-bits 3
1672
1676
DATA MEMORY
1678
Column Noise Estimates 80x1x8-bits
Row Noise Estimates 60x1x8-bits
Row 0 80x1x16-bits 4
SEM Post
Task 5
Remove Column and Row Noise From the Blur Frame (Add all) 555
1682
3 Local Pixel History Line Buffers
1680
Row 0 80x1x16-bits 5
Row 0 80x1x16-bits
Row 1 80x1x16-bits
Row 2 80x1x16-bits
Pixel Data 10-12
817
FFC/SBN Offsets Full Frame Buffer 5 (80x60x16-bits) 9600 Bytes 76,800 bits
2
Calculate Gradient Weights Multiply with High-Pass Filtered Image to create the FFC Coefficients 560/565/570/ 571/572/573/575
Row 0 80x1x16-bits 13
Row 0 80x1x16-bits 14

FIG. 16D

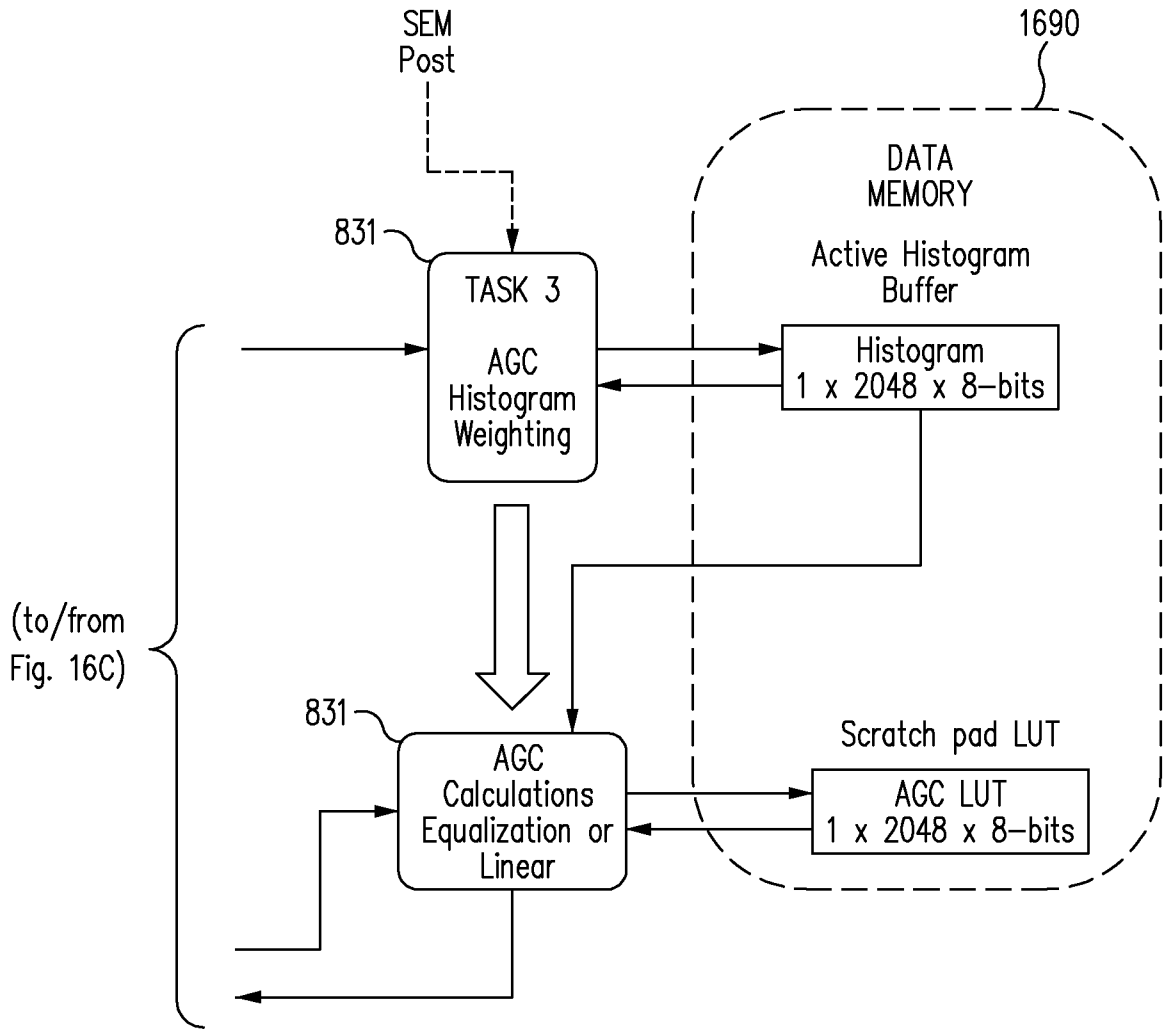

SEM
Post
1690
DATA
MEMORY
831
TASK 3
AGC
Histogram
Weighting
Active Histogram
Buffer
Histogram
1 x 2048 x 8-bits
(to/from
Fig. 16C)
831
AGC
Calculations
Equalization or
Linear
Scratch pad LUT
AGC LUT
1 x 2048 x 8-bits

FIG. 16E