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**US 6781423 B1** **US 6781422 B1**  
**US 5274274 A** **US 5068571 A**  
**US 4994955 A**

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(54) Abstract Title: **A high side transistor drive circuit**

(57) A high-side transistor drive circuit is coupled between a supply rail 208 and a half-bridge output node 210. The drive circuit receives current signals from level shifting transistors 202a and 202b. The low gain differential amplifier 212 counteracts large stray common mode signals which flow when the potential of the half bridge output node changes rapidly. The common-mode rejection of the amplifier allows the use of lower magnitude control signals. No blanking circuit is needed to disable the control circuit during transitions of the half bridge output node. The high side driver may be used in fluorescent lamp power supplies (figure 1) or in switched mode power supplies (figure 4).

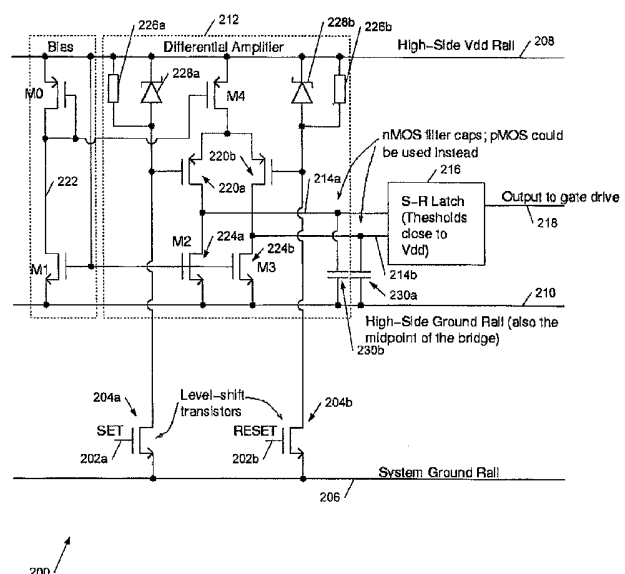


Figure 2

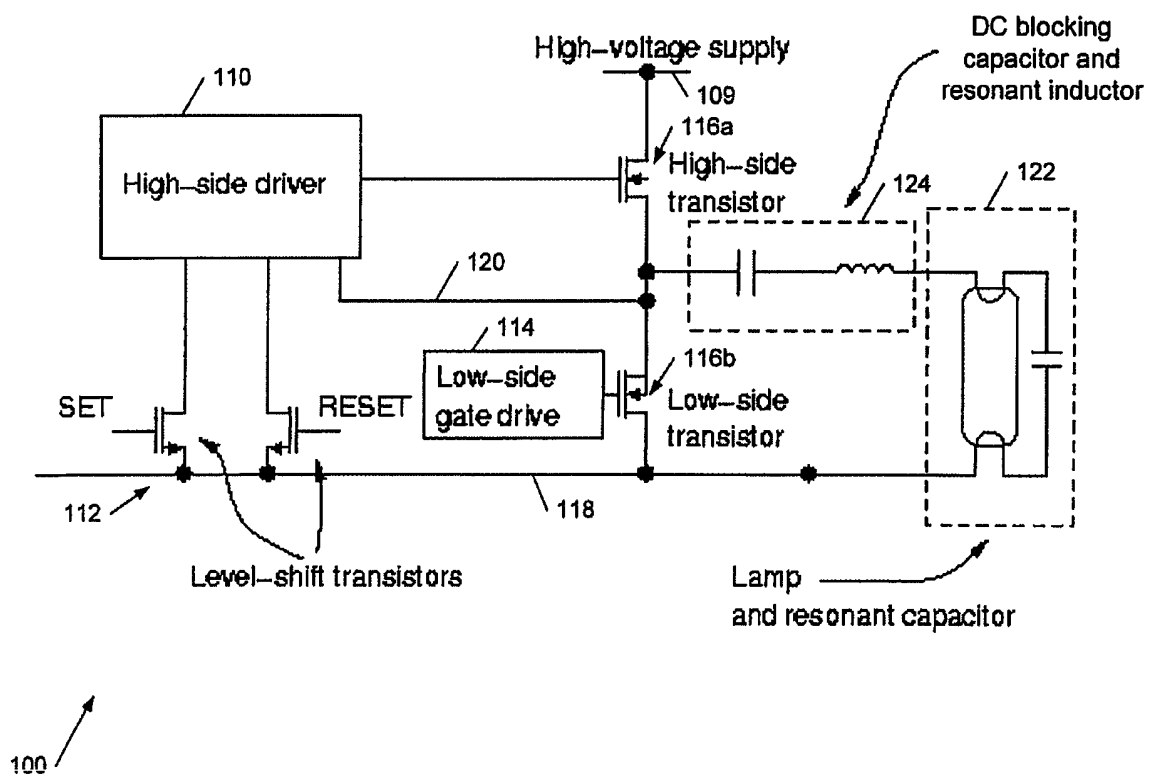
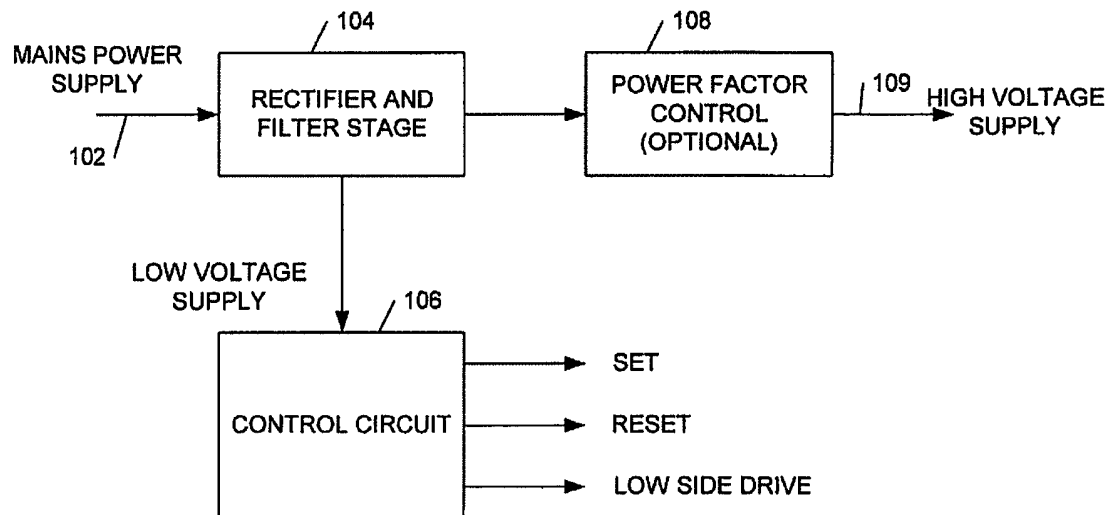


Figure 1



## Figure 2

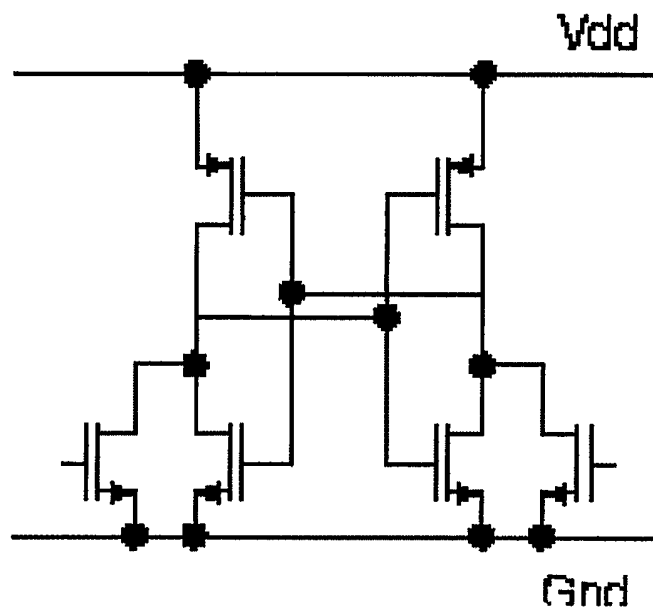


Figure 3

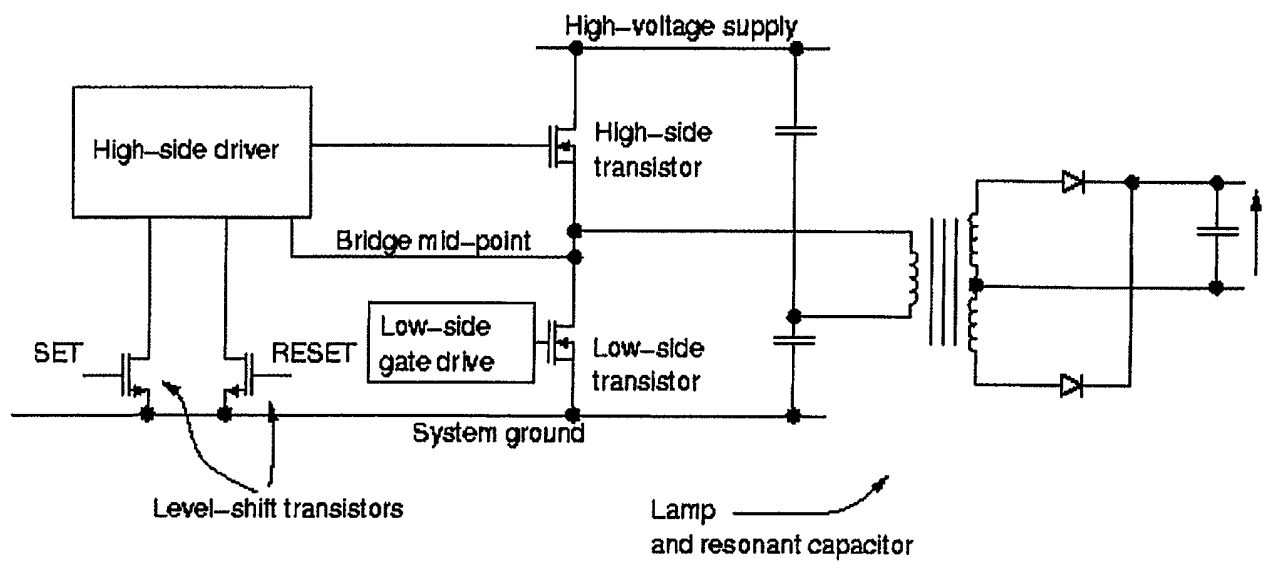


Figure 4

### Power Supply Driver Circuit

This invention is generally concerned with what are known in the art as high-side driver circuits, in particular for switching power supplies.

Broadly speaking, a high-side driver is a circuit which transforms a low-side (low voltage) gate drive signal, generally referenced to a system and/or chip ground, to a high-side (high voltage) gate drive signal which is typically referenced to the mid-point of a half bridge. This mid-point has a potential which can vary between, for example, 0 and 500 volts above the system or chip/PCB (Printed Circuit Board) ground. Often the mid-point potential is rapidly varying over a range of several hundred volts. The high-side driver circuit provides a means of translating or communicating between the low (voltage)-side and the high (voltage)-side circuitry.

Figure 1 shows an example fluorescent lamp driver circuit 100 incorporating a high-side driver 110.

The lamp driver has a mains power supply input 102 to a rectifier and filter stage 104, for example comprising a bridge rectifier and smoothing capacitors, which provides a low voltage supply to a control circuit 106. The rectifier and filter stage 104 also provides a high voltage supply 109, optionally via a PFC (Power Factor Control) stage 108.

The control circuit provides set and reset outputs to a pair of level shift transistors which provide input signals to high-side driver 110. The control circuit also provides a low-side drive signal to a low-side gate drive circuit 114. The high-side drive 110 drives a high-side switching transistor 116a and the low-side gate drive drives a low-side switching transistor 116b. Transistors 116a and 116b form a half-bridge coupled between the high voltage supply and a system ground rail 118. The high-side driver 110 is connected to a mid-point 120 of the half-bridge. This mid-point also provides a

high (alternating current) voltage output to lamp and resonant capacitor 122 via a dc blocking capacitor and resonant inductor 124.

In operation the low-side drive signal typically comprises a waveform with a duty cycle of around 40 percent. Similarly the set and reset signals are controlled so that the drive to the high-side transistor also has a duty cycle of around 40 percent. The low-side and high-side transistor drive waveforms are aligned so that the low-side transistor and high-side transistor are not on simultaneously, the less than 50 percent duty cycle waveforms providing a degree of tolerance in achieving this.

A difficulty with design of the high-side driver is that the signal (usually in the form of a current) which is used to communicate between the low-side and high-side circuitry is easily confused by system noise, especially when the half-bridge is switching.

Conventional solutions to this problem rely on either making the communicating signal very large relative to the interfering signals, with a consequent waste of power, or on using blanking signals which blank out the (regular) interfering signal. As the interfering signals happen at known times, in particular when the mid-point of the bridge is flying (transitioning) high or low, blanking pulses can be used to blank out these signals, but this approach also wastes power, is tricky to implement, and is prone to error.

According to a first aspect of the invention, there is therefore provided A high-side driver circuit for a switching power supply, the power supply having a switching control system operating from a first voltage supply and a power switching device configured to switch a second voltage supply higher than said first voltage supply, said first voltage supply having a first ground rail, said power switching device having a switching control connection for controlling switching of said second voltage supply, said high-side driver circuit being configured to translate a low-side switching control signal from said switching control system and referenced to said first ground rail to a high-side switching control signal referenced to a second, high-side ground rail for driving said switching control connection of said power switching device, said low-side switching control signal comprising a first signal for switching said power switching device on

and a second signal for switching said power switching device off, said high-side driver circuit comprising: first and second inputs to receive said first and second low-side switching control signals; a differential amplifier having a differential pair of inputs coupled to said first and second inputs and having an output, said differential amplifier having a ground connection for connection to said high-side ground rail and a power connection to receive a power supply from said second voltage supply; and an output coupled to said differential amplifier output to provide said high-side switching control signal.

As mentioned above, typically the second, high-side ground rail oscillates (because of the action of the power switching device) between around 0V and a positive voltage of 100V or more. By contrast the first (low) voltage supply typically operates at less than 20V, for example around 5V. The power switching device should therefore be suitable for switching a voltage of greater than 100V, and generally at a power of greater than 1 watt.

In preferred embodiments a level shift circuit is coupled between the first and second inputs of the high-side driver and the pair of inputs of the differential amplifier. Such a level shift circuit may comprise a pair of level shift transistors, in particular connected to the first ground rail.

The differential amplifier may have a single-ended output for driving the high-side transistor, but in preferred embodiments, the differential amplifier output comprises first and second differential outputs. These may then be used to drive a set-reset latch with inputs coupled to these differential amplifier outputs, an output of the latch being used to drive the high-side transistor.

In some particularly preferred embodiments the latch has set and reset inputs which have a threshold voltage within 20 percent of a supply voltage  $V_{dd}$  of the high-side driver circuit, more particularly of the differential amplifier. That is the threshold voltages of the latch are preferably within 20 percent of a difference between the second voltage supply and the high-side ground rail.

In preferred embodiments the differential amplifier has a tail connected to the power connection for the differential amplifier, more particularly to the second (high-side) voltage supply. The differential amplifier preferably comprises a differential pair of transistors both coupled to the tail of the differential amplifier, providing a pair of output arms. Preferably each output arm comprises a transistor connected as a resistive load (rather than a conventional current mirror-type load). Preferably each of these load transistors has a control (for example, gate) connection coupled to a fixed voltage supply, for example the high-side voltage supply rail. This helps to keep the differential mode gain of the differential amplifier low – which is advantageous because, although the differential mode gain would be larger with a current mirror-type load, the common mode gain would also be increased. Preferably the differential amplifier has a differential mode gain of less than 10 or even less than 5.

In embodiments of the circuit, broadly speaking the use of a differential amplifier helps to reduce the vulnerability of the circuit to common mode signals which arise when the mid-point of the bridge of the circuit of Figure 1 is flying (transitioning) high or low.

In some preferred embodiments the tail current of the differential amplifier is set by a current mirror output, an input current to the current mirror being set by a further transistor connected as a resistor. Preferably a control (for example gate) connection is connected to a fixed voltage, more preferably the same fixed voltage as that to which the resistive load transistors of the differential amplifier are connected, for example the high-side supply rail.

In some preferred embodiments of the high-side driver circuit the inputs to the differential amplifier, more particularly to the differential pair of the differential amplifier, are clamped by respective voltage clamps. Each voltage clamp is preferably connected between a differential input and the high-side supply rail. The voltage clamp may comprise a zener diode or, in a process without zener diodes, by one or more forward-biased diodes in series in anti-parallel with a single reverse-biased diode.

Preferably a resistor is connected across each voltage clamp or zener, to discharge its capacitance. For example, when one of the level-shift transistors turns on, providing an

input to the differential amplifier, a voltage is developed across the voltage clamp (zener) diode and its capacitance is charged. When the input, more particularly the level-shift transistor, turns off the resistor discharges this capacitance, thus attenuating an erroneous differential mode input signal to the differential amplifier which would otherwise be present.

Preferably the high-side driver circuit also includes a filter on the differential amplifier output to reduce or substantially remove noise which may arise from spurious differential mode signals.

The invention also provides a switching power supply including a high-side driver circuit as described above. Where this switching power supply includes a half-bridge, the high-side ground rail may be coupled to a mid-point of this half-bridge. The switching power supply may be configured as a (dc) switch mode power supply, or a power supply for driving a (fluorescent) lamp load or some other type of switching power supply.

The invention further provides a method of translating a low voltage control signal for a power switching device of a switching power supply into a control signal referenced to a ground which varies over a range of at least 100 volts with respect to voltage control signal as a consequence of said power device switching, the method comprising: inputting a differential control signal at a first voltage for controlling said power device switching; amplifying said differential control signal using a differential amplifier to provide a differential control signal output referenced to said varying ground.

Preferably the differential control signal amplifying has a gain of less than 10, thus reducing the sensitivity of the method to common mode signals. The method may further comprise driving the power switching device using the differential control signal output, in particular converting the differential control signal output to a single-ended control signal, for example using a set-reset latch.

The invention further provides a circuit for translating a low voltage control signal for a power switching device of a switching power supply into a control signal referenced to

a ground which varies over a range of at least 100 volts with respect to said low voltage control signal as a consequence of said power device switching, the circuit comprising: means for inputting a differential control signal at a first voltage for controlling said power device switching; and means for amplifying said differential control signal using a differential amplifier to provide a differential control signal output referenced to said varying ground.

These and other aspects of the invention will now be further described, by way of example only, with reference to the accompanying figures in which:

Figure 1 shows an example of a switching power supply driving a lamp load;

Figure 2 shows an embodiment of a high-side driver circuit according to an aspect of the invention;

Figure 3 shows an example set-reset latch circuit for use with the high-side driver circuit of Figure 2; and

Figure 4 shows an example of a switch mode power supply (SMPS) including the high-side driver circuit of Figure 2.

Referring to Figure 2, this shows an example of a high-side driver circuit 200 which may be employed, for example, in the switching power supply of Figure 1, as well as in other types of switching power supply.

Referring to Figure 2, two signals are used to communicate between the low voltage side and the high voltage side of the circuit. In this example these are “set” 202a and “reset” 202b signals which, in the example circuit of Figure 1, turn the gate of the high-side device 116a in the half-bridge 116a, b on an off respectively.

Two transistors 204a, b provide a level-shift function, having their source connections connected to a system ground rail 206 and their drain connections coupled (indirectly)

to the high-side Vdd rail 208. These transistors transmit the set and reset signals to the high-side circuit by turning on for brief periods of time.

In Figure 2, broadly speaking, the high-side part of the circuit is that drawn above high-side ground rail 210 (which in the example of Figure 1 is connected to the mid-point 120 of the half bridge 116a, b). In operation the high-side ground rail 210 moves up and down, sometimes by 300-400V or more (above system ground rail 206) but the high-side Vdd rail 208 always remains at Vdd above the ground rail 210. Typically Vdd is less than 10V, for example around 5V.

In operation, when the mid-point 120 of the half-bridge is flying high or low, common mode currents (that is, the same current in the “set” and “reset” nets) flow through the wires connecting the drains of the level shift devices to the high-side circuitry. These common-mode currents can be confused with the intended set and reset signals. Therefore, a differential amplifier, indicated by dashed box 212, is employed in the high-side circuit to differentiate between differential mode signals, such as single pulses on the set or reset transistors, and common-mode signals, which occur as described above when the mid-point bridge is flying high or low. The differential amplifier has a differential (balanced) output 214a, b which is used to set or reset an S-R latch 216 which provides an output 218 to drive the gate of a high-side switching device such as high-side transistor 116a in the circuit of Figure 1.

Referring in more detail to the circuit of Figure 2, the differential amplifier 212 comprises a differential pair of (in this example PMOS) transistors 220a, b with their source connections connected together to a current bias transistor M4. Transistor M4 is the output of a current mirror, the input to which is formed by transistor M0. The current input to the current mirror, more particularly to transistor M0 in line 222 is set by the resistance of transistor M1, which is connected as a resistor with its gate connected to the high-side Vdd rail 208.

Each of the transistors 220a, b of the differential pair has a respective load resistor 224a, b, each formed by a transistor M2, M3 with a gate connection connected to Vdd rail 208. As mentioned above, by using a resistor load for each of the differential pair of

transistors, rather than a current mirror load, the common-mode gain is reduced (albeit with the differential mode gain). If transistors M1, M2 and M3 are all the same size (width) then the same current will flow in line 222 as in the output arms of the differential pair and transistors M4 and M0 should therefore have a size ratio of  $M4:M0 = 2:1$ . Alternatively M0 and M4 could be the same size and M1 half the size of M2 and M3 (M2 and M3 having the same size).

Thus, broadly speaking, the gain of the differential amplifier is kept low by the use of resistive loads because the differential mode signals are large. The output of the differential amplifier for a given differential mode signal is set by the bias circuit (M0 and M1), the ratio of M1 to the transistors M2 and M3 used as resistive loads in the differential amplifier circuit, and the ratio of the bias transistors M0 and M4. This ensures that the output of the differential amplifier remains constant for a wide variety of process corners, supply voltages and temperatures.

Preferably the differential mode gain is set at a level which is just sufficient to give a logic-level output to drive the S-R latch 216 for a typical differential input signal, so that the common-mode gain is kept extremely low. This reduces the risk of the S-R latch 216 being accidentally set or reset when the differential amplifier sees common mode signals. More particularly, the gain of the differential amplifier is set to give a threshold voltage which is just enough to switch latch 216 in a worst case design scenario. This worst case depends upon the value of  $V_{dd}$ , and also on the operation of the voltage clamps (described below). In outline, in a typical worst case scenario the input to the differential amplifier is set by a potential divider comprising one of the resistors 226 and the resistance of the level shift transistor 204 (when in sufficient current flows through a zener diode 228 for it to perform its clamping action). For an example  $V_{dd}$  of 5V a minimum differential mode worst case input voltage may be, for example, around 4V, and the differential mode gain is chosen accordingly (given the threshold switching voltage of latch 216).

Despite the use of a differential amplifier, mismatch in the level-shift devices can cause differential mode signals to occur for brief periods when the mid-point of the bridge (line 210) is flying high or low. Therefore, preferably the output of the differential

amplifier is filtered by MOS (Metal Oxide Semiconductor) capacitors 230a, b to remove these pulses. As can be seen from Figure 2, preferably the circuit is implemented in MOS technology and either PMOS capacitors to Vdd or NMOS capacitors to ground may be employed, although the latter is preferable due to the reduced chance of coupling supply noise to the input of the S-R latch 216. The filter should have a time constant of less than 1 microsecond, for example around 200 ns and the value of the capacitor can be determined from this and the effective output resistance of transistors M2 and M3. A typical capacitance value is of order 2pF. Broadly speaking larger capacitance values (longer time constants) are better for noise immunity but it is also desirable to be able to provide short pulses to the level shift transistors 204. The filtering should not be too great otherwise the desired output pulses will be filtered and will thus fail to set and reset latch 216.

Any conventional set-reset latch design may be employed in the circuit of Figure 2. However it is preferable that the threshold voltages on lines 214a, b for setting and resetting the latch can be close to Vdd, for example, within 20 percent or even 10 percent of Vdd. Figure 3 shows an example S-R latch design which allows the threshold voltage to be biased well away from ground, thus increasing the circuits immunity to noise on the output of the differential amplifier. Referring again to Figure 2, a zener diode 228a, b connects the input of each of the transistors of the differential pair to the high-side Vdd rail 208. These zener diodes, load the level-shift transistors 204 and ensure that the inputs of the differential amplifier see the same voltage (with respect to the Vdd line). When a set or reset pulse is present, irrespective of the potential between the high-side circuit (ground rail 210 or Vdd rail 208) and system ground rail 206. In a process without zener diodes, the zener diodes in the schematic may be replaced with, for example, four forward-biased diodes in series in anti-parallel with a single reverse-biased diode.

Resistors 226a, b are connected in parallel with zener diodes 228a, b to ensure that the inputs of the differential amplifier see a high enough input voltage (that is, sufficiently below high-side Vdd rail 208 remembering that transistors 220a, b are PMOS devices) when the potential of the high-side Vdd supply is very low. This can occur, for example, when the mid-point of the bridge (and hence line 210) is close to or even

below system ground 206 (because of the resonance action of the load, the high-side ground rail 210 can go one diode drop, approximately 0.7 V below system ground rail 206). A typical zener voltage is of order 5V to 10V; the resistors may have a value of order 100k $\Omega$ . As mentioned above, the resistors 226a, b discharge the voltage developed across a zener diode and stored on its capacitance when the corresponding level-shift transistor turns off, thus damping a potential spurious differential mode signal.

When the high-side ground rail 210 is flying (transitioning) high the zener diodes 228 conduct current in reverse-bias (that is against the normal diode direction) to charge the capacitance of the level-shift transistors 204, thus generating the above-described common-mode signals. When the high-side ground rail 210 is flying (transitioning) low the zener diodes conduct current in forward-bias direction to discharge the capacitance of the level-shift transistors (because this capacitance is now charged to a higher voltage than the high-side V<sub>dd</sub> rail). In this latter case the generated common mode signal is above the high-side V<sub>dd</sub> supply rail and hence neither input transistor of the differential amplifier is turned on. Thus when the high-side ground rail 210 is flying (transitioning) low there is substantially no danger of spurious triggering of the S-R latch 216 from common-mode signals.

Figure 4 shows an example of a switch mode power supply incorporating a high-side driver circuit as shown in Figure 2, for improved reliability of transforming a low-side gate drive signal to a high-side gate drive signal.

Broadly speaking we have described the use of a differential amplifier with low gain on the high voltage side of a high-side driver to differentiate between true set-reset signals and common-mode signals due to switching taking place. Embodiments of the circuit provide a reduced power consumption and do not need circuitry to generate blanking pulses. A switching power supply with a lamp load and a dc switch mode power supply circuit have been given as examples of applications of the above described high-side driver circuit, but the skilled person will recognise that many other applications exist for this circuit.

No doubt many other effective alternatives will occur to the skilled person. It will be understood that the invention is not limited to the described embodiments and encompasses modifications apparent to those skilled in the art lying within the spirit and scope of the claims appended hereto.

**CLAIMS:**

1. A high-side driver circuit for a switching power supply, the power supply having a switching control system operating from a first voltage supply and a power switching device configured to switch a second voltage supply higher than said first voltage supply, said first voltage supply having a first ground rail, said power switching device having a switching control connection for controlling switching of said second voltage supply, said high-side driver circuit being configured to translate a low-side switching control signal from said switching control system and referenced to said first ground rail to a high-side switching control signal referenced to a second, high-side ground rail for driving said switching control connection of said power switching device, said low-side switching control signal comprising a first signal for switching said power switching device on and a second signal for switching said power switching device off, said high-side driver circuit comprising:

first and second inputs to receive said first and second low-side switching control signals;

a differential amplifier having a differential pair of inputs coupled to said first and second inputs and having an output, said differential amplifier having a ground connection for connection to said high-side ground rail and a power connection to receive a power supply from said second voltage supply; and

an output coupled to said differential amplifier output to provide said high-side switching control signal.

2. A high-side driver circuit as claimed in claim 1 wherein said driver circuit further comprises a level shift circuit coupled between said first and second inputs and said differential pair of inputs of said differential amplifier.

3. A high-side driver circuit as claimed in claim 1 or 2 wherein said differential amplifier has a pair of output arms comprising respective first and second transistors each connected as a resistive load.

4. A high-side driver circuit as claimed in claim 3 further comprising a current mirror, wherein said differential amplifier has a tail current set by said current mirror,

wherein an input current to said current mirror is set by a third transistor connected as a resistor, and wherein control connections of said first, second and third transistors are coupled to a common voltage supply.

5. A high-side driver circuit as claimed in any preceding claim wherein said differential amplifier has a differential mode gain of less than 10.
6. A high-side driver circuit as claimed in any preceding claim, wherein said differential amplifier output comprises first and second differential outputs, wherein said driver circuit further comprises a set-reset latch having set and reset inputs coupled to said first and second differential amplifier outputs and having an output coupled to said driver circuit output, and wherein said set and reset inputs have a threshold voltage for setting and resetting said latch of within 20% of a difference between said second voltage supply and said high-side ground rail.
7. A high-side driver circuit as claimed in any preceding claim wherein said differential amplifier has a tail connected to said power connection.
8. A high-side driver circuit as claimed in any preceding claim wherein each of said differential pair of inputs has a respective voltage clamp between the differential input and said power connection.
9. A high-side driver circuit as claimed in claim 8 wherein a said voltage clamp comprises a zener diode.
10. A high-side driver circuit as claimed in claim 8 or 9 further comprising a resistor connected across each said voltage clamp.
11. A high-side driver circuit as claimed in any preceding claim wherein said differential amplifier output comprises first and second differential outputs, and further comprising first and second filter capacitors coupled to said first and second differential outputs.

12. A switching power supply including the high-side driver circuit of any preceding claim.
13. A switching power supply as claimed in claim 12 wherein said switching of said power switching device causes said high-side ground rail to oscillate with a voltage variation of at least 100 volts.
14. A switching power supply as claimed in claim 12 or 13 including a half bridge, and wherein said high-side ground rail is coupled to a mid-point of said half bridge.
15. A switching power supply as claimed in any one of claims 12 to 14 configured for driving a lamp load.
16. A switching power supply as claimed in any one of claims 12 to 14 configured as a dc switch mode power supply.
17. A method of translating a low voltage control signal for a power switching device of a switching power supply into a control signal referenced to a ground which varies over a range of at least 100 volts with respect to said low voltage control signal as a consequence of said power device switching, the method comprising:  
inputting a differential control signal at a first voltage for controlling said power device switching;  
amplifying said differential control signal using a differential amplifier to provide a differential control signal output referenced to said varying ground.
18. A circuit for translating a low voltage control signal for a power switching device of a switching power supply into a control signal referenced to a ground which varies over a range of at least 100 volts with respect to said low voltage control signal as a consequence of said power device switching, the circuit comprising:  
means for inputting a differential control signal at a first voltage for controlling said power device switching; and

means for amplifying said differential control signal using a differential amplifier to provide a differential control signal output referenced to said varying ground.

**Application No:** GB0525619.3

**Examiner:** Mr K Sylvan

**Claims searched:** 1-18

**Date of search:** 6 April 2006

## Patents Act 1977: Search Report under Section 17

### Documents considered to be relevant:

| Category | Relevant to claims | Identity of document and passage or figure of particular relevance                       |
|----------|--------------------|------------------------------------------------------------------------------------------|
| X        | 1,17,18 at least   | US4994955 A<br>North American Philips. See column 5 lines 15-20 and 38-43..              |
| X        | 1, 17,18 at least  | US6897492 B2<br>IXYS. See comparator 530 in figures 3 and 5.                             |
| X        | 1,17,18 at least   | US6781422 B1<br>System General Corp. See comparator 70 in figure 3.                      |
| X        | 1,17,18 at least   | US6781423 B1<br>Dialog Semiconductor. See amplifier in slave IC2 in figure 3B.           |
| A        | -                  | US5274274 A<br>Power Integrations. See Zeners 90,92 in figure 3.                         |
| A        | -                  | US5068571 A<br>US Philips. See lamp in figure 1 and set-reset drive in figure 5.         |
| A        | -                  | WO2003/055072 A1<br>Bang & Olufsen. See the figures and page 3 line 31 to page 4 line 2. |

### Categories:

|   |                                                                                                          |   |                                                                                                                  |
|---|----------------------------------------------------------------------------------------------------------|---|------------------------------------------------------------------------------------------------------------------|
| X | Document indicating lack of novelty or inventive step                                                    | A | Document indicating technological background and/or state of the art.                                            |
| Y | Document indicating lack of inventive step if combined with one or more other documents of same category | P | Document published on or after the declared priority date but before the filing date of this invention.          |
| & | Member of the same patent family                                                                         | E | Patent document published on or after, but with priority date earlier than, the filing date of this application. |

### Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC<sup>X</sup> :

Worldwide search of patent documents classified in the following areas of the IPC

H03K

The following online and other databases have been used in the preparation of this search report



17

WPI,EPODOC, TXTE