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(54) **Title**: RADIO FREQUENCY AMPLIFIER

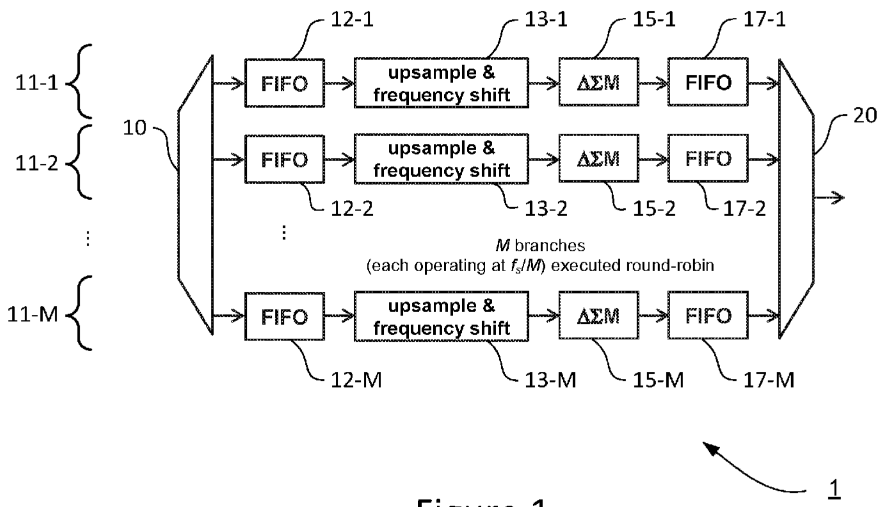

Figure 1

(57) **Abstract**: A modulator circuit is disclosed which comprises a plurality of signal processing branches, each branch comprising a modulator for performing a delta-sigma modulation of a respective data stream portion in order to generate a modulated signal. The modulator circuit receives an input data stream having a carrier frequency; splits the input data stream into a plurality of data stream portions. Delta-sigma modulation is performed in each branch on a respective data stream portion. The respective modulated signals from each branch are combined to form an output signal for outputting at the carrier frequency.

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Radio Frequency Amplifier

The present invention relates to an amplifier for amplifying radio frequency (RF) signals. The invention has particular but not exclusive relevance to delta-sigma amplifiers for wireless communications systems and devices thereof operating according to the Long Term Evolution (LTE) technologies defined by the 3rd Generation Partnership Project (3GPP).

Modern communications standards such as 3G and LTE employ modulation schemes which require linear RF amplifiers. The term ‘linear’ refers to the ability of an amplifier to produce output signals that are accurate copies of the input signal (generally) at increased power levels. Linear amplification is essential for non-constant envelope signals such as OFDM to prevent the creation of unwanted in-band interference signals. Linear amplification must be achieved for peak signal power, not just for average signal power. Peak signal power can be up to 10dB higher than average signal power for OFDM signals.

Linearity is usually achieved by backing-off the amplifier’s power level to below its maximum (and most efficient) region to a region exhibiting a more linear amplification for both the average and the expected maximum signal level. However, this effectively results in a reduction of the amplifier’s overall power efficiency compared to the case when the amplifier operates near its peak power level most of the time. Consequently, linear RF amplifiers typically have a power efficiency of less than 10%.

Various techniques have been employed to achieve more power-efficient linear RF amplifiers, which techniques include, for example, pre-distortion, envelope elimination and restoration, cartesian feedback, and/or the like.

A relatively new approach for efficient linear RF amplification is the use of a so-called S-class amplifier, which uses delta-sigma modulation to generate directly an amplified RF signal. Since S-class amplifiers use field effect transistors (e.g. metal-oxide-semiconductor, ‘MOS’ transistors) (or other transistors) for generating a modulated signal, and since transistors are either turned on or off, efficiency of S-class amplifiers can theoretically approach 100%.

However, a key problem with S-class amplifiers is how to generate a delta-sigma modulation signal that is fast enough to generate an amplified RF signal. This problem arises because the delta-sigma modulation signal frequency (also referred to as the delta sigma bitstream rate) must be at least twice (typically four times) the carrier frequency of the signal to be amplified (due to the Nyquist sampling theorem). It is difficult to compute the delta-sigma modulation signal at high speed because delta-sigma modulation has a single-cycle feedback loop, which consists of several steps including: summation of the input signal with a loop-filtered error signal; quantisation (usually as truncation of a fixed point binary number); and error feedback into a loop filter. The logic in the delta-sigma modulator must be computed at the delta sigma bitstream rate. Since cellular signals may be transmitted at around 1GHz (typically in the range of 800-900MHz for applications such as LTE) or even above 1GHz, the delta-sigma modulation signal must be generated at several GHz. This effectively means that the delta-sigma modulator logic must operate at an impractically high rate, which would inhibit feasible and/or economical implementation of delta-sigma amplification for radio frequency signals used in LTE systems and/or the like.

Accordingly, preferred embodiments of the present invention aim to provide methods and apparatus which address or at least partially deal with the above issues.

For simplicity, the present application will use the term delta-sigma ($\Delta\Sigma$) amplifier to refer to any communications device employing a delta-sigma modulation technology for amplification of a transmitted signal (e.g. a data burst). It will also be appreciated that the technology described herein can be implemented on any (mobile and/or generally stationary) communications device that can communicate with another communications device and/or a communications network.

Although for efficiency of understanding for those of skill in the art, the invention will be described in detail in the context of a delta-sigma amplifier for processing high frequency signals, the principles of the invention can be applied to other systems in which delta-sigma modulation is performed.

In one aspect, the invention provides a modulator circuit comprising: means for receiving an input data stream having a carrier frequency (which may be zero); means for splitting the input data stream into a plurality of data stream portions; a plurality of signal processing branches, each signal processing branch comprising means for performing a delta-sigma modulation of a respective data stream portion of said plurality of data stream portions in order to generate a modulated signal; and means for combining the respective modulated signal from each of said plurality of signal processing branches to form an output signal, and for outputting said output signal at said carrier frequency.

The means for receiving an input data stream, the means for splitting, the plurality of signal processing branches, and the means for combining and for outputting may all form part of a first circuit portion and the output signal of said first circuit portion may comprise a first output signal. In this case, the modulator circuit may further comprise: a second circuit portion, the second circuit portion comprising: further means for receiving the input data stream; further means for splitting the input data stream into a further plurality of data stream portions; a further plurality of signal processing branches, each further signal processing branch comprising respective further means for performing a delta-sigma modulation of a respective further data stream portion of said plurality of further data stream portions in order to generate a further modulated signal; and further means for combining the respective further modulated signal from each of said plurality of further signal processing branches to form a further output signal, and for outputting said further output signal at said carrier frequency as a second output signal; and means for generating a combined output signal from said first output signal and said second output signal, wherein said generating comprises applying a respective window function to each of said first and said second output signals and adding the resulting signals together to form said combined output signal.

The applying of a respective window function may comprise applying a respective time dependent weight to each of said first and said second output signals. The respective time dependent weights applied to said first and said second output signals may sum together to give a constant (e.g. 1).

The respective time dependent weights may vary with time in the manner of a substantially triangular waveform. In this case, the substantially triangular waveform may comprise a substantially continuous triangular waveform in which the sides of the triangular wave are substantially linear.

The respective time dependent weights may vary with time in the manner of a stepped waveform. In this case, the respective time dependent weights may vary with time in the manner of a stepped but generally triangular waveform.

The plurality of data stream portions of the first circuit portion may be offset in time compared to the further plurality of data stream portions of the second circuit portion.

The weight applied to the first output signal may be substantially zero at a start and end of each data stream portion of said plurality of data stream portions, and wherein a weight applied to said second output signal is substantially zero at a start and end of each data stream portion of said further plurality of data stream portions.

In another aspect, the invention provides an amplifier circuit comprising the above described modulator circuit.

In another aspect, the invention provides a method performed by a modulator circuit comprising a plurality of signal processing branches having means for performing a delta-sigma modulation, the method comprising: receiving an input data stream having a carrier frequency; splitting the input data stream into a plurality of data stream portions; in each of said plurality of signal processing branches, performing a delta-sigma modulation of a respective data stream portion of said plurality of data stream portions in order to generate a modulated signal; combining the respective modulated signal from each of said plurality of signal processing branches to form an output signal; and outputting said output signal at said carrier frequency.

Aspects of the invention extend to corresponding computer program products such as computer readable storage media having instructions stored thereon which are operable to program a programmable processor to carry out a method as described in the aspects and possibilities set out above or recited in the claims and/or to program a suitably adapted computer to provide the apparatus recited in any of the claims.

Each feature disclosed in this specification (which term includes the claims) and/or shown in the drawings may be incorporated in the invention independently (or in combination with) any other disclosed and/or illustrated features. In particular but without limitation the features of any of the claims dependent from a particular independent claim may be introduced into that independent claim in any combination or individually.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings in which:

Figure 1 illustrates schematically a delta-sigma modulator for processing concatenated independent blocks;

Figure 2 is a schematic diagram of an exemplary radio frequency delta-sigma amplifier circuit which includes the delta-sigma modulator shown in Figure 1;

Figure 3 is a schematic diagram illustrating an exemplary error feedback delta-sigma modulator forming part of the delta-sigma modulator shown in Figure 1;

Figure 4 illustrates an exemplary noise transfer function for bandpass delta-sigma amplifier in accordance with embodiments of the present invention;

Figure 5 is an exemplary timing snapshot illustrating the operation of a branch of a delta-sigma modulator employing concatenated independent blocks;

Figure 6 is an exemplary power spectral density diagram illustrating simulation results for different block lengths;

Figures 7a and 7b illustrate an exemplary window function and a possible implementation thereof;

Figure 8 is an exemplary power spectral density diagram illustrating simulation results when employing the window function shown in Figure 7a;

Figures 9a and 9b illustrate another exemplary window function and a possible implementation thereof; and

Figure 10 is an exemplary power spectral density diagram illustrating simulation results when employing the window function shown in Figure 9a.

Overview

Figure 1 schematically illustrates a delta-sigma modulator circuit 1 for processing RF signals. Specifically, the delta-sigma modulator circuit 1 comprises a so-called Donoghue-Phillips-Tan delta-sigma modulator (hereafter referred to as a DPT modulator 1) forming part of an exemplary (S-Class) RF amplifier 2. As illustrated in more detail in Figure 2, the RF amplifier 2 includes, amongst others, the DPT modulator 1, transistor switching circuits and a bandpass filter.

In this example, modulation of a transmit signal is achieved using concatenated independent blocks (CIBs). Specifically, each transmit burst (received at demultiplexer 10) is split into a number of consecutive blocks of output symbols and for each block upsampling, frequency shift and modulation is performed independently.

As generally shown in Figure 1, processing of the consecutive blocks is realised by demultiplexing, in a “round-robin” manner, the blocks of input baseband samples to a number of branches 11-1 to 11-M at the demultiplexer 10. Each branch 11 comprises a respective: input buffer 12-1 to 12-M; optionally an independent upsampler and frequency shift portion 13-1 to 13-M ; delta-sigma modulator portion 15-1 to 15-M (denoted ‘ΔΣM’ in Figure 1); and output buffer 17-1 to 17-M.

Each input buffer 12 and each output buffer 17 comprises a suitable ‘first-in-first-out’ (FIFO) input buffer. Each upsampler and frequency shift portion 13 may comprise, for example, a finite impulse response (FIR) filter, cascaded integrator–comb (CIC) filters, oscillator and a frequency mixer, although it will be appreciated that other types of filters and/or other filter combinations and frequency shifters may also be used. It will also be appreciated that the upsampler and frequency shift portions 13-1 to 13-M are optional and may be omitted.

Each block of symbols from the demultiplexer 10 are buffered in the input buffer 12 of a respective branch 11 for processing that block. Symbols are taken from input buffer in a FIFO manner and are (optionally) upsampled and frequency shifted by the corresponding upsampler and frequency shift portion 13 to provide an upsampled and frequency shifted output. The upsampled and frequency shifted output is modulated by the corresponding delta-sigma modulator portion 15. The modulated output from each delta-sigma modulator portion 15 (i.e. the signal corresponding to the block processed by that branch 11) is buffered in the corresponding FIFO output buffer 17. The contents of the output buffers 17 are multiplexed into an output signal at a multiplexer 20.

Thus, effectively, each part of the multiplexed signal is generated 'offline', in a round-robin manner, via a different branch 11, before being re-combined (multiplexed) at the output multiplexer 20 of the DPT modulator circuit 1 to re-combine the signals from the respective branches into a single modulated signal stream. Finally, the re-combined signal is sent to appropriate transmit circuitry (e.g. a switching amplifier and bandpass filter, shown in Figure 2) for transmission at the required power level.

Beneficially, each branch 11 (thus each delta-sigma modulator portion 15) can operate at a relatively low rate of f_s/M, where 'f_s' is the delta-sigma bitstream rate (e.g. a minimum of twice the carrier frequency), and 'M' is the number of branches. Thus, beneficially, by using an appropriate number of branches (which, in this example, effectively corresponds to the number of CIBs) and an appropriate delta-sigma bitstream rate (i.e. the internal processing frequency of the delta-sigma modulator portion 15 in each branch 11), it is possible to achieve efficient amplification whilst employing delta-sigma modulators at a significantly lower and more practical clock rate (e.g. in the range of approximately 50-200MHz) than would otherwise be required.

The resulting delta-sigma amplification circuit 2 (including the DPT modulator 1) is able to achieve the necessary parallelism and linearity for high frequency applications such as amplification of radio frequency signals (e.g. OFDM).

Operation

A more detailed description will now be given (with reference to Figures 1 to 6) of an exemplary delta-sigma modulation technique implemented in accordance with an embodiment of the present invention.

Figure 2 illustrates an exemplary S-class RF amplifier 2 which includes the DPT modulator 1 shown in Figure 1.

As can be seen, the amplifier 2 can receive (at its input) a digital (e.g. OFDM) signal which may be at baseband, at an intermediate frequency or at the carrier frequency. The digital signal is optionally upsampled and frequency shifted, and then modulated by the DPT modulator 1. The modulated input signal is sent through a complementary metal-oxide-semiconductor (CMOS) or other type of transistor circuit, which results in an amplified output signal (denoted ‘Amplified Output’ in Figure 2) being generated at the output of the transistor circuit. Finally, by applying an appropriate (typically bandpass) filtering, an output signal (substantially corresponding to a copy of the input signal, albeit at increased power level and shifted frequency) is provided at the output of the amplifier shown in Figure 2.

Figure 3 illustrates an exemplary delta-sigma error feedback model that may be used to help understand operation of the delta-sigma modulator (ΣΔM) portion 15 shown in Figure 1.

A delta-sigma modulator (ΣΔM) is effectively an infinite impulse response (IIR) filter, thus its current state depends on an infinite history of previous states (i.e. it has an impulse response which does not become zero past a certain point, but continues indefinitely). The delta-sigma modulator also has a non-linearity in its feedback loop meaning that standard linear time-invariant (LTI) analysis for the delta-sigma modulator fails.

In this example, in order to illustrate the operation of the feedback model, the quantiser shown in Figure 3 may be considered, conceptually, to be replaced with the addition of a quantisation error, +E(*z*), which equals the difference between the quantiser’s input and its output ($T_{output} - T_{input}$). Thus the following superposition can be exploited:

$$V(z)=NTF(z).E(z)+U(z)$$

where U(*z*) is the input signal, V(*z*) is the output signal, NTF(*z*) is a noise transfer function equal to 1 – H(z) (H(z) being the feedback function as shown in Figure 3), and E(*z*) is the quantisation error.

Therefore, in effect, the signal U(z) goes straight through to the output additively. Effectively, E(z) is a spectrally white quantisation error, but the feedback shapes it by the noise transfer function, NTF(z), forcing it to be correlated.

The noise transfer function (NTF(z)) is designed to dump noise energy into regions of spectrum outside a band of interest around 'U(z)'. Any signal (noise) falling into such outside or "don't care" regions may be removed from further processing by applying an appropriate filter to the signal (e.g. a bandpass filter, a pair of appropriately configured low-pass and high-pass filters, and/or the like). The resulting filtered signal is therefore more likely to comprise information corresponding to the input signal U(z) than noise.

Figure 4 illustrates the resulting noise transfer function with a sharp notch around the carrier frequency 'f_c' for an exemplary 4th order bandpass delta-sigma amplifier, configured with the following parameters:

- quantiser output is ±1;
- NTF(z) = $[1\ 0\ 2z^{-2}\ 0\ z^{-4}]$;
- $H(z)$ = 1-NTF(z) = $[0\ 0\ -2z^{-2}\ 0\ -z^{-4}]$;
- f_c = 800MHz (carrier frequency);
- $f_s = 4f_c$ = 3.2GHz (i.e. the delta-sigma bitstream rate is four times the carrier frequency);
- noise is outside of $f_S/4$ notch, removed by channel filtering after transistor amplifier; and
- it has odd/even decomposition equivalent to two interleaved high-pass delta-sigma modulators.

Modulation using concatenated independent blocks

Figure 5 is an example timing diagram (timing snapshot) illustrating a method carried out by components of the DPT modulator circuit 1 shown in Figure 1. Specifically, Figure 5 illustrates the operation of the first branch 11-1 in relation to the operation of the other branches 11 of the delta-sigma amplification circuit 1. For sake of simplicity, the number of branches in this case is four, although it will be appreciated that in practice a different (typically greater) number of branches may be used.

As illustrated generally at step S101, a processing round (for branch 11-1) begins by filling up the input buffer 12-1 with the corresponding block of data (i.e. the first demultiplexed portion of the data burst received at the input 10 of the DPT modulator circuit 1).

Next, in step S102, processing of the content of the input buffer 12-1 begins. Specifically, the delta-sigma modulator portion 15-1 reads the data from the input buffer 12-1 (e.g. following an appropriate upsampling and frequency shift by the upsampling and frequency shift portion 13-1) and performs an appropriate delta-sigma modulation at the rate of f_s/M (where 'f_s' is the delta-sigma bitstream rate; and 'M' is the number of branches, i.e. in this case, four). As generally shown in step S103, once the delta-sigma modulation for this block of data is complete, the modulated data is made available for sending to the output 20 (e.g. via output buffer 17-1).

As can be seen at step S111, prior to outputting the modulated signal at S103, the already emptied input buffer 12-1 is being filled up with the next block of data (i.e. the fourth subsequent block) that needs to be processed by this branch 11-1 so that upon outputting the processed (modulated) signal at S103, processing of the next block can begin immediately (at step S112).

Further, as shown generally at S201, the second branch 11-2 (and similarly the third and fourth branches) carries out the same procedure as explained above with reference to steps S101 to S103, albeit processing for each subsequent branch being shifted in time by the block length relative to the immediately preceding branch.

It is worth noting that, since the clock rate of the delta-sigma modulator portion 15-1 is one fourth of the overall bitstream rate (i.e. $f_s/4$), processing of each block of data will effectively take four times longer compared to conventional delta-sigma modulation techniques (which may not work at such a high frequency).

However, since each branch 11 processes its allocated block of data at the same rate, and since there are four branches (in this example) each processing one fourth of the transmit burst, the resulting output signal (at output 20) has the same rate as the original signal (at input 10).

Advantageously, as illustrated at step S111 of Figure 5, an optional "lead-in" (comprising a predetermined number of overlapping samples) may be provided when filling up the input buffers 12 of each branch 11 prior to receiving the actual data to be processed by that branch 11. Such a lead-in may allow each branch 11 to reach a comparable state (to state of the preceding branch), which in turn may beneficially reduce/minimise transients resulting from switching between output blocks from one branch 11 (stream) to another.

For example, an optional overlap of at least 1% (but preferably between 5% and 20%) of the length of the processed block of data may greatly improve the overall noise floor resulting from processing of a series of (concatenated) blocks of data via multiple parallel branches 11. However, the use and the length of a lead-in overlap may depend on implementation, e.g. the type of signal being modulated, the level of amplification to be achieved, the number of branches / blocks used, whether the FIFO buffers are shared between branches, and/or the like.

Noise floor

Figure 6 is an exemplary power spectral density diagram illustrating simulation results for different block lengths (B). Specifically, Figure 6 illustrates the results for a simple test signal and 4^{th} order delta-sigma modulator (with $f_s = 4f_c$). In this case, the bottom curve shows the ideal noise floor and the other curves (from top to bottom) show progressively better noise floors in the vicinity of the desired signal. The top curve corresponds to a block length of B=16 samples and the curve immediately above the ideal curve (i.e. the second curve from the bottom) corresponds to B=65536 samples. The lead-in time (L) used in this example is the same as the block length (i.e. L=B), which represents a pessimistically high estimate for a lead-in time that would be required in real life scenarios. In any case, it has been found empirically that varying the value of L (e.g. choosing a lower L value) has negligible effect on the curves compared to the effect of the block length (B). However, it will be appreciated that an appropriate lead-in time (e.g. L<B) may be necessary in case of the architecture shown in Figure 1 in order to flush the finite memory of the upsamplers and frequency shifter portions 13 and delta-sigma modulator portions 15 to the correct state.

The results show that with sufficiently long block-length (B), the noise-floor of the DPT modulator circuit 1 approaches that of a conventional delta-sigma modulator. The resulting noise floor is therefore sufficiently low for practical RF amplifier applications.

Extension to High-Order Modulators

The order of a delta-sigma modulator is determined by the order of noise shaping filter (H(z) in Figure 3).

Generally, high-order (e.g. sixth order and above) delta-sigma modulators are known to provide a number of performance benefits compared with lower-order (e.g. fourth order) delta-sigma modulators. For example, a sixth order delta-sigma modulator generates a significantly lower noise floor in the frequencies surrounding a wanted signal, which results in a wanted signal with higher signal to noise ratio.

Moreover, it is also beneficial to use the largest possible numerical signal at the input to a delta-sigma modulator because doing so results in generation of the largest possible wanted output signal, and maximises the ratio of wanted output signal power to the total output power, thereby simplifying the task of creating a power-efficient amplifier.

However, higher order delta-sigma modulators are only conditionally stable. As a result, only signals below a certain maximum input level can be converted without causing the modulator to become unstable. The level at which the modulator becomes unstable is a function of the modulator order with higher order modulators becoming unstable at lower input levels. A delta-sigma modulator is not useful once unstable because the delta-sigma modulator ceases to have the desired noise shaping properties. Consequently, there is a trade-off between increasing the order of the modulator and the maximum input level. Sixth-order delta-sigma modulators, for example, are known to become unstable for input signals of a level that might otherwise be desirable for simplifying the task of creating a power-efficient amplifier.

Beneficially, a variation on the above examples allows higher-order delta-sigma modulation to be applied, without causing an undesirable level of instability.

Specifically, in this example, the DPT modulator 1 employs high-order (in this example sixth-order) delta-sigma modulators 15 to process concatenated independent blocks of finite length, where the delta-sigma modulator 15 is reset to its initial state before processing each new block. Advantageously, this takes advantage of the fact that modulator instability only becomes apparent after a very large number of input samples (typically millions).

It can be shown that by resetting the delta-sigma modulator 15 between each block, the DPT modulator 1 can remain stable for significantly larger numerical input signals than would have been possible for a conventional sixth-order delta-sigma modulator. Accordingly, this allows the DPT modulator to generate a significantly larger wanted output signal than would otherwise have been possible, which simplifies the task of creating a power-efficient amplifier.

Moreover, using a fixed block length, as described above, for the DPT modulator 1 has the potential to allow the use of other complex of noise-shaping filters which would otherwise be unstable when employed within a conventional delta-sigma modulator.

Benefits

In summary, the delta-sigma amplification circuit 2 with DPT modulator circuit 1 provides at least the following benefits over conventional delta-sigma amplifiers.

The DPT modulator circuit 1 is able to achieve a higher bitstream rate (than conventional delta-sigma modulators) since each parallel path can be computed independently at a slower clock rate. The DPT modulator circuit 1 may also achieve a low noise floor (suitable for RF use) by making the block lengths arbitrarily long.

In addition, the DPT modulator circuit 1 may beneficially employ a wide range of noise-shaping filters, e.g. filters that include multi-bit multiplications (due to the lower clock rate of the filters). Similarly, the DPT modulator circuit 1 may also employ reprogrammable noise-shaping filters that include multi-bit multiplications (due to the lower clock rate of the filters).

The DPT modulator circuit 1 may be used as part of a particularly efficient, linear RF amplifier circuit 2. In this case, the following benefits may also be achieved:

- operation at a high frequency by virtue of the DPT modulator's 1 overall high delta-sigma bitstream rate (measured at its output 20);
- high linearity (due to the high delta-sigma bitstream rate);
- power efficiency; and
- high flexibility with respect to amplification level and/or operating at any frequency (typically up to half the delta-sigma bitstream rate).

Other Modifications and Alternatives

Detailed embodiments have been described above. As those skilled in the art will appreciate, a number of modifications and alternatives can be made to the above embodiments whilst still benefiting from the inventions embodied therein. By way of illustration only a number of these alternatives and modifications will now be described.

Whilst in the above examples, M parallel streams (branches 11-1 to 11-M) are shown, it will be appreciated that the actual number of parallel streams used may depend on the frequency of the RF signal to be processed by the delta-sigma amplifier. For example, the higher the frequency of the RF signal, the more streams may be used (whilst any unused streams may be switched off).

It will be appreciated that there is no limit to the number of parallel branches (M) that can be used, allowing each parallel path to operate at an arbitrarily low clock frequency.

An additional cost associated with the CIB delta-sigma amplifier of Figure 2 (compared to conventional delta-sigma amplifiers) results from the need for additional silicon area to implement the parallel branches. However, this cost is in practice quite small and can be reduced to less than US$1.

The largest potential impact on silicon area is the need for input FIFO buffers before the delta-sigma modulators. If the input buffers are placed directly at the input of their associated delta-sigma modulator then they must be greater than B samples deep. However, if the input buffers are placed at the input of their associated upsampler and frequency shift portion (as shown in Figure 1) then they may be reduced in size by the upsampling ratio (which is typically 200). The configuration shown in Figure 1 thus beneficially reduces the associated silicon size (and hence cost) for the input buffers to a negligible level.

Nevertheless, the order of the input FIFO buffers 12 and upsampler and frequency shift portions 13 may be reversed, albeit at the potential cost of an increase in the overall size of the FIFO buffer and hence silicon area or circuit board required to implement the delta-sigma amplifier.

It will be appreciated that the functionality provided by the upsampler and frequency shift portions is optional and it is not necessary for realising the DPT modulator shown in Figure 1.

As described above with reference to Figure 6, the concatenated independent blocks (CIB) based approach employed by the RF amplifier may introduce a noise floor in the band-of-interest. The noise floor is largely influenced by the number of times it is necessary to switch between parallel delta-sigma paths – i.e. the smaller the blocks are, the more often it is necessary to switch between parallel delta-sigma paths, resulting in an increased noise. In other words, the noise floor may be reduced by increasing the block length, albeit at the expense of increased latency and memory size.

It will be appreciated that it may be possible to reduce the noise transient associated with switching between parallel delta-sigma paths (i.e. from branch to branch) by having a window period over which the delta-sigma streams overlap and applying statistical fading between the outputs of the two bitstreams. Statistical fading between two bitstreams may be achieved, for example, by choosing bits from either a first or a second bitstream on a weighted random basis. In this case, at the start of the fading window, bits are more likely to be chosen from the first bitstream; at the middle of the fading window bits are equally likely to be chosen from either bitstream; and at the end of the fading window, bits are more likely to be chosen from the second bitstream.

It may also be possible to reduce the noise transient and noise floor associated with switching between parallel delta-sigma paths by providing an overlapping window period. In this case, switchover may occur, during this window period, at the cycle of minimum/optimal state difference between the two delta-sigma modulator paths.

In one particularly beneficial example, data from two parallel bit streams each representing a different respective delta-sigma path for the same data, but with the boundary of CIBs at different positions, may be combined using a predetermined window function to weight the contribution from each path version to the combined total. Such a window function (or 'weighting function') may be employed for gradually switching between the outputs of the two path versions, and then back again, such that the contribution from data at the edges of the CIBs in each path is minimised. Such gradual switching may result in a significantly reduced noise floor compared to the case when using the output of a single bitstream only (for a given block length). In other words, by gradually alternating between the outputs of the two versions of the delta-sigma path using a window function, the RF amplifier may achieve the same (or in some cases lower) noise floor even at relatively small block lengths, as a DPT circuit employing a large block length (but no weighting window). Accordingly, the drawbacks (e.g. latency) associated with increased block length can be alleviated by employing a window function based gradual switching between the outputs of two bitstreams (even for relatively small block lengths).

It will be appreciated that a number of suitable window functions may be used to achieve a reduced noise floor without requiring an increase of the block length to an undesirable level. It will be appreciated that such a window function may be applied to the bitstreams (the outputs of which are being combined) at a suitable point (e.g. after the respective multiplexer circuit outputs of two versions of the circuit shown in Figure 1). Two of such exemplary window functions are described below with reference to Figures 7a to 10.

In a first example, the outputs of two DPT modulator units are combined in a weighted fashion according to a triangular window function shown in Figures 7a and 7b. Figure 8 shows the resulting spectrum (using a 6th order 40MHz bandwidth, 3GHz sample rate).

It has been shown that using the triangular window function, the noise floor drops by 6dB for each doubling of the block length (compared to a drop of 3dB when not using the triangular window function). Importantly, the performance of a regular CIB (an RF amplifier that does not use a window function) with block length 'N' can be achieved with block length sqrt(N) when using a window function (e.g. as shown in Figures 7a and 7b).

Beneficially, this windowing approach produces a dramatic reduction in delay and required memory resources. It allows achieving a performance equivalent to conventional delta-sigma converters (where, effectively, 'N' = infinity) using block lengths in the range of N=256 to N=1000 (approximately).

Figures 9a and 9b illustrate a stepped triangular window function (with 4-bit resolution in the steps, i.e. 16 distinct steps), and Figure 10 illustrates the resulting spectrum (using a 6th order 40MHz bandwidth, 3GHz sample rate). Although the effect of such a stepped triangular window on the noise floor is not as good as that of the triangular window of Figure 7a, however, it is approximately 10 to 12dB better than using a regular CIB (that does not employ a window function). This suggests a reduction of about 3dB in the noise floor for each bit of resolution in the stepped triangular window. This also suggests that about 10 bits of resolution would be required to achieve optimal performance when using a stepped triangular window function with a blocks length of N=256.

It will be appreciated that when employing a window function, the combined weight of the contributions from the two path versions (i.e. the sum of 'weight1' and 'weight2' in Figures 7b and 9b) is constant.

It will be appreciated that the DPT modulator will typically be implemented on an application-specific integrated circuit (ASIC) or a field-programmable gate array (FPGA). The delta-sigma bitstream may be routed to multiple serializer/ deserializer (SerDes) outputs, which may allow easy connection to multiple RF driver stages with different bandpass characteristics.

It will be appreciated that FPGAs are available with SerDes that are able to switch at 28GHz. It is therefore possible to support delta-sigma RF amplifiers for microwave applications (e.g. up to 14GHz).

It will be appreciated that the delta-sigma amplifier may generate signals for multiple carriers spaced across a wide band (i.e. the same delta-sigma amplifier may be configured to operate over a wide bandwidth with several carriers spaced within that bandwidth; alternatively the same delta-sigma amplifier may be configured to operate over several narrow bands, spaced over a wide bandwidth, with a carrier in each of the narrow bands).

It will be appreciated that any non-linearity caused by RF driver transistors and/or analogue bandpass filter may be compensated via pre-distortion of the modulated signal.

It will be appreciated that certain high-power RF transistors may not be fast enough for some applications. In order to alleviate such limitations, the delta-sigma bitstream may be extended from binary to multi-bit in order to drive multiple RF transistors simultaneously. In this case, the RF transistors may have equal or weighted drive strengths.

It will be appreciated that a DPT modulator using multiple branches may be implemented as part of a digital to analogue converter and/or as part of an analogue to digital converter.

It will be appreciated that a DPT modulator using multiple branches may be implemented as part of a radio transmitter and/or a radio receiver.

In the above description, an exemplary implementation is given for a delta-sigma amplifier for LTE communications technology. However, it will also be appreciated that the above solution may also be implemented using other communications technologies such as Wi-Fi, Bluetooth, and/or the like. The above embodiments are applicable to both ‘non-mobile’ and generally stationary communication devices, such as user equipment and/or base station apparatus.

The splitting means might comprise a demultiplexer and the combining means might comprise a multiplexer.

Each delta-sigma modulation means might be configured to operate at a branch modulation rate generally inversely dependent on the number of branches. For example, the modulation rate might be at least approximately defined by the equation $f_b = f_s / M$, where 'f_b' is the branch modulation rate, 'f_s' is a fundamental modulation rate required for processing a signal having said carrier frequency using a single delta-sigma modulator, and 'M' is the number of branches.

The carrier frequency might be between 800MHz and 14GHz (preferably between 800MHz and 2600MHz as used in LTE networks) and each delta-sigma modulation means might be configured to operate at a branch modulation rate of between 50MHz and 200MHz.

The plurality of signal processing branches might be configured to perform delta-sigma modulation of each of said plurality of data stream portions in a substantially parallel manner.

The splitting means might be operable to split said input data stream into a sequence of chronologically generally consecutive blocks, each block forming a different one of said data stream portions. In this case, each of said generally consecutive blocks might have a portion that is common to at least one (preferably two) neighbouring blocks of said sequence.

Each of said plurality of signal processing branches might have a respective input buffer for buffering associated data stream portions. Each input buffer might comprise a first-in/first-out (FIFO) buffer.

Each of said plurality of signal processing branches might comprise respective means for upsampling and frequency shifting input data for modulation by said delta-sigma modulation means of that branch.

The plurality of data stream portions might comprise a plurality of concatenated independent blocks of data.

The delta-sigma modulation may advantageously be applied in an amplifier that employs a class-D output stage. This provides, *inter alia*, benefits in terms of power efficiency.

Various other modifications will be apparent to those skilled in the art and will not be described in further detail here.

CLAIMS

1. A modulator circuit comprising:

   means for receiving an input data stream having a carrier frequency;

   means for splitting the input data stream into a plurality of data stream portions;

   a plurality of signal processing branches, each signal processing branch comprising means for performing a delta-sigma modulation of a respective data stream portion of said plurality of data stream portions in order to generate a modulated signal; and

   means for combining the respective modulated signal from each of said plurality of signal processing branches to form an output signal, and for outputting said output signal at said carrier frequency.

2. The modulator circuit according to claim 1, wherein said splitting means comprises a demultiplexer and said combining means comprises a multiplexer.

3. The modulator circuit according to claim 1 or 2, wherein each delta-sigma modulation means is configured to operate at a branch modulation rate generally inversely dependent on the number of branches.

4. The modulator circuit according to claim 3, wherein said modulation rate is at least approximately defined by the following equation:

$$f_b = f_s / M$$

   where 'f_b' is the branch modulation rate, 'f_s' is a fundamental modulation rate required for processing a signal having said carrier frequency using a single delta-sigma modulator, and 'M' is the number of branches.

5. The modulator circuit according to any of claims 1 to 4, wherein said carrier frequency is between 800MHz and 14GHz and each delta-sigma modulation

means is configured to operate at a branch modulation rate of between 50MHz and 200MHz.

6. The modulator circuit according to any of claims 1 to 5, wherein said plurality of signal processing branches is configured to perform delta-sigma modulation of each of said plurality of data stream portions in a substantially parallel manner.

7. The modulator circuit according to any of claims 1 to 6, wherein said splitting means is operable to split said input data stream into a sequence of chronologically generally consecutive blocks, each block forming a different one of said data stream portions.

8. The modulator circuit according claim 7, wherein each of said generally consecutive blocks has a portion that is common to at least one (preferably two) neighbouring blocks of said sequence.

9. The modulator circuit according to any of claims 7 or 8 wherein said blocks have a length that is set to provide a desired noise floor.

10. The modulator circuit according to any of claims 1 to 8, wherein each of said plurality of signal processing branches has a respective input buffer for buffering associated data stream portions.

11. The modulator circuit according to claim 10, wherein each said input buffer comprises a first-in/first-out, FIFO, buffer.

12. The modulator circuit according to claim 10 or 11, wherein each said input buffer is provided at the input side of means for upsampling and frequency shifting input data for modulation by said delta-sigma modulation means of that branch.

13. The modulator circuit according to any of claims 1 to 11, wherein each of said plurality of signal processing branches comprises respective means for upsampling and frequency shifting input data for modulation by said delta-sigma modulation means of that branch.

14. The modulator circuit according to any of claims 1 to 13, wherein said plurality of data stream portions comprises a plurality of concatenated independent blocks of data.

15. The modulator circuit according to any of claims 1 to 14, further comprising at least one noise-shaping filter wherein said noise-shaping filter is operable to utilise a multi-bit multiplication.

16. The modulator circuit according to claim 15, wherein said noise-shaping filter comprises a reprogrammable noise-shaping filter.

17. The modulator circuit according to any of claims 1 to 16 wherein said modulator circuit is operable to reset each said means for performing a delta-sigma modulation, to its original internal state, between processing each data stream portion and processing a subsequent data stream portion.

18. The modulator circuit according to claim 17 wherein each said means for performing a delta-sigma modulation is of an order that would result in that means for performing a delta-sigma modulation becoming unstable when processing a data stream portion of above a particular length and wherein the size of each data stream portion is set to be shorter than said particular length at which said means for performing a delta-sigma modulation becomes unstable.

19. The modulator circuit according to any of claims 1 to 18 wherein the means for receiving an input data stream, the means for splitting, the plurality of signal processing branches, and the means for combining and for outputting all form part of a first circuit portion and wherein the output signal of said first circuit portion comprises a first output signal; the modulator circuit further comprising:

a second circuit portion, the second circuit portion comprising:

further means for receiving the input data stream;

further means for splitting the input data stream into a further plurality of data stream portions;

a further plurality of signal processing branches, each further signal processing branch comprising respective further means for performing a delta-sigma modulation of a respective further data stream portion of said plurality of further data stream portions in order to generate a further modulated signal; and

further means for combining the respective further modulated signal from each of said plurality of further signal processing branches to form a further output signal, and for outputting said further output signal at said carrier frequency as a second output signal; and

means for generating a combined output signal from said first output signal and said second output signal, wherein said generating comprises applying a respective window function to each of said first and said second output signals and adding the resulting signals together to form said combined output signal.

20. The modulator circuit according to claim 19 wherein said applying of a respective window function comprises applying a respective time dependent weight to each of said first and said second output signals.

21. The modulator circuit according to claim 19 or 20 wherein said respective time dependent weights applied to said first and said second output signals sum together to give a constant (e.g. 1).

22. The modulator circuit according to any of claims 19 to 21 wherein the respective time dependent weights vary with time in the manner of a substantially triangular waveform.

23. The modulator circuit according to any of claim 22 wherein the substantially triangular waveform comprises a substantially continuous triangular waveform in which the sides of the triangular wave are substantially linear.

24. The modulator circuit according to any of claims 19 to 21 wherein the respective time dependent weights vary with time in the manner of a stepped waveform.

25. The modulator circuit according to claim 24 wherein the respective time dependent weights vary with time in the manner of a stepped but generally triangular waveform.

26. The modulator circuit according to any of claims 19 to 25 wherein the plurality of data stream portions of the first circuit portion are offset in time compared to the further plurality of data stream portions of the second circuit portion.

27. The modulator circuit according to any of claims 20 to 26 wherein a weight applied to said first output signal is substantially zero at a start and end of each data stream portion of said plurality of data stream portions, and wherein a weight applied to said second output signal is substantially zero at a start and end of each data stream portion of said further plurality of data stream portions.

28. An amplifier circuit comprising the modulator circuit according to any of claims 1 to 27.

29. The amplifier circuit according to claim 28 wherein said amplifier is configured to operate up to half the frequency of a bit rate of said delta-sigma modulation.

30. The amplifier circuit according to claim 28 wherein said amplifier circuit employs delta-sigma modulation of a class-D output stage.

31. Apparatus comprising at least one of: a digital to analogue converter that employs a modulator circuit according to any of claims 1 to 27; an analogue to digital converter that employs a modulator circuit according to any of claims 1 to 27; a radio transmitter that employs a modulator circuit according to any of claims 1 to 27; and a radio receiver that employs a modulator circuit according to any of claims 1 to 27.

32. A method performed by a modulator circuit comprising a plurality of signal processing branches having means for performing a delta-sigma modulation, the method comprising:

receiving an input data stream having a carrier frequency;

splitting the input data stream into a plurality of data stream portions;

in each of said plurality of signal processing branches, performing a delta-sigma modulation of a respective data stream portion of said plurality of data stream portions in order to generate a modulated signal;

combining the respective modulated signal from each of said plurality of signal processing branches to form an output signal; and

outputting said output signal at said carrier frequency.

33. A computer implementable instructions product comprising computer implementable instructions for causing a programmable computer device to perform the method of claim 32.

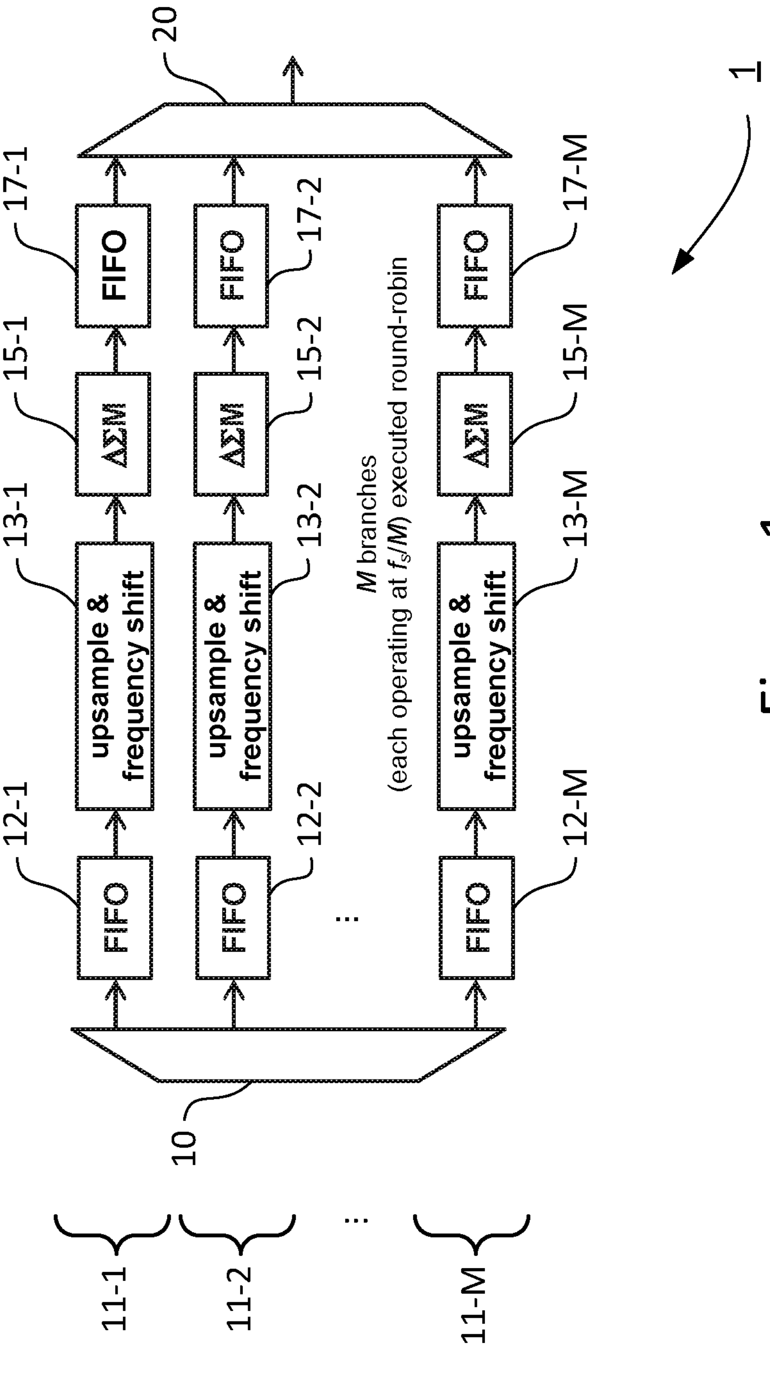

20
17-1
17-2
17-M
FIFO
15-1
15-2
15-M
ΔΣM
13-1
13-2
13-M
upsample & frequency shift
M branches
(each operating at fs/M) executed round-robin
12-1
12-2
12-M
FIFO
...
10
11-1
11-2
11-M
1

Figure 1

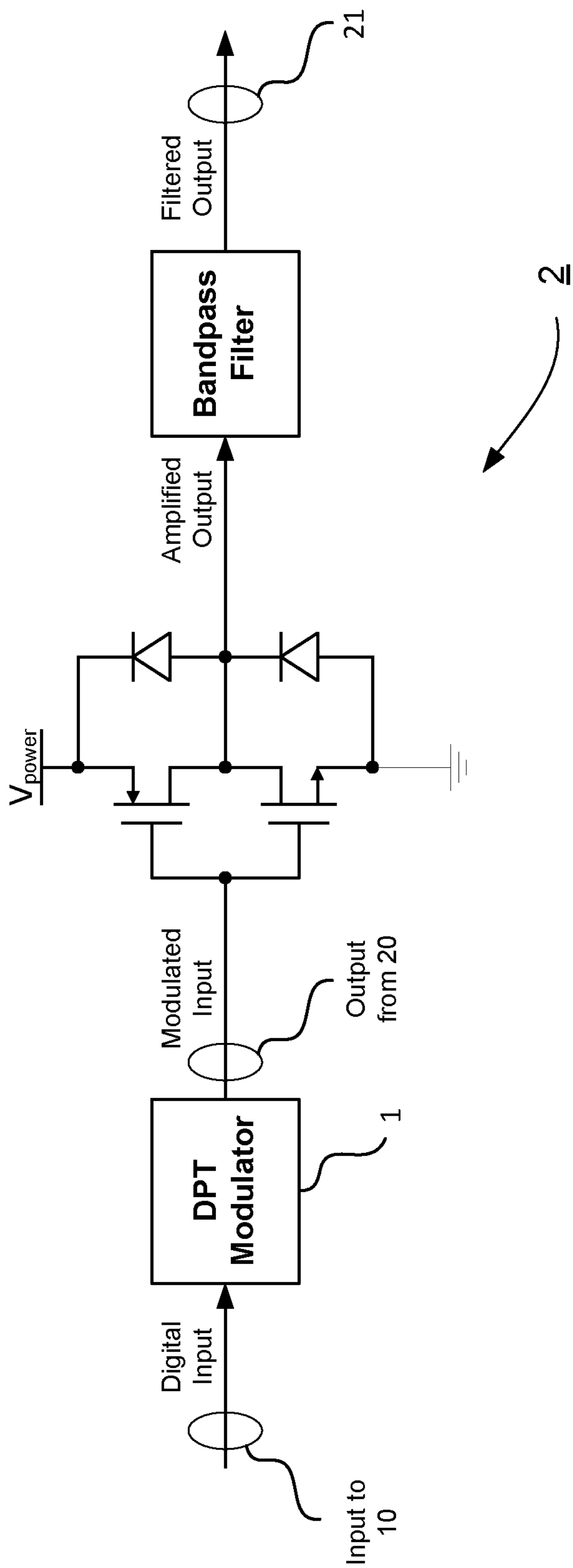

Digital Input
Input to 10
DPT Modulator
1
Modulated Input
Output from 20
V_{power}
Amplified Output
Bandpass Filter
Filtered Output
21
2

Figure 2

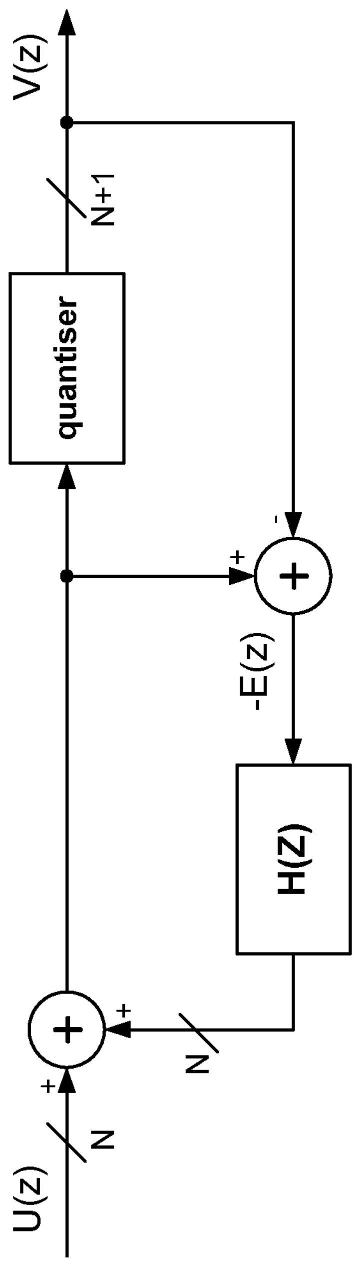


Figure 3

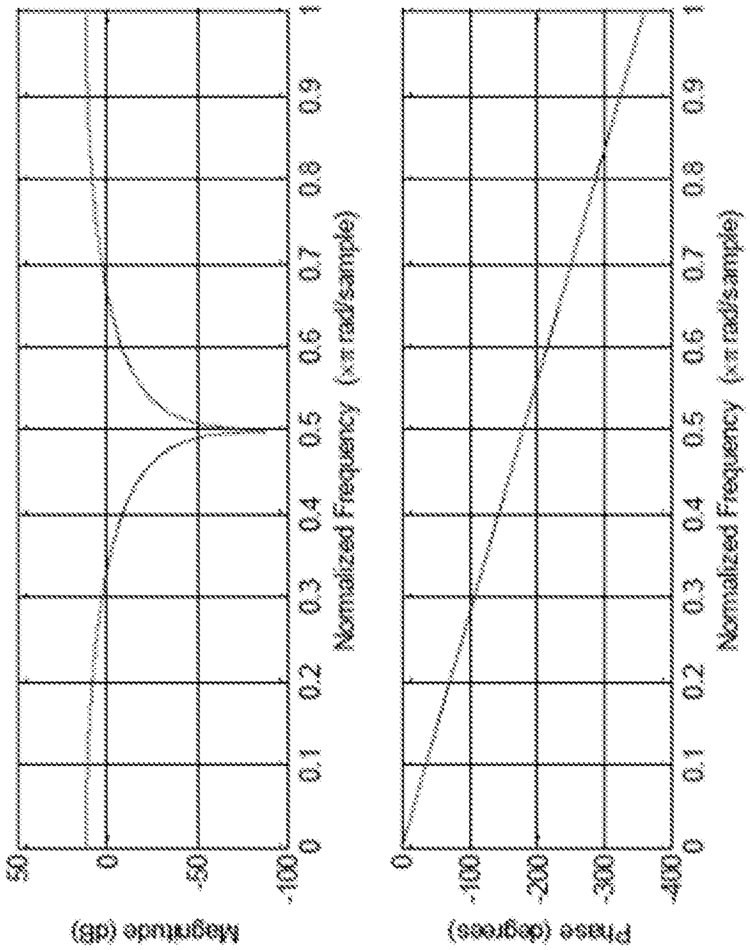
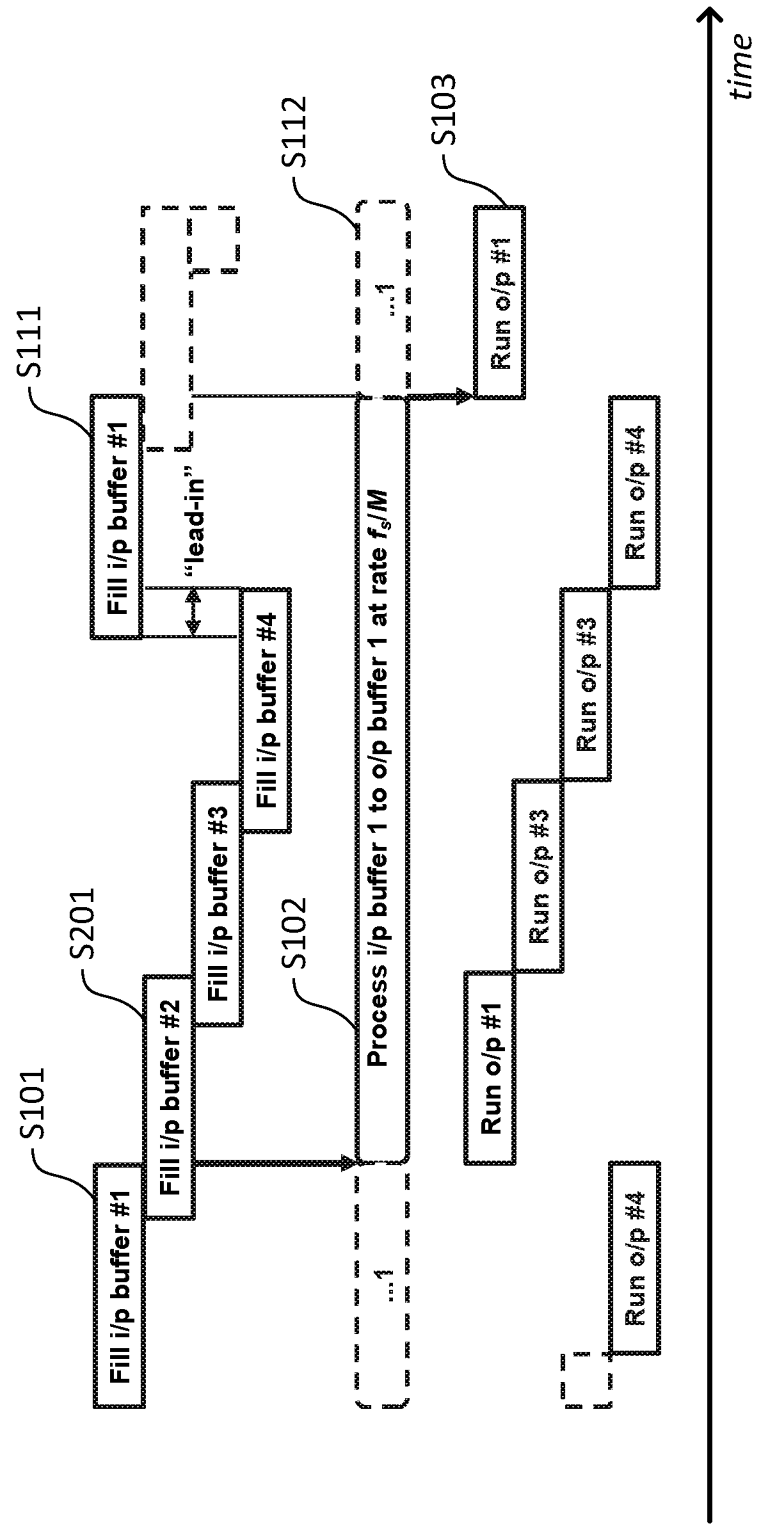

Magnitude (dB)
Phase (degrees)
Normalized Frequency (×π rad/sample)
Normalized Frequency (×π rad/sample)

Figure 4



S101
S201
S102
S111
S112
S103
Fill i/p buffer #1
Fill i/p buffer #2
Fill i/p buffer #3
Fill i/p buffer #4
Fill i/p buffer #1
"lead-in"
...1
Process i/p buffer 1 to o/p buffer 1 at rate f_s/M
...1
Run o/p #1
Run o/p #3
Run o/p #3
Run o/p #4
Run o/p #4
Run o/p #1
time

Figure 5

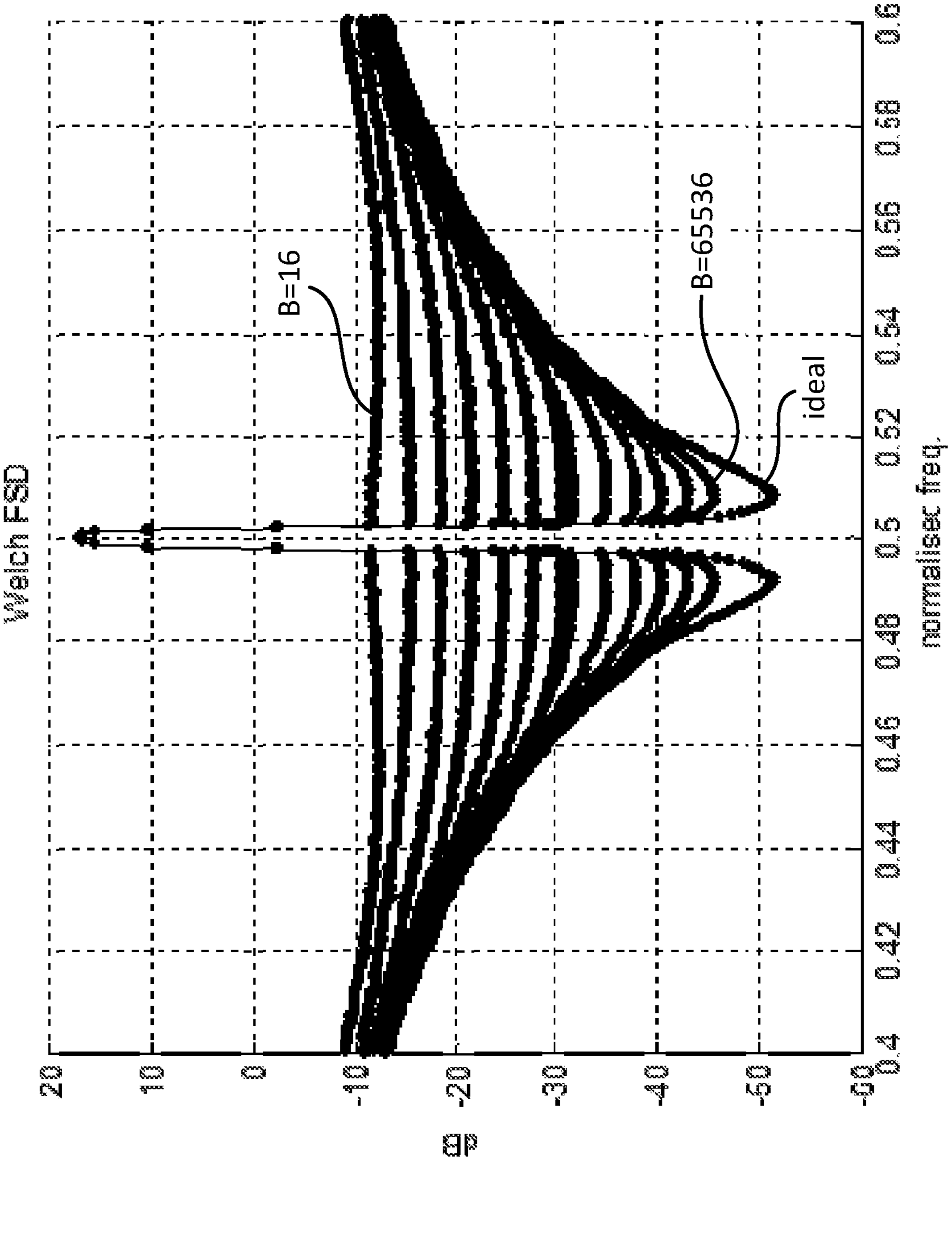


Figure 6

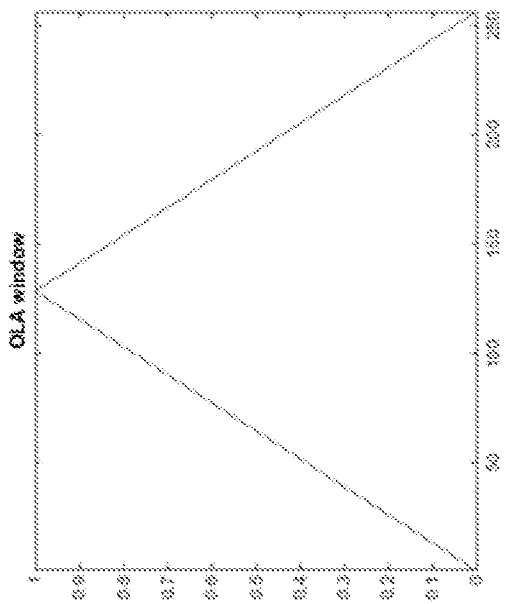


Figure 7a

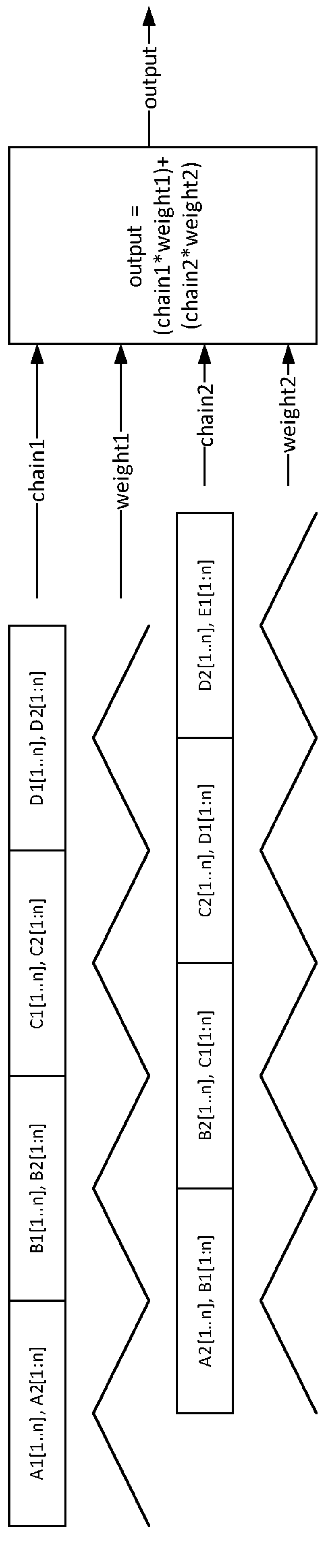


Figure 7b

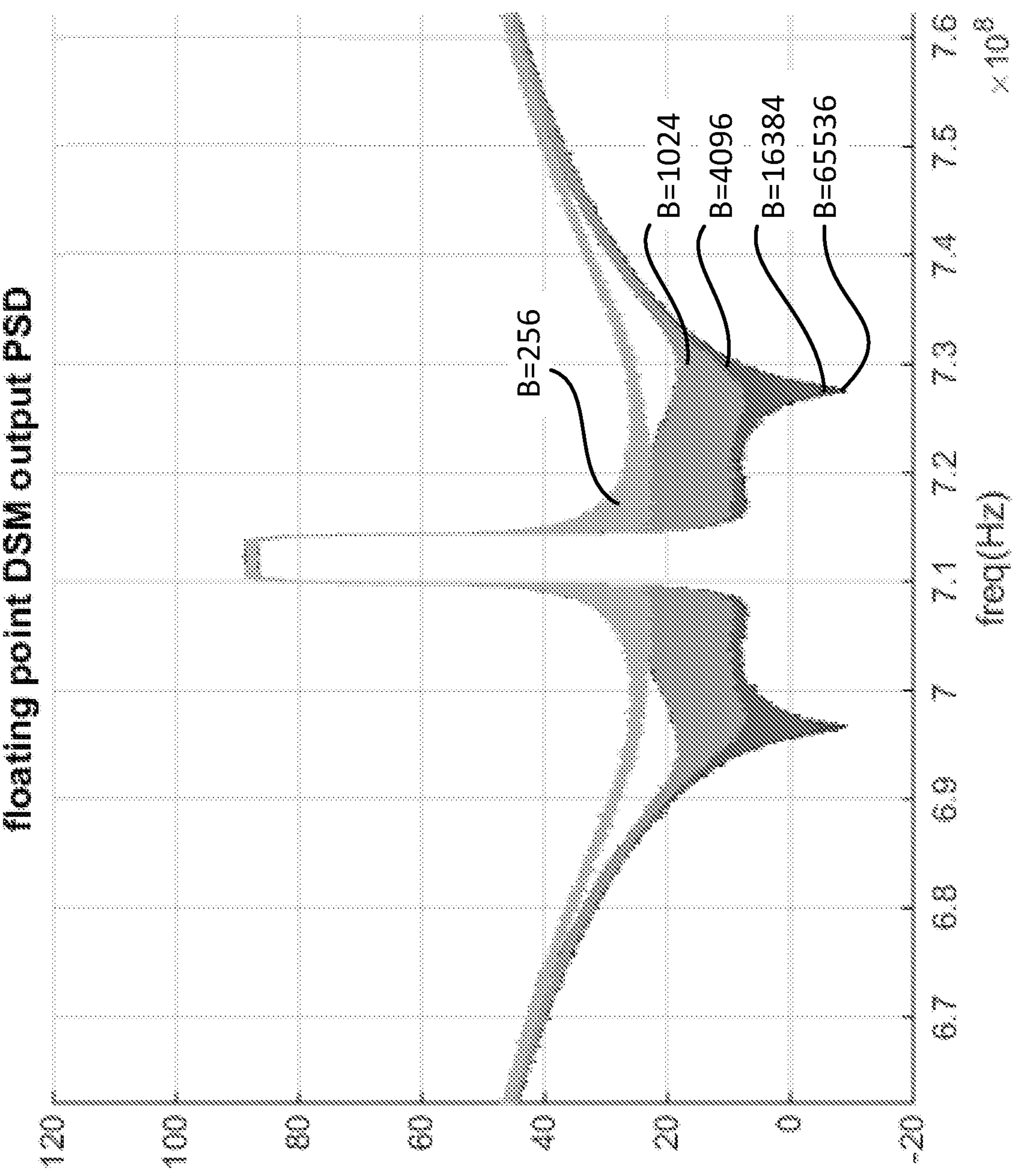

floating point DSM output PSD
gain(dB)
120
100
80
60
40
20
0
-20
6.7
6.8
6.9
7
7.1
7.2
7.3
7.4
7.5
7.6
x 10^8
freq(Hz)
B=256
B=1024
B=4096
B=16384
B=65536

Figure 8

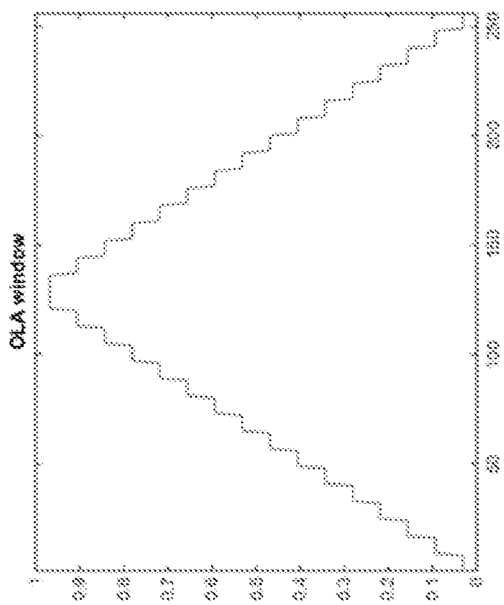


Figure 9a

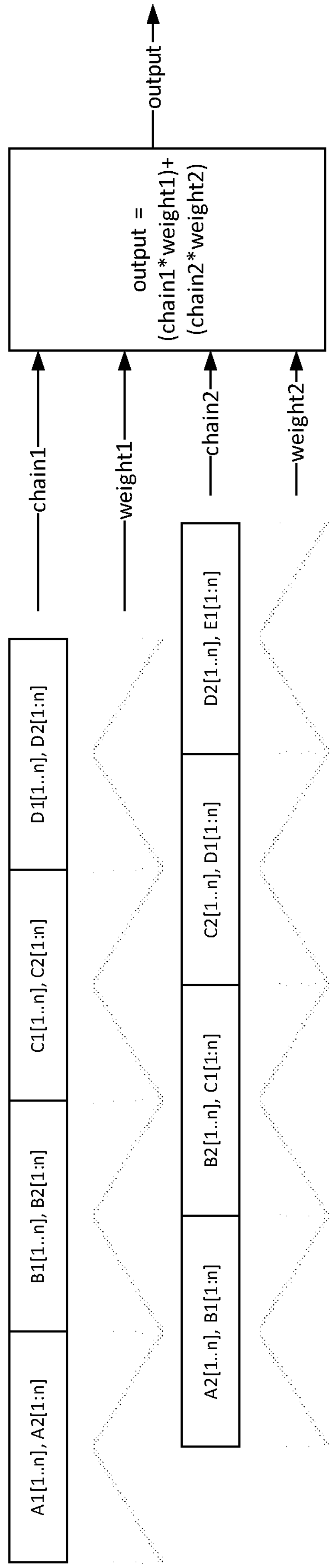


Figure 9b

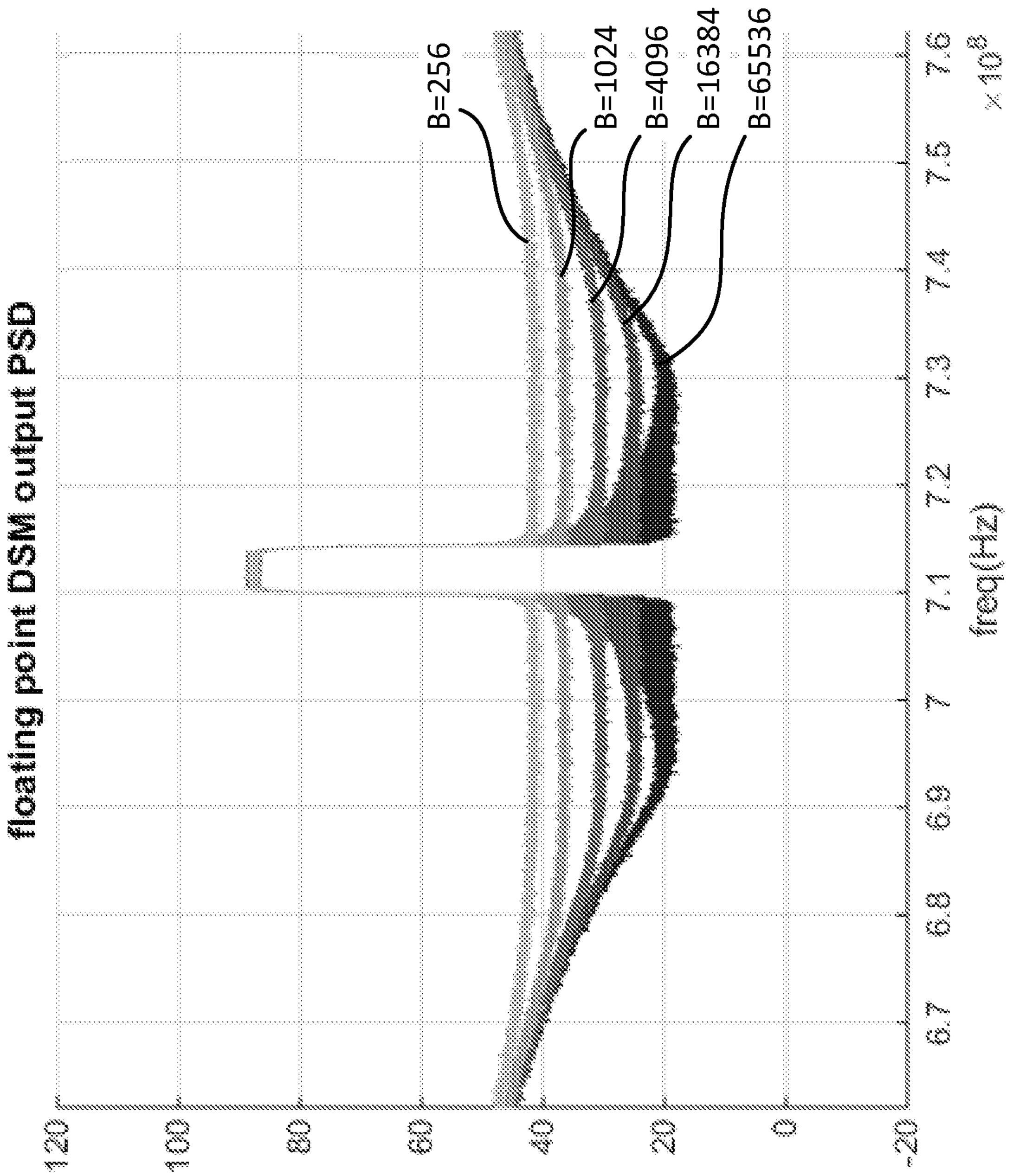

floating point DSM output PSD
gain(dB)
120
100
80
60
40
20
0
-20
freq(Hz)
6.7
6.8
6.9
7
7.1
7.2
7.3
7.4
7.5
7.6
$\times 10^8$
B=256
B=1024
B=4096
B=16384
B=65536

Figure 10

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2015/053126

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F3/217 H03M3/02
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 487 111 A1 (NORTHROP GRUMMAN CORP [US]) 15 December 2004 (2004-12-15)	1-7, 10-16, 31-33
Y	paragraphs [0025], [0026], [0029] -	28-30
A	[0031], [0035], [0036], [0048], [0069], [0077]; figures 2,3,8 -----	8,9
Y	WO 2008/114236 A2 (NAT UNIV IRELAND MAYNOOTH [IE]; FARRELL RONAN [IE]; RALPH STEPHEN [IE]) 25 September 2008 (2008-09-25) page 13, lines 4-14; figure 20 -----	28-30

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 January 2016	12/04/2016

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Zakharian, Andre

2

International application No.
PCT/GB2015/053126

INTERNATIONAL SEARCH REPORT

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. [ ] Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. [ ] Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. [ ] Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. [ ] As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. [ ] As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. [ ] As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. [X] No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-16, 28-33

Remark on Protest

- [ ] The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- [ ] The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- [ ] No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/GB2015/053126

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 1487111 A1	15-12-2004	EP 1487111 A1	15-12-2004
		JP 4065227 B2	19-03-2008
		JP 2005006273 A	06-01-2005
		US 2004252038 A1	16-12-2004
WO 2008114236 A2	25-09-2008	EP 2135356 A2	23-12-2009
		IE 20080206 A1	29-10-2008
		US 2010104043 A1	29-04-2010
		WO 2008114236 A2	25-09-2008

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-16, 28-33

   reducing transients from switching between output blocks from one branch to another in the SDM according to claim 1

   ---

2. claims: 17, 18

   improve stability of the SDM according to claim 1.

   ---

3. claims: 19-27

   reducing the noise flour of a time-interleaved SDM according to claim 1 by weighting outputs from at least two such SDMs

   ---