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(54) ELECTRONIC WATCH OR CLOCK

(71) We, BULOVA WATCH COMPANY, INC., a corporation organised and existing under the laws of the State of New York, United States of America, of Bulova Park, Flushing, New York 11370, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electronic watches and clocks. It is particularly concerned with such time-pieces in which an analog seconds hand display, or a digital seconds display, is driven by a pulse operated stepping motor, the time-piece having an accurate frequency standard and a frequency divider for dividing the frequency of the pulses derived from this frequency standard and transmitting the divided pulses to drive the motor. It has been proposed that a device operable by the user of the time-piece is provided for effecting fast correction of relatively small deviations of the seconds display, this device comprising reference counter fed by the frequency divider which is resettable by actuattion of the device, a synchronous counter synchronously driven with the time display through logic cicuitry by the frequency divider, and comparator circuitry coupled to both counters for comparing the state of the synchronous counter with that of the reference counter and which, in case of a difference detected upon actuation of the device, controls the number of pulses flowing per unit of time through the logic circuitry to the synchronous counter and to drive the stepping motor, whereby the motor is driven to correct the displayed time.

A horological instrument as just discussed is described in Swiss Patent Specification No. 556.055 (British Specification No. 1,450,461). The aim there is to create a watch or clock with seconds hand in which it is not necessary, in case of small deviations from correct time, first to stop the seconds hand at twelve o'clock and then wait for a time signal (time signal by radio, etc) for restarting it. The intention is to simplify time setting of the time-piece by providing a particular button or similar organ which can be depressed at the moment of an on-the-whole-minute time signal to establish automatic synchronisation of the time display with the time signal, this being the sole action that has to be taken to correct the time-piece. In principle this is possible because the comparator circuitry, after a resetting of the reference counter (user depresses button), by adding pulses to the synchronous counter or by inhibiting transmission of pulses, corrects the state of the synchronous counter and therefore simultaneously the state of the time display synchronized with the synchronous counter. The system proposed is suitable for correcting relatively small deviations of not more than plus or minus 30 seconds. Such a magnitude of correction is sufficient for modern electronic watches, particularly the quartz crystal watches, having a monthly accuracy remaining within these tolerances. The main advantage of this fast correction device is that a correction of the time display e.g. once a week or once a month can be accomplished merely by operating the correction pushbutton and without paying any special attention to the watch, or for example, manually correcting the display of the hands.

Unfortunately, in practice setting a watch as so far described can lead to considerable inaccuracies. For instance when setting the hands and pushing the crown, start of the display is inaccurate by one second since the next second pulse of the last frequency divider stage has to be waited for. Such inaccuracies are unacceptable for a crystal quartz watch or any other highly accurate watch.

According to the present invention there is provided an electronic watch or clock having a seconds display driven by a pulse operated stepping motor and including an accurate frequency standard, a frequency divider for dividing the frequency of the pulses derived from the frequency standard, time setting means for setting the watch or clock, and correction means operable by the user of the watch or clock for fast correction of relatively small deviations of the seconds display; said correction means comprising a resettable reference counter sup-

plied by output pulses of the frequency divider, a synchronous counter synchronously driven with the seconds display through decoding logic circuitry by the output pulses derived from the frequency divider, and comparator circuitry coupled to both counters for comparing the state of the synchronous counter with that of the reference counter for controlling, upon actuation of the correction means and in the event of a detected difference in these states, the number of pulses flowing per unit of time through the logic circuitry to the synchronous counter and to the seconds display means in order to correct the displayed time; correction contact means of said correction means and setting contact means of said setting means being connected through reset lines to several of the final stages of the frequency divider, and inputs of said decoder logic circuitry being connected in such a way to the outputs of resettable stages of the frequency divider that the two counters are only advanced during a pulse transfer period not exceeding the last quarter of the longest output pulse period of the frequency divider; inhibition means being provided actuable to prevent resetting of the frequency divider during said pulse transfer period.

In a watch or clock as just defined, because of the possibility or resetting the last stages of the frequency divider, disadvantages such as discussed above can be avoided. However, automatic rest of the frequency divider is not, alone sufficient to ensure accurate fast correction since, after starting the watch following setting, it can happen, depending on the phase position of the frequency divider at the moment the reset pulse is effective, that false pulses occur which can destroy for instance the synchronism between the two counters or the synchronism between the synchronous counter and the display. In the present watch or clock these difficulties are elminated by the provision of the pulse transfer period determined by the decoding logic circuitry, as will be made clear hereinafter.

For a better understanding of the invention and to show how the same may be put into effect, reference will now be made, by way of example, to the accompanying drawings in which:—

Figure 1 is a block circuit diagram of the main parts of an electronic watch, and

Figure 2 is a pulse diagram illustrating operation of the watch.

In the form illustrated the watch is an analog watch the hands of which are driven by means of a small stepping motor. This motor, in normal running of the watch, drives the seconds hand by one step a second. The other hands are driven in a conventional way by the seconds hand arbor through gearing not shown.

Referring to Figure 1, a quartz crystal 1 of 32 768 Hz used as frequency standard is connected to oscillator circuitry 2. The pulses derived from this circuitry flow through a NAND gate 101 and fixed programmed contact connections 3 and 4 to a resettable frequency divider which consists of sections 5, 6, 7 and 8. The section 5 comprises three binary dividing stages and operates in a dynamic mode. It has, therefore, in contrast to conventional dividers an extremely low current consumption. The binary dividers of the divider sections 6, 7 and 8 are static CMOS-dividers. All this circuitry is integrated on a single MOS chip. It is advantageous to integrate all the circuitry of the watch including the logic circuitry and the driver stages on the same chip (large scale integration). Between the dynamic divider section and the static divider sections there is an amplifying NAND gate 102 with a second input connected to a reset line A, ensuring thereby an error-free transmission of the pulses counted by section 5 and a dependable resetting of the first stage of section 6. A NAND gate 103 between the sections 7 and 8 has a similar function. NOR gates 104 and 105 are connected to the outputs of the final flip-flops stages of the divider section 8, an output to the NOR gate 104 being 2 Hz and an output to the NOR gate being 1 Hz. An additional NOR gate 106 is connected to the output of the NOR gate 105 and through an inverter 107 to a reset line B.

The three NOR gates 104, 105 and 106 have a quite particular function; they form together decoding logic circuitry by means of which an interval is defined near the end of each 1 second period, during which intervals control pulses from the frequency divider are transmitted further through the circuitry as a whole. To this end, the logic circuitry is connected in such a way to the outputs of the frequency divider that the transmission of control signals (constituted by pulse edges) from the frequency divider to two counters 10 and 12 (see below) can only be effected during a pulse transfer period not exceeding the last quarter (in the embodiment described, the last eighth) of the longest output pulse period of the frequency divider.

It is to be noted that the control signals can be derived from pulses which are not relatively long pulses of predetermined time duration, but are short pulses of uncritical duration, since their aim is merely to change the state of flip-flops and therefore only the exact location of the edges, which can be positive or negative and which must be situated within the above-mentioned intervals, is important.

The outputs of the NOR gates 106 and 104 are applied to a reference counter 10 and

to a synchronous counter 12 respectively. The output of the NOR gate 104 is also connected to a flip-flop 9. The counters 10 and 12 divide by 30 the frequency they receive at their inputs. Additional counter stages 11 and 13 provide an additional division to 60. The divider stages of the counters 10 and 12 are connected to one input of an EXCLUSIVE OR gate 108. An additional input of this gate is connected to the output of an EXCLUSIVE OR gate 109, the inputs of which are connected to the outputs of the divider stages 11 and 13.

Logic circuitry comprising a group of NOR gates 110, 111 and 112 constitutes a flip-flop which triggers a positive motor pulse in one state, while, changing to the other state it finishes the motor pulse. Further logic circuitry consisting of a group of flip-flops 113, 114 and 115 has the same function with the difference that it produces negative motor pulses. These positive and negative motor pulses drive a bipolar stepping motor. The drive coil of the motor is designated by 20. It is fed in the conventional way by driver stages 17 and 18.

The watch has furthermore programmable decoder circuitry equipped with a NOR gate 118 for defining exactly the length of the motor drive pulses. All inputs of gate 118 are connected to the corresponding stage outputs of the frequency divider section 7. The exact connection scheme depends on the desired position of the pulse edge which rests through a flip-flop 119 the motor pulse flip-flops 110-112 and 113-115. The programming of this pulse length decoding circuitry depends on the characteristics of the stepping motor used. It can be established by a suitable selection, during manufacture of the chip, of the last metal mask which determines the connections between the frequency divider stage outputs and gate 118.

An analog adaptation to the given conditions is used for activating the stages of the dynamic frequency divider section. In fact, the circuit diagram shows that the dynamic divider comprises, in addition to the active section 5, also passive sections 30, 31, 32 and 33. These can be activated if necessary by using corresponding metal masks during the manufacturing of the integrated circuit, so that an otherwise identical chip can be used for watches with frequency standards of other frequencies. Instead of the connections 3 and 4 there would be, for example, connections between gate 101 and section 30. and between sections 30, 31, 32 and 5, when using a quartz crystal of 1 048 576 Hz frequency.

In use, fast correction of the watch is effected by pressing a pushbutton set in the watch case. This button can be operated with a fingernail, a ball point pen or anything similar. It is mechanically coupled to a contact 21 which will then be pushed in the direction of arrow D to be set temporarily to ground from its normal setting to positive. Contact 21 leads to an input of a NOR gate 121 and to an input of a flip-flop 122, one additional input of which is connected to the 32 Hz output of the divider section 7. The outputs of the NOR gate 121 and the flip-flops 122 are connected to the inputs of NOR 123. This gate 123 feeds the reset line B. One additional rest line C leads from the output of NOR gate 121 to the synchronous counter 12.

Also provided is a contact 22 switchable from ground to positive by pulling out the crown in the direction of arrow K, the switch arm of this contact being connected to an input of a NAND gate 125. The output of this logic circuitry leads to the reset line A as already mentioned. As will be made clear hereinafter, the frequency divider is reset, when setting the hands, so that after a restart the seconds hand performs its first step exactly after one second.

The circuit described operates as follows:

The quartz crystal 1 produces in conjunction with the oscillator circuitry 2 an essentially sinusoidal alternating voltage of 32 768 Hz. Gate 101 is used for the purpose of pulse shaping and the rectangular pulses formed thereby are led to the dynamic mode divider 5 and scaled down by frequency division in this divider section and section 6, 7 and 8 to a frequency of 2 Hz at one input to the gate 104, and to 1 Hz at one input to the gate 105. The decoding circuitry consisting of the gates 104, 105 and 106, opens after 7/8 of a second the transmission path to the reference counter 10 which is switched by one step each second by the 1 Hz supply to the gate 105. The comparator circuitry 14 is triggered by each 1 Hz pulse to open the gate 104 through the gate 108 Consequently the synchronous counter 12 advances by one unit for each 1 Hz pulse and there is transmitted simultaneously a signal to the flip-flop 9 for triggering the motor control pulse. Because of the advance of the synchronous counter 12 as just described, the comparator circuitry detects that there is coincidence between counters 10 and 12 and inhibits the transmission of the next pulse of the 2 Hz frequency supply to the gate 104. Thus every other pulse of the 2 Hz supply to the gate 104 is suppressed to give effectively 1 Hz output at the gate 104. In other words there is normally 1 Hz at the outputs of each of the gates 104, 105 and 106.

After having changed its state, flip-flop 9 sets one of the motor pulse flip-flop groups 110-112 or 113-115 to the motor coil in the positive or negative sense.

The leading edge of each pulse stepping

the motor is located within the last eighth of the 1 Hz pulse derived from the counter section 8. The accuracy of the time positioning of the leading edges of the turn-off control pulses which define the motor drive pulses is very important. These pulses for resetting flip-flop groups 110-112 and 113-115 are derived from the section 7 of the divider. The input frequency of this section is 1024 Hz which gives an accordingly high resolution rate for the positioning of the reset pulse leading edges. The connections between divider section 7 and gate 118 can be chosen in such a way that the total motor pulse duration is e.g. 4,883 ms (interval between the setting and resetting of the motor pulse flip-flop groups). The motor drive coil 20 receives short negative or positive drive pulses. The driver stages 17 and 18 short circuit the coil 20 between the drive pulses. This improves the dynamic behaviour of the motor.

It will now be supposed that the watch is slow by a few seconds (between 0 and 29 seconds). At an on-the-whole-minute time signal obtained, for example, from the radio, the user of the watch operates the switching contact 21 by pushing the pushbutton in the direction of arrow D. The flip-flop 122 triggers a short reset pulse as soon as the next 32 Hz pulse arrives. This reset pulse flows to divider section 8 and to reference counter 10 (through gate 123 and line B) and clears divider section 8 and reference counter 10. Immediately after this resetting operation divider section 8 and reference counter 10 resume their normal functions. Therefore, a 2 Hz pulse appears at the 2 Hz output of divider section after somewhat less than half a second. The comparator circuitry now determines that the counting of counter 10 is "higher" (further advanced) than that of counter 12. For as long as counter 10 is in advance of counter 12 the comparator circuitry 14 no longer inhibits gate 104 and accordingly, by means of gates 108 and 104, the reference counter 12 and the motor receive two pulses per second until the comparator circuitry 14 determines again coincidence between the counts of the two counters 10 and 12. Thus the watch runs at twice its normal speed until correct time is reached.

The provision of the 32 Hz output is necessary since it is important that when effecting fast setting no noticeable time delays occur. This danger can be avoided if after resetting the reference counter and the final stages of the frequency divider a pulse of sufficiently high frequency derived from the frequency divider is used for enabling again the reset stages. Usually it is sufficient to use a 32 Hz pulse for this purpose. The present circuit makes use of flip-flop circuitry resetting the reference counter and several frequency divider stages, the flip-flop circuitry being connected on the other hand to the 32Hz output of the frequency divider. When the contact is actuated, this flip-flop circuitry is brought to a determined condition in which the frequency divider and reference counter are reset. Afterwards, the state of this circuitry is changed by the next 32 Hz pulse, whereupon the reset stages restart counting and therefore define the beginning of a new output pulse.

If the watch is fast when the pushbutton is depressed, the comparator circuitry determines an excess of pulse units counted by the synchronous counter 12 after the resetting and the reset of the divider section 8 and reference counter 10. As a consequence gate 104 is inhibited until the two counters 10 and 12 are again synchronous. During this time no motor drive pulses reach flip-flop 9. Thus in this case the watch stops until the time it is showing is the correct time.

As explained above, the resetting function does not take place exactly at the moment contact 21 is operated, but as soon as the next 32 Hz pulse is received. Since the next motor drive control pulse will be created after the resetting of the divider section 8 and the reference counter 10, there is thus provided inhibition means preventing the resetting to be performed during the transmission of any stepping motor control pulse.

It is now supposed that the user of the watch wants to stop the time-piece for setting the hour and minute hands, and then restart it. This occurs through the switching of contact 22 by pulling the crown into its outermost position (arrow K). The reset line A changes potential. As a result, the sections 6, 7 and 8 of the frequency divider will be reset. However, this resetting cannot be carried out during the pulse transfer interval of 1/8 of a second defined by the decoding logic circuitry 104-106 since this is prevented by the inhibition means that is constituted by NOR gate 127, flip-flop 128 and NAND gate 125. Without this security measure switching of the contact 22 at the moment of the transmission of a motor drive pulse could activate under certain circumstances the synchronous counter 12, or alternatively, the motor drive pulse could be shortened to such an extent that the motor would not be driven. This would consequently lead to a loss of synchronism between counter 12 and the seconds hand. Pushing the crown results in resetting the contact 22. The divider sections 6, 7 and 8 are again activated starting therefore the cycle for the formation of the next 1 Hz output pulse.

A particular situation occurs when the watch is set into service for the first time or when the battery is changed. The frequency divider as well as the two counters of the

correction circuitry must then be set to zero. In order to avoid any unintentional execution of this operation, in the example described this simultaneous resetting can only take place if on the one hand the crown is pulled to the position of setting the hands and on the other hand the push button of the fast correction device is pushed. In other words, switching contracts 22 and 21 must be operated simultaneously when pulling the crown, attention must be paid to the seconds hand which has to be on "0" (12 o'clock). This is essential since otherwise there would be no synchronism between the seconds hand and synchronous counter 12 after restarting the watch. Depending on whether or not the crown is pushed during zero crossing at a reference time, additional actuation of the fast correction means is not required or actuation must thereafter be effected with reference to a time signal.

The application of the invention is not limited to a watch or a clock with an analog hand display but is equally applicable to a watch with digital display. A minute and hour counter ought then to be added to the synchronous counter 12, 13. Furthermore, adequate logic circuitry and, if necessary multiplexing means would have to be inserted between the counters and the means displaying the digits.

The pulse diagrams of Figure 2 show how the motor drive pulses are positioned and precisely defined with regard to their length. A triggering pulse is shown in diagram 1 and also a pulse the trailing edge of which triggers the start of a motor feeding pulse. The triggering pulse cannot start before the end of the non-inhibited time interval. As already described, the length of the inhibition interval is determined by combining symmetrical pulses of different frequencies from divider section 8 in gates 104 and 105 of the decoding logic circuitry. In the example the duration of the inhibition interval is 1/8 of a second plus the duration of the motor pulse.

The location of the turn-off control pulses (motor reset pulses) is shown in diagram II. It can be seen that the next turn-off pulse from flip-flop 119 occuring after the trailing edge of a trigger pulse terminates a motor pulse and simultaneously an inhibit interval. This relation may be seen in diagram III. Furthermore, the alternating polarity of the feeding pulses applied to the motor coil is shown. The length of these feeding pulses is extended in the diagram in order to improve comprehension.

Although it is advantageous to choose the connections between the final stages of the frequency divider and the inputs of the pulse transfer period decoding logic circuitry in such a way that the deblocking interval is 7/8 and the inhibit interval is 1/8 of a second these periods can be different but the logic decoding circuitry should inhibit the transfer of pulses to the two counters and to the display means during a minimum of 3/4 of the duration of a full pulse transfer period (by which is meant that section of a complete period during which the transfer of pulses or pulse edges is possible whereas the reset of the frequency divider stages is inhibited). During this time interval it is therefore possible to perform rest actions without the possible trouble of generating false pulses. Furthermore, the inhibiting means block the rest function of the frequency divider during the pulse transfer interval. It is therefore possible to talk of a subdivision of the full period into an inhibit interval (pulse transfer interval) and a deblocking interval. The deblocking interval. during which the zero resetting of the frequency counter is not inhibited, should be at least three times as long as the pulse transfer or inhibition interval, so that there remains as much time as possible for carrying out any kind of manipulations.

WHAT WE CLAIM IS:—

1. An electronic watch or clock having a second display driven by a pulse operated stepping motor and including an accurate frequency standard, a frequency divider for dividing the frequency of the pulses derived from the frequency standard, time setting means for setting the watch or clock, and correction means operable by the user of the watch or clock for fast correction of relatively small deviations of the seconds display; said correction means comprising a resettable reference counter supplied by output pulses of the frequency divider, a synchronous counter synchronously driven with the seconds display through decoding logic circuitry by the output pulses derived from the frequency divider, and comparator circuitry coupled to both counters for comparing the state of the synchronous counter with that of the reference counter for controlling, upon actuation of the correction means and in the event of a detected difference in these states, the number of pulses flowing per unit of time through the logic circuitry to the synchronous counter and to the seconds display means in order to correct the displayed time; correction contact means of said correction means and setting contact means of said setting means being connected through reset lines to several of the final stages of the frequency divider, and inputs of said decoder logic circuitry being connected in such a way to the outputs of resettable stages of the frequency divider that the two counters are only advanced during a pulse transfer period not exceeding the last quarter of the longest output pulse period of the frequency divider; inhibition means being provided actuable to

prevent resetting of the frequency divider during said pulse transfer period.

2. A watch or clock as claimed in claim 1, wherein said decoding logic circuitry is arranged to ensure that the transmission of pulses from the frequency divider to the two counters can only be effected during the last eighth of the longest output pulse period of the frequency divider.

3. A watch or clock as claimed in claim 1 or 2, wherein pulses with a frequency of 1 Hz are derived from the frequency divider for feeding the reference counter and pulses with a frequency of 1 Hz and 2 Hz are so derived for feeding the synchronous counter; the synchronous counter recieving the 1 Hz pulses in normal operation of the watch, the 2 Hz pulses upon actuation of the correction means and subsequent detection of a count in the synchronous counter lower than the count in the reference counter, and no pulses upon actuation of the correction means and subsequent detection of a count in the synchronous counter higher than the count in the reference counter.

4. A watch or clock as claimed in claim 1, 2 or 3 and further comprising inhibition means that prevents resetting of the frequency divider during the transmission of any stepping motor control pulse to the pulse operated stepping motor.

5. A watch or clock as claimed in claim 4, wherein the stepping motor is fed by flip-flops set by pulses derived from the frequency divider and reset by reset pulses which are derived from earlier stages of the frequency divider.

6. A watch or clock as claimed in claim 5 and comprising pulse length decoding circuitry for producing exactly positioned pulse edges for resetting said flip-flops, this pulse length decoding circuitry being connected to the outputs of several stages of the frequency divider.

7. A watch or clock as claimed in claim 6, wherein the frequency divider comprises a final section which can be reset by said correction contact means of said correction means and by said setting contact means of said time setting means, the divider stages of this final section being connected to the pulse transfer period decoding logic circuitry and including a preceding section resettable exclusively by actuation of said setting contact means, the stages of said preceding section being connected to the pulse length decoding circuitry.

8. A watch or clock as claimed in claim 7, wherein said final section of the frequency divider comprises five binary dividing stages.

9. A watch or clock as claimed in claim 7 or 8, wherein the section of the frequency divider resettable by said correction contact means has an input frequency of 32 Hz.

10. A watch or clock as claimed in claim 7, 8 or 9 wherein said correction contact means is connected to a terminal of a flip-flop for resetting the reference counter and several frequency divider stages, this flip-flop being connected for clearing said final section of the frequency divider and said reference counter.

11. A watch or clock as claimed in any one of the preceding claims, wherein said correction contact means includes a push-button set in the watch case and actuable by a pointed object.

12. A watch or clock as claimed in any one of the preceding claims, wherein said correction contact means and said setting contact means are connected through associated logic circuitry to the reference counter and synchronous counter such that only by actuating both these contact means simultaneously can both counters be reset.

13. A watch or clock as claimed in any one of the preceding claims, wherein said time setting means is a crown which serves to actuate said setting contact means when drawn to its outermost position.

14. A watch or clock as claimed in any one of the preceding claims wherein the frequency divider comprises at least two resettable, multistage sections and one non-resettable dynamic mode section preceding these two sections.

15. A watch or clock as claimed in claim 14, wherein the dynamic mode section of the frequency divider comprises several stages, on a single MOS chip, and wherein these stages are established during manufacture of the chip by a suitable choice of the last manufacturing mask determining the connections between the stages in accordance with the frequency of the quartz crystal used as the time standard.

16. A watch or clock according to claim 15, wherein the pulse length decoding circuitry is established on said chip by a suitable choice of the last manufacturing mask establishing thereby the appropriate connections between the frequency divider outputs and the logic decoding circuitry depending on the desired length of the pulses actuating the display.

17. An electronic watch or clock, substantially as hereinbefore described with reference to the accompanying drawings.

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1575580 COMPLETE SPECIFICATION

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Sheet 1

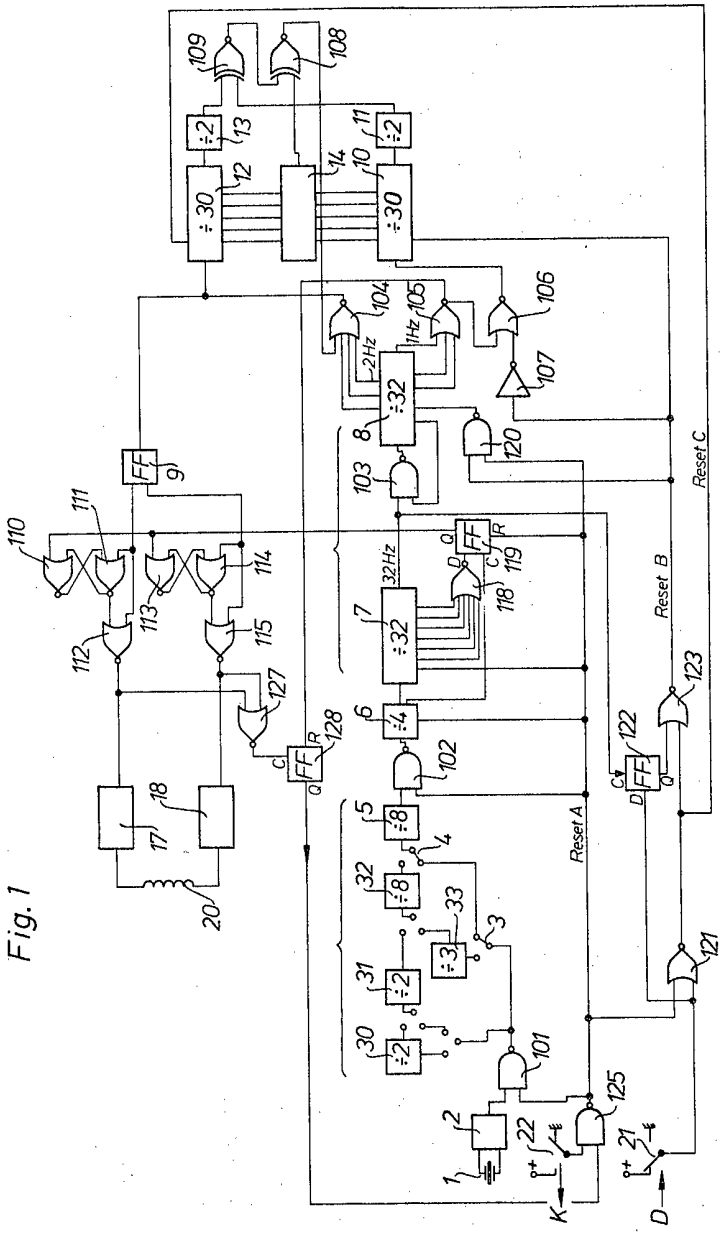

Fig. 1

1575580 COMPLETE SPECIFICATION
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Sheet 2

Fig. 2

