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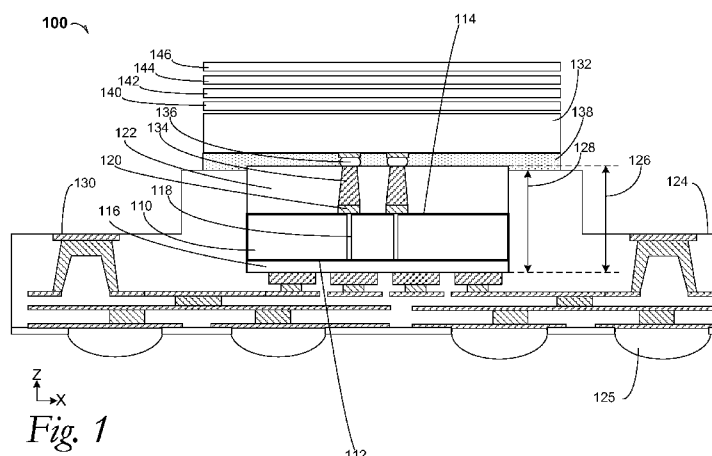
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(54) **Title:** CONTROLLED SOLDER-ON-DIE INTEGRATIONS ON PACKAGES AND METHODS OF ASSEMBLING SAME



(57) **Abstract:** A process of bumping a die backside includes opening a recess in a die backside film (DBF) to expose a through-silicon via (TSV) contact in a die, followed by filling the recess with a conductive material that contacts the TSV contact. Added solder is coupled to the conductive material at a level of the DBF. A subsequent die is coupled to the first die at the added solder to form an electrical coupling consisting of the TSV contact, the conductive material, and the added solder, an electrical bump coupled to the subsequent die. Apparatus and computer systems are assembled using the process.

CONTROLLED SOLDER-ON-DIE INTEGRATIONS ON PACKAGES AND METHODS OF ASSEMBLING SAME

TECHNICAL FIELD

Disclosed embodiments relate to die backside films that are patterned to expose
5 through-silicon via contacts and methods of coupling a stacked die to the via contacts.

BRIEF DESCRIPTION OF THE DRAWINGS

In order to understand the manner in which embodiments are obtained, a more
particular description of various embodiments briefly described above will be rendered by
reference to the appended drawings. These drawings depict embodiments that are not
10 necessarily drawn to scale and are not to be considered to be limiting in scope. Some
embodiments will be described and explained with additional specificity and detail
through the use of the accompanying drawings in which:

FIG. 1 is a cross-section elevation of an apparatus that includes an embedded die
with a controlled-deposit solder coupling according to an example embodiment;

15 FIG. 2a is a cross-section elevation of an embedded die during formation of a
controlled-deposit solder coupling according to an example embodiment;

FIG. 2b is a cross-section elevation of the embedded die depicted in FIG. 2a during
further processing according to an example embodiment;

20 FIG. 2c is a cross-section elevation of the embedded die depicted in FIG. 2b during
further processing according to an example embodiment;

FIG. 2d is a cross-section elevation of the embedded die depicted in FIG. 2b during
further processing according to an example embodiment;

FIG. 2e is a cross-section elevation of the embedded die depicted in FIG. 2d during
further processing according to an example embodiment;

25 FIG. 3b is a cross-section elevation of the embedded die depicted in FIG. 2a during
further processing according to an example embodiment;

FIG. 3c is a cross-section elevation of the embedded die depicted in FIG. 3b during
further processing according to an example embodiment;

30 FIG. 3d is a cross-section elevation of the embedded die depicted in FIG. 3c during
further processing according to an example embodiment;

FIG. 4b is a cross-section elevation of the embedded die depicted in FIG. 2a during
further processing according to an example embodiment;

FIG. 4c is a cross-section elevation of the embedded die depicted in FIG. 4b during further processing according to an example embodiment;

FIG. 4d is a cross-section elevation of the embedded die depicted in FIG. 4c during further processing according to an example embodiment;

5 FIG. 5 is a cross-section elevation of an apparatus that includes an embedded die with a controlled-deposit solder coupling according to an example embodiment;

FIG. 6d is a cross-section elevation of an embedded die during formation of a controlled-deposit solder coupling that may follow previously disclosed processing after a controlled-deposit solder processing has been accomplished according to an example
10 embodiment;

FIG. 6e is a cross-section elevation of the embedded die depicted in FIG. 6d during further processing according to an example embodiment.

FIG. 7 is a cross-section elevation of an apparatus that includes an embedded die with a controlled-deposit solder coupling according to an example embodiment;

15 FIG. 7 is a cross-section elevation of an apparatus that includes an embedded die with a controlled-deposit solder coupling according to an example embodiment;

FIG. 8 is a cross-section elevation of an apparatus that includes an embedded die with a controlled-deposit solder coupling according to an example embodiment;

FIGs. 9a and 9b illustrate a process flow for inserting conductive material into a
20 die-backside film recess according to an embodiment;

FIGs. 10a and 10b illustrate a process flow for inserting conductive material into a die-backside film recess according to an embodiment;

FIGs. 11a and 11b illustrate a process flow for inserting conductive material into a die-backside film recess according to an embodiment;

25 FIG. 12 is a computer reproduction of a photomicrograph according to an example embodiment;

FIG. 13 is a computer reproduction of a photomicrograph according to an example embodiment;

FIG. 14 is a computer reproduction of a photomicrograph according to an example
30 embodiment;

FIG. 15 is a computer reproduction of a photomicrograph according to an example embodiment;

FIG. 16 is a process and method flow diagram according to an example embodiment; and

FIG. 17 is a schematic of a computer system according to example embodiments.

DETAILED DESCRIPTION

Processes are disclosed for die backside films (DBFs) that are patterned in order to couple through-silicon vias (TSVs) to stacked devices.

5 Reference will now be made to the drawings wherein like structures may be provided with like suffix reference designations. In order to show the structures of various embodiments more clearly, the drawings included herein are diagrammatic representations of integrated circuit chips assembled with stacked-die TSV structures. Thus, the actual appearance of the fabricated chip substrates, alone or in chip packages, for example in a
10 photomicrograph, may appear different while still incorporating the claimed structures of the illustrated embodiments. Moreover, the drawings may only show the structures useful to understand the illustrated embodiments. Additional structures known in the art may not have been included to maintain the clarity of the drawings.

FIG. 1 is a cross-section elevation of an apparatus 100 that includes an embedded
15 die 110 with a controlled-deposit solder coupling 134 according to an example embodiment. The embedded die 110 includes an active surface 112 and a backside surface 114. A front-end (FE) metallization 116 is disposed on the active surface 112. A through-silicon via (TSV) 118 is disposed in the embedded die 110 and the TSV 118 contacts a TSV contact 120 on the backside surface 114.

20 Affixing the embedded die 110 includes using a die backside film (DBF) 122, which is sticky at useful processing temperatures. In an embodiment, the embedded die 110 is disposed in a coreless, bumpless build-up layer (BBUL-C) substrate 124 with land-side bumps 125. It can be seen that the DBF 122 attains a DBF height 126 above the FE metallization 116 and the BBUL-C substrate 124 also attains a BBUL-C height 128 above
25 the FE metallization 116. In an embodiment, the DBF height 126 is greater than the BBUL-C height 128, as illustrated. In an embodiment, the DBF height 126 is the same as the BBUL-C height 128. In an embodiment, the DBF height 126 is less than the BBUL-C height 128.

In an embodiment, a hybrid of some DBF 122 and some underfill 138 is formed.
30 For example, the DBF 122 may be partially removed and in combination with a complement of underfill 138, a useful warpage resistance may result from the hybrid. In an embodiment, some of the DBF 122 starts with the DBF height 126 being a first height, followed by a second height that is the result of a partially ashing out of the DBF 122. For example, the DBF 126 is ashed to result in a 5 micrometer (μm) thickness (Z-direction).

The 5 μm thickness is less than the BBUL-C height 128. Thereafter, a capillary underfilling (CUF) process is carried out. The resulting structure of a partially removed DBF and complementary underfill may be optimized for a given useful stiffness.

5 Additionally, DBF coefficient of thermal expansion (CTE) and underfill CTE can be engineered both intrinsically as well as be modulated in its dominance by its final thickness.

The BBUL-C substrate 124 is depicted with incidental internal conductive layers and vias along with the land-side bumps 125. In an embodiment, the BBUL-C substrate 124 is a package-on-package (POP) BBUL-C substrate 124. In this embodiment, the
10 BBUL-C substrate 124 has POP bond pads 130 that are provided for electrical communication to a POP package (not pictured).

Assembly of the embedded die 110 to a subsequent die 132 is accomplished by filling a conductive material 134 into a recess 123 (see, *e.g.*, recess 123 in FIG. 2b) that is disposed in the DBF 122, followed by mating the subsequent die 132 at an electrical bump
15 136. Thereafter, an underfill material 138 is flowed between the DBF 122 and the subsequent die 132. The conductive material 134 may also be referred to as a controlled-deposit solder coupling 134 according to an example embodiment.

It may now be seen that other dice may be similarly assembled as the subsequent die 132. For example, a second die 140 is depicted in compressed, simplified vertical (Z-
20 direction) scale and also simplified form (without illustrated controlled-deposit solder couplings). In an embodiment, the second die 140 is a TSV die that is mounted upon the subsequent die 132, where the subsequent die 132 also has a DBF that has been patterned according to any disclosed embodiment. Similarly, a third die 142 may be mounted on the second die 140, where the second die 140 is also a TSV die with a DBF that has been
25 patterned according to any disclosed embodiment. A fourth die 144 and a fifth die 146 is also depicted by way of non-limiting example embodiment. In an embodiment, the fourth die 144 is a TSV die that is coupled to the third die 142 with a disclosed controlled-deposit solder coupling and the fifth die 146 is a simple flip chip die.

Also, the second die 140 may be located below the BBUL-C height 128 such that
30 the first die 110, the subsequent die 132, and the second die 140 are all effectively embedded within the form factor of the BBUL-C substrate 124. It may now be understood that at least one die may be stacked above the subsequent die 132 but it would not be effectively embedded within the form factor of the BBUL-C substrate 124.

In an embodiment, the first die 110 is a logic die and the subsequent die 132 is a memory die. Location of the TSV 118 and patterning of the DBF 122 is done to interface a pin-out layout of the logic die 110 with a pin-out layout of the memory die 132. This may be called a logic-to-memory interface (LMI). In an embodiment, the first die 110 is a logic die and the subsequent die 132 is also a logic die. Location of the TSV 118 and patterning of the DBF 122 is done to interface a pin-out layout of the logic die 110 with pin-out layout of the subsequent logic die 132. This may be called a logic-to-logic interface (LLI).

In an embodiment, the first die 110 and the subsequent die 132 are logic dice with an LLI therebetween that uses a controlled-deposit solder coupling embodiment, and the second die 140 is a memory die with an LMI between the subsequent die 132 and the second die 140 that uses a controlled-deposit solder coupling embodiment. Location of the TSV 118 and patterning of the DBF 122 is done to interface pin-out layout of the logic die 110 with pin-out layout of the subsequent logic die 132, and a similar DBF on the subsequent die 132 is patterned to match interface pin-out layout of the subsequent logic die 132 with pin-out layout of the memory die 140.

It may now be appreciated that the stack of five dice 132, 140, 142, 144, and 146 is representative of LMI embodiments. It may now be appreciated that the stack of five dice 132, 140, 142, 144, and 146 is representative of LLI and LMI embodiments. Similarly, it is observed that location of the entire stack, or a portion thereof, may be effectively embedded within the form factor of the BBUL-C substrate 124 according to useful embodiments.

Stacking of the subsequent die 132 upon the embedded first die 110 may be done by compression joining according to an embodiment. Other methods may be used for creating a 3D stack that uses the controlled-deposit solder coupling embodiments. In any event, mechanical integrity and electronic contact integrity are increased by use of the controlled-deposit solder coupling embodiments. Additionally, overmolding of mold material may be eliminated where the integrity of the controlled-deposit solder coupling embodiments is relied upon such that only underfilling is necessary to create useful and reliable physical bonds and electronic contacts. Further, a lessened Z-height may be achieved by using thinned die and TSV technologies to create at least the embedded first die 110 and the subsequent die 132.

FIG. 2a is a cross-section elevation of an embedded die apparatus 201 during formation of a controlled-deposit solder coupling according to an example embodiment.

The apparatus 201 may be considered to be an embedded first die 110 disposed in a different embodiment of the BBUL-C 124 depicted in FIG. 1.

The embedded die 110 includes an active surface 112 and a backside surface 114. An FE metallization 116 is disposed on the active surface 112. A TSV 118 is disposed in the embedded die 110 and the TSV 118 contacts a TSV contact 120 on the backside surface 114.

A DBF 122 is shown extending above the BBUL-C substrate 124. It can be seen that the DBF 122 attains a DBF height 126 above the FE metallization 116 and the BBUL-C substrate 124 also attains a BBUL-C height 128 above the FE metallization 116. In an embodiment, the DBF height 126 is greater than the BBUL-C height 128, as illustrated. In an embodiment, the DBF height 126 is the same as the BBUL-C height 128. In an embodiment, the DBF height 126 is less than the BBUL-C height 128.

The BBUL-C substrate 124 is depicted with incidental internal conductive layers and vias along with the land-side bumps 125. In an embodiment, the BBUL-C substrate 124 is POP BBUL-C substrate 124. In this embodiment, the BBUL-C substrate 124 has POP bond pads 130 that are provided for electrical communication to a POP package (not pictured). Processing of the DBF 122 is carried out such as preparing it to open a recess therein that exposes the TSV contact 120.

FIG. 2b is a cross-section elevation of the embedded die depicted in FIG. 2a during further processing according to an example embodiment. The embedded die apparatus 202 has been processed to open a recess 123 that exposes the TSV contact 120. Consequently, the DBF 122 is an *in situ* mask for self-aligned placement of the conductive material 134 depicted in FIG. 1. In an embodiment, laser drilling through the DBF 122 is carried out such as by using a CO₂ laser drill. The shape of the recess 123 may have a conical form that is characteristic of a CO₂ laser drill process in an organic film that makes up the DBF 122. In an embodiment, a controlled ultraviolet (UV) process is carried out to form the recess 123.

FIG. 2c is a cross-section elevation of the embedded die depicted in FIG. 2b during further processing according to an example embodiment. The embedded die apparatus 203 has been processed by filling a solder-on-die material 134 into the recess 123 (FIG. 2b). The solder-on-die material 134 is conductive material that contacts the TSV contact 120. In an embodiment, the solder-on-die material 134 has a topology 148 that extends above the DBF height 126 such that an abundance of solder material is presented above the DBF height 126. The solder-on-die material 148 may be referred to as a dome-top

form factor 148 where some solder material extends above the solder-on-die material 148. The dome-top form factor is useful to present a smaller tip dome top of the solder-on-die material 134 such that less epoxy flux filler, if any, must be used. As such, the dome-top form factor 148 may also be referred to as forming added solder to the conductive material

5 in abundance at the DBF level 126. Consequently, “at a level” may be understood to be at the DBF level 126 of the DBF 122.

FIG. 2d is a cross-section elevation of the embedded die depicted in FIG. 2b during further processing according to an example embodiment. The embedded die apparatus 204 has been processed by filling a solder-on-die material 134 into the recess 123 (FIG.

10 2b). In an embodiment, the solder-on-die material 134 has been added to with discrete added solder 150 that has a topology that extends above the DBF height 126 such that an abundance of solder material is presented at a level of the DBF, particularly above the DBF height 126. The solder-on-die material 134 may be referred to as a dome-top form factor where some discrete added solder 150 extends above the solder-on-die material 134.

15 Formation of the conductive material that contacts the TSV contact may be done by any useful process.

FIGs. 9a and 9b illustrate a useful process embodiment 900 for forming the conductive material 934 that contacts the TSV contact 920 as well as the dome-top form factor 948, which is also known as the added solder 148 that contacts the conductive

20 material 948. A conductive material precursor 933 is being squeegeed into a recess 923 of a DBF 922. In FIG. 9b, the process has resulted in a controlled-deposit solder coupling 934 that may include a dome-top form factor 948, which may be formed based upon deposition techniques.

FIGs. 10a and 10b illustrate a useful process embodiment 1000 for forming the

25 conductive material 1034 that contacts the TSV contact as well as the dome-top form factor 1048, which is also known as the added solder 1048 that contacts the conductive material 1034. A conductive material precursor 1033 is being injected by jet action into a recess 1023 of a DBF 1022. In FIG. 10b, the process has resulted in a controlled-deposit solder coupling 1034 that may include a dome-top form factor 1048, which may be formed

30 based upon deposition techniques.

FIGs. 11a and 11b illustrate a useful process embodiment 1100 for forming the conductive material 1134 that contacts the TSV contact as well as the dome-top form factor 1150, which is also known as the discrete added solder 1150 that contacts the conductive material 1134. A conductive material precursor 1133 has been plated into the

recess. The conductive material precursor also plates onto the upper surfaces of the DBF 1122. In an embodiment, the TSV contact 1120 is used for plating as a cathode, whether plating is electroless or electrolytic. The dome-top form factor 1150 is depicted as a solder paste that is mingled with a fugitive organic carrier. Further processing such as
5 reflow may be done to convert the solder paste of the dome-top form factor 1150 into a substantially reflowed solder. In FIG. 11b, the process has resulted in a controlled-deposit solder coupling 1134 that may include a dome-top form factor 1150, which may be formed based upon deposition techniques such as jet action.

FIG. 2e is a cross-section elevation of the embedded die depicted in FIG. 2d during
10 further processing according to an example embodiment. The embedded die apparatus 205 has been processed by mating the subsequent die 132 to the discrete added solder 150 that is the dome-top form factor added to the conductive material 134. The subsequent die 132 also has an electrical bump 136. In combination with the added solder 150, the electrical bump 136 of the subsequent die 132 makes a useful contact between the
15 embedded die 110 and the subsequent die 132.

Assembly of the embedded die 110 to the subsequent die 132 has been accomplished by filling the conductive material 134 into the recess that is disposed in the DBF 122, followed by mating the subsequent die 132 at the electrical bump 136. Thereafter, an underfill material 138 is flowed between the DBF 122 and the subsequent
20 die 132 as seen in FIG. 1. In an embodiment, the underfilling process is carried out by CUF processing.

FIG. 3b is a cross-section elevation of the embedded die depicted in FIG. 2a during further processing according to an example embodiment. The embedded die apparatus 302 is processed with a soft mask 352 and a light-reactive DBF 322. Other structures may be
25 similar to those depicted in the series 2 FIGs. In an embodiment, the soft mask 352 has been spin-on processed and cured. In an embodiment, the soft mask 352 is a dry-film resist lamination.

FIG. 3c is a cross-section elevation of the embedded die depicted in FIG. 3b during further processing according to an example embodiment. The embedded die apparatus
30 303 has been processed by patterning opens in the soft mask 352 and by treating the light-reactive DBF 322 such that affected areas 353 have been formed above the TSV contacts 120.

FIG. 3d is a cross-section elevation of the embedded die depicted in FIG. 3c during further processing according to an example embodiment. The embedded die apparatus

304 has been processed by rinsing the affected areas 353 (FIG. 3c) such that the TSV contacts 120 are exposed in recesses 323. Processing may therefore continue by removal of the soft mask 322 and filling the recesses 323 according to any of the disclosed embodiments. Further processing may therefore include mating a subsequent die to the added solder form factor, followed by forming an underfill material between the DBF 322 and the subsequent die.

It may be appreciated that similar to the series 2 embodiments illustrated in FIGs. 2a – 2e, the DBF 322 may attain any disclosed DBF height above the FE metallization 116 in comparison to the BBUL-C height 128 above the FE metallization 116. In an embodiment, the fourth die 144 is a TSV die that is coupled to the third die 142 with a disclosed controlled-deposit solder coupling and the fifth die 146 is a simple flip chip die.

Also, the second die 140 may be located below the BBUL-C height 128 such that the first die 110, the subsequent die 132, and the second die 140 are all effectively embedded within the form factor of the BBUL-C substrate 124. It may now be understood that at least one die may be stacked above the subsequent die 132 but it would not be effectively embedded within the form factor of the BBUL-C substrate 124.

FIG. 4b is a cross-section elevation of the embedded die depicted in FIG. 2a during further processing according to an example embodiment. The embedded die apparatus 402 is processed with a hard mask 452 that overlies the DBF 422. Other structures may be similar to those depicted in the series 2 FIGs.

FIG. 4c is a cross-section elevation of the embedded die depicted in FIG. 4b during further processing according to an example embodiment. The embedded die apparatus 403 has been processed by patterning opens in the hard mask 452 in preparation for an etching process that will stop on the TSV contact 120.

FIG. 4d is a cross-section elevation of the embedded die depicted in FIG. 4c during further processing according to an example embodiment. The embedded die apparatus 404 has been processed by directional etching through the hard mask 452 to open recesses 423 that expose the TSV contacts 120. Processing may therefore continue by removal of the hard mask 422 and filling the recesses 423 according to any of the disclosed embodiments. Further processing may therefore include mating a subsequent die to the added solder form factor, followed by forming an underfill material between the DBF 422 and the subsequent die.

It may be appreciated that similar to the series 2 embodiment illustrated in FIGs. 2a – 2e, the DBF 422 may attain any disclosed DBF height above the FE metallization 116 in

comparison to the BBUL-C height 128 above the FE metallization 116. In an embodiment, the fourth die 144 is a TSV die that is coupled to the third die 142 with a disclosed controlled-deposit solder coupling and the fifth die 146 is a simple flip chip die.

Also, the second die 140 may be located below the BBUL-C height 128 such that
5 the first die 110, the subsequent die 132, and the second die 140 are all effectively embedded within the form factor of the BBUL-C substrate 124. It may now be understood that at least one die may be stacked above the subsequent die 132 but it would not be effectively embedded within the form factor of the BBUL-C substrate 124.

FIG. 5 is a cross-section elevation of an apparatus that includes an embedded die
10 with a controlled-deposit solder coupling according to an example embodiment. Structures depicted in FIG. 5 are similar to those depicted in FIG. 1, with the addition that the underfill process is altered. It can be seen in FIG. 5 that the underfill material 538 has filled into a space that has no remaining DBF. As a consequence of this process embodiment, the underfill material 538 may be selected to act as the sole spacer structure
15 between the die backside surface 114 and the subsequent die 532.

Vertical spacing may still be controlled by differences between the DBF height 126 above the FE metallization 116 and the BBUL-C height 128 above the FE metallization 116. Actual spacing between the die backside 114 and the bond pads of the subsequent die 532 may be controlled by the DBF height 126 being greater than the
20 BBUL-C height 128.

FIG. 6d is a cross-section elevation of an embedded die during formation of a controlled-deposit solder coupling that may follow previously disclosed processing after a controlled-deposit solder processing has been accomplished according to an example embodiment. The controlled-deposit solder coupling 134 has been formed including a
25 form of the added solder (in this example embodiment the discrete added solder 650) dome-top form factor.

In an embodiment, the DBF has been removed by a plasma-ashing process according to known technique. Processing may cause roughening of the surfaces of the controlled-deposit solder coupling 134 and the discrete added solder 650. Such processing
30 may also remove incidental oxides on the surfaces of the controlled-deposit solder coupling 134 and the discrete added solder 650, which makes more useful contact surfaces for mating with a subsequent-die bump.

FIG. 6e is a cross-section elevation of the embedded die depicted in FIG. 6d during further processing according to an example embodiment. The subsequent die 632 has

been mated to the added solder 650 at the electrical bump 636. By use of this embodiment, sufficient solder is present to make a useful connection between the embedded die 110 and the subsequent die 632. It may now be appreciated that processing to achieve the configuration in FIG. 6e may be done by first removing any DBF.

5 Similarly, it may now be understood that processing to achieve the configuration in FIG. 6e may be done by using the DBF height (such as the DBF height 126 depicted in FIG. 1) as a fixed distance, followed by ashing the DBF after mating the subsequent die 632 to the embedded die 110.

After the structure depicted in FIG. 6e is achieved, processing may then continue
10 by underfilling to achieve the apparatus depicted in FIG. 5. In an embodiment, fluxless bonding of the electrical bump 136, depicted in FIG. 5, with the discrete added material 650 is carried out. Similarly in an embodiment, fluxless bonding of the electrical bump 136, depicted in FIG. 5, with the added material such as the dome-top form factor 148 depicted in FIG. 2c is carried out. In an embodiment, the underfilling process is carried
15 out by CUF action.

FIG. 7 is a cross-section elevation of an apparatus 700 that includes an embedded die 710 with a controlled-deposit solder coupling 734 according to an example embodiment. The embedded die 710 includes an active surface 712 and a backside surface 714. An FE metallization 716 is disposed on the active surface 712. A TSV 718
20 is disposed in the embedded die 710 and the TSV 718 contacts a TSV contact 720 on the backside surface 714.

The apparatus 700 includes a subsequent die 732 that can be seen to have a lateral (X-direction) dimension that is less than that of the DBF 722. Consequently, the entire subsequent die 732 may rest upon the DBF 722 during mating thereof. This embodiment
25 facilitates useful pre-selected spacing between the die backside and the active surface of the subsequent die 732. It can be seen the DBF 722 attains a DBF height 726 above the FE metallization 716 and the BBUL-C substrate 724 also attains a BBUL-C height 728 above the FE metallization 716. In an embodiment, the DBF height 726 is greater than the BBUL-C height 728. In an embodiment, the DBF height 726 is the same as the BBUL-C
30 height 728, as illustrated. In an embodiment, the DBF height 726 is less than the BBUL-C height 728.

In an embodiment, the embedded die 710 is disposed in a BBUL-C substrate 724 similar to other embodiments described and illustrated. Assembly of the embedded die 710 to the subsequent die 732 is accomplished by filling a conductive material 734 into a

recess that is disposed in the DBF 722, followed by mating the subsequent die 732 at a DBF height 726 that avoids secondary height adjustment by virtue of the DBF having a pre-selected. The conductive material 734 may also be referred to as a controlled-deposit solder coupling 734 according to an example embodiment.

5 It may now be appreciated that die stacks may include non-equivalent interface combinations such as LMI, LMI with additional MMI^n where n equals 1 to 3, LLI, LLI with additional MMI^n where n equals 1 to 4, and LLI^2 with additional LMI^n . where n equals 1 to 3.

10 Similarly, it may now be appreciated that LMI, LLI, and MMI permutations so disclosed may be formed with the second die 140 located below the BBUL-C height 128 such that the first die 110, the subsequent die 132, and the second die 140 are all effectively embedded within the form factor of the BBUL-C substrate 124. It may now be understood that at least one die may be stacked above the subsequent die 132 but it would not be effectively embedded within the form factor of the BBUL-C substrate 124.

15 FIG. 8 is a cross-section elevation of an apparatus 800 that includes an embedded die 810 with a controlled-deposit solder coupling 834 according to an example embodiment. The embedded die 810 includes an active surface 812 and a backside surface 814. An FE metallization 816 is disposed on the active surface 812. A TSV 818 is disposed in the embedded die 810 and the TSV 818 contacts a TSV contact 820 on the
20 backside surface 814.

The apparatus 800 includes a subsequent die 832 that can be seen to have a lateral (X-direction) dimension that is less than that of an underfill material 738 that has entirely replaced a DBF such as the DBF 722 depicted in FIG. 7. Consequently, the entire subsequent die 832 may rest upon the underfill material 832 after mating thereof. This
25 embodiment facilitates useful pre-selected spacing between the die backside and the active surface of the subsequent die 832. It can be seen the underfill material 832 attains a DBF height 826 above the FE metallization 816 and the BBUL-C substrate 824 also attains a BBUL-C height 828 above the FE metallization 816. In an embodiment, the DBF height 826 is greater than the BBUL-C height 828. In an embodiment, the DBF height 826 is the
30 same as the BBUL-C height 828, as illustrated. In an embodiment, the DBF height 826 is less than the BBUL-C height 828.

In an embodiment, the embedded die 810 is disposed in a BBUL-C substrate 824 similar to other embodiments described and illustrated. Assembly of the embedded die 810 to the subsequent die 832 is accomplished by filling a conductive material 834 into a

recess that is disposed in the DBF, followed by mating the subsequent die 832 at a DBF height 826 that avoids secondary height adjustment by virtue of the DBF having a pre-selected thickness. Thereafter, the DBF is removed such as by ashing and the underfill material 838 is flowed between the die backside surface 814 and the subsequent die 832.

- 5 The conductive material 834 may also be referred to as a controlled-deposit solder coupling 834 according to an example embodiment.

It may now be appreciated that die stacks may include non-equivalent interface combinations such as LMI, LMI with additional MMIⁿ where n equals 1 to 3, LLI, LLI with additional MMIⁿ where n equals 1 to 4, and LLI² with additional LMIⁿ where n
10 equals 1 to 3.

Similarly, it may now be appreciated that LMI, LLI, and MMI permutations so disclosed may be formed with the second die 140 located below the BBUL-C height 128 such that the first die 110, the subsequent die 132, and the second die 140 are all effectively embedded within the form factor of the BBUL-C substrate 124. It may now be
15 understood that at least one die may be stacked above the subsequent die 132 but it would not be effectively embedded within the form factor of the BBUL-C substrate 124.

FIG. 12 is a computer reproduction of a photomicrograph according to an example embodiment. An embedded first die 1210 has a connection on the die backside thereof with a controlled-deposit solder coupling 1234. A subsequent die 1232 is coupled to the
20 embedded first die 1210 by an electrical bump 1236, and added solder such as discrete added solder 1250 is shown to fill voids in underfill material 1238 between the controlled-deposit solder coupling 1234 and the electrical bump 1236.

FIG. 13 is a computer reproduction of a photomicrograph according to an example embodiment. A TSV contact 1320 that is part of an embedded first die has a connection
25 with a controlled-deposit solder coupling 1334. A subsequent die 1332 is coupled to the TSV contact 1320 by a controlled-deposit solder coupling 1334 which included added solder (such as the dome-top form factor 148 seen in FIG. 2c) to fill voids in underfill material 1338.

FIG. 14 is a computer reproduction of a photomicrograph according to an example
30 embodiment. An embedded first die 1410 has a connection on the die backside thereof with a controlled-deposit solder coupling 1434. A subsequent die 1432 is coupled to the embedded first die 1410 by an electrical bump 1436, and added solder such as discrete added solder 1450 is shown to fill voids in underfill material 1438 between the controlled-deposit solder coupling 1434 and the electrical bump 1436.

FIG. 15 is a computer reproduction of a photomicrograph according to an example embodiment. A TSV contact 1520 that is part of an embedded first die has a connection with a controlled-deposit solder coupling 1534 that has added solder such as discrete added solder 1550 that is useful to fill voids in underfill material 1538.

5 FIG. 16 is a process and method flow diagram according to an example embodiment.

At 1608, the process includes assembling a microelectronic die to a coreless substrate. In a non-limiting example embodiment, the first die 110 is embedded in the BBUL-C 124. It may now be appreciated that this process may be selected to be after
10 patterning opens in the DBF.

At 1610, the process includes opening a recess in a DBF to expose a TSV contact.

At 1612, the process includes opening the recess by laser drilling.

At 1614, the process includes opening the recess by patterning a soft mask over light-sensitive DBF material and rinsing affected areas of the DBF.

15 At 1616, the process includes patterning a hard mask over the DBF and opening the recess by a directional etch.

At 1620, the process includes filling the recess with a conductive material that contacts the TSV contact.

At 1630, the process includes forming added solder to the conductive material at a
20 level of the DBF. In a non-limiting example embodiment, the added solder 148 is formed above the controlled-deposit solder coupling 134 as illustrated in FIG. 2c. In a non-limiting example embodiment, the discrete added solder 150 is formed above the controlled-deposit solder coupling 134 as illustrated in FIG. 2d.

At 1640, the process includes assembling the microelectronic die to a subsequent
25 die. In a non-limiting example embodiment, the first die 110 is assembled to a subsequent die 132.

At 1650, the microelectronic device is assembled to a computing system. In a non-limiting example embodiment, the apparatus 100 including at least the BBUL-C, the first die 110, and the subsequent die 132 is assembled to a computer system such as the
30 computer system 1700 depicted in FIG. 17.

FIG. 17 is a schematic of a computer system according to an embodiment. The computer system 1700 (also referred to as the electronic system 1700) as depicted can embody a controlled-deposit solder coupling according to any of the several disclosed

embodiments and their equivalents as set forth in this disclosure. An apparatus that includes a controlled-deposit solder coupling that is assembled to a computer system.

The computer system 1700 may be a smartphone. The computer system 1700 may be a tablet computer. The computer system 1700 may be a mobile device such as a
5 notebook computer. The computer system 1700 may be a mobile device such as an ultrabook computer. The computer system 1700 may be a desktop computer. The computer system 1700 may be integral to an automobile. The computer system 1700 may be integral to a television. The computer system 1700 may be integral to a DVD player. The computer system 1700 may be integral to a digital camcorder.

10 In an embodiment, the electronic system 1700 is a computer system that includes a system bus 1720 to electrically couple the various components of the electronic system 1700. The system bus 1720 is a single bus or any combination of busses according to various embodiments. The electronic system 1700 includes a voltage source 1730 that provides power to an integrated circuit 1710. In some embodiments, the voltage source
15 1730 supplies current to the integrated circuit 1710 through the system bus 1720.

The integrated circuit 1710 is electrically coupled to the system bus 1720 and includes any circuit, or combination of circuits according to an embodiment. In an embodiment, the integrated circuit 1710 includes a processor 1712 that can be of any type of an apparatus that includes a controlled-deposit solder coupling embodiment. As used
20 herein, the processor 1712 may mean any type of circuit such as, but not limited to, a microprocessor, a microcontroller, a graphics processor, a digital signal processor, or another processor. In an embodiment, SRAM embodiments are found in memory caches of the processor 1712. Other types of circuits that can be included in the integrated circuit 1710 are a custom circuit or an application-specific integrated circuit (ASIC), such as a
25 communications circuit 1714 for use in non-equivalent wireless devices such as cellular telephones, smartphones, pagers, portable computers, two-way radios, and other electronic systems. In an embodiment, the processor 1710 includes on-die memory 1716 such as static random-access memory (SRAM). In an embodiment, the processor 1710 includes embedded on-die memory 1716 such as embedded dynamic random-access memory
30 (eDRAM). Disclosed COB embodiments and their art-recognized equivalents are integral memory cells in the eDRAM.

In an embodiment, the integrated circuit 1710 is complemented with a subsequent integrated circuit 1711 such in any LLI, LMI, or MMI embodiment as set forth in this disclosure. In an embodiment, the subsequent integrated circuit 1711 is as a graphics

processor or a radio-frequency integrated circuit or both. In an embodiment, the dual integrated circuit 1711 includes embedded on-die memory 1717 such as eDRAM with any disclosed controlled-deposit solder coupling embodiments. The dual integrated circuit 1711 includes an RFIC dual processor 1713 and a dual communications circuit 1715 and
5 dual on-die memory 1717 such as SRAM. In an embodiment, the dual communications circuit 1715 is particularly configured for RF processing.

In an embodiment, at least one passive device 1780 is coupled to the subsequent integrated circuit 1711 such that the integrated circuit 1711 and the at least one passive device are part of the any apparatus embodiment that includes a controlled-deposit solder
10 coupling that includes the integrated circuit 1710 and the integrated circuit 1711. In an embodiment, the at least one passive device is a sensor such as an accelerometer for a tablet or smartphone.

In an embodiment, the electronic system 1700 includes an antenna element 1782 such as any controlled-deposit solder coupling embodiment set forth in this disclosure. By
15 use of the antenna element 1782, a remote device 1784 such as a television, may be operated remotely through a wireless link by an apparatus embodiment. For example, an application on a smart telephone that operates through a wireless link broadcasts instructions to a television up to about 30 meters distant such as by Bluetooth® technology. In an embodiment, the remote device(s) includes a global positioning system
20 of satellites for which the antenna element(s) are configured as receivers.

In an embodiment, the electronic system 1700 also includes an external memory 1740 that in turn may include one or more memory elements suitable to the particular application, such as a main memory 1742 in the form of RAM, one or more hard drives 1744, and/or one or more drives that handle removable media 1746, such as diskettes,
25 compact disks (CDs), digital variable disks (DVDs), flash memory drives, and other removable media known in the art. In an embodiment, the external memory 1740 is part of a POP package that is stacked upon an apparatus that includes a controlled-deposit solder coupling according to any disclosed embodiments. In an embodiment, the external memory 1740 is embedded memory 1748 such an apparatus that includes a controlled-
30 deposit solder coupling according to any disclosed embodiment.

In an embodiment, the electronic system 1700 also includes a display device 1750, and an audio output 1760. In an embodiment, the electronic system 1700 includes an input device such as a controller 1770 that may be a keyboard, mouse, touch pad, keypad, trackball, game controller, microphone, voice-recognition device, or any other input

device that inputs information into the electronic system 1700. In an embodiment, an input device 1770 includes a camera. In an embodiment, an input device 1770 includes a digital sound recorder. In an embodiment, an input device 1770 includes a camera and a digital sound recorder.

5 A foundation substrate 1790 may be part of the computing system 1700. The foundation substrate 1790 is a motherboard that supports an apparatus that includes a controlled-deposit solder coupling embodiment. In an embodiment, the foundation substrate 1790 is a board which supports an apparatus that includes a controlled-deposit solder coupling embodiment. In an embodiment, the foundation substrate 1790
10 incorporates at least one of the functionalities encompassed within the dashed line 1790 and is a substrate such as the user shell of a wireless communicator.

As shown herein, the integrated circuit 1710 can be implemented in a number of different embodiments, an apparatus that includes a controlled-deposit solder coupling according to any of the several disclosed embodiments and their equivalents, an electronic
15 system, a computer system, one or more methods of fabricating an integrated circuit, and one or more methods of fabricating and assembling an apparatus that includes a controlled-deposit solder coupling according to any of the several disclosed embodiments as set forth herein in the various embodiments and their art-recognized equivalents. The elements, materials, geometries, dimensions, and sequence of operations can all be varied
20 to suit particular I/O coupling requirements including controlled-deposit solder coupling embodiments and their equivalents.

Although a die may refer to a processor chip, an RF chip, an RFIC chip, or a memory chip may be mentioned in the same sentence, but it should not be construed that they are equivalent structures. Reference throughout this disclosure to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described
25 in connection with the embodiment is included in at least one embodiment of the present invention. The appearance of the phrases "in one embodiment" or "in an embodiment" in various places throughout this disclosure are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be
30 combined in any suitable manner in one or more embodiments.

Terms such as "upper" and "lower" "above" and "below" may be understood by reference to the illustrated X-Z coordinates, and terms such as "adjacent" may be understood by reference to X-Y coordinates or to non-Z coordinates.

The Abstract is provided to comply with 37 C.F.R. §1.72(b) requiring an abstract that will allow the reader to quickly ascertain the nature and gist of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims.

5 In the foregoing Detailed Description, various features are grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the claimed embodiments of the invention require more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter lies in less than all features of a
10 single disclosed embodiment. Thus the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate preferred embodiment.

 It will be readily understood to those skilled in the art that various other changes in the details, material, and arrangements of the parts and method stages which have been
15 described and illustrated in order to explain the nature of this invention may be made without departing from the principles and scope of the invention as expressed in the subjoined claims.

CLAIMS

What is claimed is:

1. A process of bumping a die backside, comprising:
opening a recess in a die backside film (DBF) to expose a through-silicon via
5 (TSV) contact in a die, the die including an active surface and a backside surface;
filling the recess with a conductive material that contacts the TSV contact; and
forming added solder to the conductive material at a level of the DBF.
2. The process of claim 1, wherein opening the recess includes laser drilling
into the DBF to expose the TSV contact.
- 10 3. The process of claim 1, wherein opening the recess includes using a photo-
sensitive DBF, further including:
patterning a mask over the DBF that creates an open above the TSV contact;
exposing the DBF through the mask to weaken the DBF above the TSV; and
rinsing the TSV to open the recess.
- 15 4. The process of claim 4, further including:
patterning a hard mask over the DBF that creates an open above the TSV contact;
and
dry etching the DBF to open the recess.
- 20 5. The process of claim 1, wherein the die is a first die, the process further
including coupling a subsequent die to the first die at the added solder to form an electrical
coupling consisting of the TSV contact, the conductive material, the added solder, an
electrical bump coupled to the subsequent die, and a subsequent die bond pad coupled to
the electrical bump.
- 25 6. The process of claim 1, further including embedding the die in a coreless,
bumpless build-up layer (BBUL-C) substrate, wherein the backside surface is exposed and
the active surface is coupled to the BBUL-C substrate.
7. The process of claim 1, further including:
embedding the die in a coreless, bumpless build-up layer (BBUL-C) substrate,
wherein the backside surface is exposed and the active surface is coupled to the BBUL-C
30 substrate; and
removing the DBF.
8. The process of claim 1, further including:

embedding the die in a coreless, bumpless build-up layer (BBUL-C) substrate, wherein the backside surface is exposed and the active surface is coupled to the BBUL-C substrate to achieve an embedded die;

removing the DBF; and
5 coupling a subsequent die to the embedded die at the added solder.

9. The process of claim 1, further including:

embedding the die in a coreless, bumpless build-up layer (BBUL-C) substrate, wherein the backside surface is exposed and the active surface is coupled to the BBUL-C substrate to achieve an embedded die;

10 removing the DBF;
coupling a subsequent die to the embedded die at the added solder; and
underfilling a material between the subsequent die and the embedded die by capillary underfill (CUF) action.

10. The process of claim 1, further including:

15 embedding the die in a coreless, bumpless build-up layer (BBUL-C) substrate, wherein the backside surface is exposed and the active surface is coupled to the BBUL-C substrate to achieve an embedded die;
removing the DBF;
coupling a subsequent die to the embedded die at the added solder; and
20 underfilling a material between the subsequent die and the embedded die by epoxy flux action.

11. The process of claim 1, wherein the DBF has a first thickness, wherein the die is a first die, and the process further including:

coupling a subsequent die to the first die by seating the subsequent die upon the
25 DBF such that the first thickness creates a selected offset between the first die and the subsequent die.

12. The process of claim 1, wherein the DBF has a first thickness, wherein the die is a first die, and the process further including:

coupling a subsequent die to the first die by seating the subsequent die upon the
30 DBF such that the first thickness creates a selected offset between the first die and the subsequent die;

removing the DBF; and
underfilling a material between the subsequent die and the first die by capillary underfill (CUF) action.

13. The process of claim 1, wherein the DBF has a first thickness, wherein the die is a first die, and the process further including:

coupling a subsequent die to the first die by seating the subsequent die upon the DBF such that the first thickness creates a selected offset between the first die and the

5 subsequent die;

removing the DBF; and

underfilling a material between the subsequent die and the first die by epoxy flux action.

14. The process of claim 1, wherein filling the recess with the conductive
10 material is carried out by wiping solder precursor across the DBF to fill the recess.

15. The process of claim 1, wherein filling the recess with the conductive material is carried out by jetting solder precursor to fill the recess.

16. The process of claim 1, wherein filling the recess with the conductive material is carried out by plating solder onto the TSV contact and to fill the recess.

15 17. The process of claim 1, wherein the DBF has a first thickness, the process further including:

removing the DBF; and

underfilling an underfill material to contact at least one of the the conductive material and the added material.

20 18. The process of claim 1, wherein the DBF has a first thickness, the process further including:

removing a fraction of the DBF; and

underfilling an underfill material to contact at least one of the the conductive material and the added material.

25 19. An apparatus comprising:

a die including a through-silicon via (TSV) disposed therein, the die including an active surface and a backside surface;

a TSV contact that contacts the TSV;

a die backside film (DBF) disposed on the backside surface;

30 a recess that exposes the TSV contact;

conductive material disposed in the recess that contacts the TSV contact; and

added solder that contacts the conductive material, wherein the added solder is disposed at a level of the DBF.

20. The apparatus of claim 19, wherein the die is an embedded die that is embedded in a coreless, bumpless build-up layer (BBUL-C) substrate, the apparatus further including a subsequent die coupled to the added solder.

21. The apparatus of claim 19, wherein the die is an embedded die that is
5 embedded in a coreless, bumpless build-up layer (BBUL-C) substrate, the apparatus further including a subsequent die coupled to the added solder, and wherein the subsequent die is seated on the DBF.

22. The apparatus of claim 19, wherein the die is a first die, that apparatus further including a subsequent die coupled to the added solder, wherein the first die is a
10 logic die with a first pin-out pitch, wherein the subsequent die is a logic die with a subsequent pin-out pitch, and wherein the first pin-out pitch matches the subsequent pin-out pitch.

23. The apparatus of claim 19, wherein the die is a first die, the apparatus further including a subsequent die coupled to the added solder, wherein the first die is a
15 logic die with a first pin-out pitch, wherein the subsequent die is a memory die with a subsequent pin-out pitch, and wherein the first pin-out pitch is different from the subsequent pin-out pitch.

24. The apparatus of claim 19, wherein the die is an embedded die that is embedded in a coreless, bumpless build-up layer (BBUL-C) substrate, the apparatus
20 further including:

a subsequent die coupled to the added solder, and wherein the embedded die and the subsequent die are coupled by:

the TSV contact;
the conductive material contacting the TSV contact;
25 the added solder contacting the conductive material;
an electrical bump coupled to the subsequent die;
and a subsequent die bond pad that contacts the electrical bump.

25. The apparatus of claim 19, wherein the die is embedded in a coreless, bumpless build-up layer (BBUL-C) substrate, wherein the backside surface is exposed and
30 the active surface is coupled to the BBUL-C substrate to achieve an embedded die.

26. An apparatus comprising:
a die including a through-silicon via (TSV) disposed therein, the die including an active surface and a backside surface;
a TSV contact that contacts the TSV;

an underfill material that contacts the backside surface with a contour characteristic of a removed die backside film (DBF) that was disposed on the backside surface;

conductive material with a contour that is characteristic of having been disposed in a recess of a removed die backside film (DBF), wherein the conductive material contacts

5 the TSV contact; and

added solder that contacts the conductive material.

27. The apparatus of claim 26, wherein the die is an embedded die that is embedded in a coreless, bumpless build-up layer (BBUL-C) substrate, the apparatus further including a subsequent die coupled to the added solder.

10 28. The apparatus of claim 26, wherein the die is a first die, the apparatus further including a subsequent die coupled to the added solder, wherein the first die is a logic die with a first pin-out pitch, wherein the subsequent die is a logic die with a subsequent pin-out pitch, and wherein the first pin-out pitch matches the subsequent pin-out pitch.

15 29. The apparatus of claim 26, wherein the die is a first die, the apparatus further including a subsequent die coupled to the added solder, wherein the first die is a logic die with a first pin-out pitch, wherein the subsequent die is a memory die with a subsequent pin-out pitch, and wherein the first pin-out pitch is different from the subsequent pin-out pitch.

20 30. The apparatus of claim 26, wherein the die is an embedded die that is embedded in a coreless, bumpless build-up layer (BBUL-C) substrate, the apparatus further including:

a subsequent die coupled to the added solder, and wherein the embedded die and the subsequent die are coupled by:

25 the TSV contact;

the conductive material contacting the TSV contact;

the added solder contacting the conductive material;

an electrical bump coupled to the subsequent die;

and a subsequent die bond pad that contacts the electrical bump.

30 31. A computer system comprising:

a die including a through-silicon via (TSV) disposed therein, the die including an active surface and a backside surface;

a TSV contact that contacts the TSV;

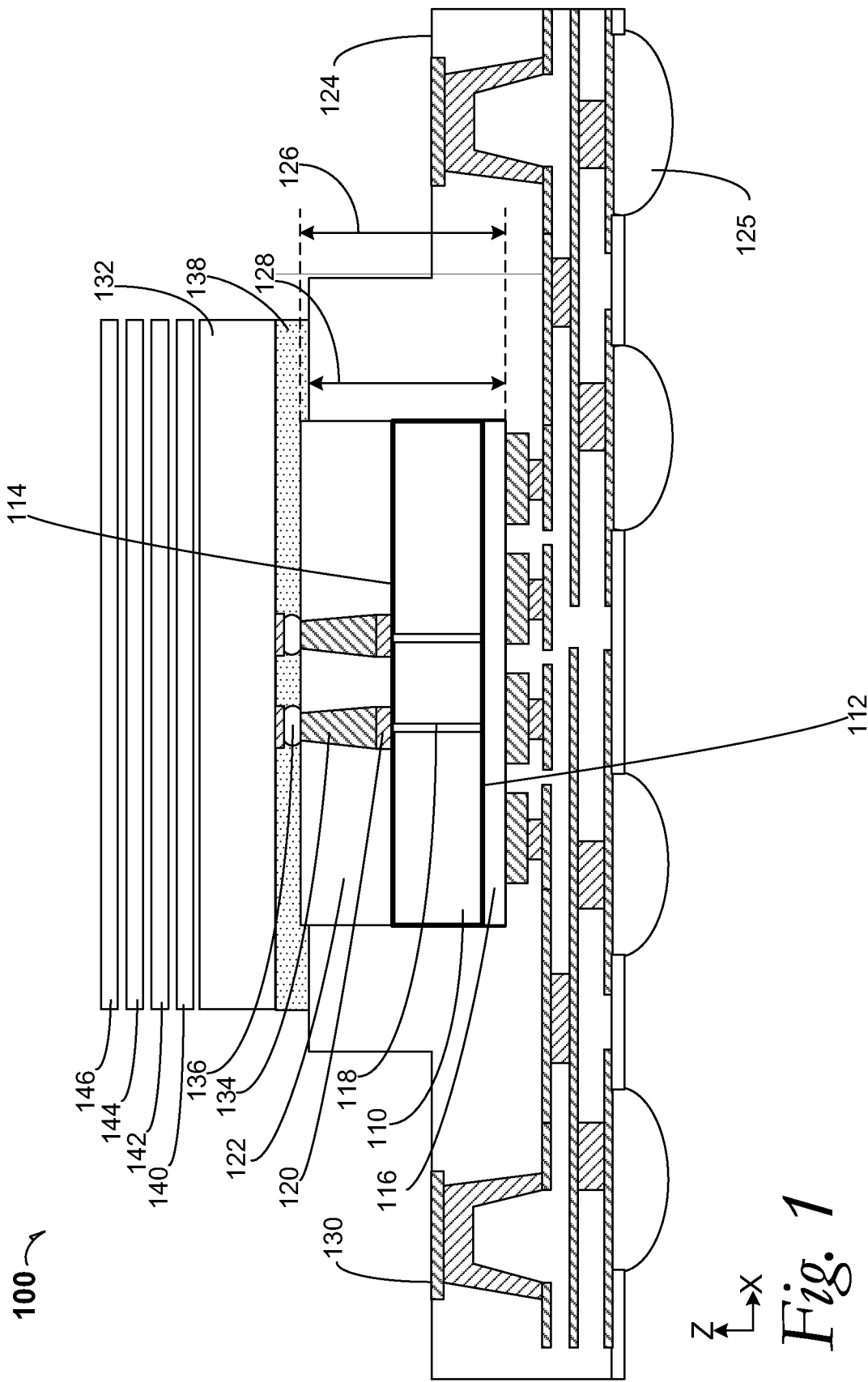
an underfill material that contacts the backside surface with a contour characteristic of a removed die backside film (DBF) that was disposed on the backside surface;

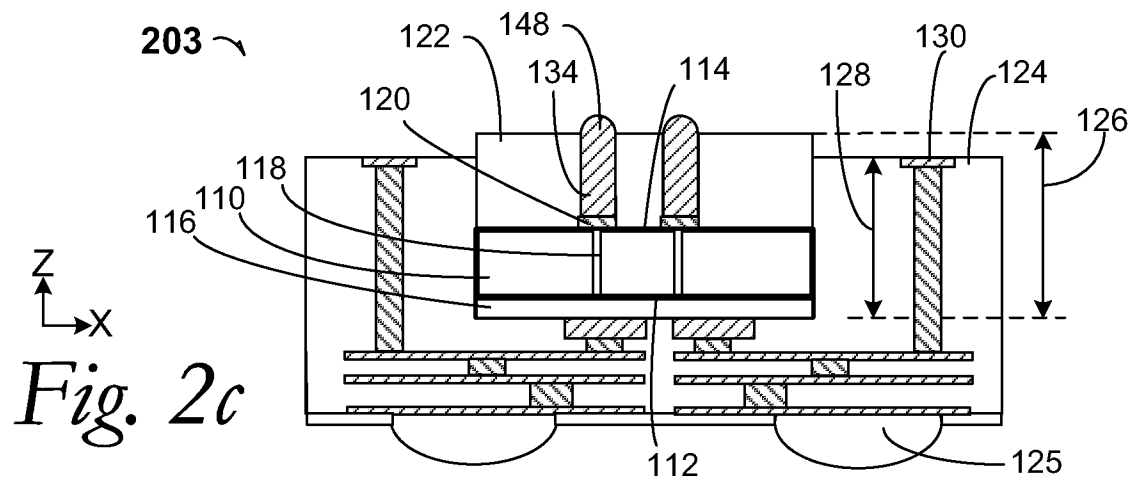
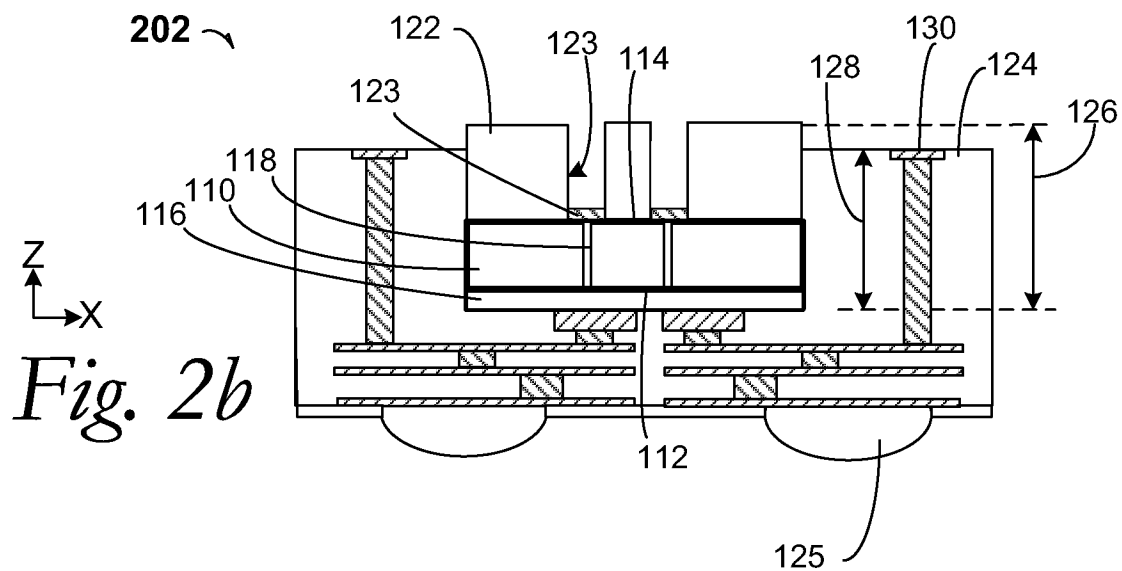
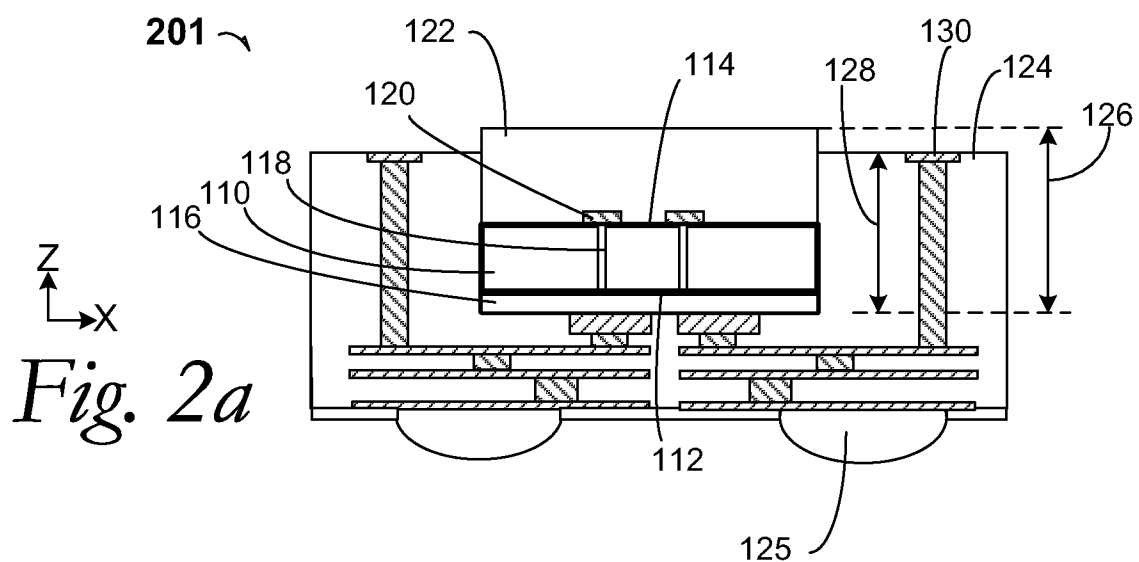
conductive material with a contour that is characteristic of having been disposed in a recess of a removed die backside film (DBF), wherein the conductive material contacts
5 the TSV contact;

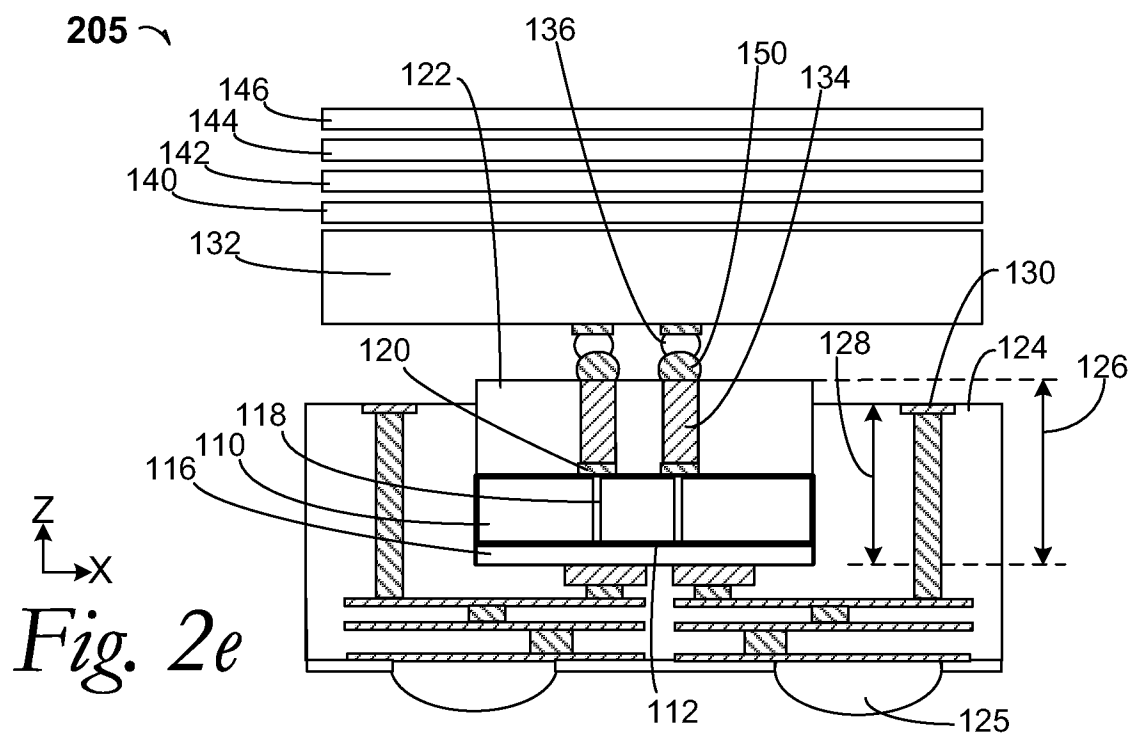
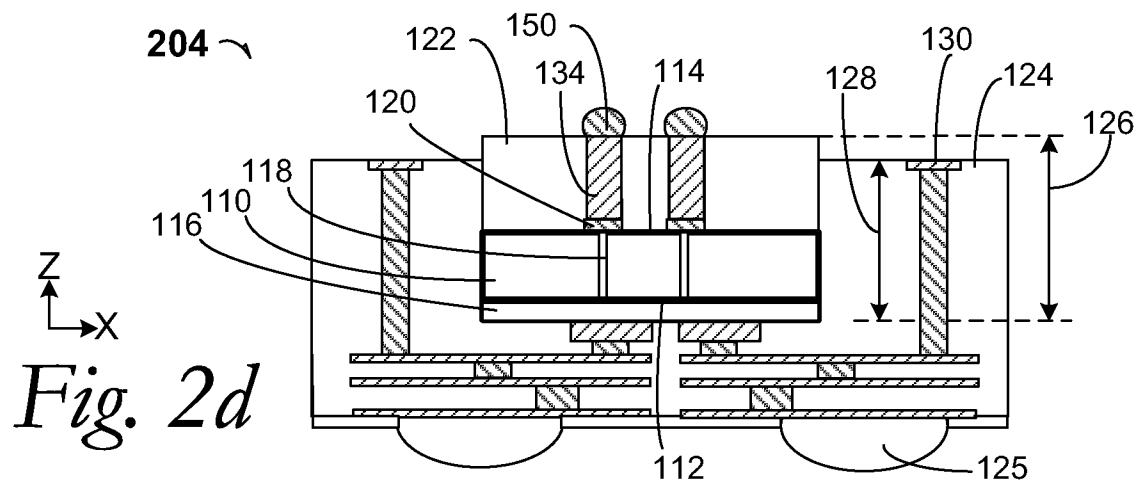
added solder that contacts the conductive material, wherein the die is an embedded die that is embedded in a coreless, bumpless build-up layer (BBUL-C) substrate, the apparatus further including a subsequent die coupled to the added solder;
and

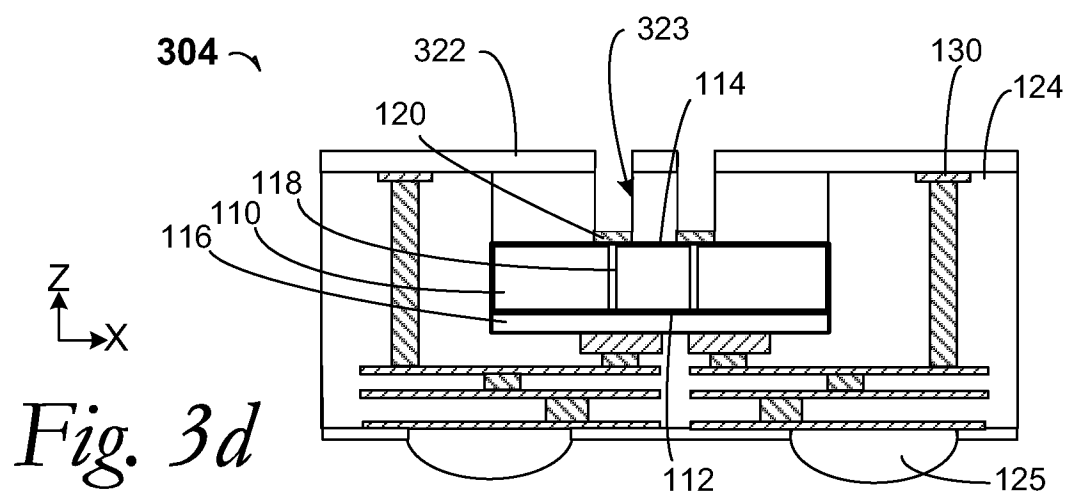
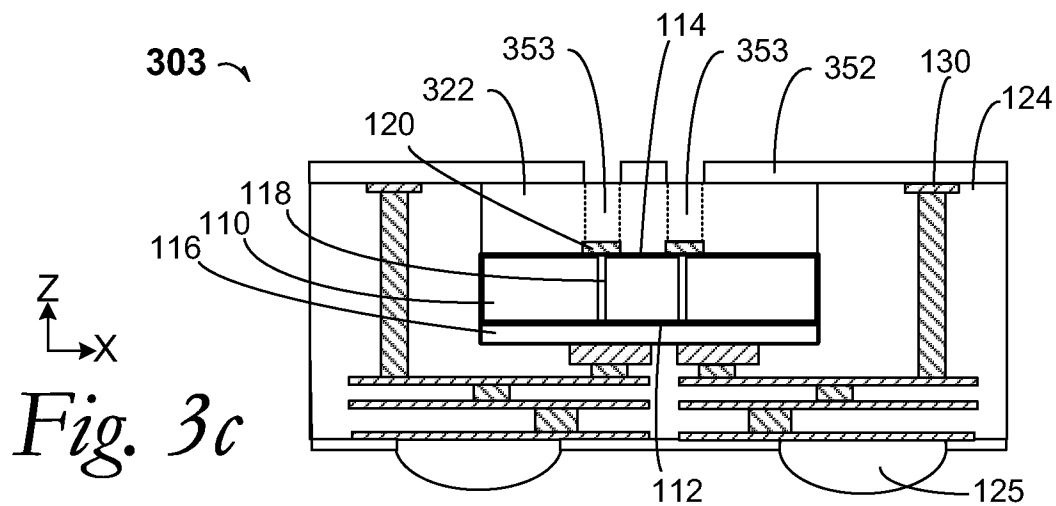
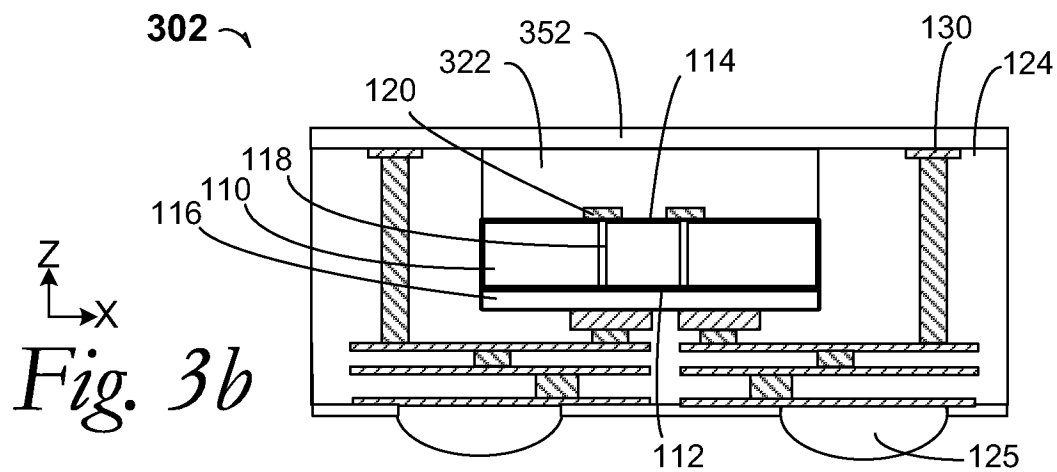
10 a foundation substrate that supports the semiconductive substrate.

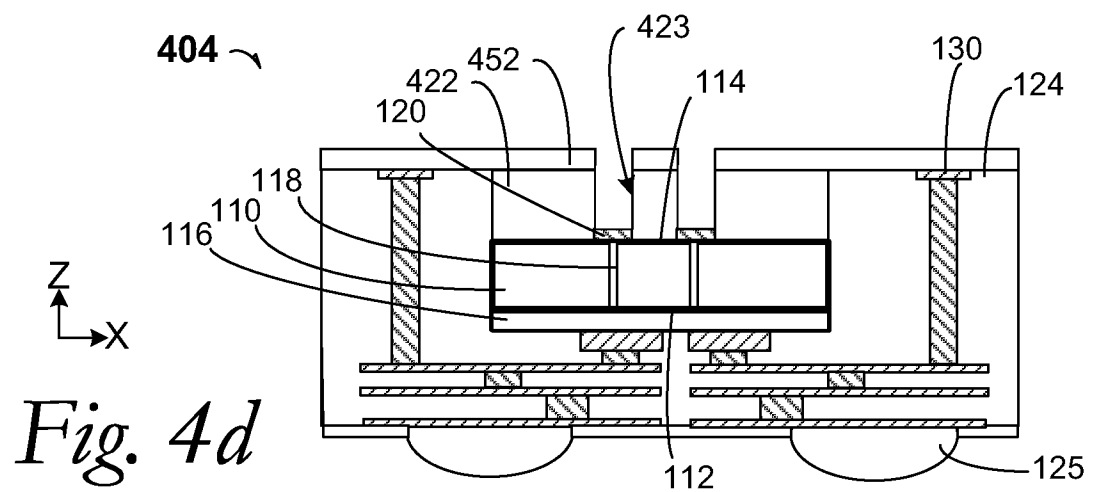
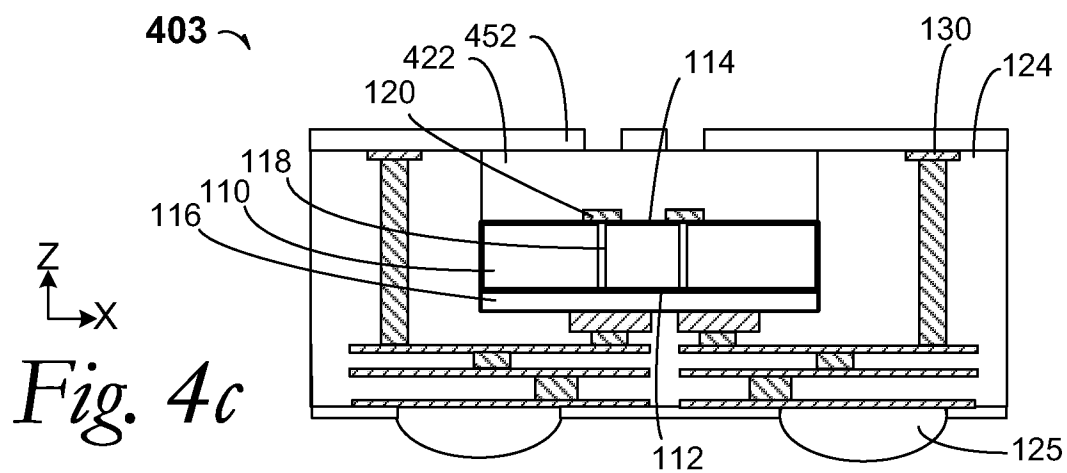
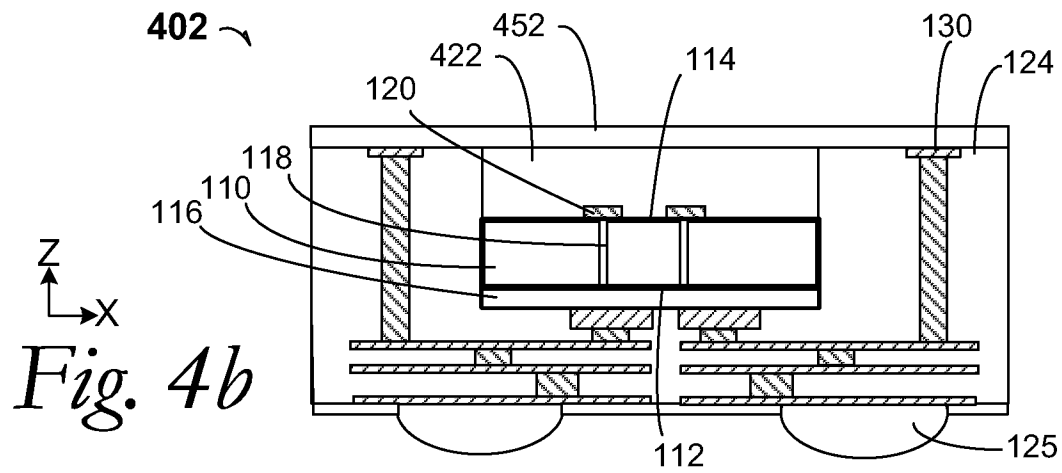
32. The computer system of claim 29, wherein the foundation substrate is part of a device selected from the group consisting of mobile device, a smartphone device, a tablet computer device, a vehicle, and a television.

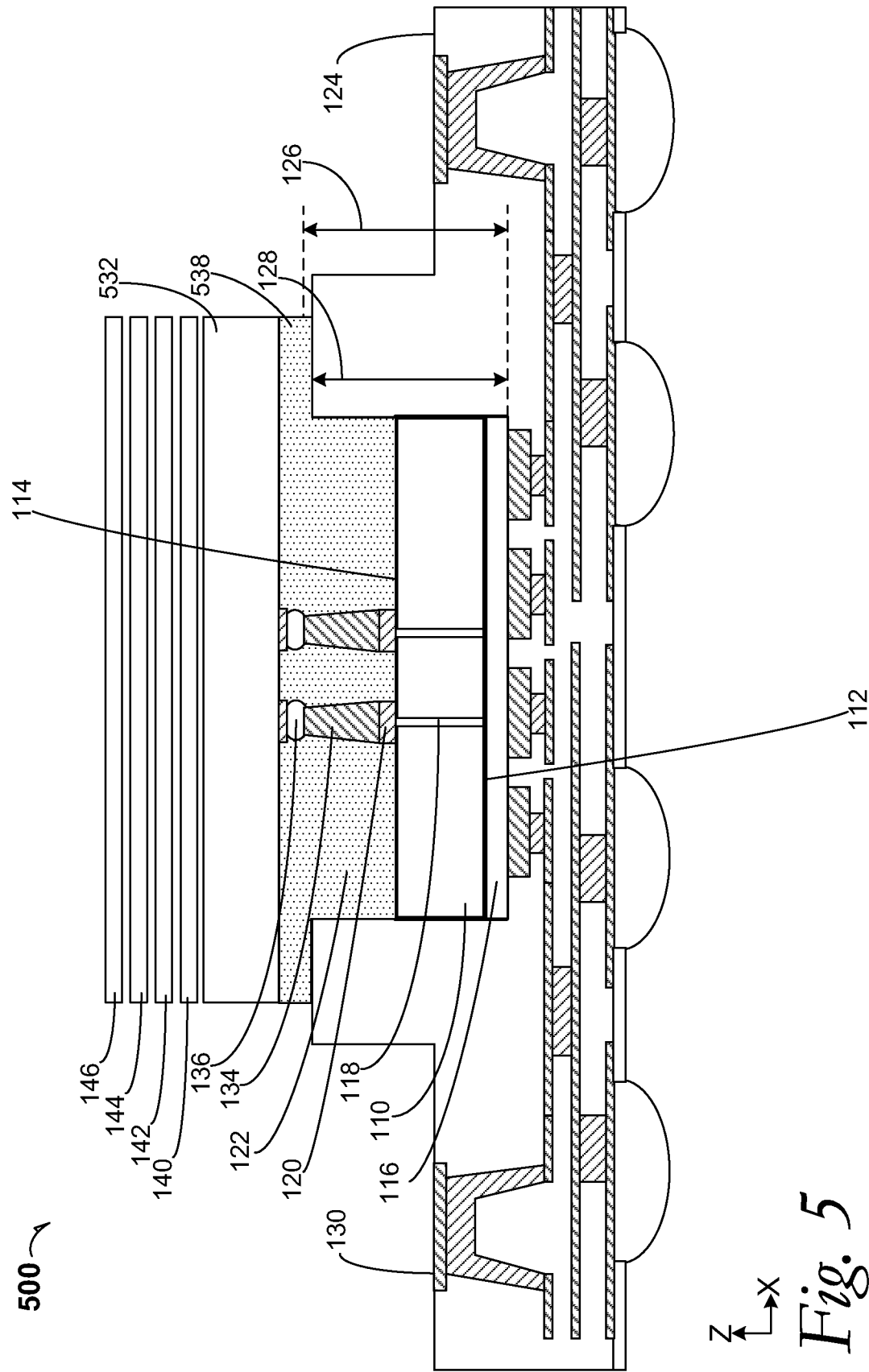


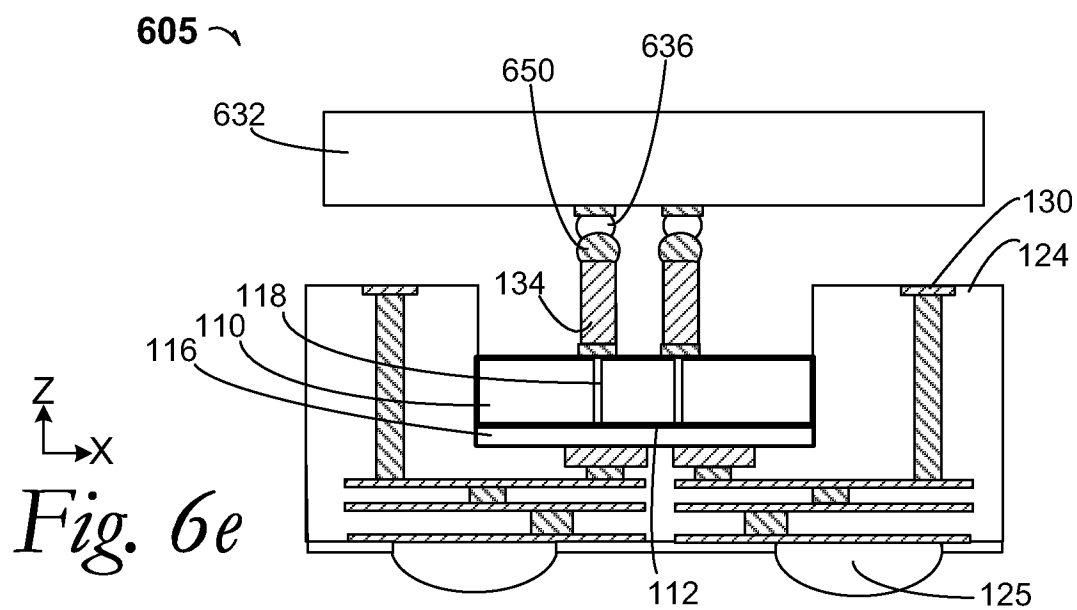
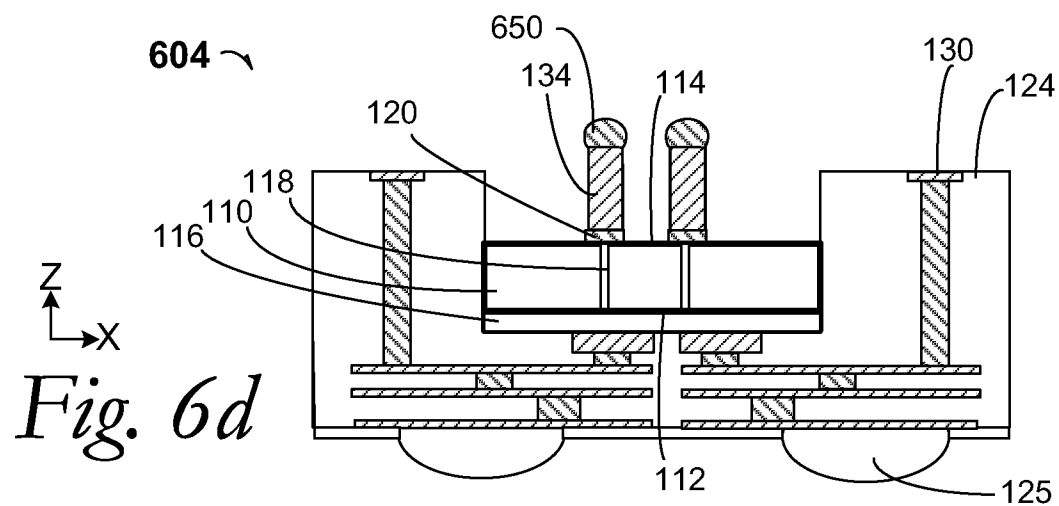












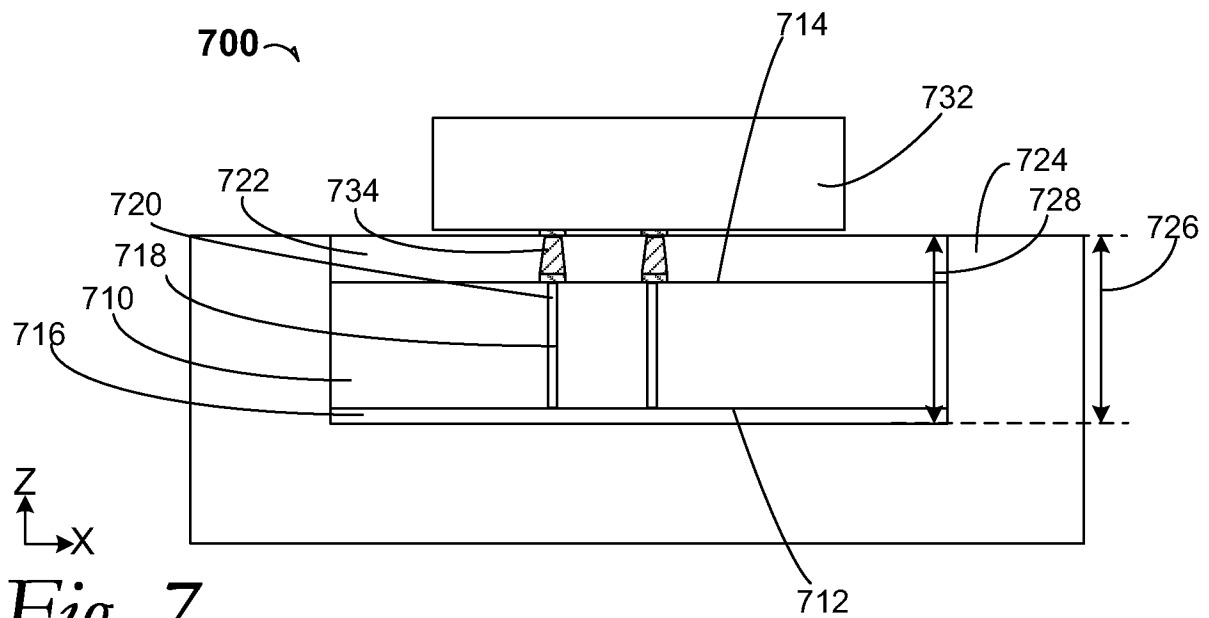


Fig. 7

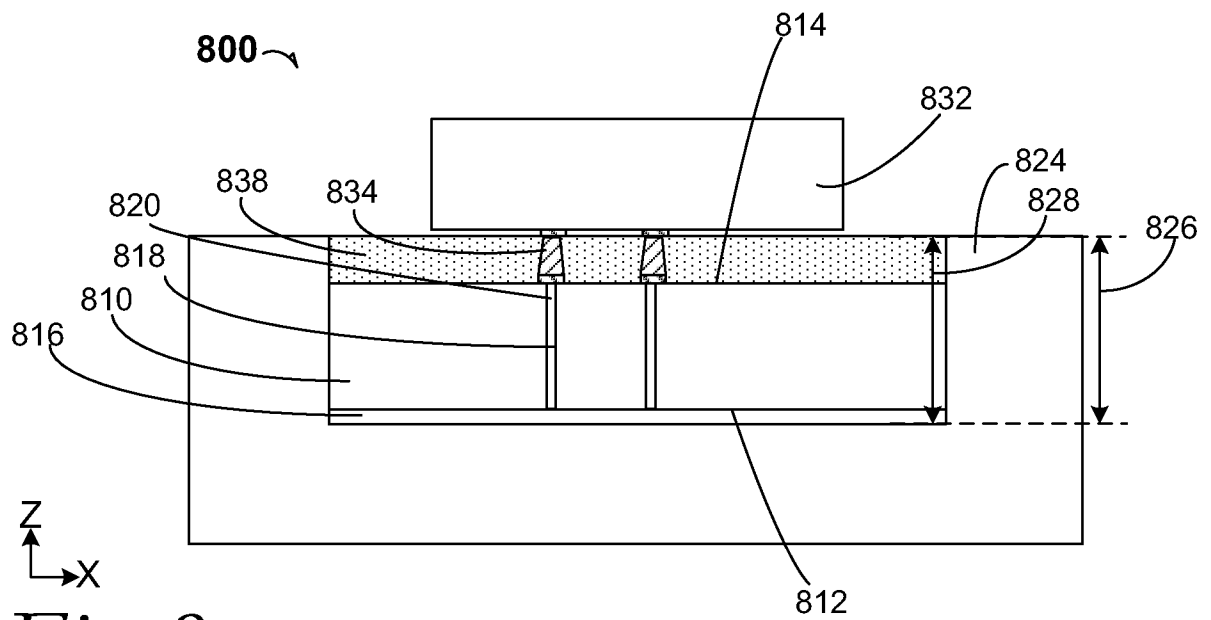


Fig. 8

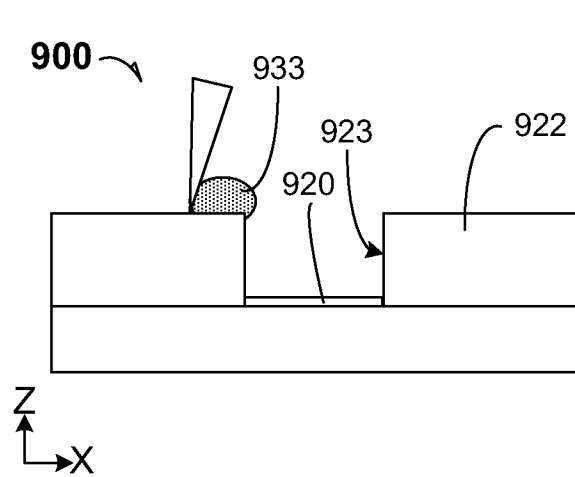


Fig. 9a

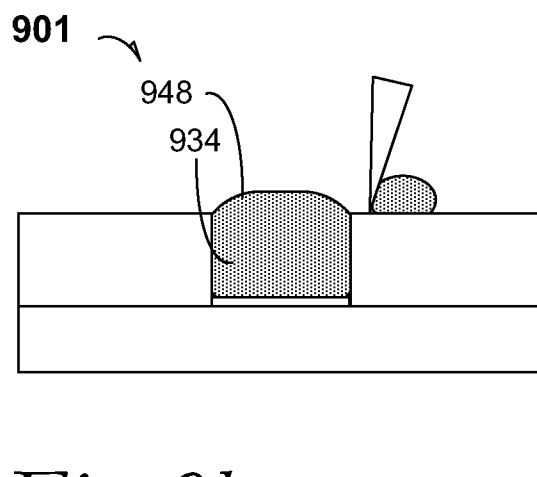


Fig. 9b

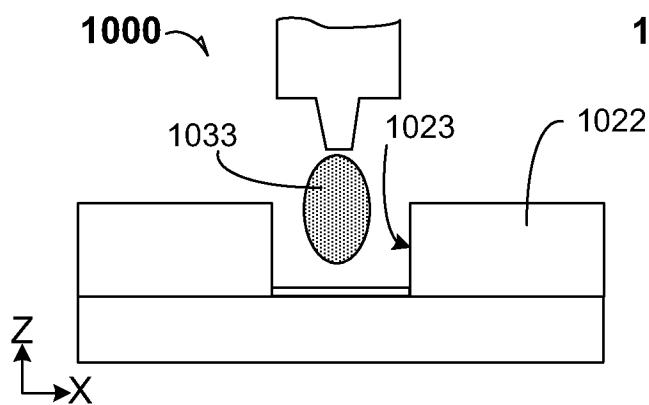


Fig. 10a

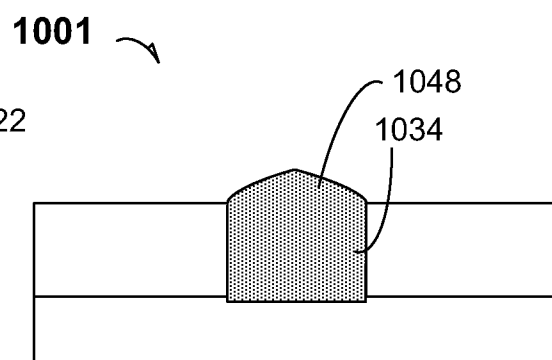


Fig. 10b

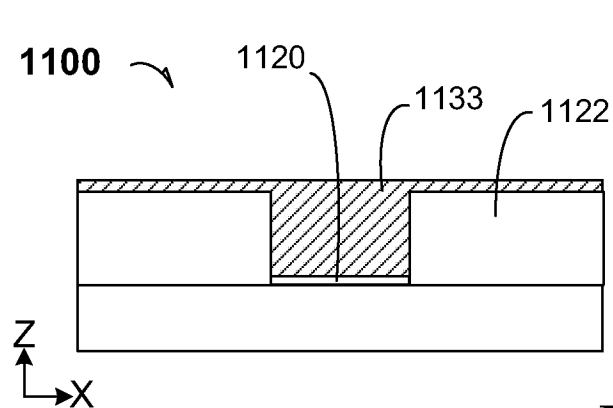


Fig. 11a

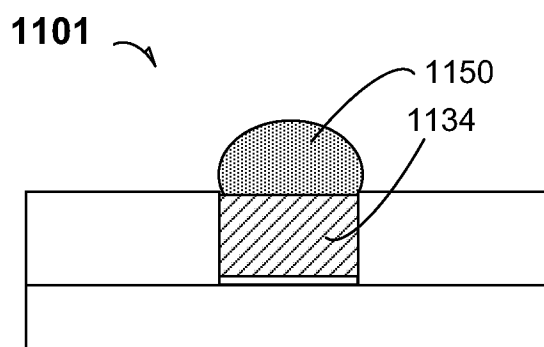
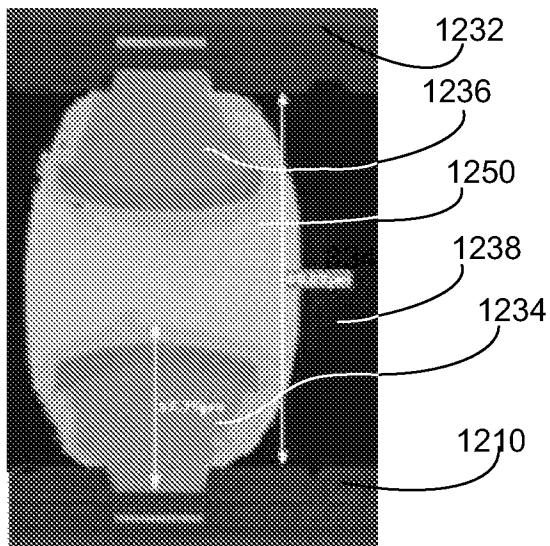
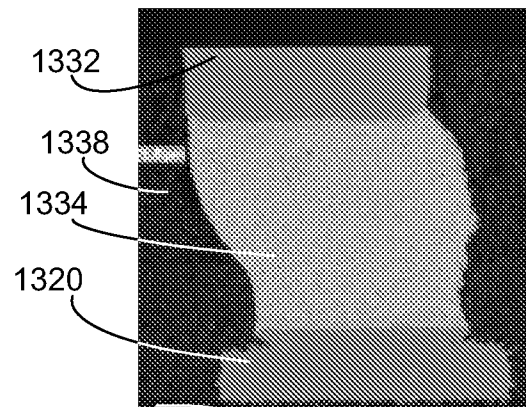
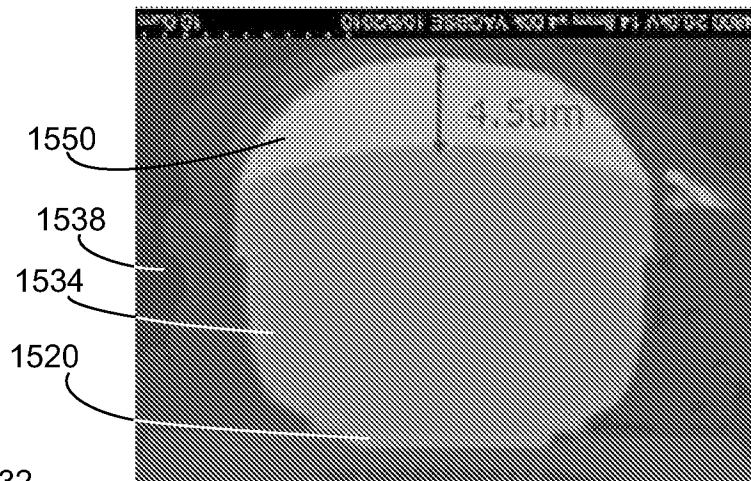
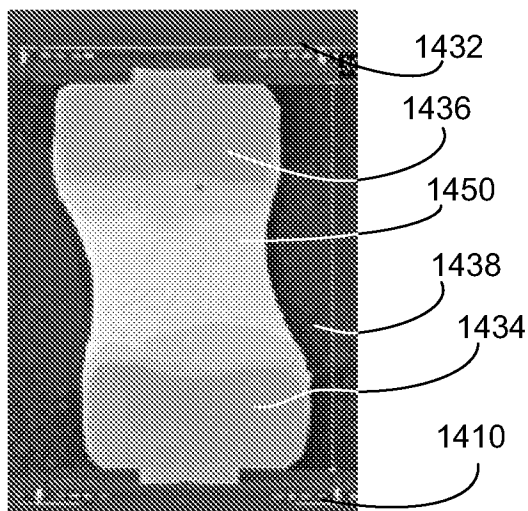
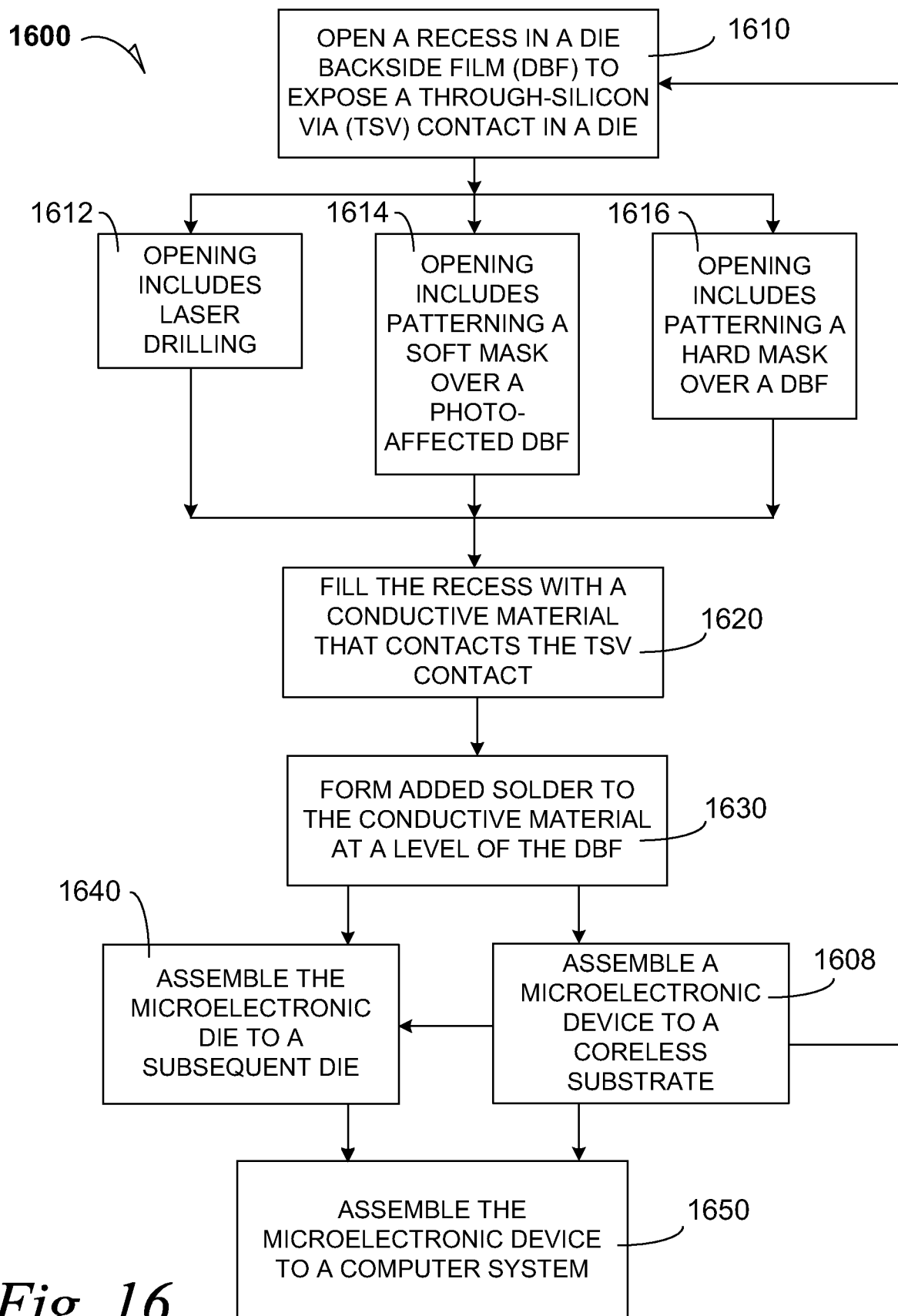


Fig. 11b

*Fig. 12**Fig. 13**Fig. 15**Fig. 14*

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*Fig. 16*

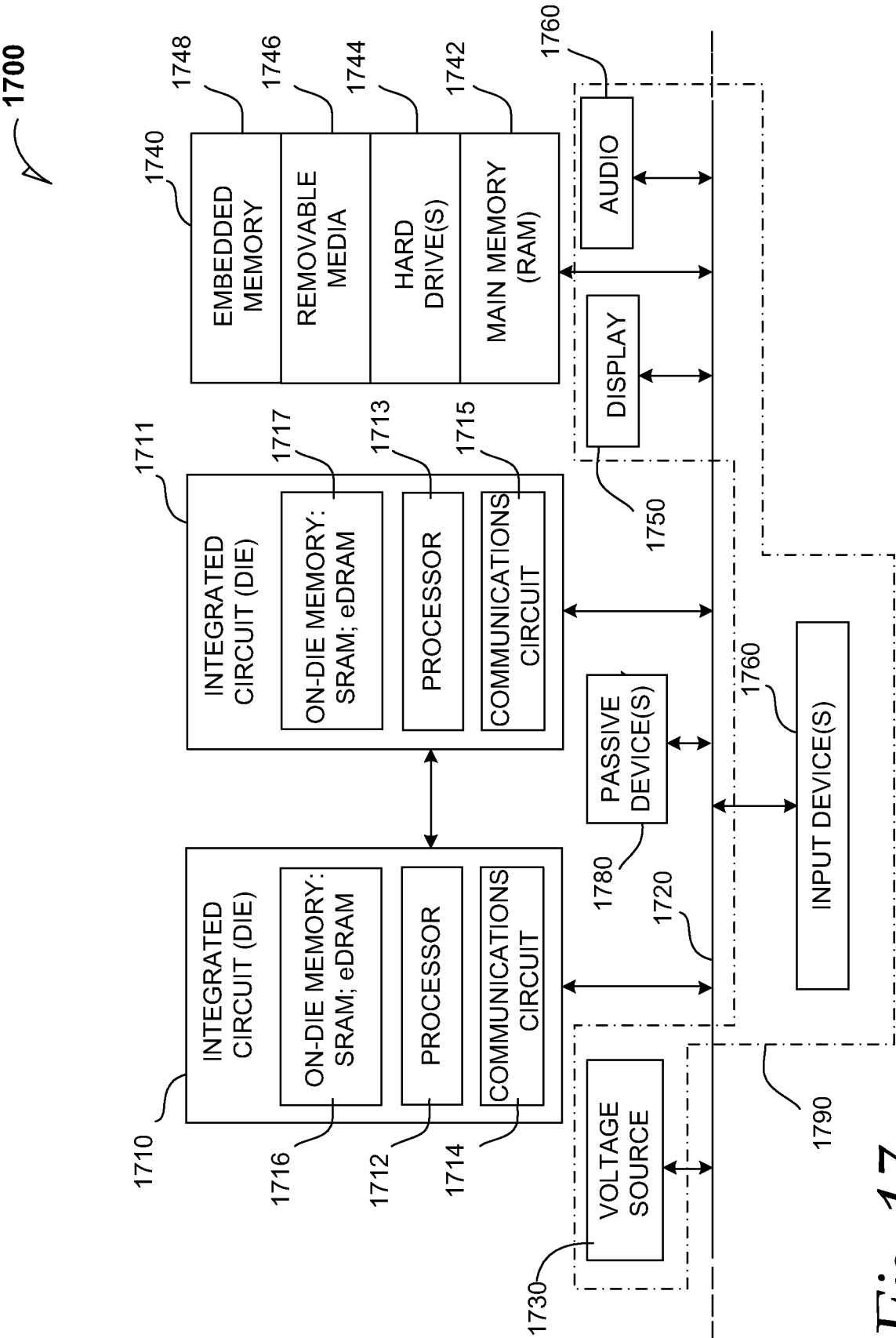


Fig. 17

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/060522**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/60(2006.01)i, H01L 23/48(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/60; H01L 21/70; H01L 21/50; H05K 7/20; H01L 23/522; H01L 23/552; H01L 23/538; H01L 27/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: TSV,package,stack,DBF,backside film,solder,bumpless,coreless

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2010-0187671 A1 (LIN CHUAN-YI et al.) 29 July 2010 See abstract; figures 1-9; paragraphs [0016]-[0038]	1-2, 4-5, 19, 22-23 6, 20-21, 24-25
Y	US 2011-0241186 A1 (NALLA RAVI K. et al.) 06 October 2011 See abstract; figure 1j; paragraphs [0015]-[0016]	6, 20-21, 24-25
A	US 2011-0254124 A1 (NALLA RAVI K. et al.) 20 October 2011 See abstract; figures 1a-1h; paragraphs [0008]-[0016]	1-32
A	US 2009-0008792 A1 (KO CHENG-TA et al.) 08 January 2009 See abstract; figure 4; paragraphs [0044]-[0050]	1-32

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

26 JULY 2012 (26.07.2012)

Date of mailing of the international search report

30 JULY 2012 (30.07.2012)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2011/060522

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010-0187671 A1	29.07.2010	US 8168529 B2	01.05.2012
US 2011-0241186 A1	06.10.2011	WO 2011-126973 A2	13.10.2011
		WO 2011-126973 A3	13.10.2011
US 2011-0254124 A1	20.10.2011	WO 2011-130717 A2	20.10.2011
		WO 2011-130717 A3	20.10.2011
US 2009-0008792 A1	08.01.2009	US 2006-0110853 A1	25.05.2006
		US 2009-0179347 A1	16.07.2009
		US 8048716 B2	01.11.2011