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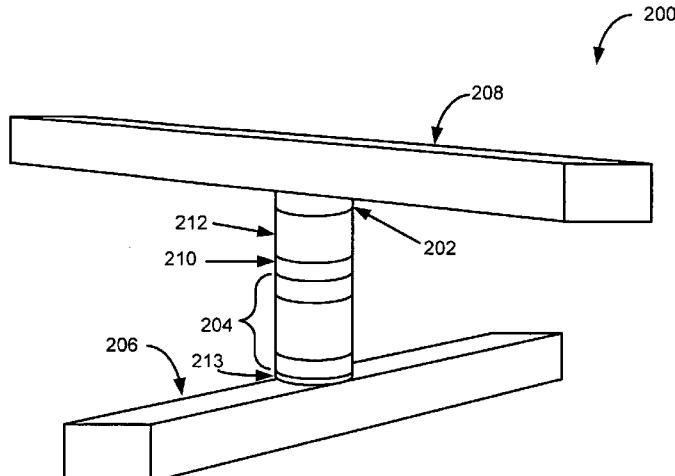


Fig. 2A

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(57) Abstract: In some aspects, a method of forming a memory cell is provided that includes (1) forming a first conductor above a substrate; (2) forming a diode above the first conductor; (3) forming a reversible resistance-switching element above the first conductor using a selective deposition process; and (4) forming a second conductor above the diode and the reversible resistance-switching element. Numerous other aspects are provided.

**MEMORY CELL THAT EMPLOYS A SELECTIVELY DEPOSITED
REVERSIBLE RESISTANCE-SWITCHING
ELEMENT AND METHODS OF FORMING THE SAME**

5 The present application claims priority from U.S. Patent Application Serial No. 11/772,090, filed June 29, 2007, titled "MEMORY CELL THAT EMPLOYS A SELECTIVELY DEPOSITED REVERSIBLE RESISTANCE-SWITCHING ELEMENT AND METHODS OF FORMING THE SAME," (Attorney Docket No. SD-MXD-0333X) and claims priority from U.S. Patent Application Serial No. 11/772,084, filed June 29, 2007, titled "MEMORY CELL THAT EMPLOYS A SELECTIVELY DEPOSITED REVERSIBLE RESISTANCE-SWITCHING ELEMENT AND METHODS OF FORMING THE SAME," (Attorney Docket No. SD-MXD-0333Y), both of which are 10 hereby incorporated by reference herein in their entirety. 15

CROSS REFERENCE TO RELATED APPLICATIONS

The present application is related to the following patent applications, each of which is hereby incorporated by 20 reference herein in its entirety for all purposes:

U.S. Patent Application Serial No. 11/772,081, filed on June 29, 2007 and titled "METHOD TO FORM A REWRITEABLE MEMORY CELL COMPRISING A DIODE AND A RESISTIVITY-SWITCHING GROWN OXIDE" (Docket No. MD-304X).

25 U.S. Patent Application Serial No. 11/772,082, filed on June 29, 2007 and titled "MEMORY CELL THAT EMPLOYS A SELECTIVELY GROWN REVERSIBLE RESISTANCE-SWITCHING ELEMENT AND METHODS OF FORMING THE SAME" (Docket No. MD-335X).

30 U.S. Patent Application Serial No. 11/772,088, filed on June 29, 2007 and titled "MEMORY CELL THAT EMPLOYS A SELECTIVELY GROWN REVERSIBLE RESISTANCE-SWITCHING ELEMENT AND METHODS OF FORMING THE SAME" (Docket No. MD-335Y).

FIELD OF THE INVENTION

The present invention relates to non-volatile memories and more particularly to a memory cell that employs a selectively deposited reversible resistance-switching element and methods of forming the same.

BACKGROUND OF THE INVENTION

Non-volatile memories formed from reversible resistance-switching elements are known. For example, U.S. Patent Application Serial No. 11/125,939, filed May 9, 2005 and titled "REWRITABLE MEMORY CELL COMPRISING A DIODE AND A RESISTANCE-SWITCHING MATERIAL" (hereinafter "the '939 Application"), which is hereby incorporated by reference herein in its entirety, describes a rewriteable non-volatile memory cell that includes a diode coupled in series with a reversible resistivity-switching material such as a metal oxide or metal nitride.

However, fabricating memory devices from rewriteable resistivity-switching materials is difficult; and improved methods of forming memory devices that employ resistivity-switching materials are desirable.

SUMMARY OF THE INVENTION

In a first aspect of the invention, a method of forming a memory cell is provided that includes (1) forming a steering element above a substrate; and (2) forming a reversible resistance-switching element coupled to the steering element using a selective deposition process.

In a second aspect of the invention, a method of forming a memory cell is provided that includes (1) forming a first conductor above a substrate; (2) forming a diode above the first conductor; (3) forming a reversible resistance-switching element above the first conductor using

a selective deposition process; and (4) forming a second conductor above the diode and the reversible resistance-switching element.

In a third aspect of the invention, a method of forming 5 a memory cell is provided that includes (1) forming a first conductor above a substrate; (2) forming a vertical polycrystalline diode above the first conductor; (3) selectively forming a reversible resistance-switching element including a nickel oxide layer above the vertical 10 polycrystalline diode; and (4) forming a second conductor above the vertical polycrystalline diode.

In a fourth aspect of the invention, a method of forming a memory cell is provided that includes (1) forming 15 a thin film transistor having a source region and a drain region; (2) forming a first conductor coupled to the source region or the drain region of the transistor; (3) selectively forming a reversible resistance-switching element including a nickel oxide layer above the first conductor; and (4) forming a second conductor above the 20 reversible resistance-switching element.

In a fifth aspect of the invention, a memory cell is provided that includes (1) a steering element; and (2) a reversible resistance-switching element coupled to the steering element and formed using a selective deposition 25 process.

In a sixth aspect of the invention, a memory cell is provided that includes (1) a first conductor; (2) a second conductor formed above the first conductor; (3) a diode formed between the first and second conductors; and (4) a reversible resistance-switching element formed between the 30 first and second conductors using a selective deposition process.

In a seventh aspect of the invention, a memory cell is provided that includes (1) a first conductor; (2) a vertical polycrystalline diode formed above the first conductor; (3) a reversible resistance-switching element including a nickel oxide layer selectively formed above the vertical polycrystalline diode; and (4) a second conductor formed above the vertical polycrystalline diode.

In an eighth aspect of the invention, a memory cell is provided that includes (1) a thin film transistor having a source region and a drain region; (2) a first conductor coupled to the source region or the drain region; (3) a reversible resistance-switching element including a nickel oxide layer selectively formed above the first conductor; and (4) a second conductor formed above the reversible resistance-switching element.

In a ninth aspect of the invention, a plurality of non-volatile memory cells are provided that include (1) a first plurality of substantially parallel, substantially coplanar conductors extending in a first direction; (2) a plurality of diodes; (3) a plurality of reversible resistance-switching elements; and (4) a second plurality of substantially parallel, substantially coplanar conductors extending in a second direction different from the first direction. In each memory cell, one of the diodes and one of the reversible resistance-switching elements are arranged in series, disposed between one of the first conductors and one of the second conductors. Further, each reversible resistance-switching element is formed using a selective deposition process.

In a tenth aspect of the invention, a monolithic three dimensional memory array is provided that includes a first memory level formed above a substrate. The first memory level includes a plurality of memory cells each having (1) a

steering element; and (2) a reversible resistance-switching element coupled to the steering element and formed using a selective deposition process. The monolithic three dimensional memory array also includes at least a second 5 memory level monolithically formed above the first memory level. Numerous other aspects are provided in accordance with these and other embodiments of the invention.

Other features and aspects of the present invention will become more fully apparent from the following detailed 10 description, the appended claims and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic illustration of an exemplary 15 memory cell provided in accordance with the present invention.

FIG. 2A is a simplified perspective view of a first embodiment of a memory cell provided in accordance with the present invention.

20 FIG. 2B is a simplified perspective view of a portion of a first memory level formed from a plurality of the memory cells of FIG. 2A.

FIG. 2C is a simplified perspective view of a portion 25 of a first exemplary three dimensional memory array provided in accordance with the present invention.

FIG. 2D is a simplified perspective view of a portion of a second exemplary three dimensional memory array provided in accordance with the present invention.

30 FIG. 3 is a cross-sectional view of an exemplary embodiment of the memory cell of FIG. 2A.

FIGS. 4A-D illustrate cross sectional views of a portion of a substrate during fabrication of a single memory level in accordance with the present invention.

FIG. 5 is a cross sectional view of a first alternative memory cell provided in accordance with the present invention.

FIG. 6 is a cross sectional view of a second 5 alternative memory cell provided in accordance with the present invention.

DETAILED DESCRIPTION

As stated above, fabricating memory devices from 10 rewriteable resistivity-switching materials is difficult.

For example, many rewriteable resistivity-switching materials are difficult to etch chemically, increasing fabrication costs and complexity associated with their use in integrated circuits.

15 In accordance with the present invention, difficult-to-etch-chemically rewriteable resistivity-switching materials may be used within a memory cell without being etched. For example, in at least one embodiment, a memory cell is provided that includes a reversible resistivity-switching 20 material formed using a selective deposition process so that the reversible resistivity-switching material may be used within the memory cell without being etched.

In one or more exemplary embodiments, a reversible 25 resistance-switching element may be formed using nickel oxide as a reversible resistivity-switching material. Nickel oxide films have been shown to be suitable for use in memory cells, as described, for example, in the '939 Application, previously incorporated.

Nickel-containing films such as Ni, Ni_xPy , NiO , NiO_x , 30 NiO_xPy , etc., are difficult to etch chemically. In at least one embodiment, through use of a selective deposition process, a nickel oxide layer may be used in a reversible resistance-switching element of a memory cell without the

nickel oxide layer being etched. For example, a reversible resistance-switching element may be formed by employing a deposition process such as electroplating, electroless deposition, or the like, to selectively deposit a nickel-containing layer only on conductive surfaces formed above a substrate. In this manner, only the conductive surfaces on the substrate are patterned and/or etched (prior to deposition of the nickel-containing layer) and not the nickel-containing layer.

10 In some embodiments, nickel oxide may be selectively deposited while in other embodiments, nickel may be selectively deposited and then oxidized to form nickel oxide. In either case, the need for etching of nickel and/or nickel oxide layers may be eliminated and memory cell 15 fabrication significantly simplified.

Other materials may be selectively deposited, and then annealed and/or oxidized if necessary, in accordance with the present invention to form reversible or one-time-programmable resistivity-switching materials for use in 20 memory cells. For example, a layer of Nb, Ta, V, Al, Ti, Co, cobalt-nickel alloy, etc., may be selectively deposited, such as by electroplating, and oxidized to form a reversible resistivity-switching material.

25 **Exemplary Inventive Memory Cell**

FIG. 1 is a schematic illustration of an exemplary memory cell 100 provided in accordance with the present invention. The memory cell 100 includes a reversible resistance-switching element 102 coupled to a steering element 104.

The reversible resistance-switching element 102 includes a reversible resistivity-switching material (not separately shown) having a resistivity that may be

reversibly switched between two or more states. For example, the reversible resistivity-switching material of the element 102 may be in an initial, low-resistivity state upon fabrication that is switchable to a high-resistivity 5 state upon application of a first voltage and/or current. Application of a second voltage and/or current may return the reversible resistivity-switching material to a low-resistivity state. Alternatively, the reversible 10 resistance-switching element 102 may be in an initial, high-resistance state upon fabrication that is reversibly switchable to a low-resistance state upon application of the appropriate voltage(s) and/or current(s). When used in a memory cell, one resistance state may represent a binary "0" while another resistance state may represent a binary "1", 15 although more than two data/resistance states may be used. Numerous reversible resistivity-switching materials and operation of memory cells employing reversible resistance-switching elements are described, for example, the '939 Application, previously incorporated.

20 In at least one embodiment of the invention, the reversible resistance-switching element 102 is formed using a selective deposition process. As will be described further below, use of a selective deposition process allows a reversible resistivity-switching material to be provided 25 within the reversible resistance-switching element 102 without the reversible resistivity-switching material having to be etched. Fabrication of the reversible resistance-switching element 102 thereby is simplified.

30 The steering element 104 may include a thin film transistor, a diode, or another suitable steering element that exhibits non-ohmic conduction by selectively limiting the voltage across and/or the current flow through the reversible resistance-switching element 102. In this

manner, the memory cell 100 may be used as part of a two or three dimensional memory array and data may be written to and/or read from the memory cell 100 without affecting the state of other memory cells in the array.

5 Exemplary embodiments of the memory cell 100, the reversible resistance-switching element 102 and the steering element 104 are described below with reference to FIGS. 2A-6.

10 **First Exemplary Embodiment Of A Memory Cell**

FIG. 2A is a simplified perspective view of a first embodiment of a memory cell 200 provided in accordance with the present invention. With reference to FIG. 2A, the memory cell 200 includes a reversible resistance-switching element 202 coupled in series with a diode 204 between a first conductor 206 and a second conductor 208. In some embodiments, a barrier layer 210 and/or a conductive layer 212 may be formed between the reversible resistance-switching element 202 and the diode 204. For example, the 15 barrier layer 210 may include titanium nitride, tantalum nitride, tungsten nitride, etc., and the conductive layer 212 may include tungsten or another suitable metal layer. As will be described further below, the barrier layer 210 and/or conductive layer 212 may serve as a hard mask during 20 formation of the diode 204. Such a hard mask is described, for example, in U.S. Patent Application Serial No. 25 11/444,936, filed May 13, 2006 and titled "CONDUCTIVE HARD MASK TO PROTECT PATTERNED FEATURES DURING TRENCH ETCH" (hereinafter "the '936 Application") which is hereby 30 incorporated by reference herein in its entirety. An additional barrier layer 213, such as titanium nitride, tantalum nitride, tungsten nitride, etc., also may be formed between the diode 204 and the first conductor 206.

As will be described further below, the reversible resistance-switching element 202 is selectively formed so as to simplify fabrication of the memory cell 200. In at least one embodiment, the reversible resistance-switching element 5 202 includes at least a portion of a nickel oxide layer formed by selectively depositing nickel and then oxidizing the nickel layer. For example, Ni, Ni_xPy or another similar form of nickel may be selectively deposited using electroless deposition, electroplating or a similar 10 selective process, and then oxidized to form nickel oxide (e.g., using rapid thermal oxidation or another oxidation process). In other embodiments, nickel oxide itself may be selectively deposited. For example, an NiO-, NiO_x- or NiO_xPy-containing layer may be selectively deposited above 15 the diode 204 using a selective deposition process and then annealed and/or oxidized (if necessary). These and other embodiments are described further below with reference to FIG. 3. While the reversible resistance-switching element 202 is shown as being positioned above the diode 204 in FIG. 20 2A, it will be understood that in alternative embodiments, the reversible resistance-switching element 202 may be positioned below the diode 204 (as described below, for example, with reference to FIG. 6). In some embodiments, only a portion, such as one or more filaments, of the 25 reversible resistance-switching element 202 may switch and/or be switchable.

The diode 204 may include any suitable diode such as a vertical polycrystalline p-n or p-i-n diode, whether upward pointing with an n-region above a p-region of the diode or 30 downward pointing with a p-region above an n-region of the diode. Exemplary embodiments of the diode 204 are described below with reference to FIG. 3.

The first and/or second conductor 206, 208 may include any suitable conductive material such as tungsten, any appropriate metal, heavily doped semiconductor material, a conductive silicide, a conductive silicide-germanide, a 5 conductive germanide, or the like. In the embodiment of FIG. 2A, the first and second conductors 206, 208 are rail-shaped and extend in different directions (e.g., substantially perpendicular to one another). Other conductor shapes and/or configurations may be used. In some 10 embodiments, barrier layers, adhesion layers, antireflection coatings and/or the like (not shown) may be used with the first and/or second conductors 206 to improve device performance and/or aid in device fabrication.

As stated, other materials may be used to form the 15 reversible resistance-switching element 202. For example, materials such as Nb, Ta, V, Al, Ti, Co, cobalt-nickel alloy, etc., may be similarly selectively deposited over diode 204 (such as over the barrier layer 210 and/or over the conductive layer 212 as shown in Fig. 2A) and, if 20 necessary, oxidized and/or annealed to form the reversible resistance-switching element 202.

FIG. 2B is a simplified perspective view of a portion of a first memory level 214 formed from a plurality of the memory cells 200 of FIG. 2A. For simplicity, the reversible 25 resistance-switching element 202, the diode 204, the barrier layers 210 and 213 and the conductive layer 212 are not separately shown. The memory array 214 is a "cross-point" array including a plurality of bit lines (second conductors 208) and word lines (first conductors 206) to which multiple 30 memory cells are coupled (as shown). Other memory array configurations may be used, as may multiple levels of memory. For example, FIG. 2C is a simplified perspective view of a portion of a monolithic three dimensional array

216 that includes a first memory level 218 positioned below a second memory level 220. In the embodiment of FIG. 2C, each memory level 218, 220 includes a plurality of memory cells 200 in a cross-point array. It will be understood 5 that additional layers (e.g., an interlevel dielectric) may be present between the first and second memory levels 218 and 220, but are not shown in FIG. 2C for simplicity. Other memory array configurations may be used, as may additional levels of memory. In the embodiment of FIG. 2C, all diodes 10 may "point" in the same direction, such as upward or downward depending on whether p-i-n diodes having a p-doped region on the bottom or top of the diode are employed, simplifying diode fabrication.

In some embodiments, the memory levels may be formed, 15 as described, for example, in U.S. Patent No. 6,952,030, "High-density three-dimensional memory cell" which is hereby incorporated by reference herein in its entirety for all purposes. For instance, the upper conductors of a first memory level may be used as the lower conductors of a second 20 memory level that is positioned above the first memory level as shown in FIG. 2D. In such embodiments, the diodes on adjacent memory levels preferably point in opposite directions as described in U.S. Patent Application Serial No. 11/692,151, filed March 27, 2007 and titled "LARGE ARRAY 25 OF UPWARD POINTING P-I-N DIODES HAVING LARGE AND UNIFORM CURRENT" (hereinafter "the '151 Application"), which is hereby incorporated by reference herein in its entirety for all purposes. For example, the diodes of the first memory level 218 may be upward pointing diodes as indicated by 30 arrow A₁ (e.g., with p regions at the bottom of the diodes), while the diodes of the second memory level 220 may be downward pointing diodes as indicated by arrow A₂ (e.g., with n regions at the bottom of the diodes), or vice versa.

A monolithic three dimensional memory array is one in which multiple memory levels are formed above a single substrate, such as a wafer, with no intervening substrates. The layers forming one memory level are deposited or grown 5 directly over the layers of an existing level or levels. In contrast, stacked memories have been constructed by forming memory levels on separate substrates and adhering the memory levels atop each other, as in Leedy, U.S. Patent No. 5,915,167, "Three dimensional structure memory." The 10 substrates may be thinned or removed from the memory levels before bonding, but as the memory levels are initially formed over separate substrates, such memories are not true monolithic three dimensional memory arrays.

FIG. 3 is a cross-sectional view of an exemplary 15 embodiment of the memory cell 200 of FIG. 2A. With reference to FIG. 3, the memory cell 200 includes the reversible resistance-switching element 202, the diode 204 and the first and second conductors 206, 208.

As stated, the diode 204 may be a vertical p-n or p-i-n 20 diode, which may either point upward or downward. In the embodiment of FIG. 2D in which adjacent memory levels share conductors, adjacent memory levels preferably have diodes that point in opposite directions such as downward-pointing p-i-n diodes for a first memory level and upward-pointing p-25 i-n diodes for an adjacent, second memory level (or vice versa).

In some embodiments, the diode 204 may be formed from a polycrystalline semiconductor material such as polysilicon, a polycrystalline silicon-germanium alloy, polygermanium or 30 any other suitable material. For example, the diode 204 may include a heavily doped n+ polysilicon region 302, a lightly doped or an intrinsic (unintentionally doped) polysilicon region 304 above the n+ polysilicon region 302 and a heavily

doped, p+ polysilicon region 306 above the intrinsic region 304. In some embodiments, a thin (e.g., a few hundred angstroms or less) germanium and/or silicon-germanium alloy layer (not shown), with about 10 at% or more of germanium 5 when using a silicon-germanium alloy layer, may be formed on the n+ polysilicon region 302 to prevent and/or reduce dopant migration from the n+ polysilicon region 302 into the intrinsic region 304, as described, for example, in U.S. Patent Application Serial No. 11/298,331, filed December 9, 10 2005 and titled "DEPOSITED SEMICONDUCTOR STRUCTURE TO MINIMIZE N-TYPE DOPANT DIFFUSION AND METHOD OF MAKING" (hereinafter "the '331 Application"), which is hereby incorporated by reference herein in its entirety for all purposes. It will be understood that the locations of the 15 n+ and p+ regions may be reversed. A barrier layer 308, such as titanium nitride, tantalum nitride, tungsten nitride, etc., may be formed between the first conductor 206 and the n+ region 302 (e.g., to prevent and/or reduce migration of metal atoms into the polysilicon regions).

20 When the diode 204 is fabricated from deposited silicon (e.g., amorphous or polycrystalline), a silicide layer 310 may be formed on the diode 204 to place the deposited silicon in a low resistivity state, as fabricated. Such a low resistivity state allows for easier programming of the 25 memory cell 200 as a large voltage is not required to switch the deposited silicon to a low resistivity state. For example, a silicide-forming metal layer 312 such as titanium or cobalt may be deposited on the p+ polysilicon region 306. During a subsequent anneal step (described below) employed 30 to crystallize the deposited silicon that forms the diode 204, the silicide-forming metal layer 312 and the deposited silicon of the diode 204 interact to form the silicide layer

310, consuming all or a portion of the silicide-forming metal layer 312.

As described in U.S. Patent No. 7,176,064, "Memory Cell Comprising a Semiconductor Junction Diode Crystallized 5 Adjacent to a Silicide," which is hereby incorporated by reference herein in its entirety, silicide-forming materials such as titanium and/or cobalt react with deposited silicon during annealing to form a silicide layer. The lattice spacings of titanium silicide and cobalt silicide are close 10 to that of silicon, and it appears that such silicide layers may serve as "crystallization templates" or "seeds" for adjacent deposited silicon as the deposited silicon crystallizes (e.g., the silicide layer 310 enhances the crystalline structure of the silicon diode 204 during 15 annealing). Lower resistivity silicon thereby is provided. Similar results may be achieved for silicon-germanium alloy and/or germanium diodes.

In the embodiment of FIG. 3, the reversible resistance-switching element 202 is formed by a selective deposition 20 process. In some embodiments, the reversible resistance-switching element 202 may be formed over the conductive silicide-forming metal layer 312 (or on a conductive barrier layer formed over the silicide-forming metal layer 312).

(Such layers may be patterned during formation of the diode 25 204 as described below with reference to FIGS. 4A-4D.) However, in other embodiments, a metal hard mask may be formed over the silicide-forming metal layer 312 prior to formation of the resistance-switching element 202. For example, a barrier layer 314 and/or a conductive layer 316 30 may be formed over the silicide-forming metal layer 312. The barrier layer 314 may include titanium nitride, tantalum nitride, tungsten nitride, etc., and the conductive layer 316 may include tungsten or another suitable metal layer.

As will be described further below, the barrier layer 314 and/or conductive layer 316 may serve as a hard mask during formation of the diode 204 and may mitigate any overetching that may occur during formation of the top conductor 208 (as 5 described in the '936 Application, previously incorporated). For example, the barrier layer 314 and conductive layer 316 may be patterned and etched, and then serve as a mask during etching of the diode 204. Etching of the conductive layer 316, barrier layer 314, silicide-forming metal layer 312, 10 diode 204 (p+ polysilicon layer 306, intrinsic layer 304, n+ polysilicon layer 302) and barrier layer 308 creates a pillar structure 318. Dielectric material 320 is deposited on top of and around the pillar structure 318 so as to 15 isolate the pillar structure 318 from other similar pillar structures of other memory cells (not shown) fabricated on a memory level that includes the memory cell 200. A CMP or dielectric etchback step then is performed to planarize the dielectric material 320 and remove the dielectric material from the top of the conductive layer 316.

20 After planarization of the dielectric material 320, the reversible resistance-switching element 202 may be formed over the patterned and etched conductive layer 316 by a selective deposition process. For example, a nickel oxide layer may be selectively formed over the patterned and 25 etched conductive layer 316 by (1) selectively depositing nickel oxide, such as NiO, NiO_x, NiO_xP_y and, if needed, annealing and/or oxidizing the nickel oxide; and/or (2) selectively depositing nickel and then oxidizing the nickel. In either case, because the nickel oxide only deposits on 30 the patterned and etched top surface of the conductive layer 316, the need for etching of nickel and/or nickel oxide layers may be eliminated and memory cell fabrication significantly simplified. Further, any desired thickness of

nickel oxide may be formed. In some embodiments, a nickel oxide layer thickness of about 1000 angstroms or less, and more preferably about 500 angstroms or less, is employed for the reversible resistance-switching element 202 (although 5 other thickness ranges may be used).

In one embodiment, after formation, patterning and etching of the conductive layer 316, an electroless deposition process is employed to selectively deposit nickel or nickel oxide on the conductive layer 316. For example, 10 an aqueous solution may be employed to selectively form nickel or nickel oxide on the conductive layer 316 by submerging the conductive layer 316 in the aqueous solution. The aqueous solution may include, for example, one or more dissolved salts/precursors, complexing agents and/or buffers 15 for regulating pH of the solution. In some embodiments, the aqueous solution may include nickel salts and/or nickel salt hydroxides, such as nickel sulfates, nickel sulfites, nickel phosphates, nickel phosphides, nickel hydroxides, ammonia phosphates, or mixtures of the same. Further exemplary components may include NiSO_4 , NaH_2PO_2 , sodium citrate, 20 $(\text{NH}_4)_2\text{SO}_4$, or the like. It will be understood that either nickel or nickel oxide (or both) may be deposited on the conductive layer 316 depending on the exact components used 25 to form the aqueous solution and/or other process conditions.

Exemplary process conditions include submerging the conductive layer 316 in an aqueous nickel-containing solution for about 1 second to about 5 minutes while the aqueous solution is maintained at a temperature of between 30 about 20 to 85 °C. Additional exemplary aqueous solutions and/or process conditions that may be used to selectively form a nickel or nickel oxide layer are described in N. Takano et al., "Mechanism of the Chemical Deposition of

Nickel on Silicon Wafers in Aqueous Solution", Journal of Electrochemical Society, 146(4) pp. 1407-1411 (1999), which is hereby incorporated by reference herein in its entirety for all purposes. As stated, deposited nickel or nickel oxide may include Ni, Ni_xPy , NiO, NiO_x , NiO_xPy , or other similar materials.

Following formation of nickel or nickel oxide, a thermal oxidation process may be used to either form nickel oxide from selectively deposited nickel or to improve the morphology and/or electrical characteristics of selectively deposited nickel oxide. Exemplary oxidation conditions include rapid thermal oxidation in an oxygen environment such as O_2 for about 20 seconds to 10 minutes at a temperature of about 400 to 800 °C. Other oxidation or annealing processes, oxygen species, times and/or temperatures may be used.

Another suitable selective deposition process that may be used to form a nickel-containing layer on the patterned and etched conductive layer 316 includes conventional nickel electroplating. Any suitable electroplating process may be employed to selectively deposit nickel on the conductive layer 316. Thereafter, the electroplated nickel may be oxidized to form nickel oxide as described above.

As stated, other materials may be used to form the reversible resistance-switching element 202. For example, materials such as Nb, Ta, V, Al, Ti, Co, cobalt-nickel alloy, etc., may be similarly selectively deposited over diode 204 (such as over the barrier layer 210 and/or over the conductive layer 212 as shown in Fig. 2A) and annealed and/or oxidized, if necessary.

Following formation of the reversible resistance-switching element 202, the top conductor 208 is formed. In some embodiments, one or more barrier layers and/or adhesion

layers 322 may be formed over the reversible resistance-switching element 202 prior to deposition of a conductive layer 324. The conductive layer 324 and barrier layer 322 may be patterned and/or etched together to form the top 5 conductor 208. In some embodiments, the top conductor 208 may be formed using a damascene process as described below with reference to FIGS. 4A-4D.

Following formation of the top conductor 208, the memory cell 200 may be annealed to crystallize the deposited 10 semiconductor material of the diode 204 (and/or to form the silicide layer 310). In at least one embodiment, the anneal may be performed for about 10 seconds to about 2 minutes in nitrogen at a temperature of about 600 to 800°C, and more preferably between about 650 and 750°C. Other annealing 15 times, temperatures and/or environments may be used. As stated, the silicide layer 310 may serve as a "crystallization template" or "seed" during annealing for underlying deposited semiconductor material that forms the diode 204. Lower resistivity diode material thereby is 20 provided.

An exemplary process for fabricating a memory cell in accordance with the present invention is described below with reference to FIGS. 4A-D.

25 **Exemplary Fabrication Process For A Memory Cell**

FIGS. 4A-D illustrate cross sectional views of a portion of a substrate 400 during fabrication of a first memory level in accordance with the present invention. As will be described below, the first memory level includes a 30 plurality of memory cells that each include a reversible resistance-switching element formed using a selective deposition process. Additional memory levels may be

fabricated above the first memory level (as described previously with reference to FIGS. 2C-2D).

With reference to FIG. 4A, the substrate 400 is shown as having already undergone several processing steps. The 5 substrate 400 may be any suitable substrate such as a silicon, germanium, silicon-germanium, undoped, doped, bulk, silicon-on-insulator (SOI) or other substrate with or without additional circuitry. For example, the substrate 400 may include one or more n-well or p-well regions (not 10 shown).

Isolation layer 402 is formed above the substrate 400. In some embodiments, the isolation layer 402 may be a layer of silicon dioxide, silicon nitride, silicon oxynitride or any other suitable insulating layer.

15 Following formation of the isolation layer 402, an adhesion layer 404 is formed over the isolation layer 402 (e.g., by physical vapor deposition or another method). For example, the adhesion layer 404 may be about 20 to about 500 angstroms, and preferably about 100 angstroms, of titanium 20 nitride or another suitable adhesion layer such as tantalum nitride, tungsten nitride, combinations of one or more adhesion layers, or the like. Other adhesion layer materials and/or thicknesses may be employed. In some embodiments, the adhesion layer 404 may be optional.

25 After formation of the adhesion layer 404, a conductive layer 406 is deposited over the adhesion layer 404. The conductive layer 406 may include any suitable conductive material such as tungsten or another appropriate metal, heavily doped semiconductor material, a conductive silicide, 30 a conductive silicide-germanide, a conductive germanide, or the like deposited by any suitable method (e.g., chemical vapor deposition (CVD), physical vapor deposition (PVD), etc.). In at least one embodiment, the conductive layer 406

may comprise about 200 to about 2500 angstroms of tungsten. Other conductive layer materials and/or thicknesses may be used.

Following formation of the conductive layer 406, the 5 adhesion layer 404 and the conductive layer 406 are patterned and etched. For example, the adhesion layer 404 and the conductive layer 406 may be patterned and etched using conventional lithography techniques, with a soft or hard mask, and wet or dry etch processing. In at least one 10 embodiment, the adhesion layer 404 and conductive layer 406 are patterned and etched so as to form substantially parallel, substantially co-planar conductors 408 (as shown in FIG. 4A). Exemplary widths for the conductors 408 and/or spacings between the conductors 408 range from about 200 to 15 about 2500 angstroms, although other conductor widths and/or spacings may be used.

After the conductors 408 have been formed, a dielectric layer 410 is formed over the substrate 400 so as to fill the voids between the conductors 408. For example, 20 approximately 3000-7000 angstroms of silicon dioxide may be deposited on the substrate 400 and planarized using chemical mechanical polishing or an etchback process to form a planar surface 412. The planar surface 412 includes exposed top surfaces of the conductors 408 separated by dielectric 25 material (as shown). Other dielectric materials such as silicon nitride, silicon oxynitride, low K dielectrics, etc., and/or other dielectric layer thicknesses may be used. Exemplary low K dielectrics include carbon doped oxides, silicon carbon layers, or the like.

30 In other embodiments of the invention, the conductors 408 may be formed using a damascene process in which the dielectric layer 410 is formed and patterned to create openings or voids for the conductors 408. The openings or

voids then may be filled with the adhesion layer 404 and the conductive layer 406 (and/or a conductive seed, conductive fill and/or barrier layer if needed). The adhesion layer 404 and conductive layer 406 then may be planarized to form 5 the planar surface 412. In such an embodiment, the adhesion layer 404 will line the bottom and sidewalls of each opening or void.

Following planarization, the diode structures of each memory cell are formed. With reference to FIG. 4B, a 10 barrier layer 414 is formed over the planarized top surface 412 of the substrate 400. The barrier layer 414 may be about 20 to about 500 angstroms, and preferably about 100 angstroms, of titanium nitride or another suitable barrier layer such as tantalum nitride, tungsten nitride, 15 combinations of one or more barrier layers, barrier layers in combination with other layers such as titanium/titanium nitride, tantalum/tantalum nitride or tungsten/tungsten nitride stacks, or the like. Other barrier layer materials and/or thicknesses may be employed.

20 After deposition of the barrier layer 414, deposition of the semiconductor material used to form the diode of each memory cell begins (e.g., diode 204 in FIGS. 2A-3). Each diode may be a vertical p-n or p-i-n diode as previously described. In some embodiments, each diode is formed from a 25 polycrystalline semiconductor material such as polysilicon, a polycrystalline silicon-germanium alloy, polygermanium or any other suitable material. For convenience, formation of a polysilicon, downward-pointing diode is described herein. It will be understood that other materials and/or diode 30 configurations may be used.

With reference to FIG. 4B, following formation of the barrier layer 414, a heavily doped n+ silicon layer 416 is deposited on the barrier layer 414. In some embodiments,

the n+ silicon layer 416 is in an amorphous state as deposited. In other embodiments, the n+ silicon layer 416 is in a polycrystalline state as deposited. CVD or another suitable process may be employed to deposit the n+ silicon layer 416. In at least one embodiment, the n+ silicon layer 416 may be formed, for example, from about 100 to about 1000 angstroms, preferably about 100 angstroms, of phosphorus or arsenic doped silicon having a doping concentration of about 10^{21} cm^{-3} . Other layer thicknesses, doping types and/or 10 doping concentrations may be used. The n+ silicon layer 416 may be doped in situ, for example, by flowing a donor gas during deposition. Other doping methods may be used (e.g., implantation).

After deposition of the n+ silicon layer 416, a lightly doped, intrinsic and/or unintentionally doped silicon layer 418 is formed over the n+ silicon layer 416. In some embodiments, the intrinsic silicon layer 418 is in an amorphous state as deposited. In other embodiments, the intrinsic silicon layer 418 is in a polycrystalline state as deposited. CVD or another suitable deposition method may be employed to deposit the intrinsic silicon layer 418. In at least one embodiment, the intrinsic silicon layer 418 may be about 500 to about 4800 angstroms, preferably about 2500 angstroms, in thickness. Other intrinsic layer thicknesses 25 may be used.

A thin (e.g., a few hundred angstroms or less) germanium and/or silicon-germanium alloy layer (not shown) may be formed on the n+ silicon layer 416 prior to deposition of the intrinsic silicon layer 418 to prevent 30 and/or reduce dopant migration from the n+ silicon layer 416 into the intrinsic silicon layer 418 (as described in the '331 Application, previously incorporated).

Heavily doped, p-type silicon is either deposited and doped by ion implantation or is doped in situ during deposition to form a p+ silicon layer 420. For example, a blanket p+ implant may be employed to implant boron a 5 predetermined depth within the intrinsic silicon layer 418. Exemplary implantable molecular ions include BF₂, BF₃, B and the like. In some embodiments, an implant dose of about 1-5x10¹⁵ ions/cm² may be employed. Other implant species and/or doses may be used. Further, in some embodiments, a 10 diffusion process may be employed. In at least one embodiment, the resultant p+ silicon layer 420 has a thickness of about 100-700 angstroms, although other p+ silicon layer sizes may be used.

Following formation of the p+ silicon layer 420, a 15 silicide-forming metal layer 422 is deposited over the p+ silicon layer 420. Exemplary silicide-forming metals include sputter or otherwise deposited titanium or cobalt. In some embodiments, the silicide-forming metal layer 422 has a thickness of about 10 to about 200 angstroms, 20 preferably about 20 to about 50 angstroms and more preferably about 20 angstroms. Other silicide-forming metal layer materials and/or thicknesses may be used.

A barrier layer 424 is deposited over the silicide-forming metal layer 422. The barrier layer 424 may be about 25 20 to about 500 angstroms, and preferably about 100 angstroms, of titanium nitride or another suitable barrier layer such as tantalum nitride, tungsten nitride, combinations of one or more barrier layers, barrier layers in combination with other layers such as titanium/titanium 30 nitride, tantalum/tantalum nitride or tungsten/tungsten nitride stacks, or the like. Other barrier layer materials and/or thicknesses may be employed.

Following formation of the barrier layer 424, a conductive layer 426 is formed over the barrier layer 424. The conductive layer 426 may be about 50 to about 1000 angstroms, and preferably about 500 angstroms of conductive 5 material such as tungsten or another suitable metal.

The barrier layer 414, silicon regions 416, 418, and 420, silicide-forming metal layer 422, barrier layer 424 and conductive layer 426 are then patterned and etched into pillars 428. For example, initially, the conductive layer 10 426 and barrier layer 424 are etched. The etch continues, etching silicide-forming metal layer 422, silicon regions 420, 418, and 416 and barrier layer 414. Conductive layer 426 and barrier layer 414 serve as a hard mask during the silicon etch. A hard mask is an etched layer which serves 15 to pattern the etch of an underlying layer; if all of the photoresist present on the conductive layer 426 has been consumed, the hard mask can provide the pattern in its stead. In this manner, the pillars 428 are formed in a single photolithographic step. Conventional lithography 20 techniques, and wet or dry etch processing may be employed to form the pillars 428. Each pillar 428 includes a p-i-n, downward-pointing diode 430. Upward-pointing p-i-n diodes may be similarly formed.

After the pillars 428 have been formed, a dielectric 25 layer 432 is deposited over the pillars 428 to fill the voids between the pillars 428. For example, approximately 200 - 7000 angstroms of silicon dioxide may be deposited and planarized using chemical mechanical polishing or an etchback process to form a planar surface 434. The planar 30 surface 434 includes exposed top surfaces of the pillars 428 separated by dielectric material 432 (as shown). Other dielectric materials such as silicon nitride, silicon oxynitride, low K dielectrics, etc., and/or other dielectric

layer thicknesses may be used. Exemplary low K dielectrics include carbon doped oxides, silicon carbon layers, or the like.

After formation of the planar surface 434, a reversible 5 resistance-switching element 436 (FIG. 4C) is selectively formed over each pillar 428. For example, a nickel oxide layer may be selectively formed over each conductive pillar 428 by selectively depositing (1) nickel oxide; and/or (2) selectively depositing nickel and then oxidizing the nickel. 10 In either case, the need for etching of nickel and/or nickel oxide layers may be eliminated and memory cell fabrication significantly simplified. As described previously, any suitable method for selectively depositing nickel or a nickel oxide may be used such as electroless deposition, 15 electroplating or the like. In at least one embodiment, the reversible resistance-switching element 436 formed over each conductive pillar 428 includes a nickel oxide layer having a thickness of about 1000 angstroms or less, and more preferably a thickness of about 500 angstroms or less. 20 Other nickel oxide thicknesses may be employed. The nickel oxide layer may include, for example, NiO , NiO_x , and NiO_xP_y , or other similar materials. Other materials such as Nb, Ta, V, Al, Ti, Co, cobalt-nickel alloy, etc., may be similarly 25 selectively deposited, oxidized and/or annealed to form a selectively deposited, reversible resistance-switching element over each pillar 428.

With reference to FIG. 4D, following formation of the reversible resistance-switching elements 436, a second set of conductors 438 maybe formed above the pillars 428 in a 30 manner similar to the formation of the bottom set of conductors 408. For example, as shown in FIG. 4D, in some embodiments, one or more barrier layers and/or adhesion layers 440 may be deposited over the reversible resistance-

switching elements 436 prior to deposition of a conductive layer 442 used to form the upper, second set of conductors 438.

The conductive layer 442 may be formed from any suitable conductive material such as tungsten, another suitable metal, heavily doped semiconductor material, a conductive silicide, a conductive silicide-germanide, a conductive germanide, or the like deposited by any suitable method (e.g., CVD, PVD, etc.). Other conductive layer materials may be used. Barrier layers and/or adhesion layers 440 may include titanium nitride or another suitable layer such as tantalum nitride, tungsten nitride, combinations of one or more layers, or any other suitable material(s). The deposited conductive layer 442 and barrier and/or adhesion layer 440, may be patterned and etched to form the second set of conductors 438. In at least one embodiment, the upper conductors 438 are substantially parallel, substantially coplanar conductors that extend in a different direction than the lower conductors 408.

In other embodiments of the invention, the upper conductors 438 may be formed using a damascene process in which a dielectric layer is formed and patterned to create openings or voids for the conductors 438. As described in the '936 Application, the conductive layer 426 and barrier layer 424 may mitigate the affects of overetching of such a dielectric layer during formation of the openings or voids for the upper conductors 438, preventing accidental shorting of the diodes 430.

The openings or voids may be filled with the adhesion layer 440 and the conductive layer 442 (and/or a conductive seed, conductive fill and/or barrier layer if needed). The adhesion layer 440 and conductive layer 442 then may be planarized to form a planar surface.

Following formation of the upper conductors 438, the structure may be annealed to crystallize the deposited semiconductor material of the diodes 430 (and/or to form silicide regions by reaction of the silicide-forming metal 5 layer 422 with p+ region 420). In at least one embodiment, the anneal may be performed for about 10 seconds to about 2 minutes in nitrogen at a temperature of about 600 to 800°C, and more preferably between about 650 and 750°C. Other annealing times, temperatures and/or environments may be 10 used. The silicide regions formed as each silicide-forming metal layer region 422 and p+ region 420 react may serve as "crystallization templates" or "seeds" during annealing for underlying deposited semiconductor material that forms the diodes 430 (e.g., changing any amorphous semiconductor 15 material to polycrystalline semiconductor material and/or improving overall crystalline properties of the diodes 430). Lower resistivity diode material thereby is provided.

First Alternative Exemplary Memory Cell

20 FIG. 5 is a cross sectional view of an exemplary memory cell 500 provided in accordance with the present invention. The memory cell 500 includes a thin film transistor (TFT), such as a thin film, metal oxide semiconductor field effect transistor (MOSFET) 502 coupled to a reversible resistance-25 switching element 504 formed above a substrate 505. For example, the MOSFET 502 may be an n-channel or a p-channel thin film MOSFET formed on any suitable substrate. In the embodiment shown, an insulating region 506 such as silicon dioxide, silicon nitride, oxynitride, etc., is formed above 30 the substrate 505 and a deposited semiconductor region 507 such as deposited silicon, germanium, silicon-germanium, etc., is formed above the insulating region 506. The thin film MOSFET 502 is formed within the deposited semiconductor

region 507 and is insulated from the substrate 505 by the insulating region 506.

The MOSFET 502 includes source/drain regions 508, 510 and channel region 512, as well as gate dielectric layer 514, gate electrode 516 and spacers 518a-b. In at least one embodiment, the source/drain regions 508, 510 may be doped p-type and the channel region 512 may be doped n-type, while in other embodiments the source/drain regions 508, 510 may be doped n-type and the channel region 512 may be doped p-type. Any other MOSFET configuration or any suitable fabrication techniques may be employed for the thin film MOSFET 502. In some embodiments, the MOSFET 502 may be electrically isolated by isolation regions (not shown) formed using an STI, LOCOS or other similar process.

15 Alternatively, gate, source and/or drain regions of the MOSFET 502 may be shared with other transistors (not shown) formed on the substrate 505.

The reversible resistance-switching element 504 includes a reversible resistivity-switching material 522 formed over a conductive plug 526. In at least one embodiment, the reversible resistivity-switching material 522 is formed using a selective deposition process as previously described with reference to the embodiments of FIGS. 1-4D. For example, a nickel oxide layer may be selectively formed over the conductive plug 526 by selectively depositing (1) nickel oxide; and/or (2) selectively deposited nickel and then oxidizing the nickel. Exemplary selective deposition processes include electroless deposition, electroplating, or the like. Other materials may be selectively deposited, oxidized and/or annealed in accordance with the present invention to form reversible resistivity-switching materials for use in memory cell 500 (e.g., Nb, Ta, V, Al, Ti, Co, cobalt-nickel alloy, etc.).

As shown in FIG. 5, the reversible resistance-switching element 504 is coupled to the source/drain region 510 of the MOSFET 502 by the first conductive plug 526 and to a first metal level (M1) line 528 by a second conductive plug 530 5 (which extend through a dielectric layer 532). Likewise, a third conductive plug 534 couples the source/drain region 508 of the MOSFET 502 to an M1 line 536. The conductive plugs and/or lines may be formed from any suitable materials (without or without barriers layers) such as tungsten, 10 another metal, heavily doped semiconductor material, a conductive silicide, a conductive silicide-germanide, a conductive germanide, or the like. Note that when the MOSFET 502 is an n-channel device, the region 508 serves as the drain and the region 510 serves as the source for the 15 MOSFET 502; and when the MOSFET 502 is an p-channel device, the region 508 serves as the source and the region 510 serves as the drain for the MOSFET 502. The dielectric layer 532 may include any suitable dielectric such as silicon dioxide, silicon nitride, silicon oxynitride, low K 20 dielectrics, etc.

In the memory cell 500, the thin film MOSFET 502 operates as a steering element in a manner similar to that of the diodes employed in the memory cells of FIGS. 2A-4D, selectively limiting the voltage applied across and/or the 25 current flow through the reversible resistance-switching element 504.

In at least one embodiment, the reversible resistance-switching element 504 includes a nickel oxide layer having a thickness of about 1000 angstroms or less, and more 30 preferably a thickness of about 500 angstroms or less. Other nickel oxide thicknesses may be employed.

Second Alternative Memory Cell

FIG. 6 is a cross sectional view of an exemplary memory cell 600 provided in accordance with the present invention. The memory cell 600 is similar to the memory cell 200 of FIG. 3, with the exception that the reversible resistance-switching element 202 is formed below the diode 204.

Specifically, as shown in FIG. 6, the reversible resistance-switching element 202 is formed by selectively depositing a conductive material 602 on the patterned and etched bottom conductor 206. The conductive material 602 then may be annealed and/or oxidized if necessary, in accordance with the present invention, to form a reversible resistivity-switching material 604 for use in memory cell 600. For example, the conductive material 602 may include a layer of Ni, Ni_xPy , NiO , NiO_x , NiO_xPy , Nb, Ta, V, Al, Ti, Co, cobalt-nickel alloy, etc., selectively deposited, such as by electroplating, and oxidized to form the reversible resistivity-switching material layer 604. A portion of the reversible resistivity-switching material layer 604 that vertically overlaps and/or aligns with the diode 204 may serve as the reversible resistance-switching element 202 between the diode 204 and the first conductor 206 of the memory cell 600. In some embodiments, only a portion, such as one or more filaments, of the reversible resistance-switching element 202 may switch and/or be switchable.

Because the layer 604 is selectively deposited on the already patterned and etched bottom conductor 206, the reversible resistivity-switching material layer 604 does not require etching.

The foregoing description discloses only exemplary embodiments of the invention. Modifications of the above disclosed apparatus and methods which fall within the scope of the invention will be readily apparent to those of

ordinary skill in the art. For instance, although the present invention has been described primarily with regard to selective deposition of nickel and nickel oxide, it will be understood that other materials may be selectively deposited for use in a reversible resistance-switching element such as Ta, Nb, Al, V, Co, cobalt-nickel alloy, Ti, etc., forming, for example, Ta_2O_5 , Nb_2O_5 , Al_2O_3 , V_2O_5 , CoO , $(Co_xNi_y)O_z$, and TiO_2 .

Accordingly, while the present invention has been disclosed in connection with exemplary embodiments thereof, it should be understood that other embodiments may fall within the spirit and scope of the invention, as defined by the following claims.

THE INVENTION CLAIMED IS:

1. A method of forming a memory cell comprising:
forming a steering element above a substrate;

5 and

forming a reversible resistance-switching
element coupled to the steering element using a selective
deposition process.

10 2. The method of claim 1 wherein forming the
steering element comprises forming a diode.

3. The method of claim 1 wherein forming the
steering element comprises forming a polycrystalline diode.

15 4. The method of claim 1 wherein forming the
steering element comprises forming a vertical
polycrystalline diode.

20 5. The method of claim 1 wherein forming the
steering element comprises forming a vertical
polycrystalline diode having polycrystalline material that
is in a low-resistivity state.

25 6. The method of claim 1 wherein forming the
steering element comprises forming a p-n diode or a p-i-n
diode.

30 7. The method of claim 1 wherein forming the
steering element comprises forming a thin film transistor.

8. The method of claim 1 wherein forming the steering element comprises forming a thin film, metal oxide semiconductor field effect transistor (MOSFET).

5 9. The method of claim 1 wherein forming the reversible resistance-switching element comprises forming at least one of NiO, NiO_x, and NiO_xPy.

10 10. The method of claim 9 wherein forming the reversible resistance-switching element comprises forming a reversible resistance-switching element having an oxide thickness of about 1000 angstroms or less.

15 11. The method of claim 10 wherein forming the reversible resistance-switching element comprises forming a reversible resistance-switching element having an oxide thickness of about 500 angstroms or less.

20 12. The method of claim 1 wherein forming the reversible resistance-switching element comprises selectively forming a nickel-containing layer.

25 13. The method of claim 12 wherein forming the nickel-containing layer comprises selectively forming a NiO-, NiO_x- or NiO_xPy-containing layer.

14. The method of claim 13 further comprising annealing or oxidizing the NiO-, NiO_x- or NiO_xPy-containing layer.

30

15. The method of claim 12 wherein forming the nickel-containing layer comprises selectively forming a Ni

or Ni_xPy layer and further comprising oxidizing the Ni or Ni_xPy layer.

16. The method of claim 13 wherein forming the
5 nickel-containing layer comprises electrolessly depositing
the nickel-containing layer.

17. The method of claim 13 wherein forming the
nickel-containing layer comprises forming the nickel-
10 containing layer using electroplating.

18. The method of claim 1 further comprising
coupling the steering element and reversible resistance-
switching element in series.

15

19. A memory cell formed using the method of
claim 1.

20. A memory cell formed using the method of
20 claim 9.

21. A method of forming a memory cell comprising:
forming a first conductor above a substrate;
forming a diode above the first conductor;
25 forming a reversible resistance-switching
element above the first conductor using a selective
deposition process; and
forming a second conductor above the diode
and the reversible resistance-switching element.

30

22. The method of claim 21 wherein forming the
diode comprises forming a vertical polycrystalline diode.

23. The method of claim 22 further comprising forming a silicide, silicide-germanide or germanide region in contact with polycrystalline material of the vertical polycrystalline diode so that the polycrystalline material 5 is in a low-resistivity state.

24. The method of claim 21 wherein forming the reversible resistance-switching element comprises forming a reversible resistance-switching element having an oxide 10 thickness of about 500 angstroms or less.

25. The method of claim 21 wherein forming the reversible resistance-switching element comprises selectively forming a nickel-containing layer.

15

26. The method of claim 25 wherein forming the nickel-containing layer comprises selectively forming an NiO_- , NiO_x- or $\text{NiO}_x\text{Py}-$ containing layer.

20

27. The method of claim 25 wherein forming the nickel-containing layer comprises selectively forming an Ni or Ni_xPy layer and further comprising oxidizing the Ni or Ni_xPy layer.

25

28. A memory cell formed using the method of claim 21.

29. A memory cell formed using the method of claim 24.

30

30. A method of forming a memory cell comprising: forming a first conductor above a substrate;

forming a vertical polycrystalline diode above the first conductor;

selectively forming a reversible resistance-switching element including a nickel oxide layer above the 5 vertical polycrystalline diode; and

forming a second conductor above the vertical polycrystalline diode.

31. The method of claim 30 further comprising 10 forming a silicide, silicide-germanide or germanide region in contact with polycrystalline material of the vertical polycrystalline diode so that the polycrystalline material is in a low-resistivity state.

15 32. The method of claim 30 wherein selectively forming the reversible resistance-switching element comprises forming a reversible resistance-switching element having an oxide thickness of about 500 angstroms or less.

20 33. The method of claim 30 wherein forming the vertical polycrystalline diode comprises forming a vertical polysilicon diode.

25 34. A memory cell formed using the method of claim 30.

35. A method of forming a memory cell comprising: 30 forming a thin film transistor having a source region and a drain region above a substrate; forming a first conductor coupled to the source region or the drain region of the transistor;

selectively forming a reversible resistance-switching element including a nickel oxide layer above the first conductor; and

5 forming a second conductor above the reversible resistance-switching element.

36. The method of claim 35 wherein forming the thin film transistor comprises forming an n-channel or a p-channel thin film, metal oxide semiconductor field effect 10 transistor.

37. The method of claim 35 wherein selectively forming the reversible resistance-switching element comprises forming a reversible resistance-switching element 15 having an oxide thickness of about 500 angstroms or less.

38. A memory cell formed using the method of claim 35.

20 39. The method of claim 1 wherein forming the reversible resistance-switching element comprises forming at least one of Ta_2O_5 , Nb_2O_5 , Al_2O_3 , V_2O_5 , CoO , $(Co_xNi_y)O_z$, and TiO_2 .

25 40. A memory cell comprising:
a steering element; and
a reversible resistance-switching element
coupled to the steering element and formed using a selective deposition process.

30 41. The memory cell of claim 40 wherein the steering element comprises a diode.

42. The memory cell of claim 41 wherein the diode comprises a vertical polycrystalline diode.

5 43. The memory cell of claim 42 wherein the vertical polycrystalline diode includes polycrystalline material that is in a low-resistivity state.

44. The memory cell of claim 41 wherein the diode comprises a p-n diode or a p-i-n diode.

10

45. The memory cell of claim 40 wherein the steering element comprises a thin film transistor.

15 46. The memory cell of claim 45 wherein the thin film transistor comprises a metal oxide semiconductor field effect transistor (MOSFET).

20 47. The memory cell of claim 40 wherein the reversible resistance-switching element comprises at least one of NiO, NiO_x and NiO_xPy.

25

48. The memory cell of claim 47 wherein the reversible resistance-switching element has an oxide thickness of about 1000 angstroms or less.

30

49. The memory cell of claim 47 wherein the reversible resistance-switching element has an oxide thickness of about 500 angstroms or less.

50. The memory cell of claim 40 further comprising a nickel-containing layer and wherein the reversible resistance-switching element is formed by oxidizing or annealing the nickel-containing layer.

51. The memory cell of claim 50 wherein the nickel-containing layer is selectively deposited using an electroless deposition or electroplating process.

5

52. The memory cell of claim 40 wherein the steering element and reversible resistance-switching element are coupled in series.

10

53. A memory cell comprising:
a first conductor;
a second conductor formed above the first conductor;
a diode formed between the first and second conductors; and
a reversible resistance-switching element formed between the first and second conductors using a selective deposition process.

15

54. The memory cell of claim 53 wherein the diode comprises a vertical polycrystalline diode.

20

55. The memory cell of claim 54 further comprising a silicide, silicide-germanide or germanide region in contact with polycrystalline material of the vertical polycrystalline diode so that the polycrystalline material is in a low-resistivity state.

30

56. The memory cell of claim 53 wherein the reversible resistance-switching element comprises at least one of NiO, NiO_x and NiO_xP_y.

57. The memory cell of claim 40 further comprising a nickel-containing layer and wherein the reversible resistance-switching element is formed by oxidizing or annealing the nickel-containing layer.

5

58. The memory cell of claim 53 wherein the nickel-containing layer is selectively deposited using an electroless deposition or electroplating process.

10

59. A memory cell comprising:
a first conductor;
a vertical polycrystalline diode formed above the first conductor;
a reversible resistance-switching element including a nickel oxide layer selectively formed above the vertical polycrystalline diode; and
a second conductor formed above the vertical polycrystalline diode.

20

60. The memory cell of claim 59 further comprising a silicide, silicide-germanide or germanide region in contact with polycrystalline material of the vertical polycrystalline diode so that the polycrystalline material is in a low-resistivity state.

25

61. The memory cell of claim 59 wherein the reversible resistance-switching element comprises at least one of NiO , NiO_x and NiO_xPy .

30

62. The memory cell of claim 61 wherein the reversible resistance-switching element has an oxide thickness of about 1000 angstroms or less.

63. The memory cell of claim 61 wherein the reversible resistance-switching element has an oxide thickness of about 500 angstroms or less.

5 64. A memory cell comprising:
a thin film transistor having a source region and a drain region;
a first conductor coupled to the source region or the drain region;
10 a reversible resistance-switching element including a nickel oxide layer selectively formed above the first conductor; and
a second conductor formed above the reversible resistance-switching element.

15 65. The memory cell of claim 64 wherein the thin film transistor comprises an n-channel or a p-channel metal oxide semiconductor field effect transistor.

20 66. The memory cell of claim 64 wherein the reversible resistance-switching element comprises at least one of NiO, NiO_x and NiO_xPy.

25 67. The memory cell of claim 66 wherein the reversible resistance-switching element has an oxide thickness of about 1000 angstroms or less.

30 68. The memory cell of claim 66 wherein the reversible resistance-switching element has an oxide thickness of about 500 angstroms or less.

69. A plurality of nonvolatile memory cells comprising:

a first plurality of substantially parallel, substantially coplanar conductors extending in a first direction;

a plurality of diodes;

5 a plurality of reversible resistance-switching elements; and

a second plurality of substantially parallel, substantially coplanar conductors extending in a second direction different from the first direction;

10 wherein, in each memory cell, one of the diodes and one of the reversible resistance-switching elements are arranged in series, disposed between one of the first conductors and one of the second conductors; and

15 wherein each reversible resistance-switching element is formed using a selective deposition process.

70. The plurality of memory cells of claim 69 wherein each diode is a vertical polycrystalline diode.

20 71. The plurality of memory cells of claim 70 further comprising a silicide, silicide-germanide or germanide region in contact with polycrystalline material of each vertical polycrystalline diode so that the polycrystalline material is in a low-resistivity state.

25 72. The plurality of memory cells of claim 69 wherein each reversible resistance-switching element comprises at least one of NiO, NiO_x and NiO_xP_y.

30 73. A monolithic three dimensional memory array comprising:

a first memory level formed above a substrate, the first memory level comprising:

a plurality of memory cells, wherein each memory cell of the first memory level comprises:
a steering element; and
a reversible resistance-switching element coupled to the steering element and formed using a selective deposition process; and
at least a second memory level monolithically formed above the first memory level.

10 74. The monolithic three dimensional memory array
of claim 73 wherein each steering element comprises a
vertical polycrystalline diode.

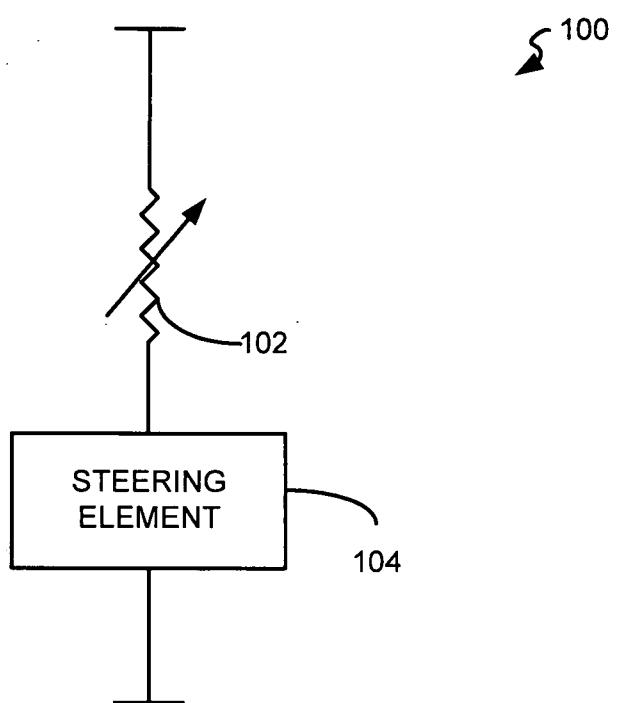
75. The monolithic three dimensional memory array
15 of claim 74 wherein each vertical polycrystalline diode
comprises a vertical polysilicon diode.

76. The monolithic three dimensional memory array of claim 73 wherein each reversible resistance-switching element comprises at least one of NiO, NiO_x and NiO_xPy .

77. The monolithic three dimensional memory array of claim 73 wherein a respective steering element and reversible resistance-switching element of each memory cell are coupled in series.

78. The memory cell of claim 40 wherein the reversible resistance-switching element comprises at least one of Ta_2O_5 , Nb_2O_5 , Al_2O_3 , V_2O_5 , CoO , $(Co_xNi_y)O_z$, and TiO_2 .

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**FIG. 1**

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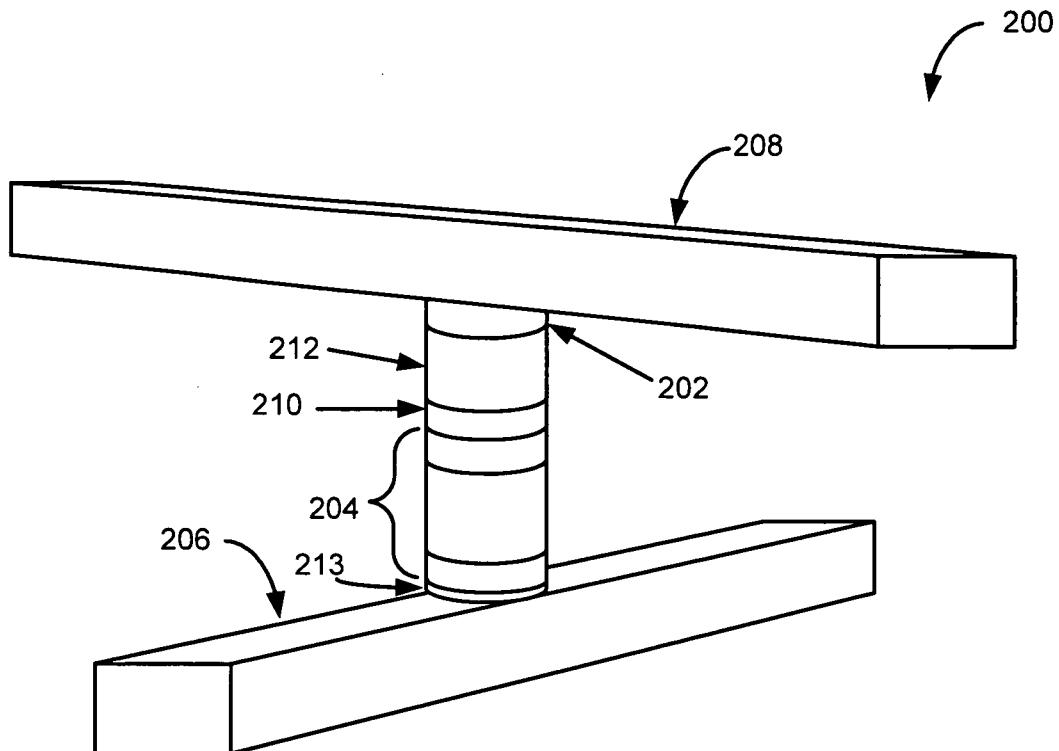


Fig. 2A

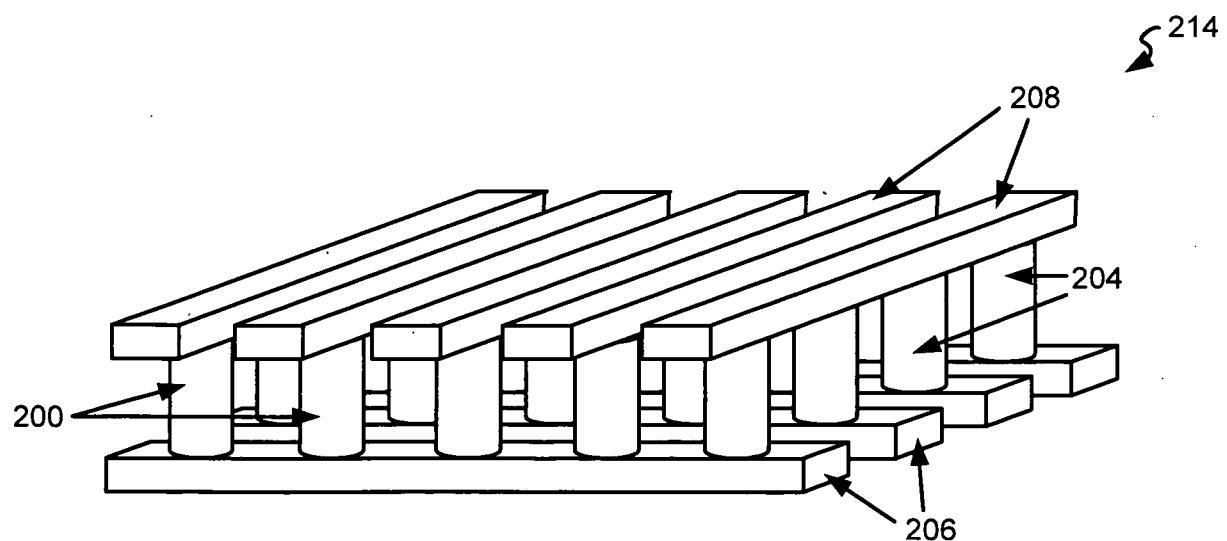


Fig. 2B

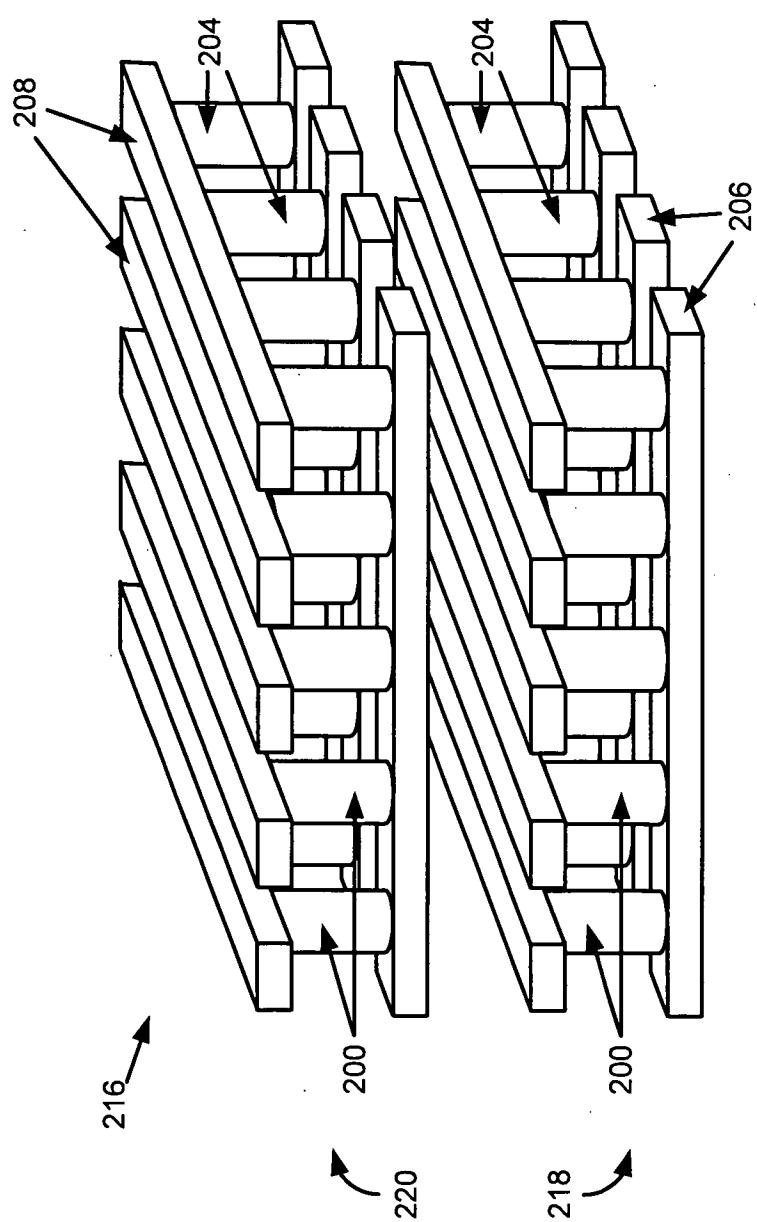


Fig. 2C

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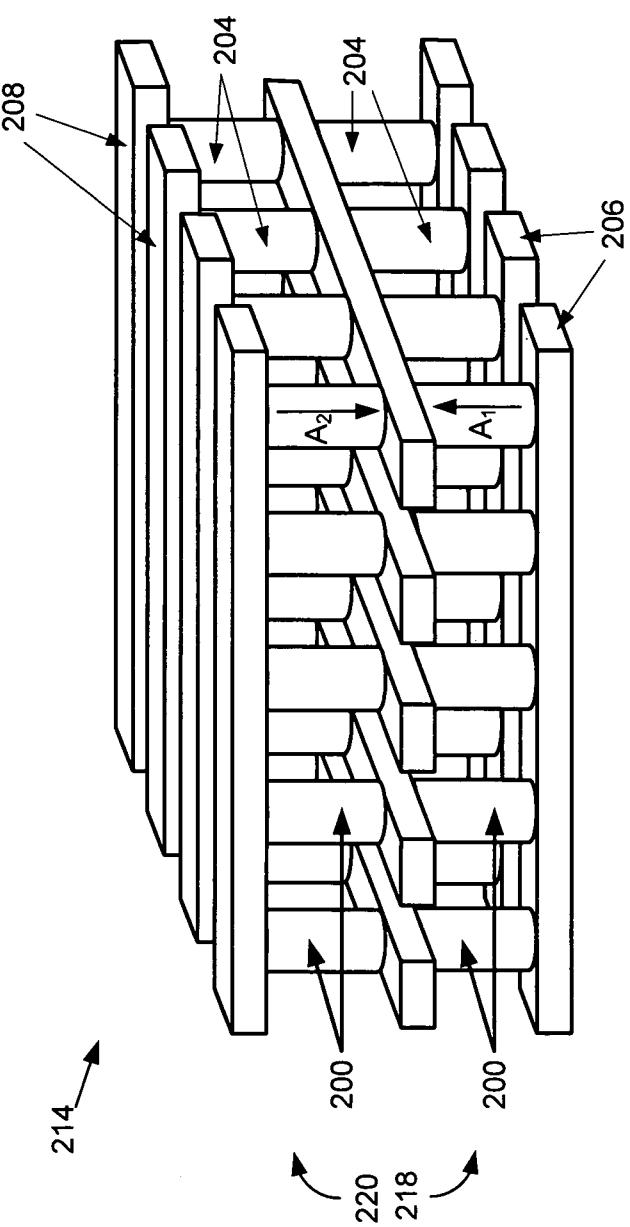


Fig. 2D

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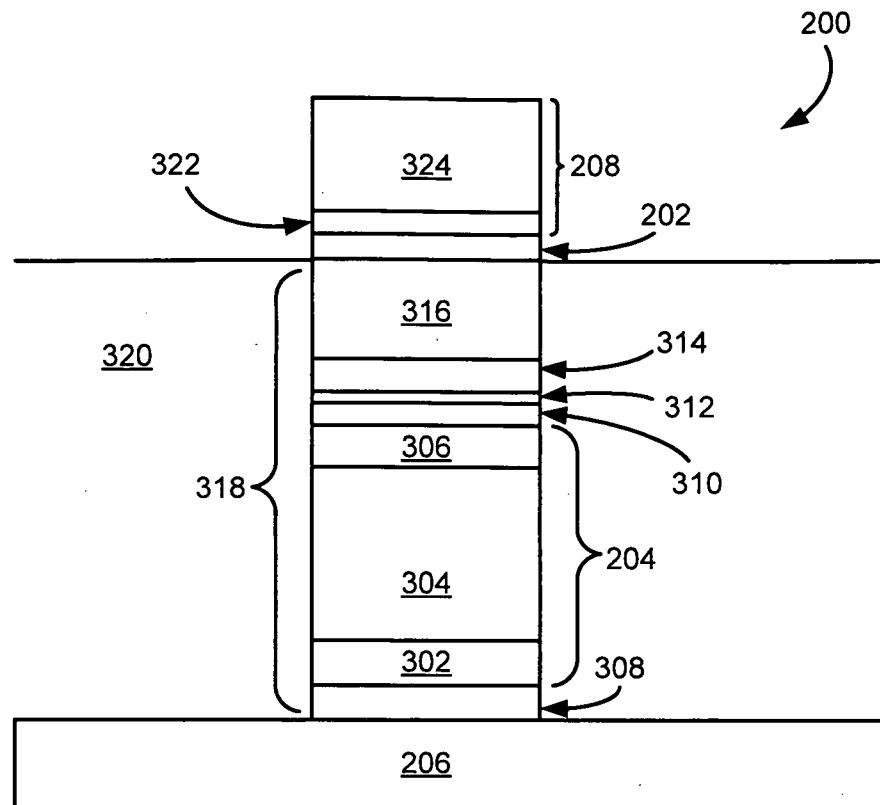


Fig. 3

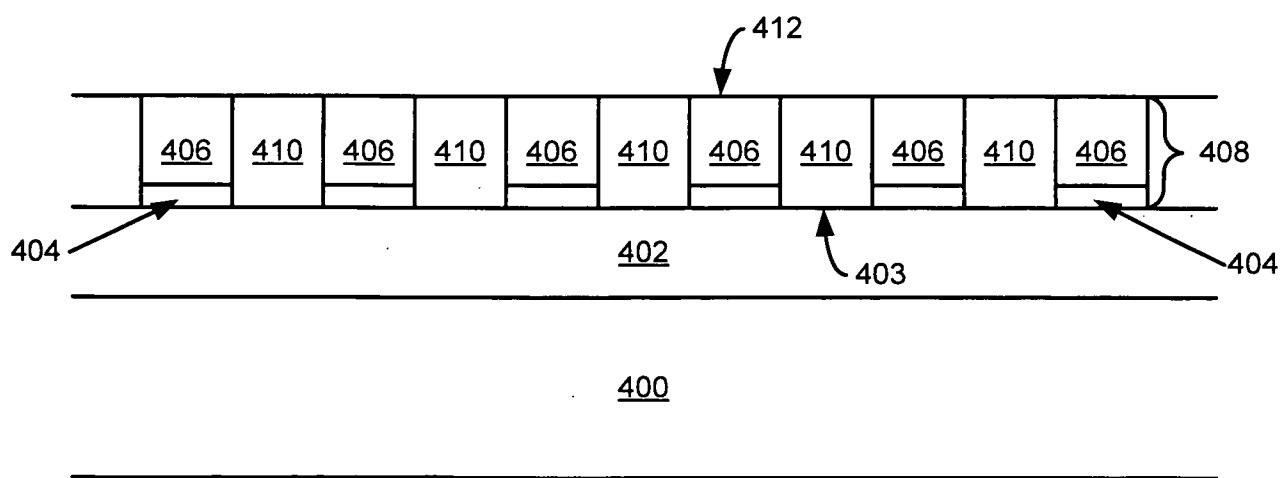


Fig. 4A

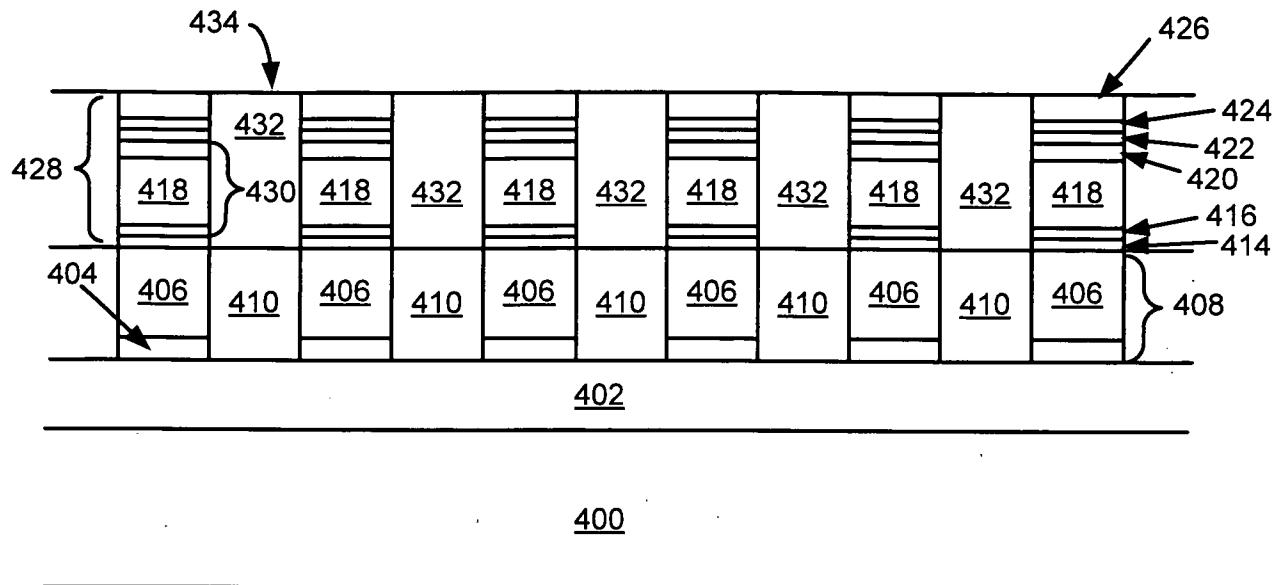


Fig. 4B

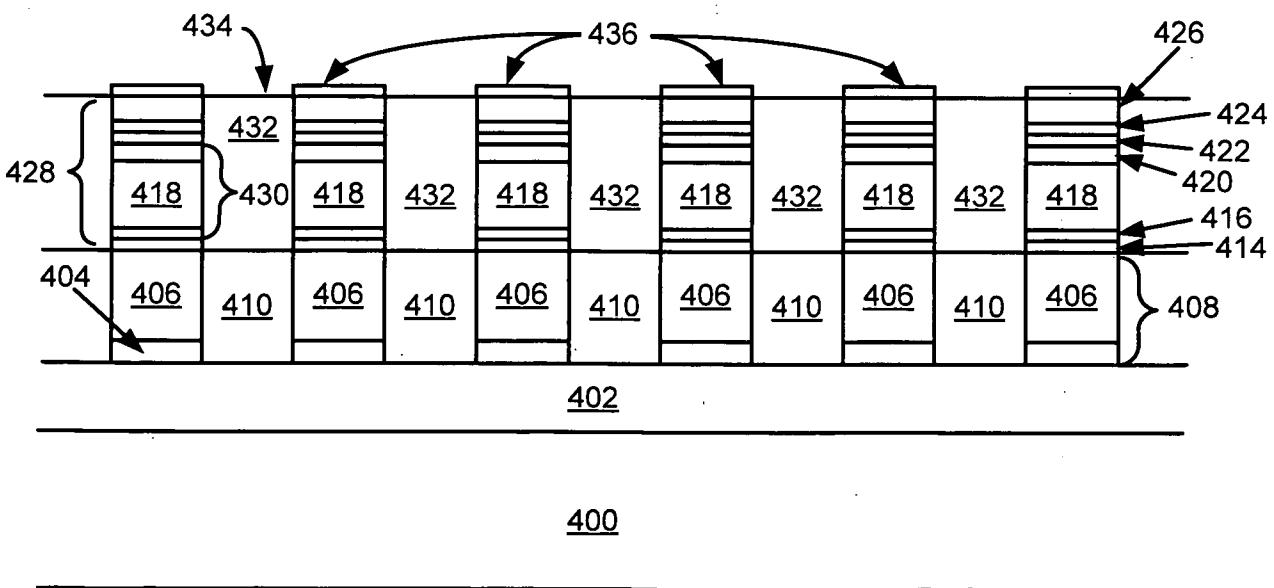


Fig. 4C

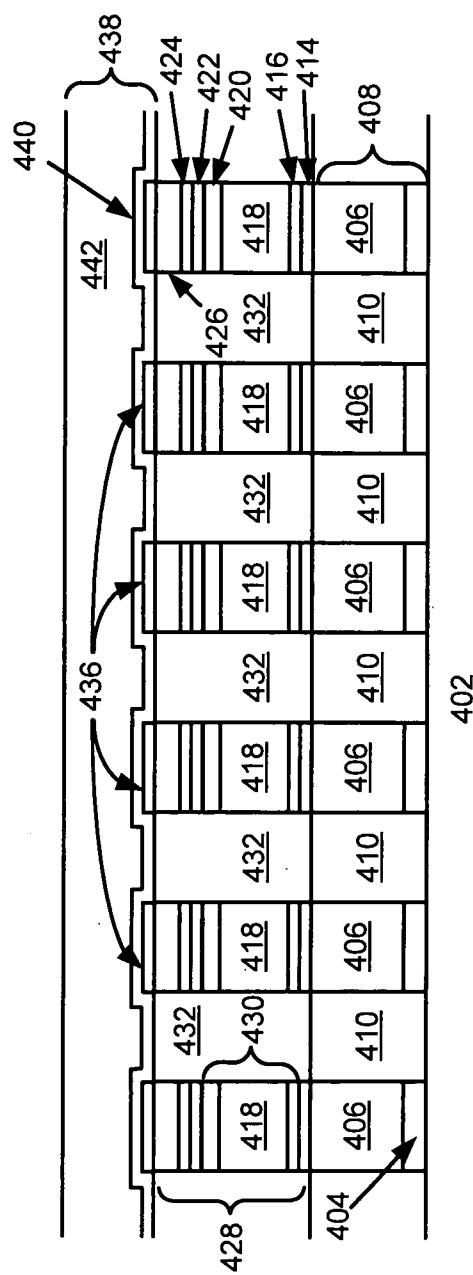


Fig. 4D

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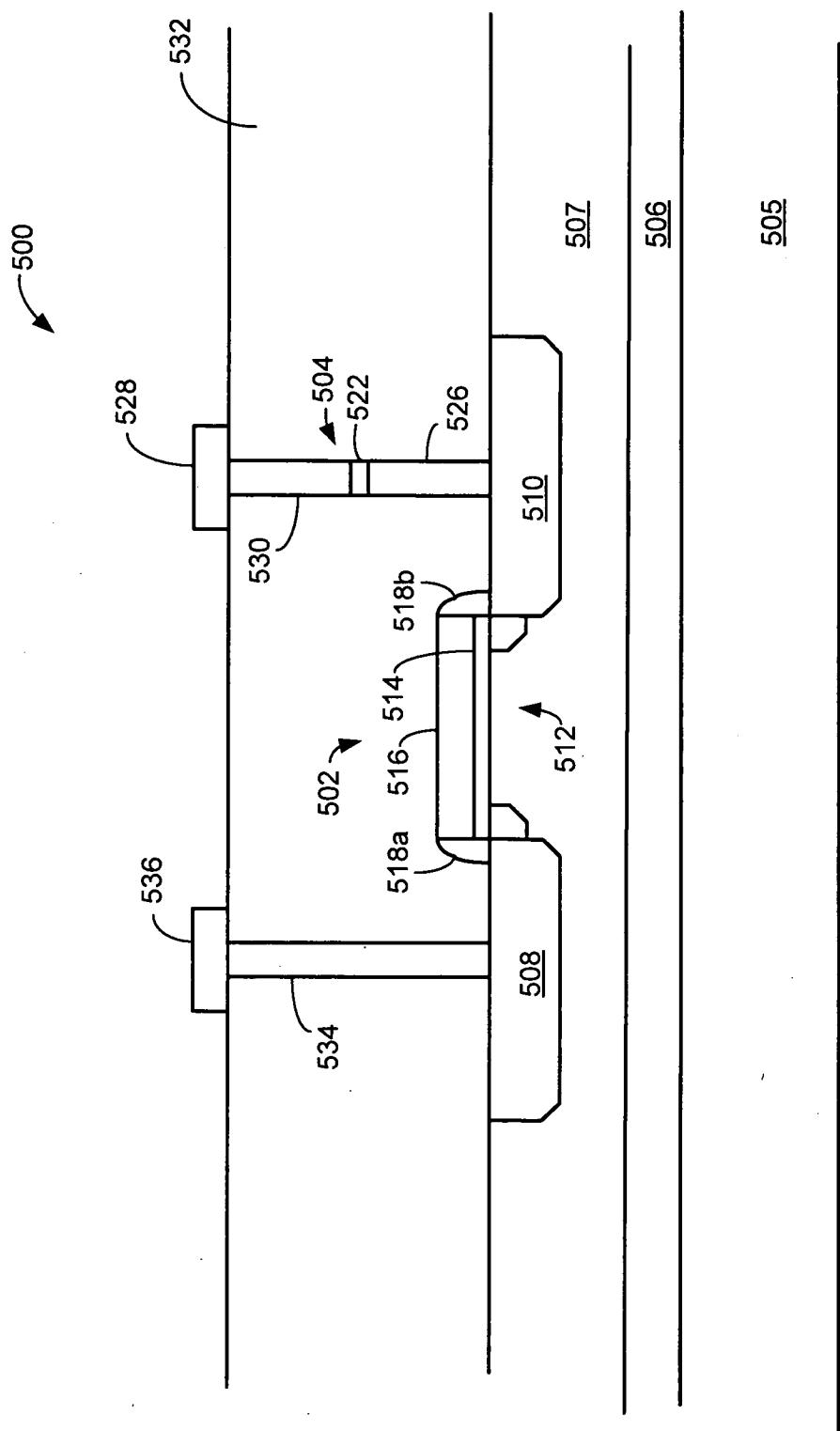


FIG. 5

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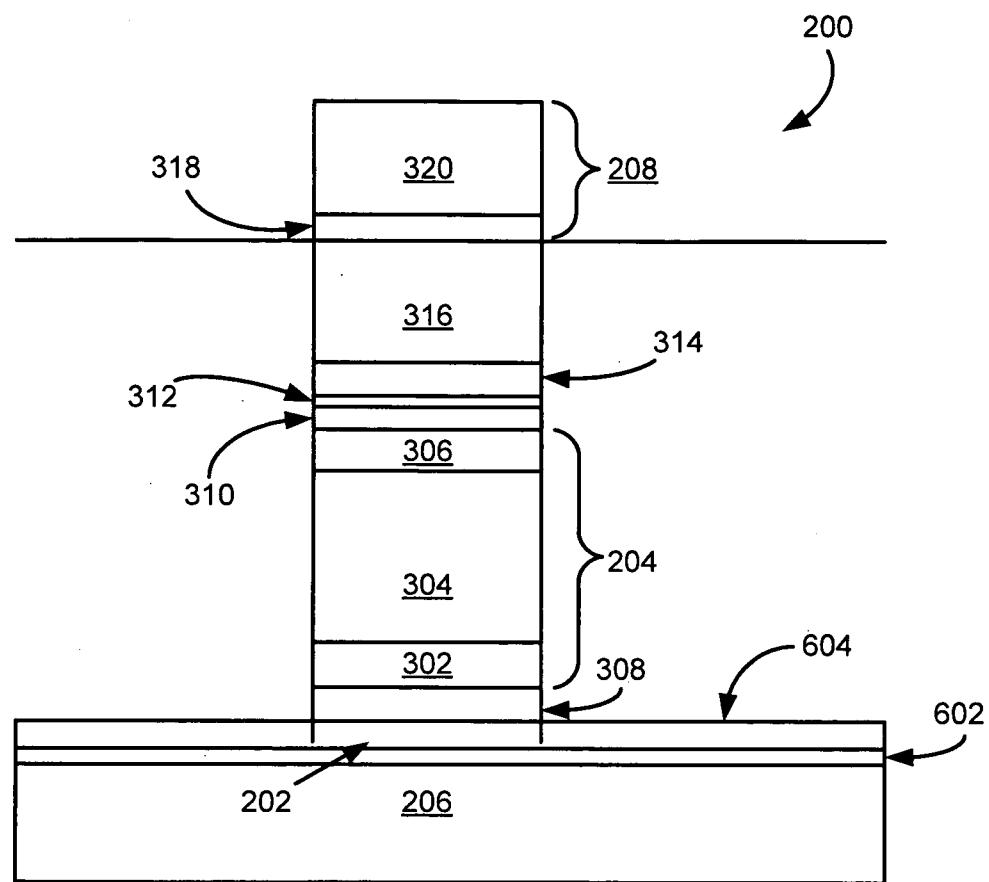


Fig. 6