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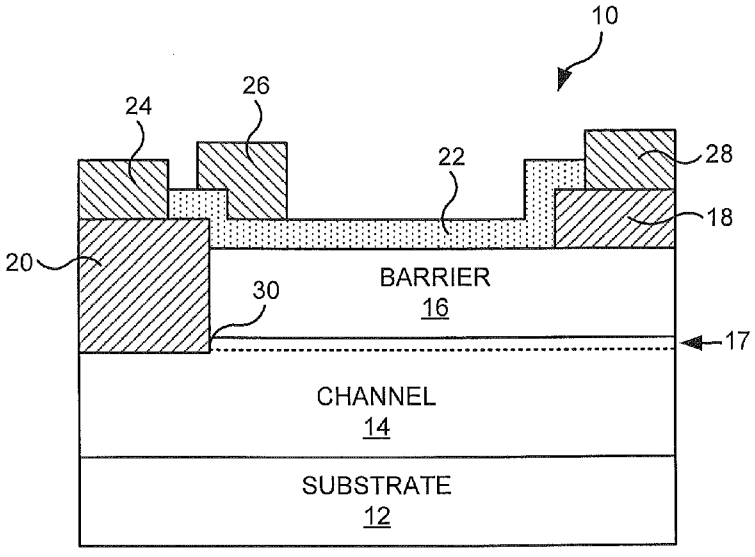

FIGURE 1

(57) Abstract: Methods of forming a transistor include providing a semiconductor epitaxial structure including a channel layer and barrier layer on the channel layer, forming a gate electrode on the barrier layer, etching the semiconductor epitaxial structure using the gate electrode as an etch mask to form a trench in the semiconductor epitaxial structure, and depositing a source metal in the trench. The trench extends at least to the channel layer, and the source metal forms a Schottky junction with the channel layer. Related semiconductor device structures are also disclosed.

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TUNNEL JUNCTION FIELD EFFECT TRANSISTORS HAVING SELF-ALIGNED SOURCE AND GATE ELECTRODES

FIELD

[0001] The present disclosure relates to semiconductor processing, and in particular relates to the fabrication of high electron mobility transistors.

BACKGROUND

[0002] A nitride-based semiconductor high-electron-mobility transistor (HEMT) has an epitaxial layer structure including a barrier layer (typically AlGaN) and a channel layer (typically GaN) that together generate a two-dimensional electron gas (2DEG) at their interface. The two-dimensional electron gas forms due to piezoelectric polarization electric fields at gallium nitride/aluminum gallium nitride (GaN/AlGaN) interfaces. The conductivity of the channel layer can be modulated by a gate contact on the barrier layer, which allows current to flow between source and drain contacts on the channel layer.

[0003] While nitride-based HEMTs are useful for microwave frequency applications, their usefulness for other applications is limited due to the fact that they are normally ON devices. A normally OFF nitride-based HEMT has been developed by providing a Schottky junction between the source contact and the channel. An example of a normally OFF nitride-based HEMT is shown in L. Yuan et al., " Normally Off AlGaN/GaN Metal–2DEG Tunnel-Junction Field-Effect Transistors," IEEE Electron Device Letters, Vol. 32, p. 303 (March 2011).

[0004] A conventional structure of a normally OFF nitride-based tunnel junction HEMT is illustrated in Figure 1. As shown therein, a normally OFF nitride-based tunnel junction HEMT 10 includes a substrate 12 on which a GaN channel layer 14 is formed. An AlGaN barrier layer 16 is on the GaN channel layer 12 and forms a two-dimensional electron gas 15 at the AlGaN/GaN heterojunction 17.

[0005] A reactive ion etching (RIE) mesa isolation using a chlorine/helium (Cl2/He) inductively coupled plasma etch process may be used to define a device mesa. An ohmic drain electrode 18 is deposited using electron-beam (e-beam) evaporation and a rapid thermal anneal.

[0006] A source electrode 20 is formed on the opposite side of the channel layer 14 from the drain electrode 18. To form the source electrode 20, the epitaxial structure is etched at least to the level of the 2DEG 15 using, for example, a further Cl2/He etch. The source electrode 20 is formed of a metal, such as titanium-gold, that forms a Schottky contact with the material of the channel layer 14. The source electrode 20 may be deposited using e-beam evaporation and lift-off. The source electrode may be self-aligned to the etched side of the 2DEG 15 by combining photolithography for etch and acetone lift-off steps.

[0007] The source electrode 20 forms a tunnel junction 30 with the 2DEG 15 in the channel layer 14. The Schottky barrier height of the contact is about 0.8eV, while the Schottky barrier width is only a few nanometers. Thus, efficient quantum tunneling may occur at larger currents.

[0008] An insulating layer 22, which may include aluminum oxide, is formed on the barrier layer 16 and extending onto the source electrode 20 and drain electrode 18. A gate electrode 26 is then formed, for example by e-beam deposition and liftoff, on the insulating layer between the source 20 and drain 18 electrodes.

[0009] Source 24 and drain 28 pads are formed on the source 20 and drain 18 electrodes, respectively.

[0010] A HEMT as shown in Figure 1 may be a normally-off device with a positive threshold voltage, which may reduce power consumption in some applications. The device may also exhibit reverse current blocking at the source–channel interface, which may suppress leakage through the buffer layer as compared to conventional HEMT structures.

SUMMARY

[0011] Methods of forming a transistor according to some embodiments includes providing a semiconductor epitaxial structure including a channel layer and barrier layer on the channel layer, forming a gate electrode on the barrier layer, etching the semiconductor epitaxial structure using the gate electrode as an etch mask to form a trench in the semiconductor epitaxial structure, and depositing a source metal in the trench. The trench extends at least to the channel layer, and the source metal forms a Schottky junction with the channel layer.

[0012] The methods may further include forming an insulation layer on the barrier layer, and forming the gate electrode may include forming the gate electrode on the insulation layer.

[0013] The methods may further include reflowing the source metal after depositing the source metal in the trench to cause the source metal to contact a sidewall of the trench.

[0014] The source metal may form a tunnel junction with a two-dimensional electron gas at an interface between the barrier layer and the channel layer.

[0015] The methods may further include forming a drain electrode on the semiconductor epitaxial structure, with the drain electrode spaced apart from the gate electrode in a first direction.

[0016] The Schottky junction may extend along a sidewall of the channel layer in a second direction that is perpendicular to the first direction. In some embodiments, the Schottky junction may extend along a sidewall of the channel layer in the first direction.

[0017] Etching the semiconductor epitaxial structure may include etching the semiconductor epitaxial layer using the gate electrode as an etch mask to form a pair of trenches in the semiconductor epitaxial layer on opposite sides of the gate electrode. The trenches may extend at least to the channel layer. Depositing the source metal may include depositing the source metal in the trenches. The source metal may form Schottky junctions with the channel layer on opposite sides of the gate electrode, with the Schottky junctions extending in the first direction.

[0018] Etching the semiconductor epitaxial structure using the gate electrode as the etch mask to form the trench in the semiconductor epitaxial structure may include forming an etch mask on the insulation layer and on the gate electrode, and patterning the etch mask to expose a portion of the insulation layer adjacent the gate electrode and to expose a portion of the gate electrode.

[0019] The etch mask may include a first mask layer and a second mask layer on the first mask layer. Patterning the etch mask may include isotropically etching the first mask layer to undercut the second mask layer.

[0020] Etching the semiconductor epitaxial structure may include recessing a sidewall of the trench beneath an edge of the gate electrode, and reflowing the source metal after depositing the source metal in the trench to cause the source metal to contact the recessed sidewall of the trench.

[0021] A transistor structure according to some embodiments includes a channel layer, and an epitaxial layer structure including a barrier layer on the channel layer. The barrier layer and the channel layer induce a two dimensional electron gas in the channel layer at an interface between the channel layer and the barrier layer. The transistor structure further includes a drain electrode on the epitaxial layer structure, and a gate electrode on the barrier layer and spaced apart from the drain electrode. The gate electrode includes a sidewall opposite the drain electrode. The transistor structure further includes a trench in the epitaxial structure adjacent the sidewall of the gate electrode. The trench extends through the barrier layer and into the channel layer and exposes a sidewall of the channel layer beneath the sidewall of the gate electrode. The transistor structure further includes a source electrode in the trench. The source electrode contacts the sidewall of the channel layer and forms a Schottky junction with the channel layer, and the sidewall of the gate electrode is laterally spaced from the sidewall of the channel layer by less than about 0.2 microns.

[0022] The sidewall of the gate electrode may be substantially aligned with the sidewall of the channel layer.

[0023] The drain electrode may be spaced apart from the gate electrode in a first direction, and the Schottky junction may extend along a sidewall of the channel layer in a second direction that is perpendicular to the first direction.

[0024] The drain electrode may be spaced apart from the gate electrode in a first direction, and the Schottky junction may extend along a sidewall of the channel layer in the first direction.

[0025] The structure may further include a second trench in the semiconductor epitaxial layer on an opposite side of the gate electrode from the first trench and a second source electrode in the second trench and contacting the channel layer. The first and second source electrodes may form Schottky junctions with the channel layer on opposite sides of the gate electrode, with the Schottky junctions extending in the first direction.

[0026] Other systems, methods, and/or computer program products according to embodiments of the invention will be or become apparent to one with skill in the art upon review of the following drawings and detailed description. It is intended that all such additional systems, methods, and/or computer program products be included within this

description, be within the scope of the present invention, and be protected by the accompanying claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate certain embodiment(s) of the invention. In the drawings:

[0028] Figure 1 illustrates a conventional structure of a nitride-based tunnel junction HEMT.

[0029] Figure 2A is a plan view of a single tunneling junction FET structure according to some embodiments.

[0030] Figure 2B is a cross-sectional view of the single tunneling junction FET structure of Figure 2A.

[0031] Figure 3A is a plan view of a double tunneling junction FET structure according to some embodiments.

[0032] Figure 3B is a cross-sectional view of the double tunneling junction FET structure of Figure 3A.

[0033] Figures 4A to 12A are plan views that illustrate intermediate structures in the formation of tunnel junction FET devices according to various embodiments.

[0034] Figures 4B to 12B are cross-sectional views showing the structures of Figures 4A to 12A taken along lines B-B of Figures 4A to 12A, respectively.

[0035] Figure 13 is a flowchart illustrating operations according to some embodiments.

DETAILED DESCRIPTION OF EMBODIMENTS

[0036] Embodiments of the present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will

fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout.

[0037] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present invention. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0038] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes" and/or "including" when used herein, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0039] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0040] As discussed above, nitride-based tunnel junction field effect devices can be desirable for certain applications. The operation of such devices is dependent on the ability to fabricate a controllable tunnel junction between the Schottky source electrode and the two-dimensional electron gas (2DEG) in the channel layer.

[0041] It is presently understood that the behavior of the tunnel junction is highly sensitive to the spacing between the source electrode and the gate electrode, i.e., the source-gate gap. For example, the switching/modulation operation of a tunnel junction FET is based on the interaction between the voltage applied to the gate electrode and the conduction state of the Schottky junction between the source electrode and the 2DEG in the

channel layer. The threshold voltage of the device may be dependent on the geometry of the gate electrode and the spacing between the gate electrode and the tunnel junction.

[0042] Yuan et al. disclose that the gate electrode 26 may overlap the source electrode 20 by 0.25μm so that the tunnel junction can be controlled effectively. However, conventional fabrication methods of nitride-based tunnel junction field effect devices use separate photolithography layers for defining the gate and source electrodes. The precision of the gate-source alignment may therefore be determined by the precision of a stepper.

[0043] In contrast, some embodiments of the present inventive concept provide methods of forming a tunnel junction FET in which the gate electrode is self-aligned to the source electrode, and in particular is self-aligned to the junction between the source electrode and the channel layer. Further embodiments provide tunnel junction field effect transistors in which the gate electrode is self-aligned to the source electrode, and in particular is self-aligned to the junction between the source electrode and the channel layer.

[0044] The resulting structure may provide an improved level of control over the shape of the electrical field that modulates the conductive state of the junction.

[0045] Referring to Figures 2A and 3A, tunnel junction transistor structures 110, 110' according to some embodiments are illustrated. Figures 2B and 3B are cross-sectional views taken along lines B-B of Figures 2A and 3A, respectively. Figures 2A and 2B illustrate a single tunneling junction FET that may be suitable, for example, for a device having a wide channel layout, while Figures 3A and 3B illustrated a double tunneling junction FET that may be suitable, for example, for a device having a narrow channel layout.

[0046] Figures 2A and 2B illustrate a single tunneling junction FET structure 110 including an epitaxial structure 150 including a channel layer 114 and a barrier layer 116 that together induce a two-dimensional electron gas 115 at the interface thereof. The channel layer 114 and the barrier layer 116 may include nitride-based materials, such as GaN, AlGaN, InGaN, InAlGaN, AlN, etc. However, it will be appreciated that other semiconductor materials, such as GaAs, AlGaAs, etc. may be used.

[0047] An insulator layer 122 is formed on the barrier layer 116. The insulator may include aluminum oxide, silicon oxide, silicon nitride, silicon oxynitride, or any other suitable insulator material. A gate electrode 126 is on the insulator layer 122. A drain electrode 118

that forms an ohmic contact with the 2DEG 115 in the channel layer 114 is on the epitaxial structure 150 and is spaced apart from the gate electrode 126.

[0048] The epitaxial structure 150 is recessed on the side of the gate electrode 126 opposite the drain electrode 118 such that a sidewall of the portion of the channel layer 114 in which the 2DEG 115 is formed is exposed.

[0049] A Schottky metal 125 is on the structure. A portion of the Schottky metal 125 is on the exposed portion of the channel layer 114 and forms a source electrode 120. Another portion of the Schottky metal 125 is on the gate electrode 126. The source electrode 120 contacts the exposed sidewall of the channel layer to form a lateral metal-semiconductor tunnel junction 130 between the source electrode 120 and the 2DEG 115.

[0050] The double tunneling junction FET 110' shown in Figures 3A and 3B is similar to the single tunneling junction FET 110 shown in Figures 2A and 2B, except that in the FET 110', the Schottky metal 125' is deposited on opposing sides of the gate electrode 126. The Schottky metal 125' forms tunnel junctions 130' with the 2DEG regions 115 of the epitaxial structure 150' that run parallel to a side 150A of the epitaxial region that extends between the gate electrode 126 and the drain electrode 118.

[0051] Accordingly, in the double tunneling junction device 110' illustrated in Figures 3A and 3B, current flow from the drain electrode 118 to the source electrode 120' follows a right angle path. In contrast, in the single tunneling junction device 110 illustrated in Figures 2A and 2B, current flow from the drain electrode 118 to the source electrode 120 follows a straight line path.

[0052] Figures 4A to 12A illustrate intermediate structures in the formation of tunnel junction FET devices according to various embodiments. Figures 4B to 12B are cross-sectional views showing the structures of Figures 4A to 12A taken along lines B-B of Figures 4A to 12A, respectively.

[0053] Referring to Figures 4A and 4B, an epitaxial structure 150 including a channel layer 114 and a barrier layer 116 is provided. The channel layer 114 and the barrier layer 116 may include nitride-based materials, such as GaN, AlGaN, InGaN, InAlGaN, AlN, etc., or non-nitride materials, such as GaAs, AlGaAs, etc., that can form a 2DEG 115 at their interface. An active region 155 may be defined by implanted isolation regions 160.

[0054] An insulator layer 122 is formed on the barrier layer 116. The insulation layer may include, for example, aluminum oxide, silicon oxide, silicon nitride, silicon oxynitride,

etc. The insulation layer may be formed, for example, by atomic layer deposition, chemical vapor deposition, or any other suitable method.

[0055] A drain contact region 140 is formed in the active region 155. The drain contact region 140 may be formed, for example, by implanting n-type dopants, such as silicon, in the barrier layer 116. To form the drain contact region 140, an n-type dopant, such as silicon, may be implanted into the substrate. Typically, a Si dose of 1E15 at/cm2 or higher may be sufficient to form a low resistance ohmic contact.

[0056] Referring to Figures 5A and 5B, the insulation layer 122 is masked and etched to expose the drain contact region 140. A drain electrode 118 is formed on the drain contact region 140. The drain electrode 118 may form an ohmic contact with the drain contact region 140. The drain electrode 118 may be formed, for example, by e-beam deposition and/or evaporation and liftoff of a conductive material, such as Ti-Al, Ti-Al-Au, Ti-Al-Ni, Ti-Al-Ni-Au or Ni-Si. The material may be annealed at a temperature above 500 ºC to form an ohmic contact.

[0057] Referring to Figures 6A and 6B, a gate electrode 126 is formed on the insulation layer 122. The gate electrode 126 may be formed, for example, by e-beam deposition and/or evaporation and liftoff of Ti/Pt/Au. The gate electrode 126 may be formed on the insulation layer 122 as shown in Figure 6B, or may be formed directly on the barrier layer 116, in which case the gate electrode 126 may form a non-ohmic junction with the barrier layer 116

[0058] Referring to Figures 7A and 7B, a mask 170 is formed on the insulation layer 122 and the gate electrode 126 and pattern to expose a region 124 that overlaps a portion of the gate electrode 126 and the insulation layer 122 opposite the drain electrode 118 on which the source metal will be deposited. (For clarity, Figure 7A illustrates the complement of the region 124 that is exposed by the mask 170.) The exposed region 124 of the gate electrode 126 and the insulation layer 122 that is exposed by the mask 170 may also overlap the implant isolation region 160 adjacent the active region 155, as illustrated in Figure 7B.

[0059] The mask 170 may be a bi-layer photoresist including a first mask layer 172 and a second mask layer 174. Bi-layer photoresists are known in the art. The first mask layer 172 may be a polydimethylglutarimide based resist, and the second mask layer 174 may be an imaging resist. When the second mask layer 174 is exposed and developed, the first mask layer may dissolve to form the overhang shown in Figure 7B.

[0060] Referring to Figures 8A and 8B, the epitaxial structure 150 is etched using the gate electrode 126 and the mask 170 as an etch mask to define a trench 195 in the epitaxial structure 150. The etch may be performed using an anisotropic etch based on Cl_2, BCl_3 or $SiCl_4$ chemistry. A directional high density ion etch should provide the vertical sidewall profile illustrated in Figure 8b. The trench 195 is formed to be deeper than the thickness of the barrier layer 116, so that the trench 195 exposes a sidewall 150A of the epitaxial structure 150 including a sidewall of the epitaxial structure adjacent the interface between the channel layer 114 and the barrier layer 116 where the 2DEG 115 is induced.

[0061] Still referring to Figures 8A and 8B, a source metal 125 is deposited on the etched portion of the epitaxial structure 150 and on the gate electrode 126. The source metal 125 may be deposited, for example, using e-beam deposition and/or evaporation and liftoff. The metal choice should provide a high electron barrier height for the Schottky contact. The metal stack needs to be compatible with a directional deposition method (e.g. evaporation) that reduces/minimizes the sidewall coverage. Possible choices for the source metal include Ni, Ir, Pt, Pd, Mo, TiSi, NiSi or other alloys. The thickness of the source metal 125 may be chosen in such a way that its top surface lays above the interface between epitaxial layers 114 and 116, but is below the interface defined by epitaxial layer 116 and the insulation layer 122. In other words, the boundary limits are defined by the need to contact the channel (layer 115) but to avoid contact with the insulation layer 122 .

[0062] As deposited, the source metal 125 may contact an exposed sidewall of the channel layer 114 where the 2DEG is induced between the channel layer 114 and the barrier layer 116. The source metal 125 may form a Schottky source contact 120 with the channel layer 114 that may under appropriate conditions conduct current to the 2DEG 115 through tunneling.

[0063] As shown in Figure 8A, because the gate electrode 126 is used as an etch mask to define a sidewall of the trench 195 adjacent the channel layer 114, the junction 130 between the source electrode 120 and the channel layer 114 may be formed to be self-aligned with a sidewall 126A of the gate electrode 126. Self-alignment of the junction 130 and the gate electrode 126 may obviate the need to align these features using conventional photolithographic methods, and may increase control over the threshold voltage and/or conductivity of the tunnel junction between the source electrode 120 and the 2DEG 115.

[0064] Figures 9A, 9B, 10A and 10B illustrated formation of the source electrode 120 and the tunnel junction between the source electrode 120 and the 2DEG 115 according to further embodiments.

[0065] Referring to Figures 9A and 9B, in some embodiments, the etch process in which the trench 195 is etched using the gate electrode 126 as an etch mask may result in an undercut 215 of the epitaxial structure 150 beneath the gate electrode 126. Thus, as shown in Figures 10A and 10B, when the source metal 125 is deposited in the trench 195, a gap 190 may exist between the source metal 125 and the sidewall 150B of the epitaxial structure 150. The gap 190 may have a width of about 0.05 microns to 0.2 microns, and it can be accomplished by using an isotropic etch. A high pressure, low energy reactive etch based on Cl_2, BCl_3 or $SiCl_4$ chemistries may create an etch profile as illustrated in Figure 9B.

[0066] Referring still to Figures 10A and 10B, the source metal 125 may be reflowed to cause it to contact the sidewall 150B of the epitaxial structure 150 so as to form the junction 130 between the source electrode 120 and the 2DEG 115. In general, heat treating a thin film metal (or alloy) at half its melting temperature will cause it to deform and reflow into a low energy state. The choice of the metal source electrode will depend on the thermal budget of the structure.

[0067] Figures 11A, 11B, 12A and 12B illustrated formation of the source electrode 120 and the tunnel junction between the source electrode 120 and the 2DEG 115 according to further embodiments.

[0068] Referring to Figures 11A and 11B, in some embodiments, an additional spacer layer 180 may be formed between the insulation layer 122 and the gate electrode 126. The spacer layer 180 is part of an enhanced metal lift-off structure that consists of a bi-layer photo resist. It's role is to improve the lift-off process and provide a clean breaking point for the source metal.

[0069] When the spacer layer 180 is present, the etch process in which the trench 195 is etched using the gate electrode 126 as an etch mask may result in an undercut 215 of the epitaxial structure 150 beneath the gate electrode 126. A high pressure, low energy reactive etch based on Cl_2, BCl_3 or $SiCl_4$ chemistries may create an etch profile as illustrated in Figure 11B. Thus, as shown in Figures 11A and 11B, when the source metal 125 is deposited in the trench 195, a gap 190 may exist between the source metal 125 and the sidewall 150B of the epitaxial structure 150.

[0070] Referring to Figures 12A and 12B, the source metal 125 may be reflowed to cause it to contact the sidewall 150B of the epitaxial structure 150 so as to form the junction 130 between the source electrode 120 and the 2DEG 115. As noted above, heat treating a thin film metal (or alloy) at half its melting temperature will cause it to deform and reflow into a low energy state. The choice of the metal source electrode will depend on the thermal budget of the structure.

[0071] Figure 13 is a flowchart illustrating operations 200 according to some embodiments. As shown therein, an epitaxial structure 150 is provided (block 202). An insulation layer 122 is formed on the epitaxial structure 150 (block 204). A gate metal is then deposited and patterned on the insulation layer 122 to form a gate electrode 126 (block 206). As noted above, the insulation layer may be patterned to allow the gate metal to be deposited directly on the epitaxial structure in some embodiments.

[0072] Next, the epitaxial structure 150 is etched using the gate electrode 126 as an etch mask to define a trench 195 in the epitaxial structure 150 (block 208). The trench 195 is formed to be at least deeper than the thickness of the barrier layer 116, so that the trench 195 exposes a sidewall 150A of the epitaxial structure 150 including a sidewall of the epitaxial structure adjacent the interface between the channel layer 114 and the barrier layer 116 where the 2DEG 115 is induced.

[0073] A source metal 125 is then deposited in trench 195 and may be at least partially deposited on the gate electrode 126 (block 210). The source metal 125 may contact the 2DEG 115 as deposited and/or may be reflowed to cause it to contact the 2DEG.

[0074] Many different embodiments have been disclosed herein, in connection with the above description and the drawings. It will be understood that it would be unduly repetitious and obfuscating to literally describe and illustrate every combination and subcombination of these embodiments. Accordingly, all embodiments can be combined in any way and/or combination, and the present specification, including the drawings, shall be construed to constitute a complete written description of all combinations and subcombinations of the embodiments described herein, and of the manner and process of making and using them, and shall support claims to any such combination or subcombination.

[0075] In the drawings and specification, there have been disclosed typical embodiments of the invention and, although specific terms are employed, they are used in a

generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

WHAT IS CLAIMED IS:

1. A method of forming a transistor, comprising:

providing a semiconductor epitaxial structure including a channel layer and barrier layer on the channel layer;

forming a gate electrode on the barrier layer;

etching the semiconductor epitaxial structure using the gate electrode as an etch mask to form a trench in the semiconductor epitaxial structure, wherein the trench extends at least to the channel layer; and

depositing a source metal in the trench, wherein the source metal forms a Schottky junction with the channel layer.

2. The method of Claim 1, further comprising:

forming an insulation layer on the barrier layer, wherein forming the gate electrode comprises forming the gate electrode on the insulation layer.

3. The method of Claim 1, further comprising reflowing the source metal after depositing the source metal in the trench to cause the source metal to contact a sidewall of the trench.

4. The method of Claim 1, wherein the source metal forms a tunnel junction with a two-dimensional electron gas formed at an interface between the barrier layer and the channel layer.

5. The method of Claim 1, further comprising forming a drain electrode on the semiconductor epitaxial structure, wherein the drain electrode is spaced apart from the gate electrode in a first direction.

6. The method of Claim 5, wherein the Schottky junction extends along a sidewall of the channel layer in a second direction that is perpendicular to the first direction.

7. The method of Claim 5, wherein the Schottky junction extends along a sidewall of the channel layer in the first direction.

8. The method of Claim 7, wherein etching the semiconductor epitaxial structure comprises etching the semiconductor epitaxial layer using the gate electrode as an etch mask to form a pair of trenches in the semiconductor epitaxial layer on opposite sides of the gate electrode, wherein the trenches extend at least to the channel layer; and

wherein depositing the source metal comprises depositing the source metal in the trenches, wherein the source metal forms Schottky junctions with the channel layer on opposite sides of the gate electrode, the Schottky junctions extending in the first direction.

9. The method of Claim 1, wherein etching the semiconductor epitaxial structure using the gate electrode as the etch mask to form the trench in the semiconductor epitaxial structure comprises forming an etch mask on the insulation layer and on the gate electrode, and patterning the etch mask to expose a portion of the insulation layer adjacent the gate electrode and to expose a portion of the gate electrode.

10. The method of Claim 9, wherein the etch mask comprises a first mask layer and a second mask layer on the first mask layer, wherein patterning the etch mask comprises isotropically etching the first mask layer to undercut the second mask layer.

11. The method of Claim 1, wherein etching the semiconductor epitaxial structure comprises recessing a sidewall of the trench beneath an edge of the gate electrode, and reflowing the source metal after depositing the source metal in the trench to cause the source metal to contact the recessed sidewall of the trench.

12. The method of Claim 1, wherein the transistor structure comprises a high electron mobility transistor structure.

13. A transistor structure, comprising:

a channel layer;

an epitaxial layer structure including a barrier layer on the channel layer, wherein the barrier layer and the channel layer induce a two dimensional electron gas in the channel layer at an interface between the channel layer and the barrier layer;

a drain electrode on the epitaxial layer structure;

a gate electrode on the barrier layer and spaced apart from the drain electrode, the gate electrode including a sidewall opposite the drain electrode;

a trench in the epitaxial structure adjacent the sidewall of the gate electrode, the trench extending through the barrier layer and into the channel layer and exposing a sidewall of the channel layer beneath the sidewall of the gate electrode; and

a source electrode in the trench, the source electrode contacting the sidewall of the channel layer and forming a Schottky junction with the channel layer;

wherein the sidewall of the gate electrode is laterally spaced from the sidewall of the channel layer by less than about 0.2 microns.

14. The transistor structure of Claim 13, wherein the sidewall of the gate electrode is substantially aligned with the sidewall of the channel layer.

15. The transistor structure of Claim 13, wherein the drain electrode is spaced apart from the gate electrode in a first direction, and wherein the Schottky junction extends along a sidewall of the channel layer in a second direction that is perpendicular to the first direction.

16. The transistor structure of Claim 13, wherein the drain electrode is spaced apart from the gate electrode in a first direction, and wherein the Schottky junction extends along a sidewall of the channel layer in the first direction.

17. The transistor structure of Claim 13, wherein the trench comprises a first trench and the source electrode comprises a first source electrode, the structure further comprising a second trench in the semiconductor epitaxial layer on an opposite side of the gate electrode from the first trench and a second source electrode in the second trench and contacting the channel layer;'

wherein the first and second source electrodes form Schottky junctions with the channel layer on opposite sides of the gate electrode, the Schottky junctions extending in the first direction.

18. The transistor structure of Claim 13, wherein the source metal forms a tunnel junction with a two-dimensional electron gas formed at an interface between the barrier layer and the channel layer.

19. The transistor structure of Claim 13, wherein the transistor structure comprises a high electron mobility transistor structure.

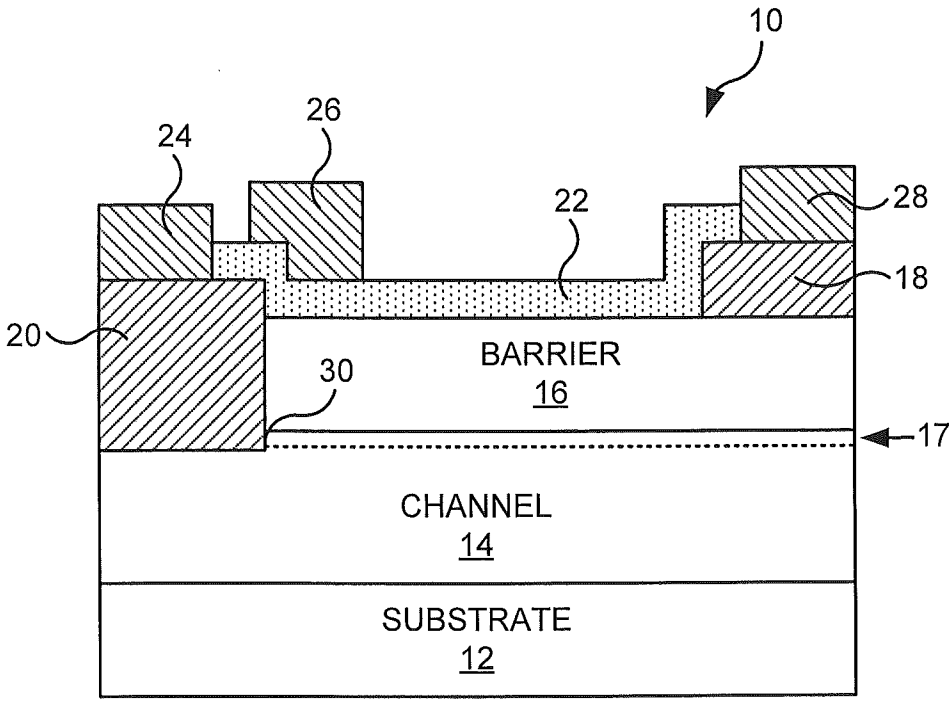

FIGURE 1
(PRIOR ART)

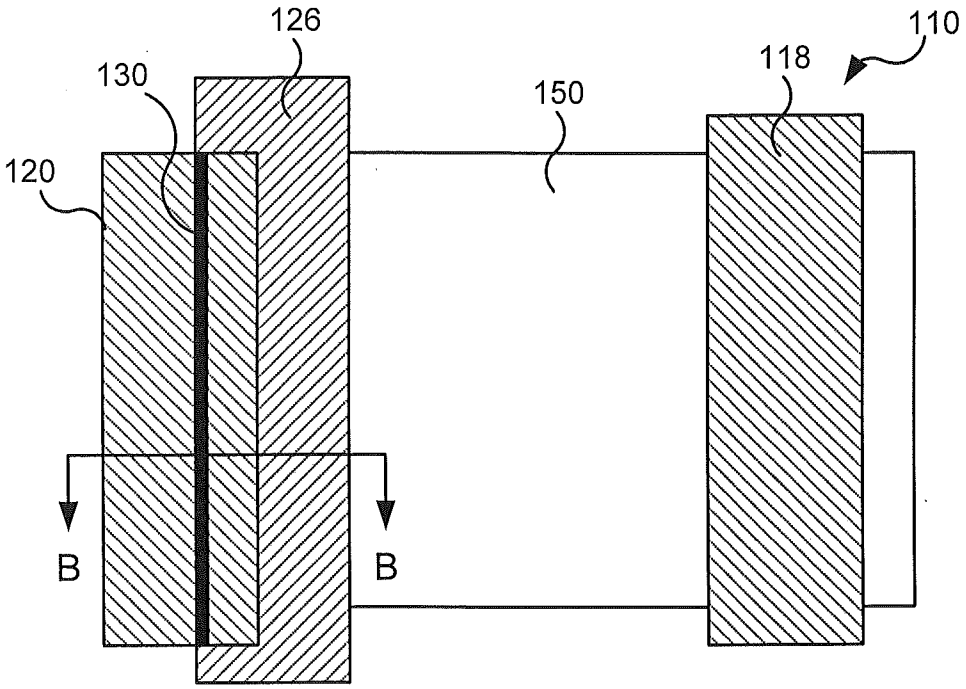

FIGURE 2A

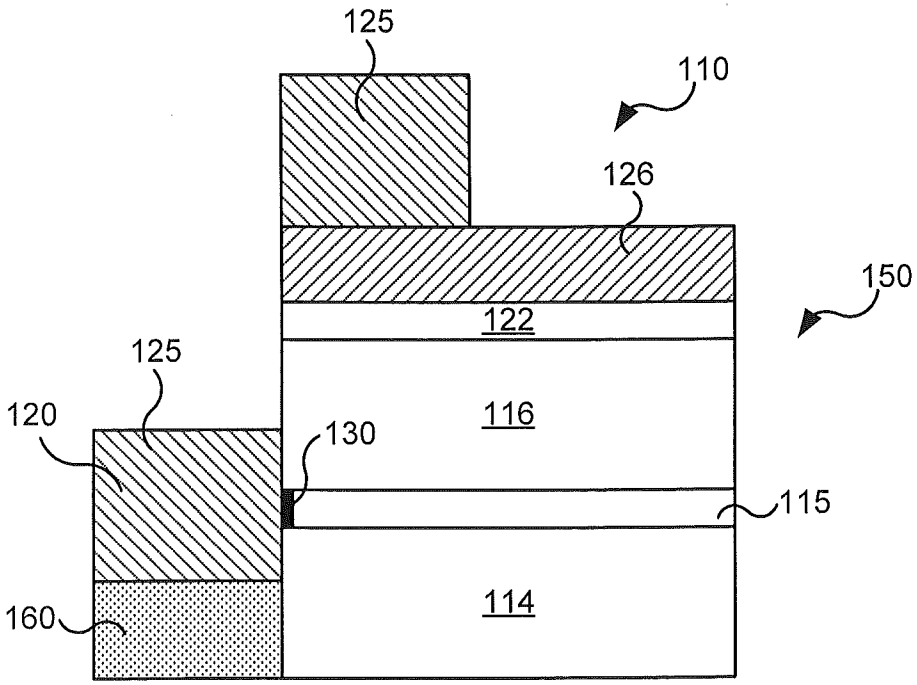

FIGURE 2B

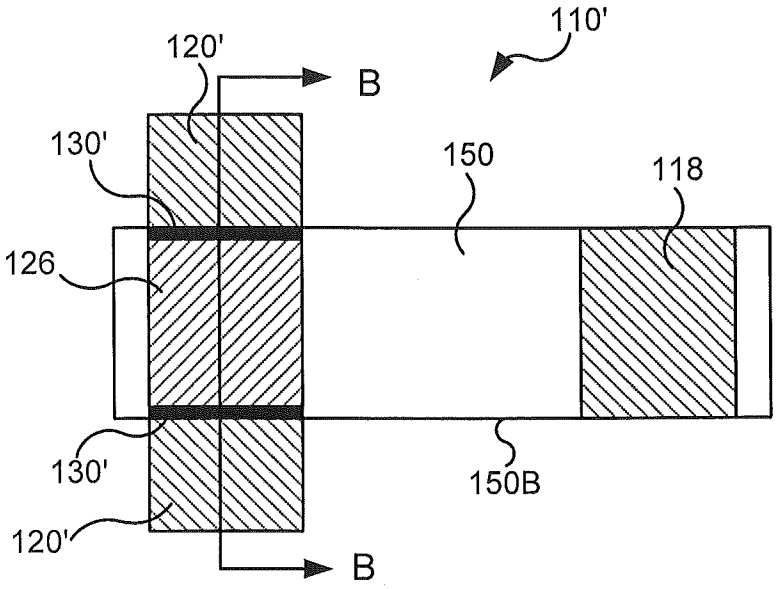

FIGURE 3A

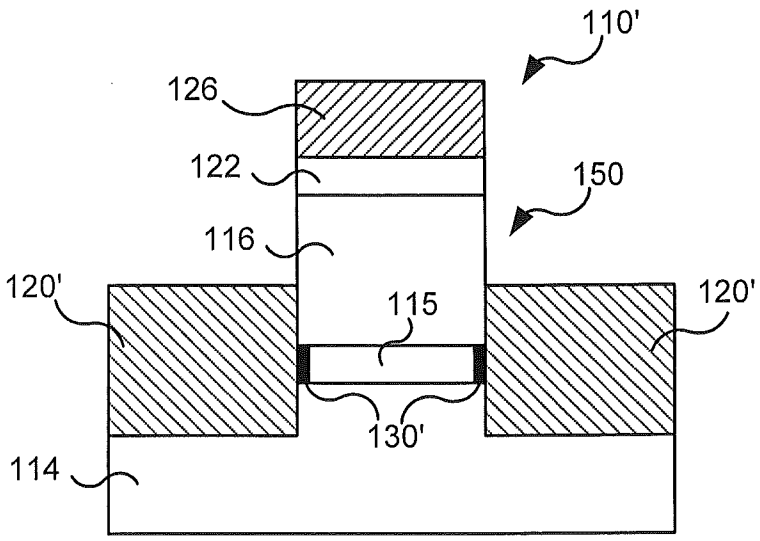

FIGURE 3B

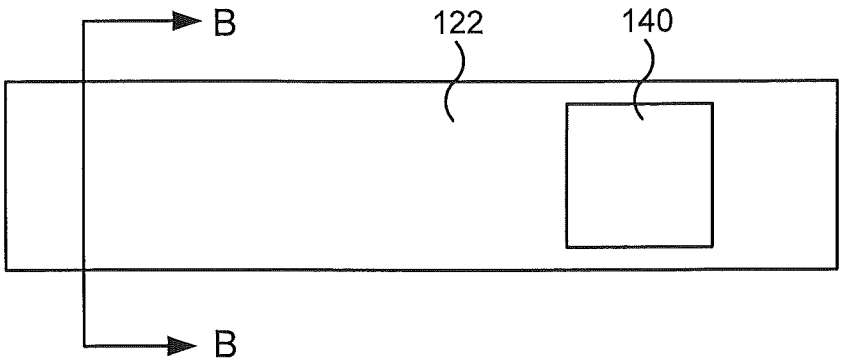

FIGURE 4A

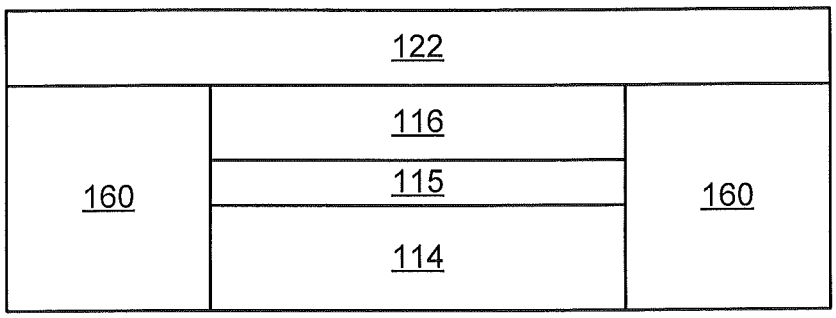

FIGURE 4B

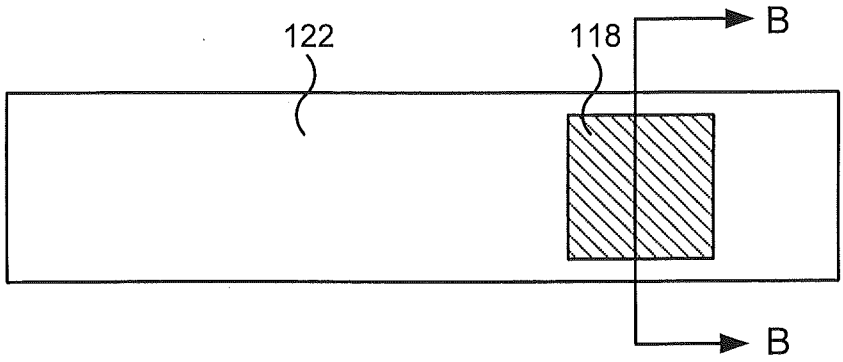

FIGURE 5A

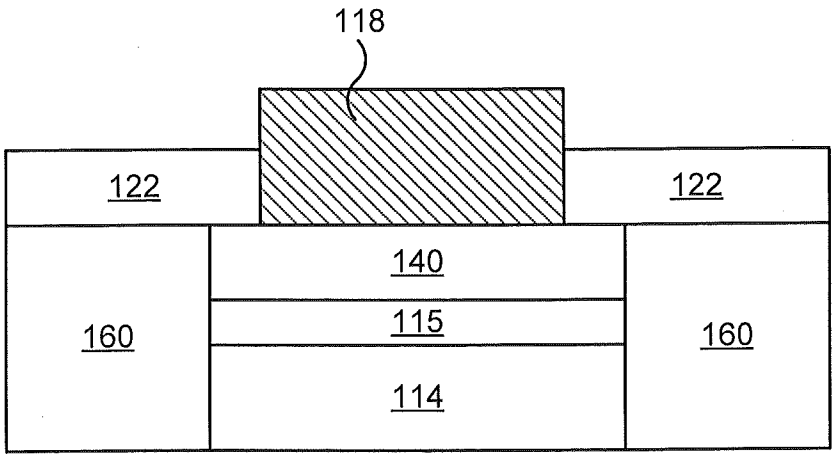

FIGURE 5B

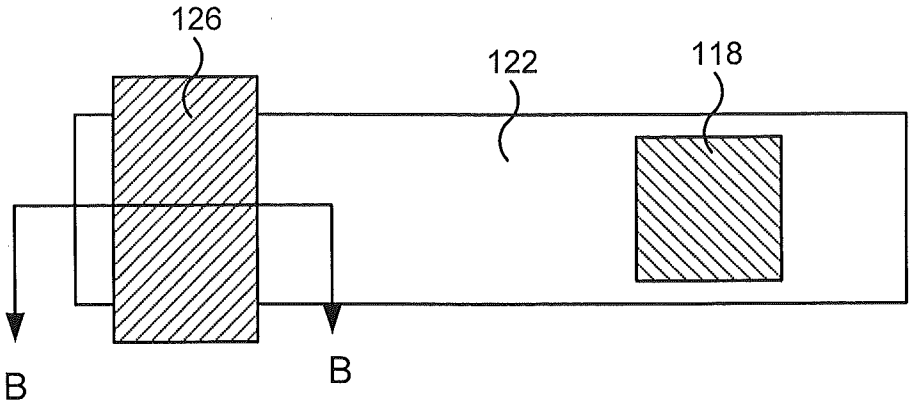

FIGURE 6A

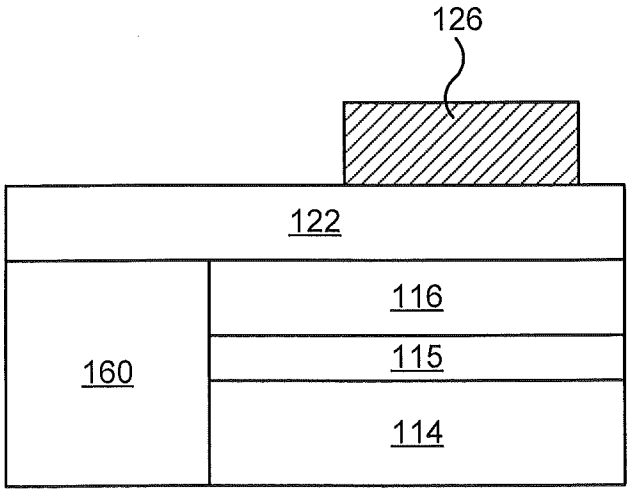

FIGURE 6B

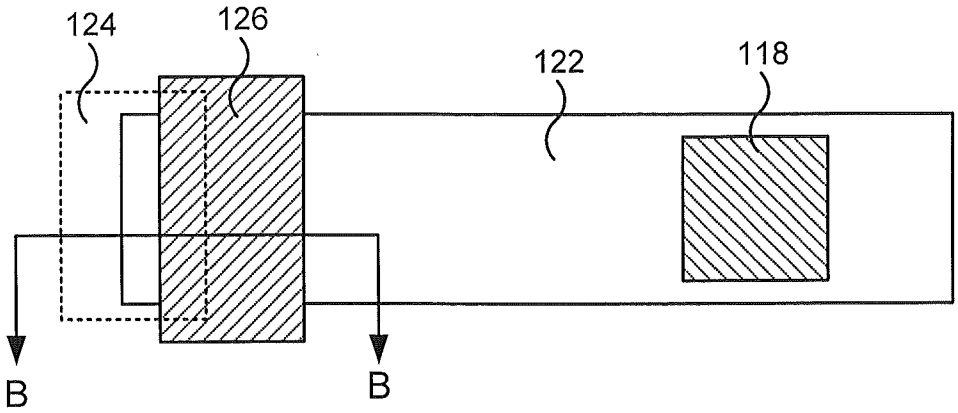

FIGURE 7A

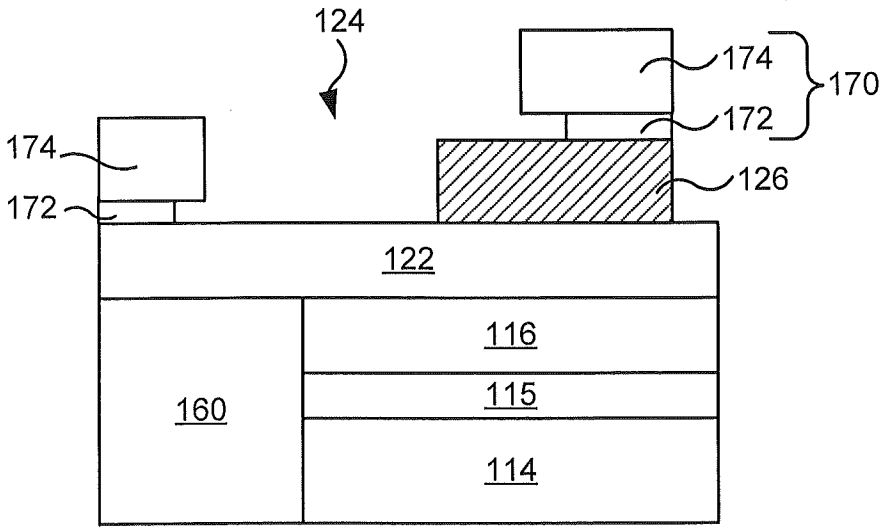

FIGURE 7B

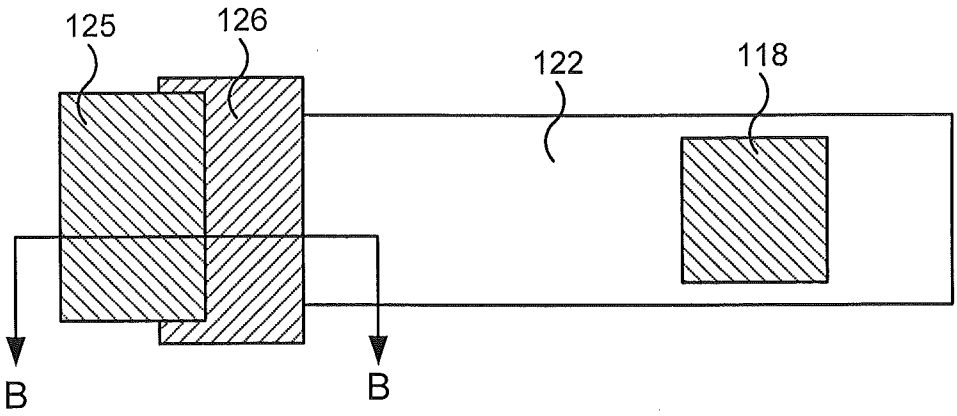

FIGURE 8A

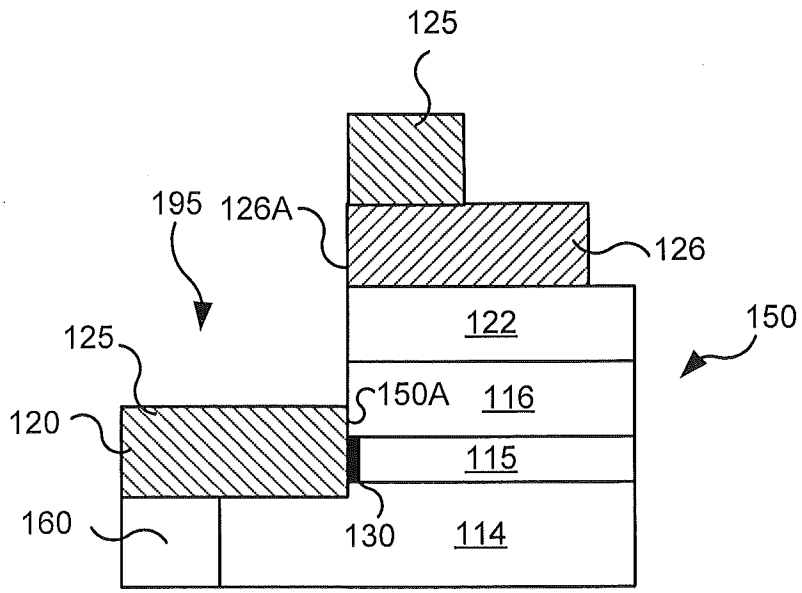

FIGURE 8B

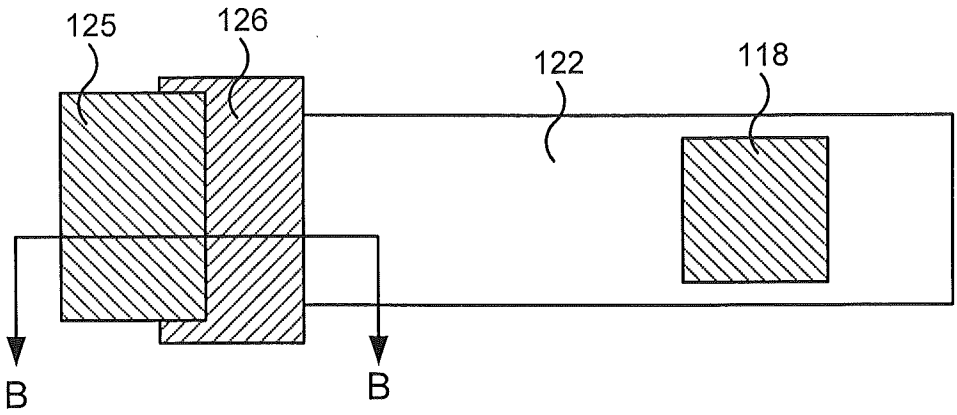

FIGURE 9A

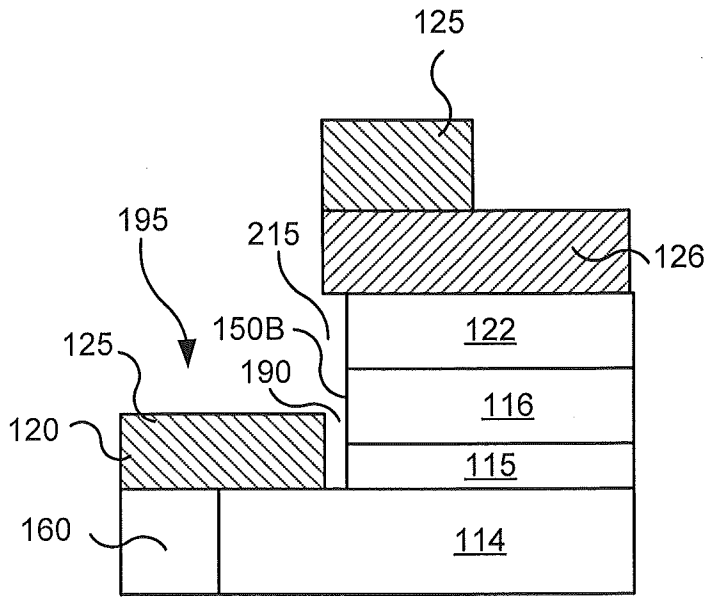

FIGURE 9B

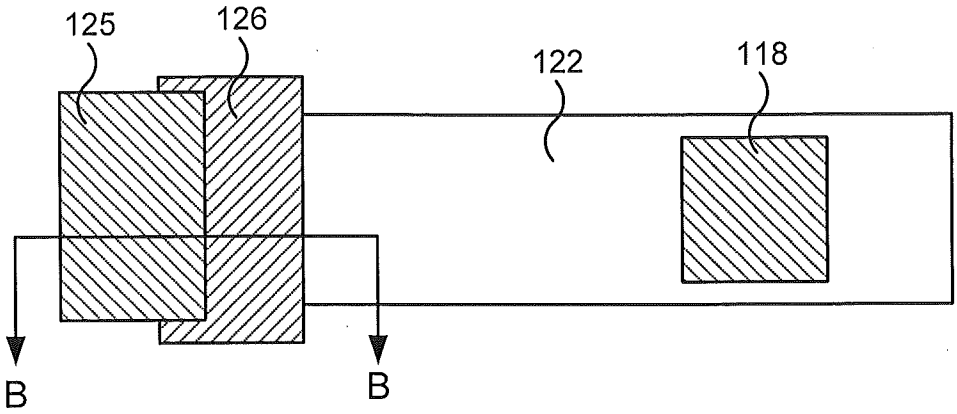

FIGURE 10A

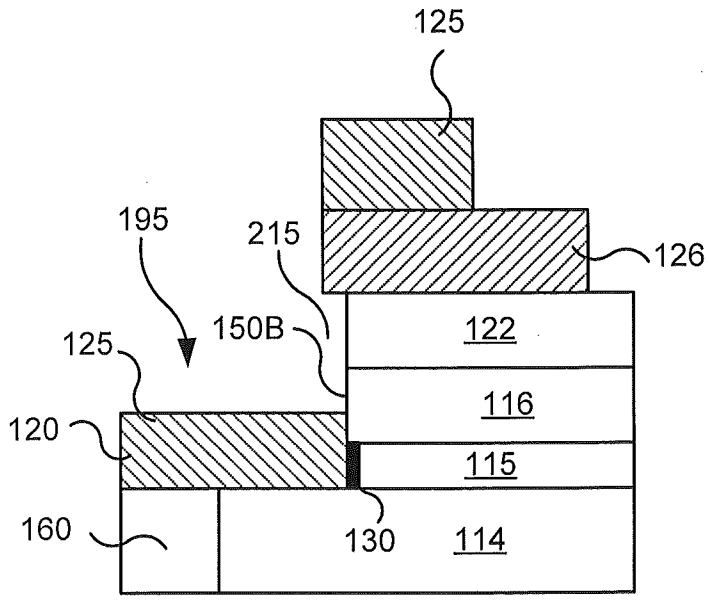

FIGURE 10B

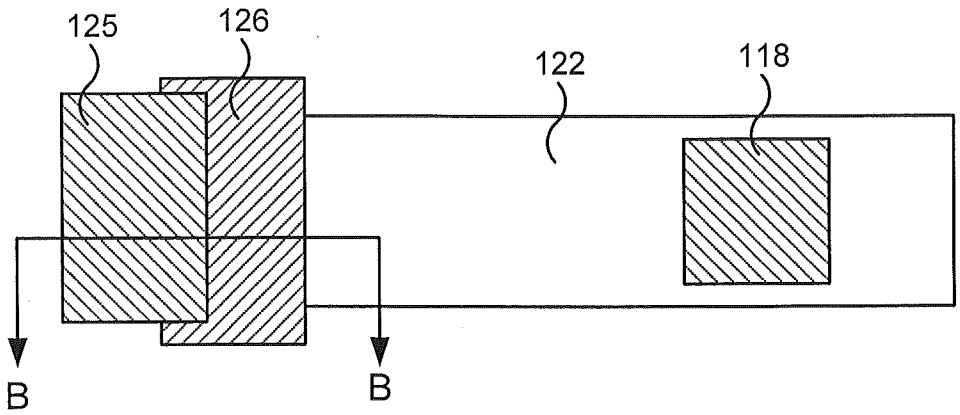

FIGURE 11A

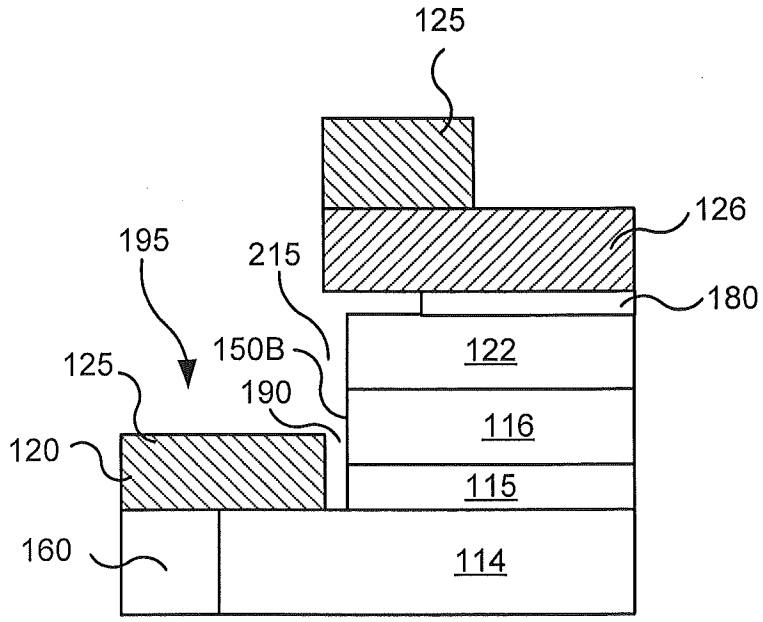

FIGURE 11B

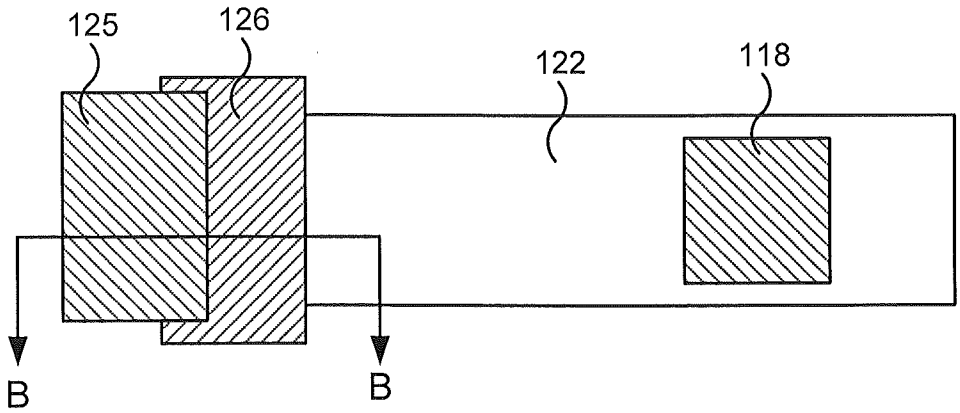

FIGURE 12A

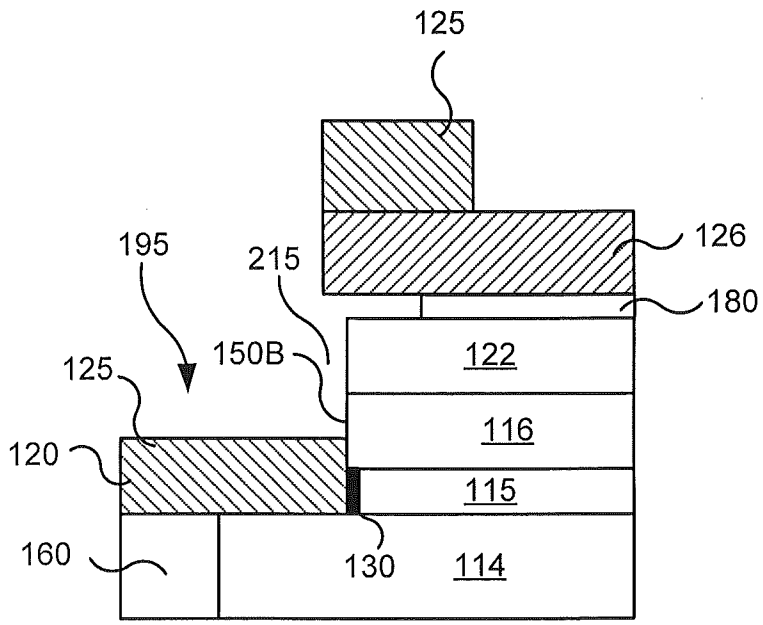

FIGURE 12B

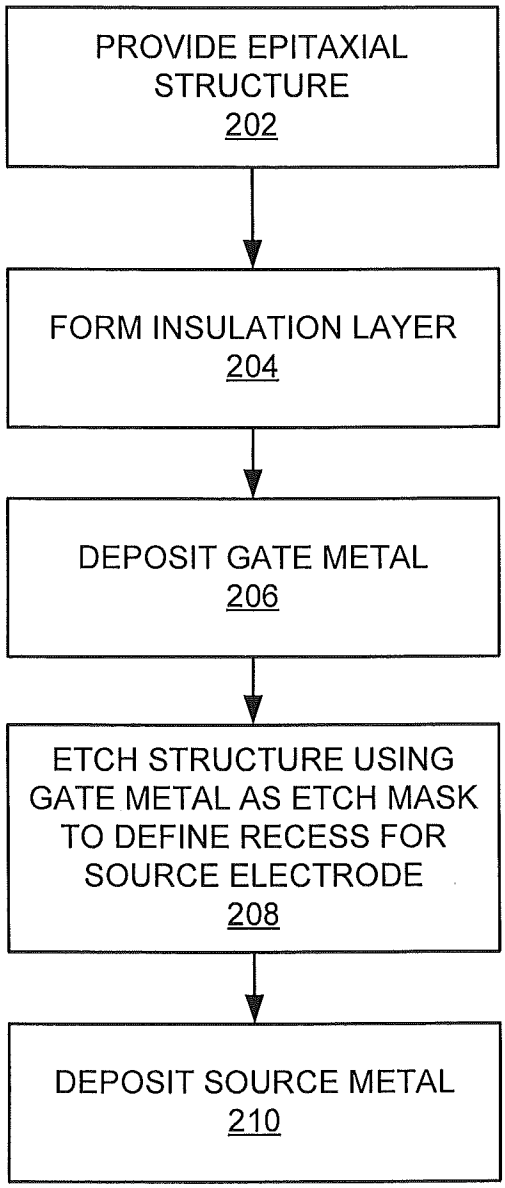
PROVIDE EPITAXIAL STRUCTURE
202
FORM INSULATION LAYER
204
DEPOSIT GATE METAL
206
ETCH STRUCTURE USING GATE METAL AS ETCH MASK TO DEFINE RECESS FOR SOURCE ELECTRODE
208
DEPOSIT SOURCE METAL
210

FIGURE 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 14/19410

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/338 (2014.01)
USPC - 438/172; 438/478
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC - 438/172; 438/478
IPC(8) - H01L 21/338 (2014.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 438/172; 257/E21.09; 257/E21.403; 438/182 (text search - see terms below)
IPC(8) - H01L 21/338 (2014.01)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatBase; PubWEST; Google
Search Terms Used: epitaxial, channel, barrier layer, schottky, mask, etch, gate, reflow, re flow, high, electron, mobility, electron gas, 2deg, undercut, under cut, second mask, tunnel, junction

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2012/003609 A1 (CHEN et al.) 12 January 2012 (12.01.2012), entire document especially pg 10, ln 1-9; pg 11, ln 5-10; pg 30, ln 7-15; pg 30, ln 7-15; Fig 1-6, 22-25	1-19
Y	US 2012/0104502 A1 (IMORI et al.) 03 May 2012 (03.05.2012), entire document especially Fig 1E; para [0031], [0053], [0059]	1-19
Y	US 6,545,357 B1 (CHOPRA) 08 April 2003 (08.04.2003), entire document especially col 3, lns 56-65	3, 11
Y	US 4,729,967 A (ARMIENTO) 08 March 1988 (08.03.1988), entire document especially Fig 3; col 4, lns 2-9	10, 11
Y	US 2010/0327322 A1 (KUB et al.) 30 December 2010 (30.12.2010), entire document especially Abstract; para [0003]	12, 19
A	US 2011/0186855 (RAMDANI) 04 August 2011 (04.08.2011), entire document especially Fig 4; paras [0016], [0020]-[0023]	1-19

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 May 2014 (27.05.2014)	20 JUN 2014
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)