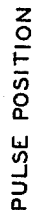


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XS3 ZONE	0000 0001 0010 0011 0100 0101 0110 0111								1000 1001 1010 1011 1100 1101 1110 1111								
	00	01	10	11	—	0	1	2	3	\$	%	#	&	'	/	C	9
00	Δ				—	0	1	2	3	\$	%	#	&	'	/	C	9
01	Δ				:	:	A	B	C	D	E	F	G	H	I		
10	Δ				:	?	J	K	L	M	N	O	P	Q	R	Y	✓
11	Δ				@	+	S	T	U	V	W	X	Y	Z	∅		

P = PRINTER BREAKPOINT STOP V = SHIFT LOCK R = CARRIAGE RETURN
 Δ = SPACE Ø = ONE SHIFT (SINGLE SHIFT) T = TAB
 X = IGNORE P = PRINTER STOP U = UNSHIFT
 BLANK SQUARES NOT USED

FIG. 1c

BY

INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
George V. Zitzguth
ATTORNEY

May 12, 1964

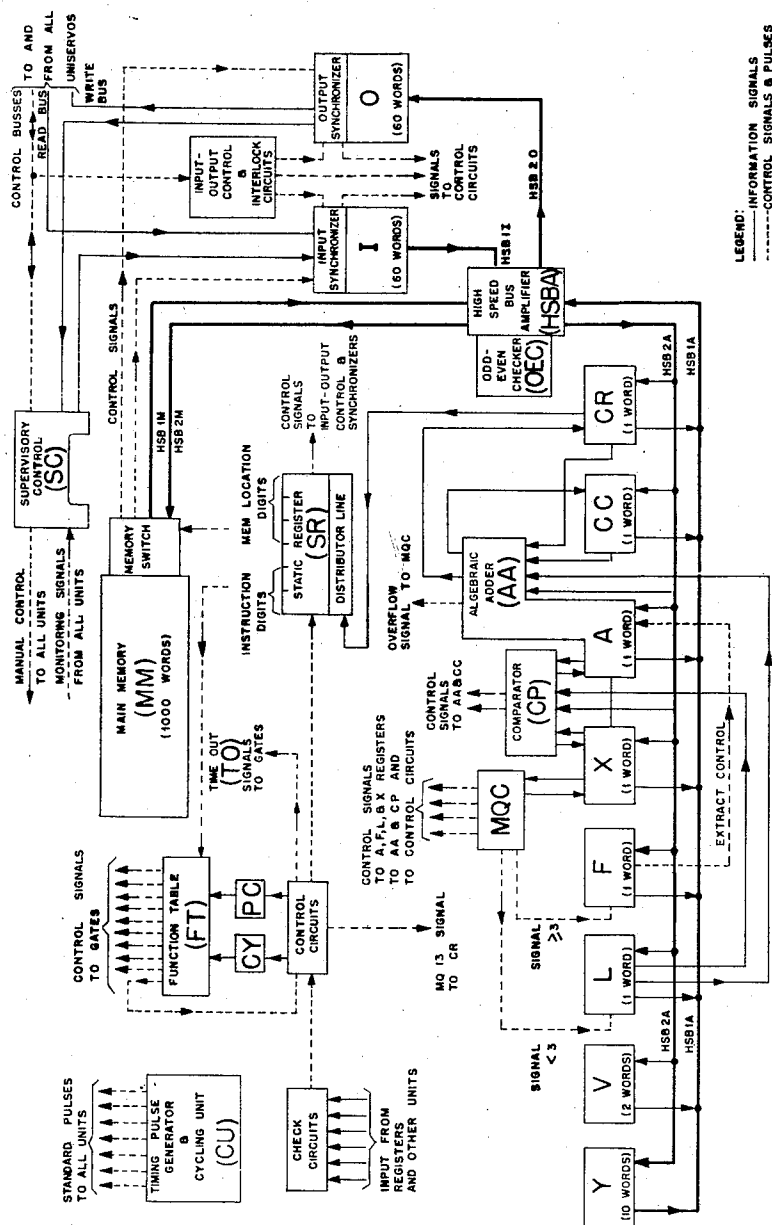
J. P. ECKERT, JR., ETAL
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FIG. 3



LEGEND:
----- INFORMATION SIGNALS
----- CONTROL SIGNALS & PULSES

INVENTORS

J. PRESER ECKERT, JR.
JAMES R. WEINER
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H. FRAZER WELSH

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George V. Zetser
ATTORNEY

May 12, 1964

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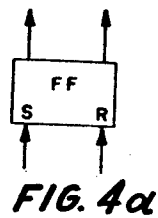


FIG. 4a

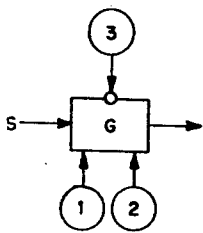


FIG. 4b

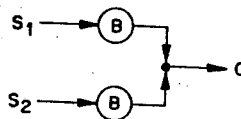


FIG. 4c

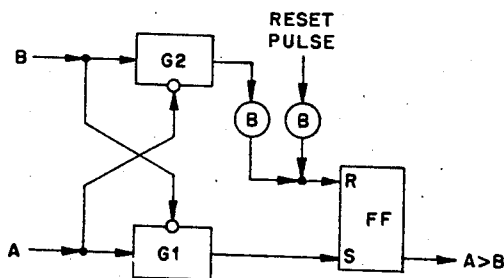


FIG. 4d

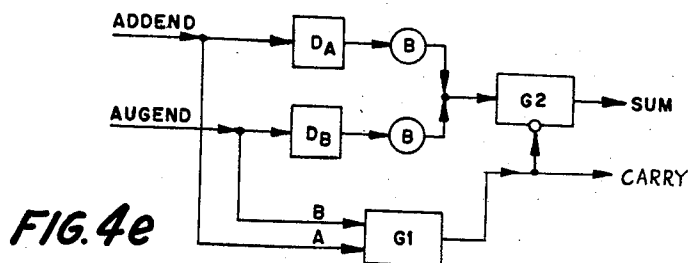


FIG. 4e

INVENTORS

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JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

BY

George V. Zettrath
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May 12, 1964

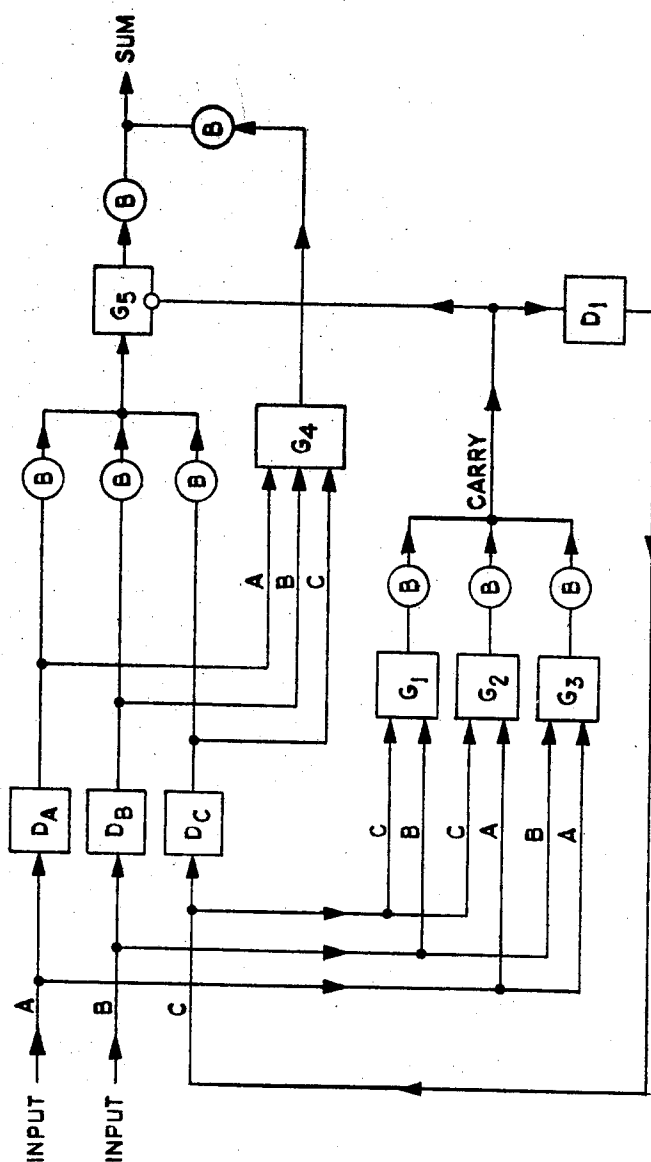
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FIG. 5



INVENTORS

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JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

BY

George V. Zetser
ATTORNEY

May 12, 1964

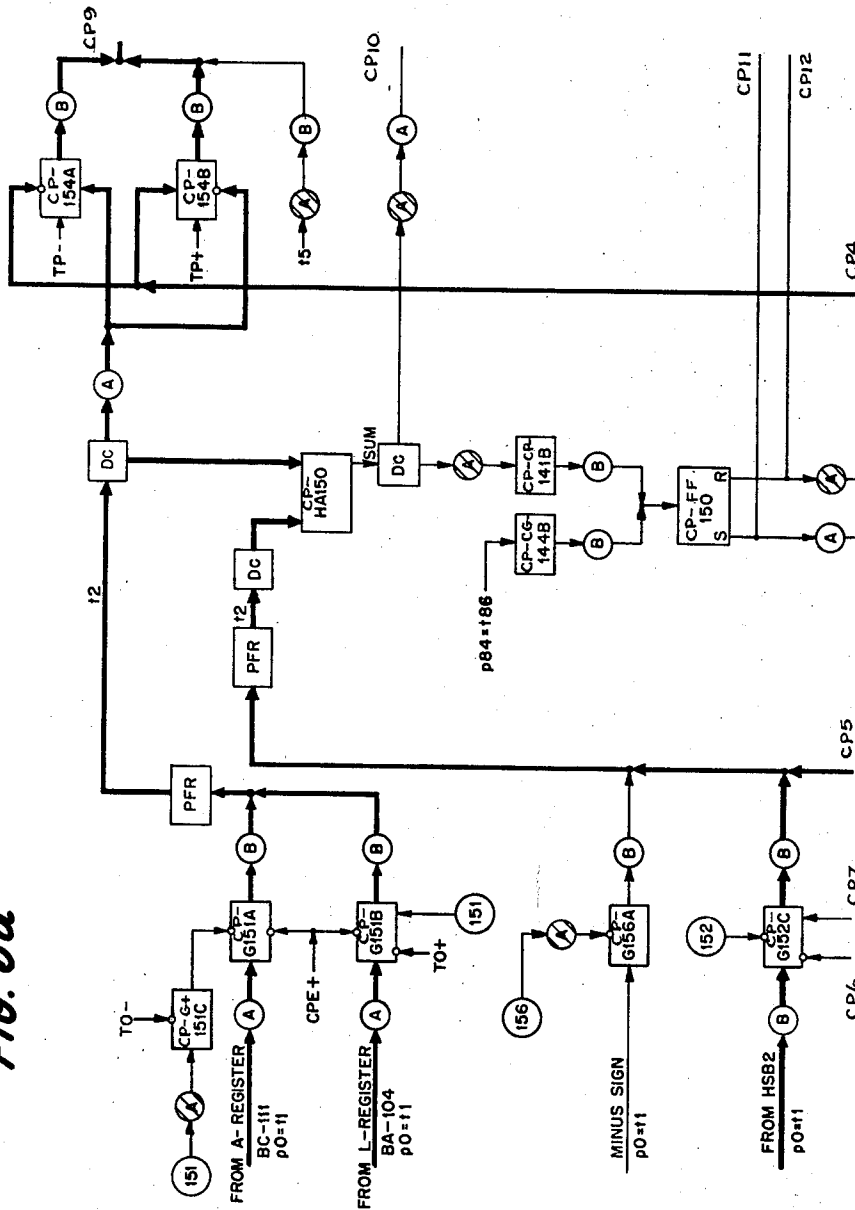
J. P. ECKERT, JR., ETAL
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FIG. 6a



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George V. Roth
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J. P. ECKERT, JR., ET AL
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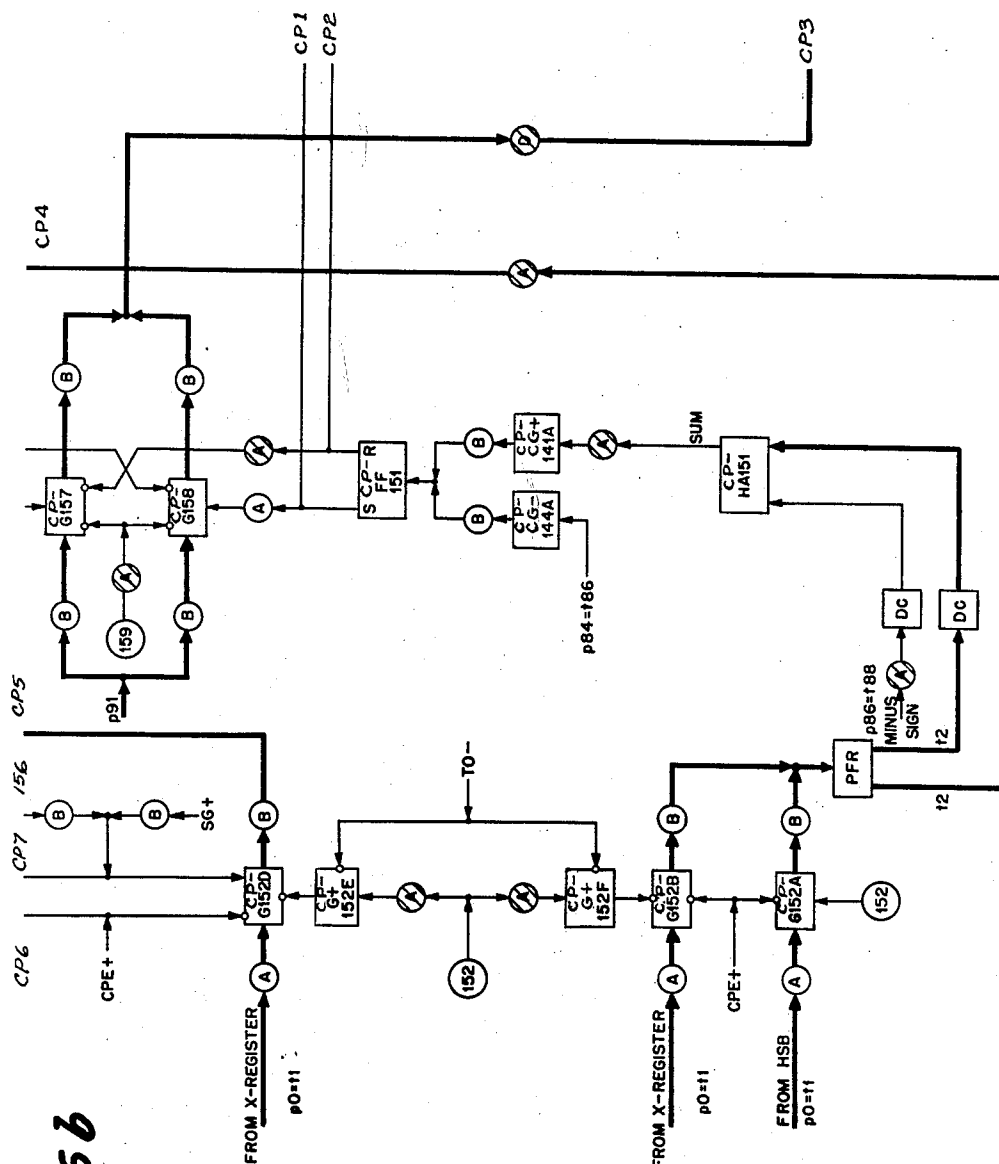


FIG. 6b

BY

INVENTORS
J. PRESPEER ECKERT, JR.
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ROBERT F. SHAW
H. FRAZER WELSH
George V. Retzger
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110 Sheets-Sheet 7



J. PRESPEER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
George V. Elyroth
ATTORNEY

BY

May 12, 1964

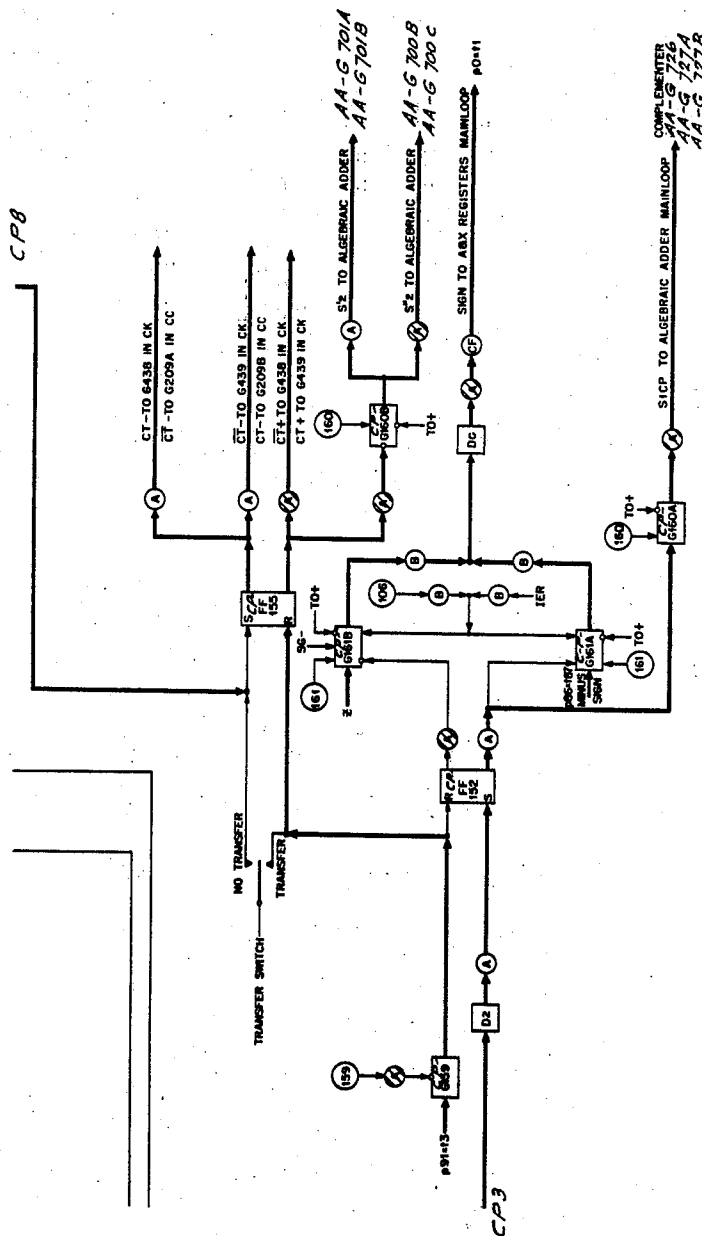
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FIG. 6d



INVENTORS
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H. FRAZER WELSH
BY *George V. Ritz*
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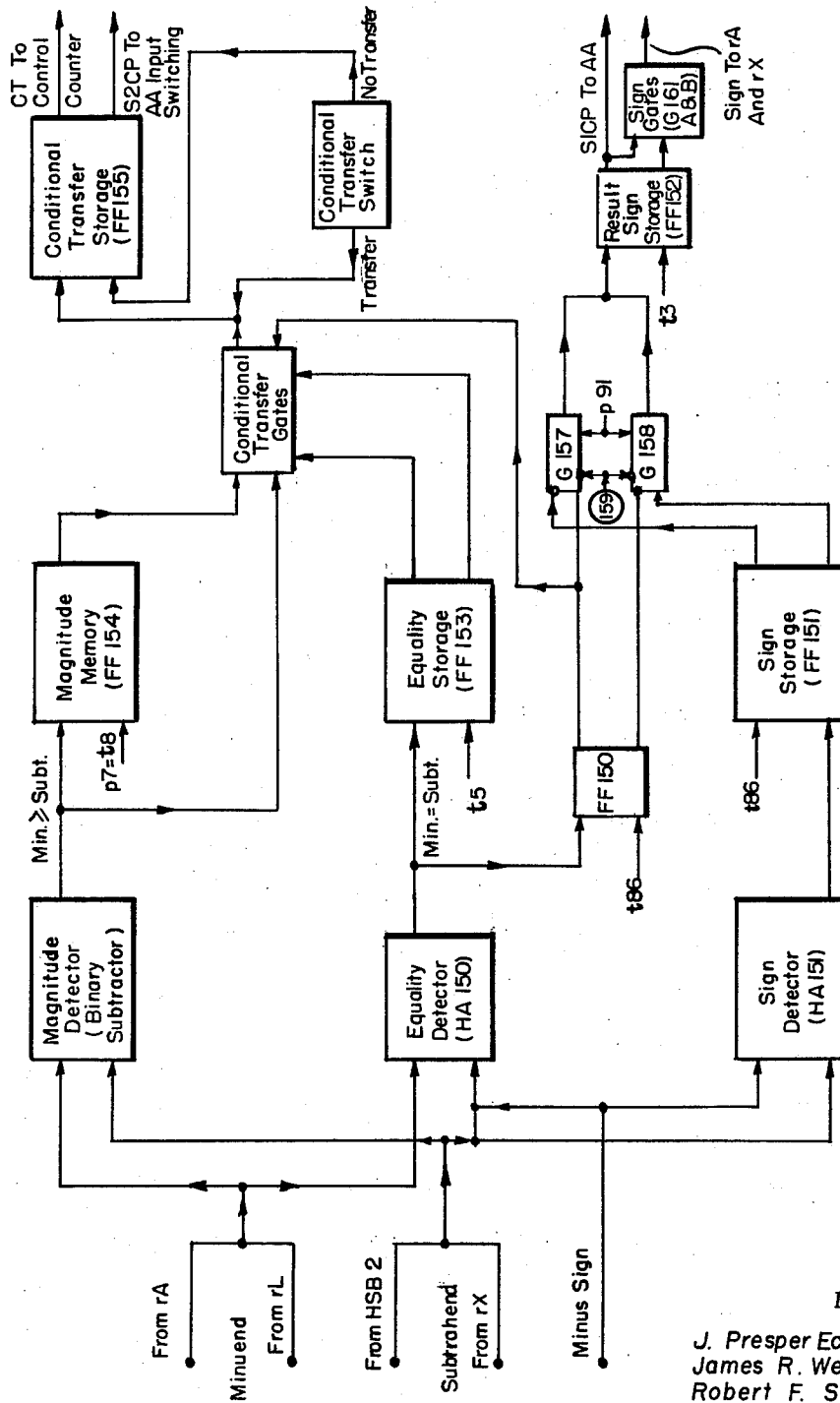


FIG. 6e

INVENTORS

J. Presper Eckert, Jr.
James R. Weiner
Robert F. Shaw
H. Frazer Welsh

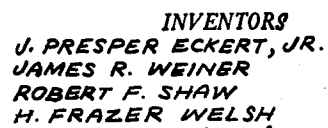
BY

William Holman
ATTORNEY

May 12, 1964 J. P. ECKERT, JR., ETAL 3,133,190
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FIG. 7a



BY *George Veltzsch*
ATTORNEY.

May 12, 1964

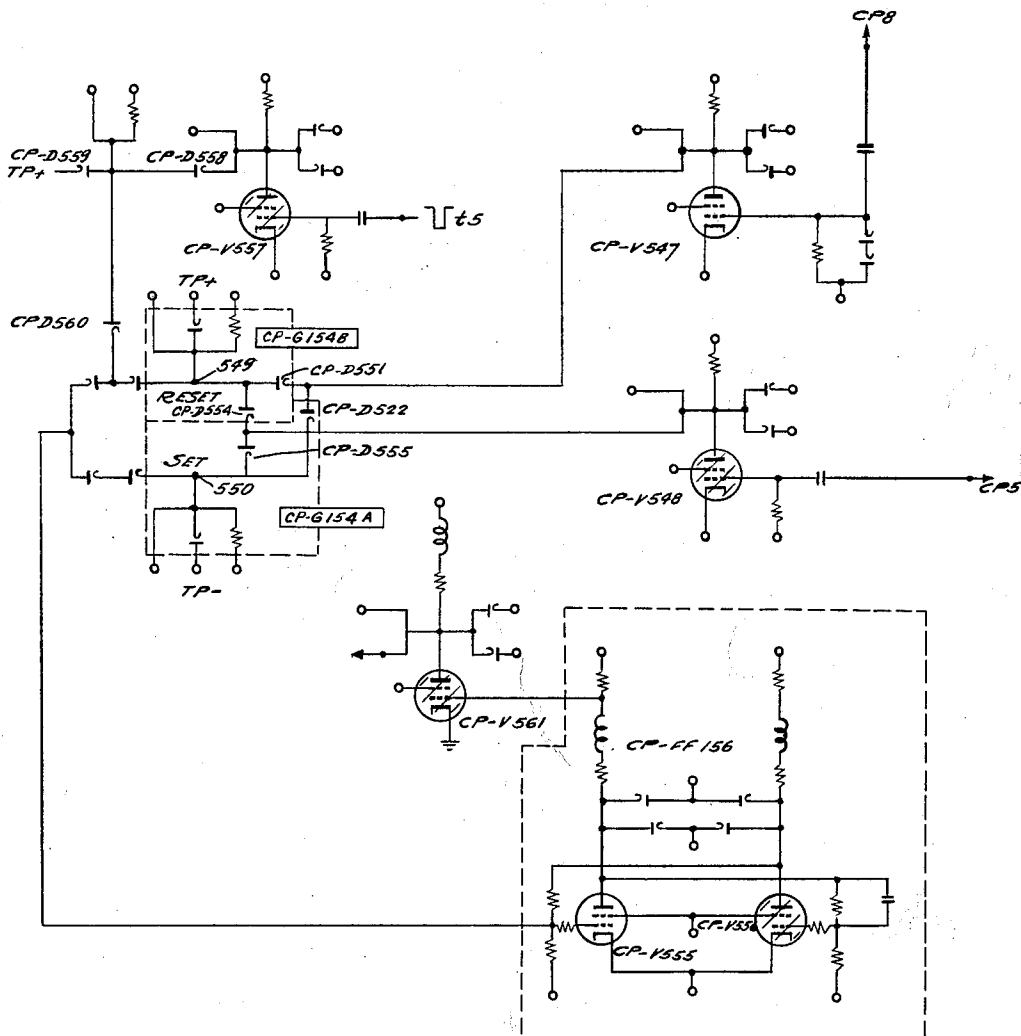
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FIG. 7b



INVENTORS
J. PRESER ECKERT, JR.
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ROBERT F. SHAW
H. FRAZER WELSH

BY *George V. Veltz*
ATTORNEY

May 12, 1964

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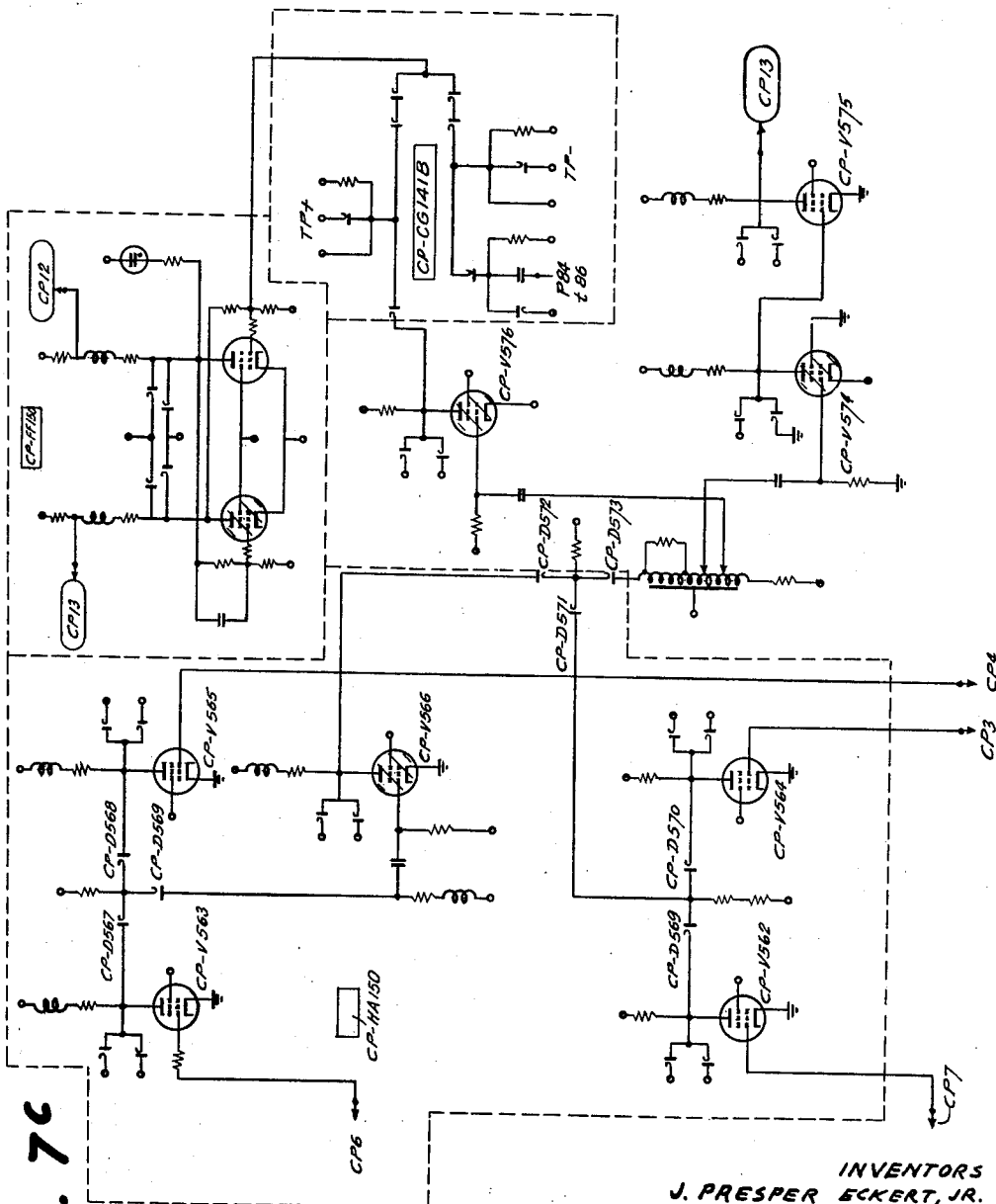


FIG. 7C

INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

BY *George F. Kelly* ATTORNEY

May 12, 1964

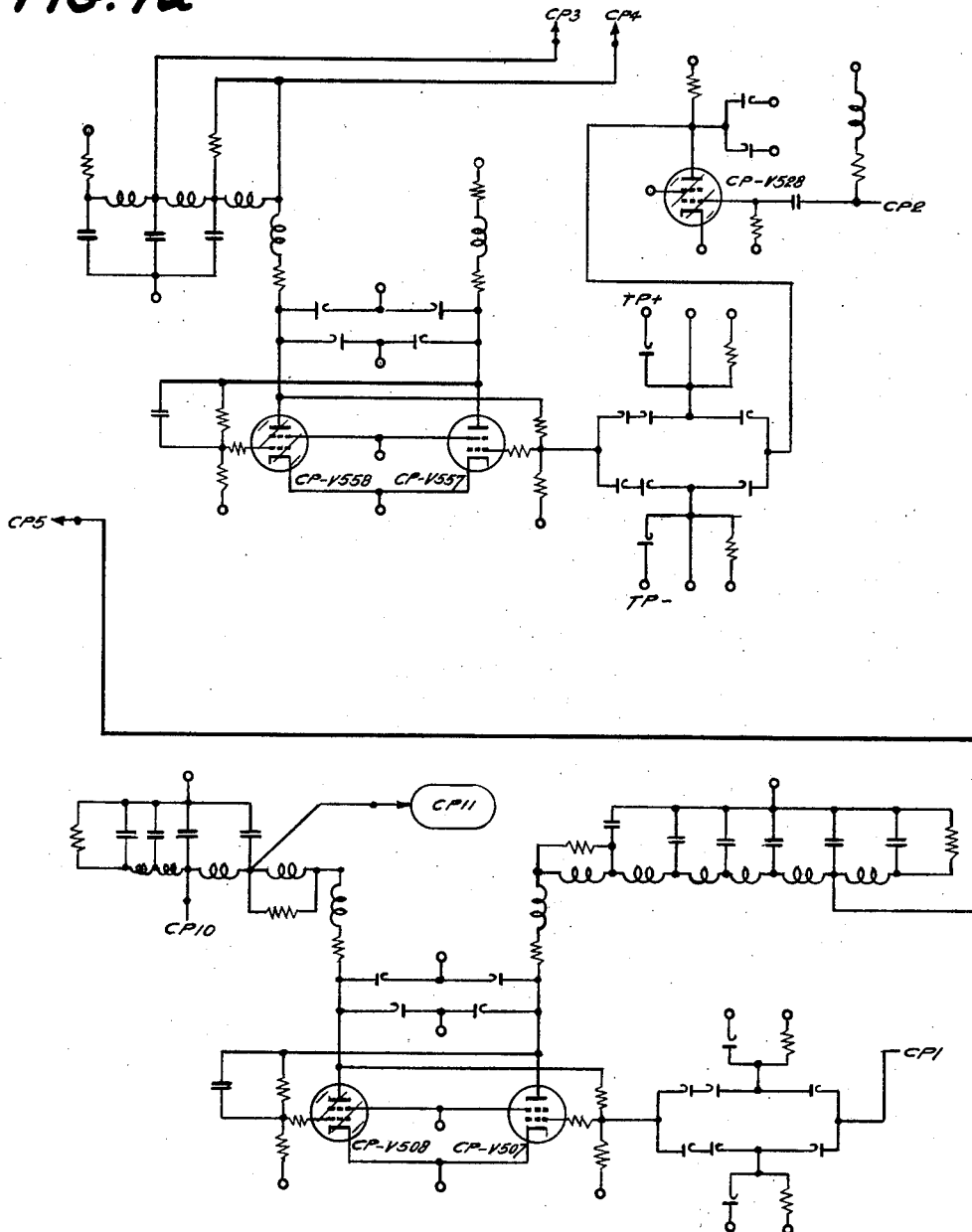
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FIG. 7d



INVENTORS
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ROBERT F. SHAW
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BY *Henry R. [Signature]*
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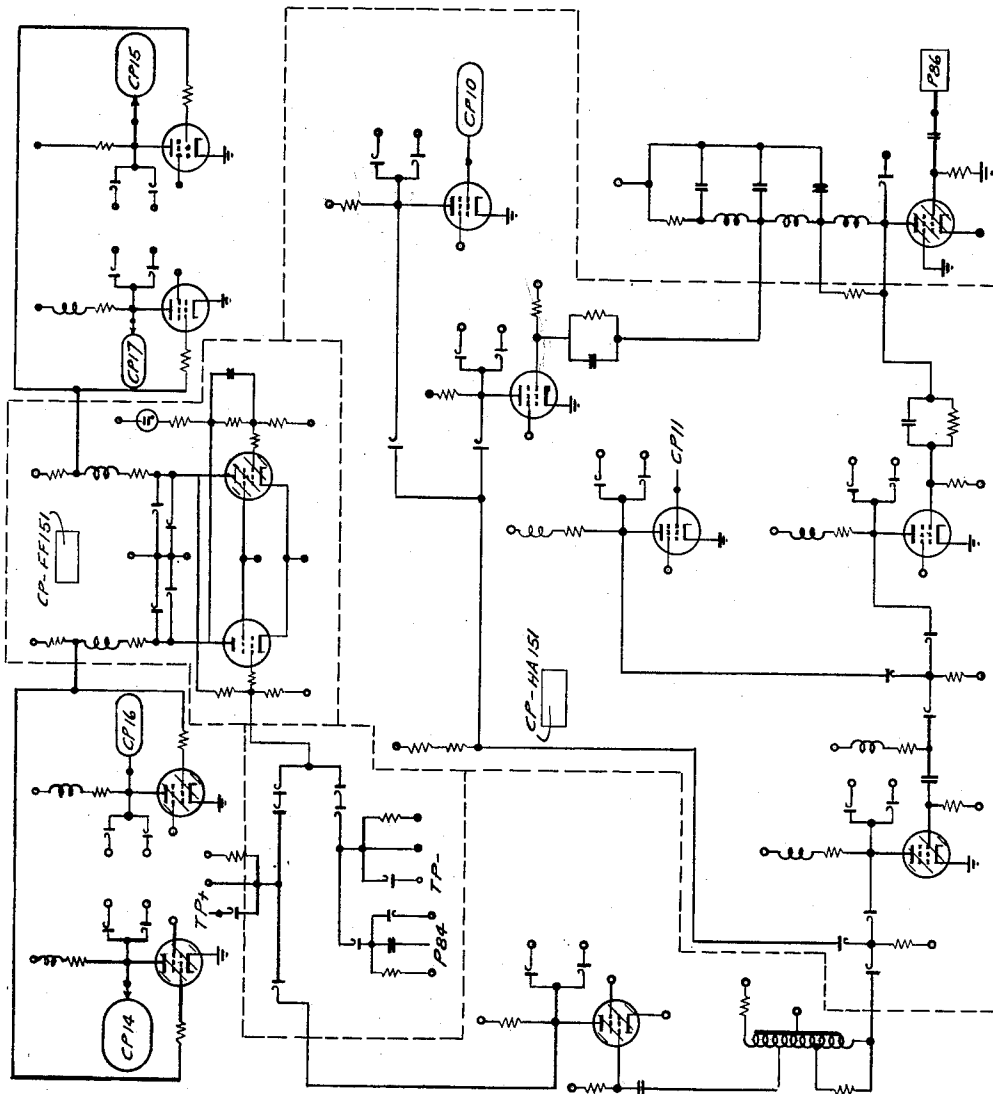


FIG. 7e

INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

BY

George Feltz
ATTORNEY

May 12, 1964

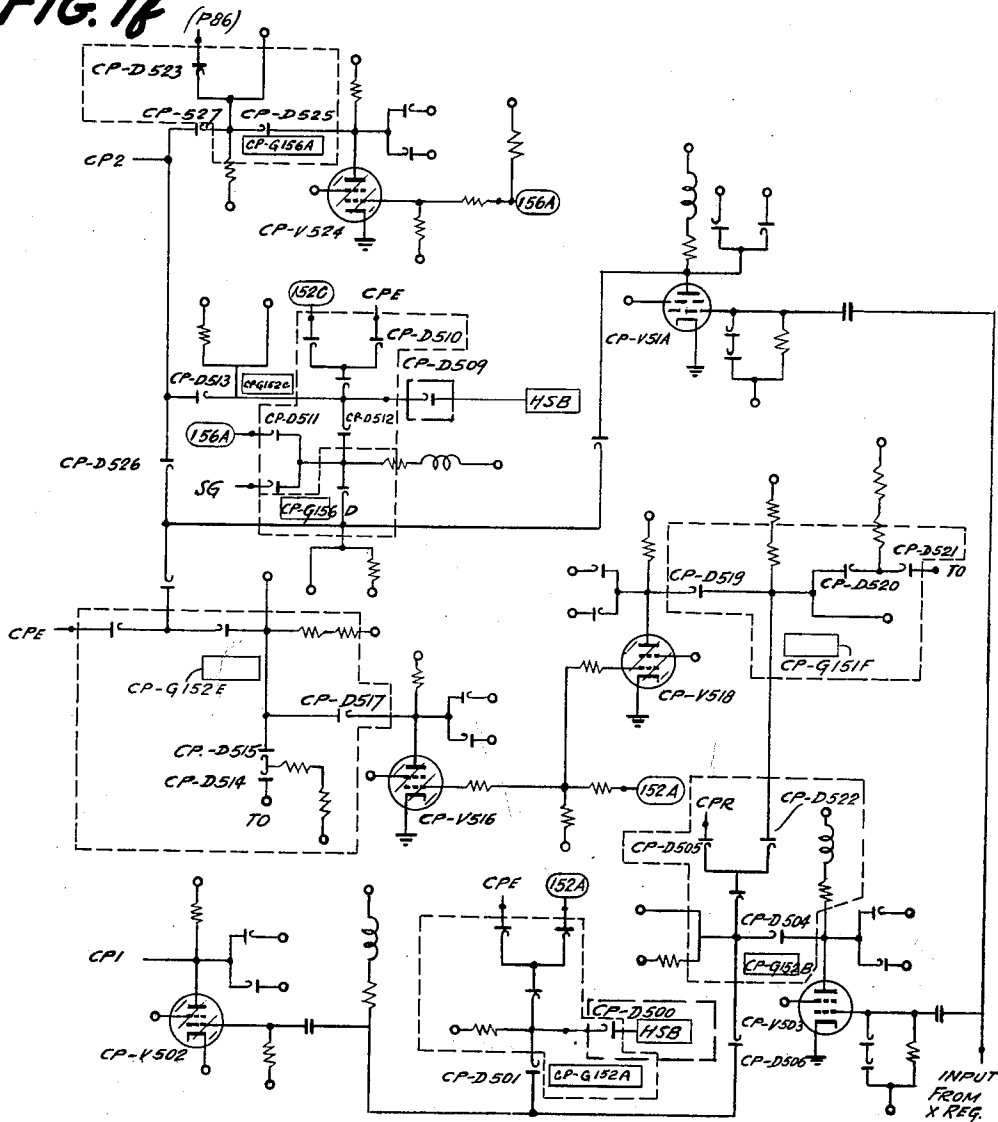
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FIG. 7f



INVENTORS

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H. FRAZER WELSH

BY

George Dellgroth
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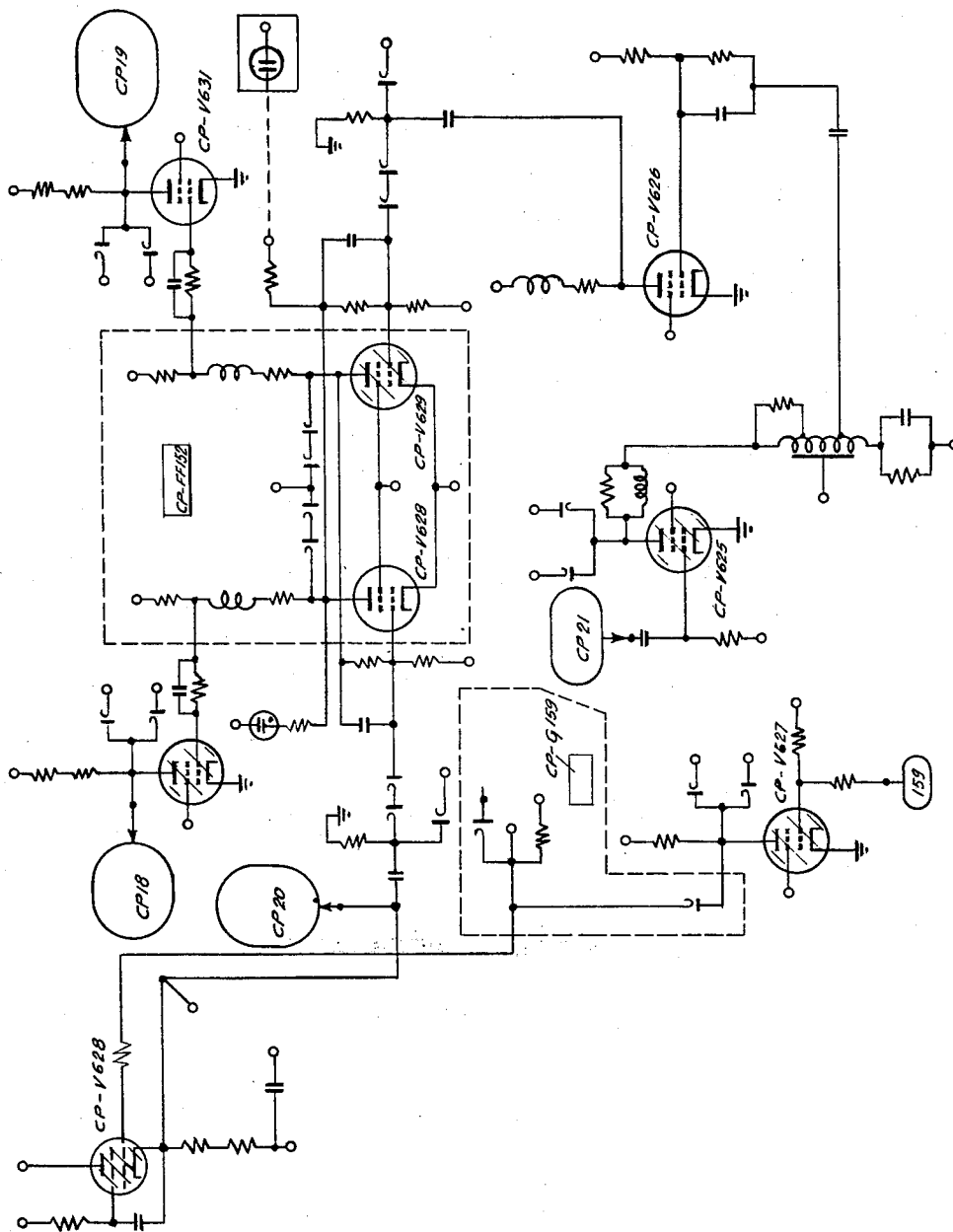


FIG. 79

INVENTORS

U. PRESER ECKERT, JR.

JAMES R. WEINER

ROBERT F. SHAW

H. FRAZER WELSH

BY

George F. Welch
ATTORNEY

May 12, 1964

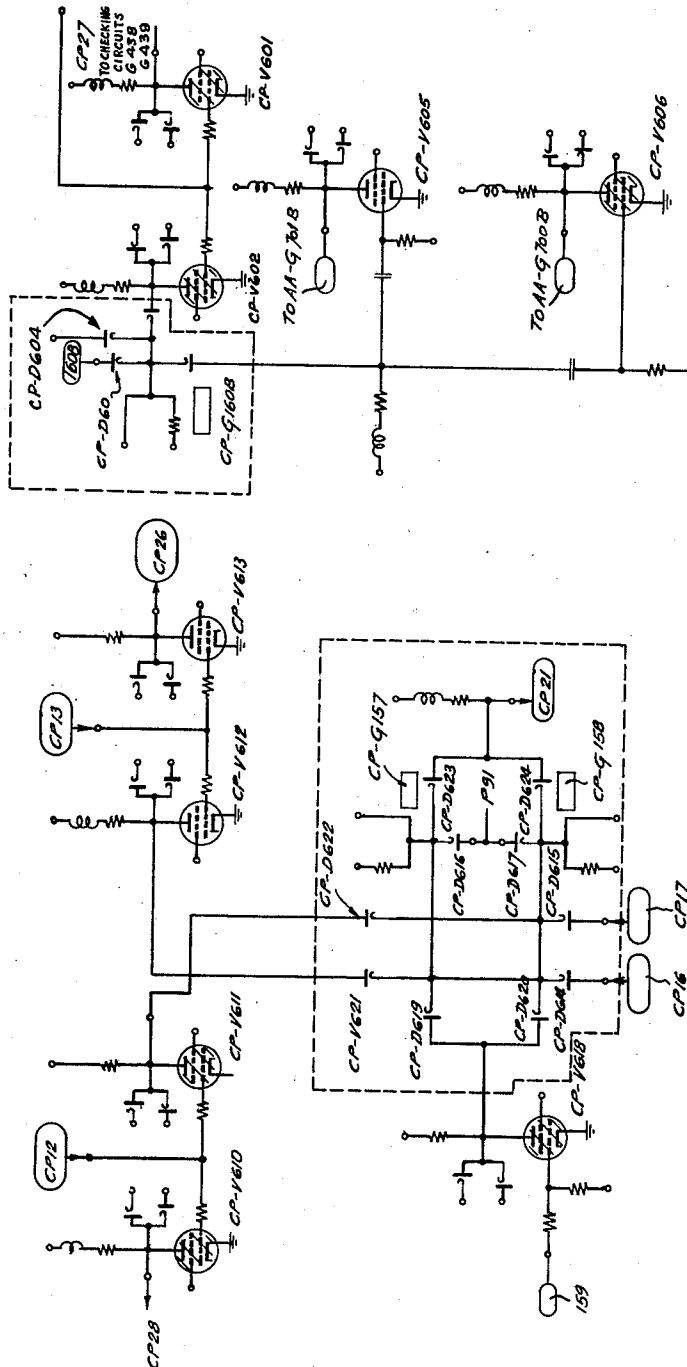
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FIG. 7c



INVENTORS
J. PRESER ECKERT, JR.
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H. FRAZER WELSH

BY *George V. Veltz* ATTORNEY

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J. P. ECKERT, JR., ETAL
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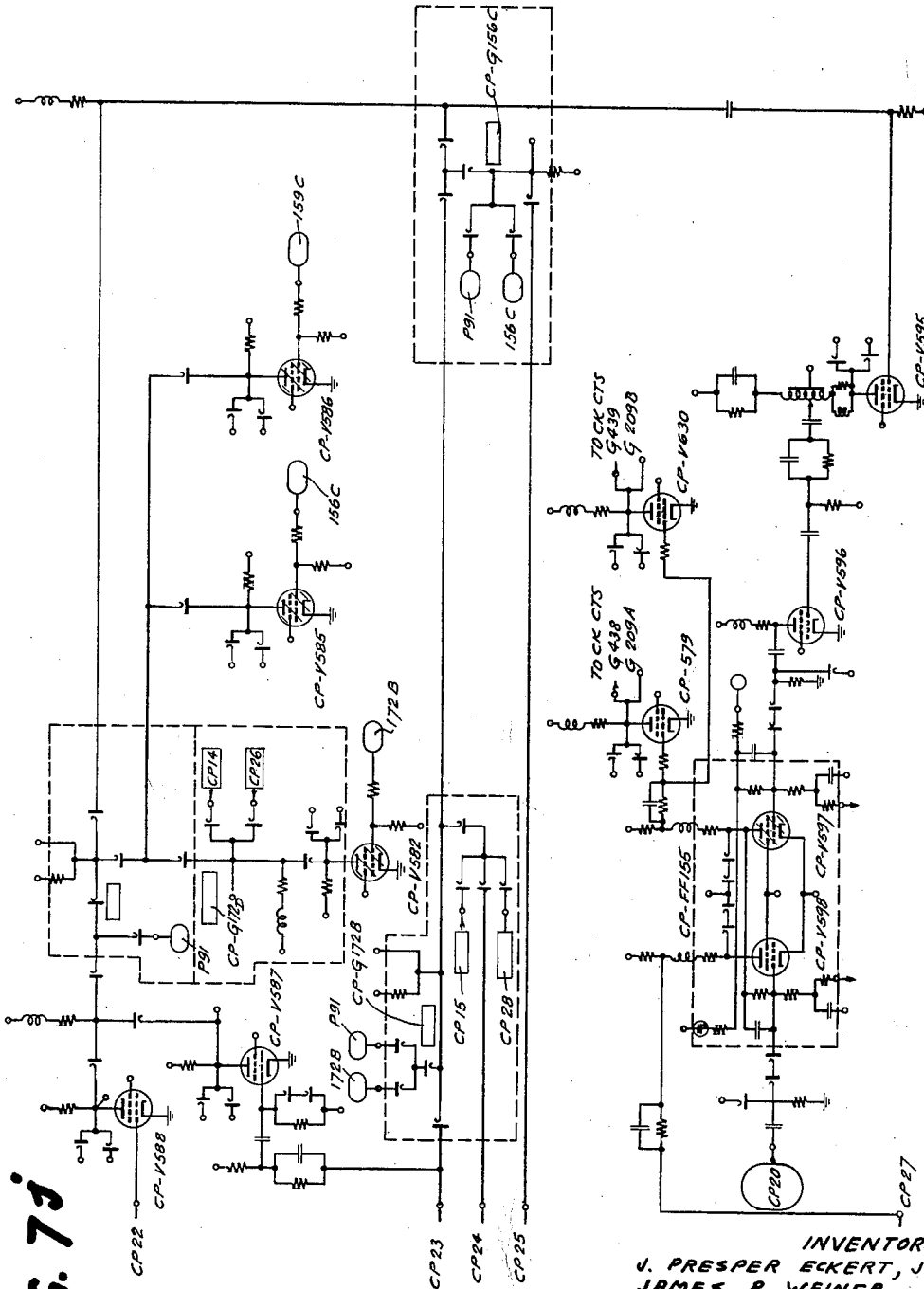


FIG. 7j

INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

BY *Samuel W. Elgert*
ATTORNEY

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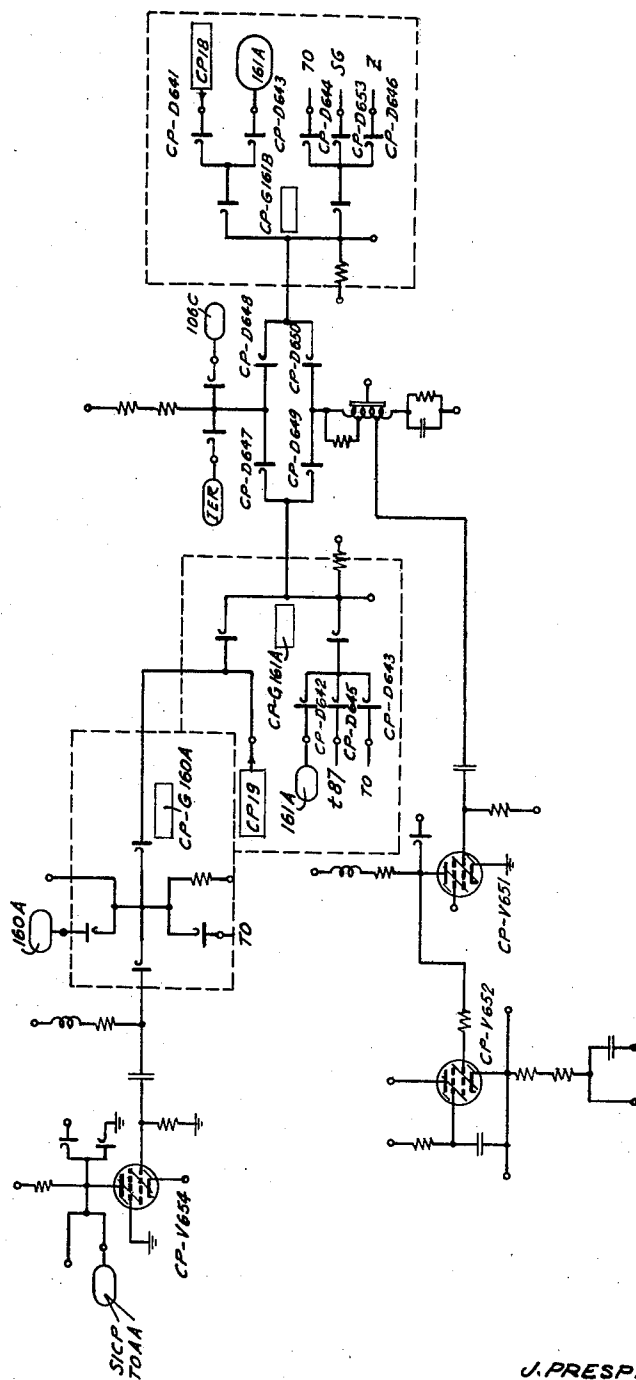


FIG. 7k

J. PRESPEER ECKERT, JR
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

BY *George W. Ritz*
ATTORNEY

May 12, 1964

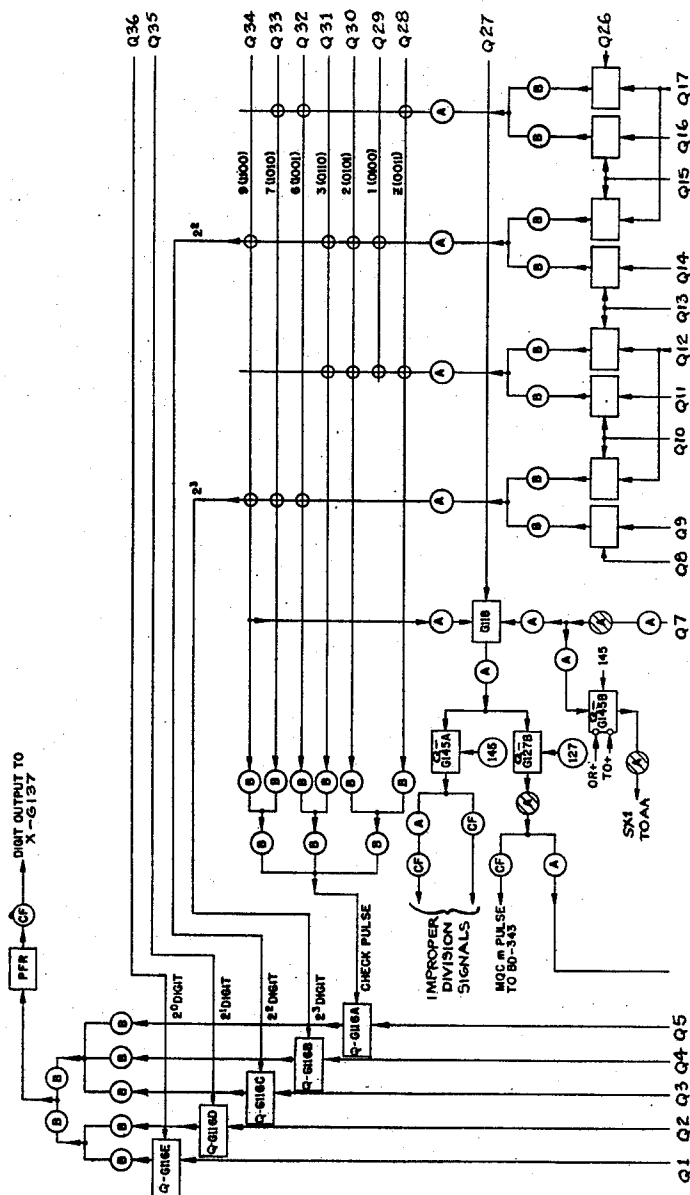
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110 Sheets-Sheet 21

FIG. 8a



INVENTORS

J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

BY

George V. Retzsch
ATTORNEY

May 12, 1964

J. P. ECKERT, JR., ETAL
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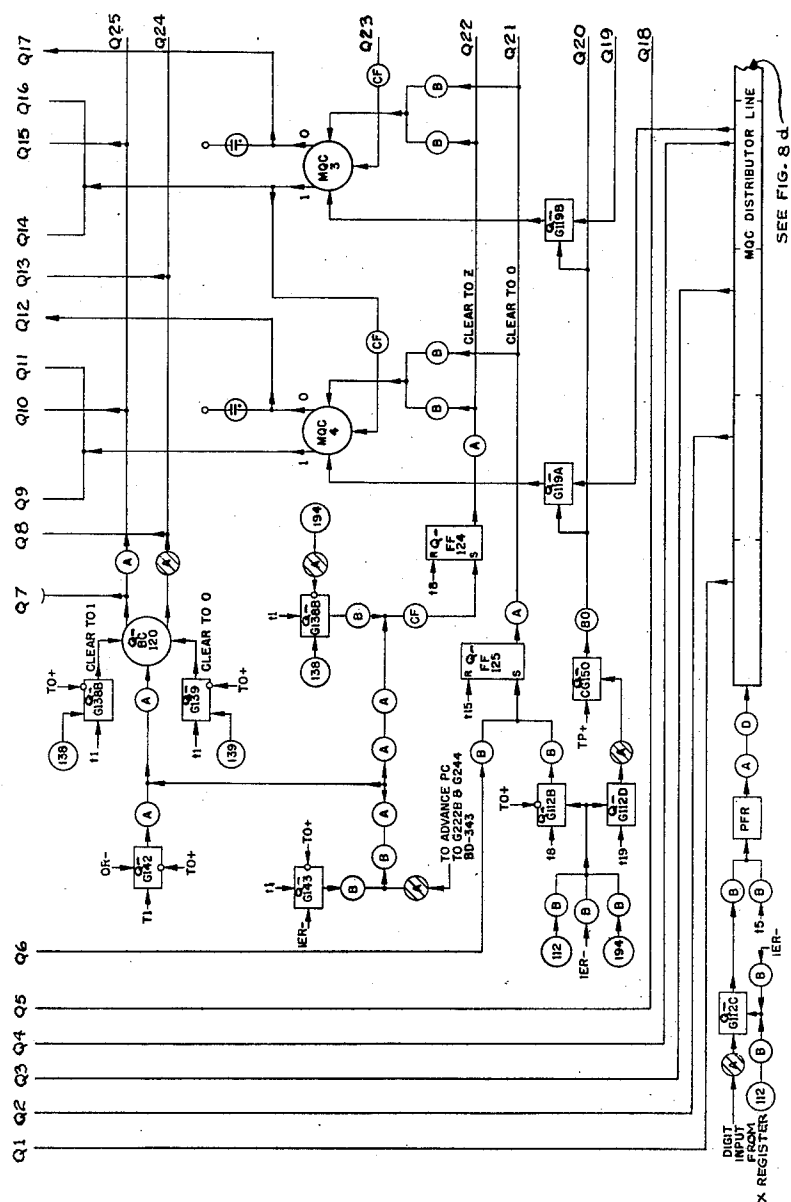


FIG. 8b

INVENTORS

J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

BY

George V. Retzsch
ATTORNEY

May 12, 1964

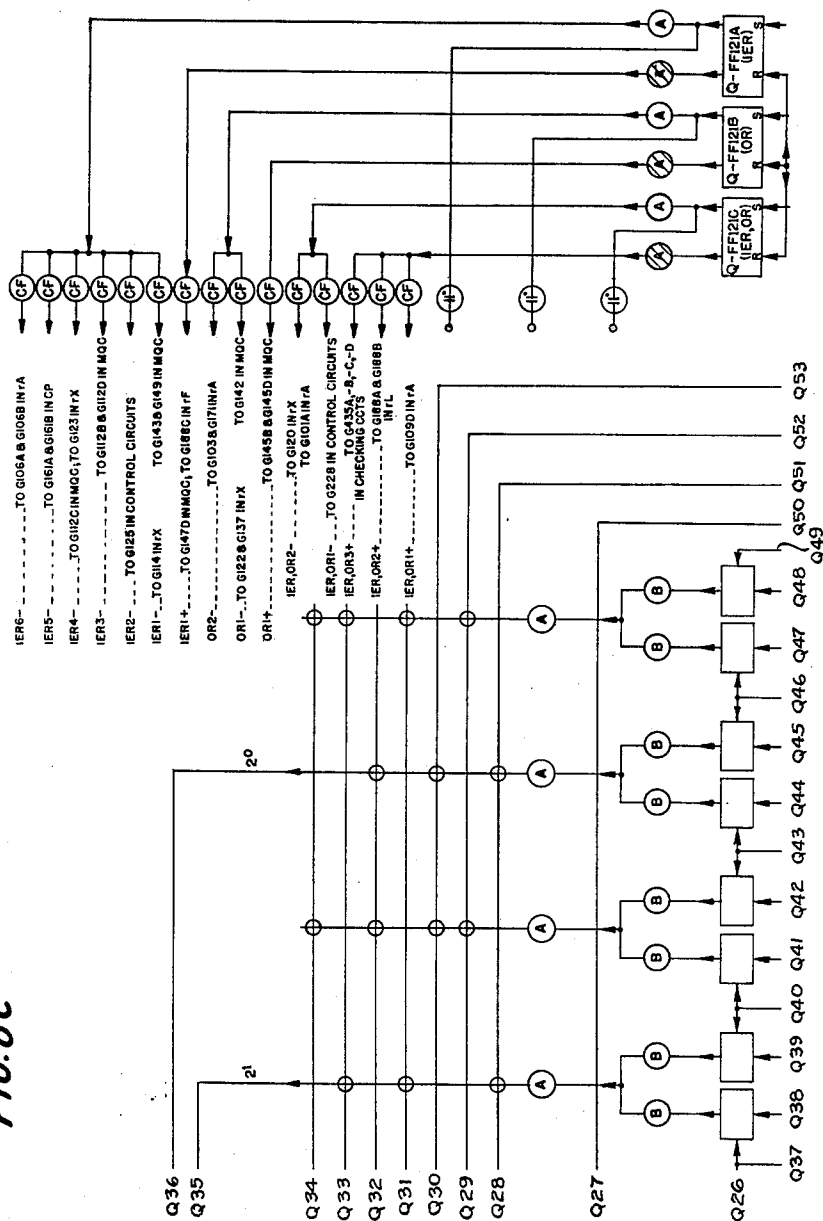
J. P. ECKERT, JR., ETAL
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BINARY CODED ALPHANUMERIC CHARACTERS

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110 Sheets-Sheet 23

FIG. 8c



INVENTORS

J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

BY

George V. Retzsch
ATTORNEY

May 12, 1964

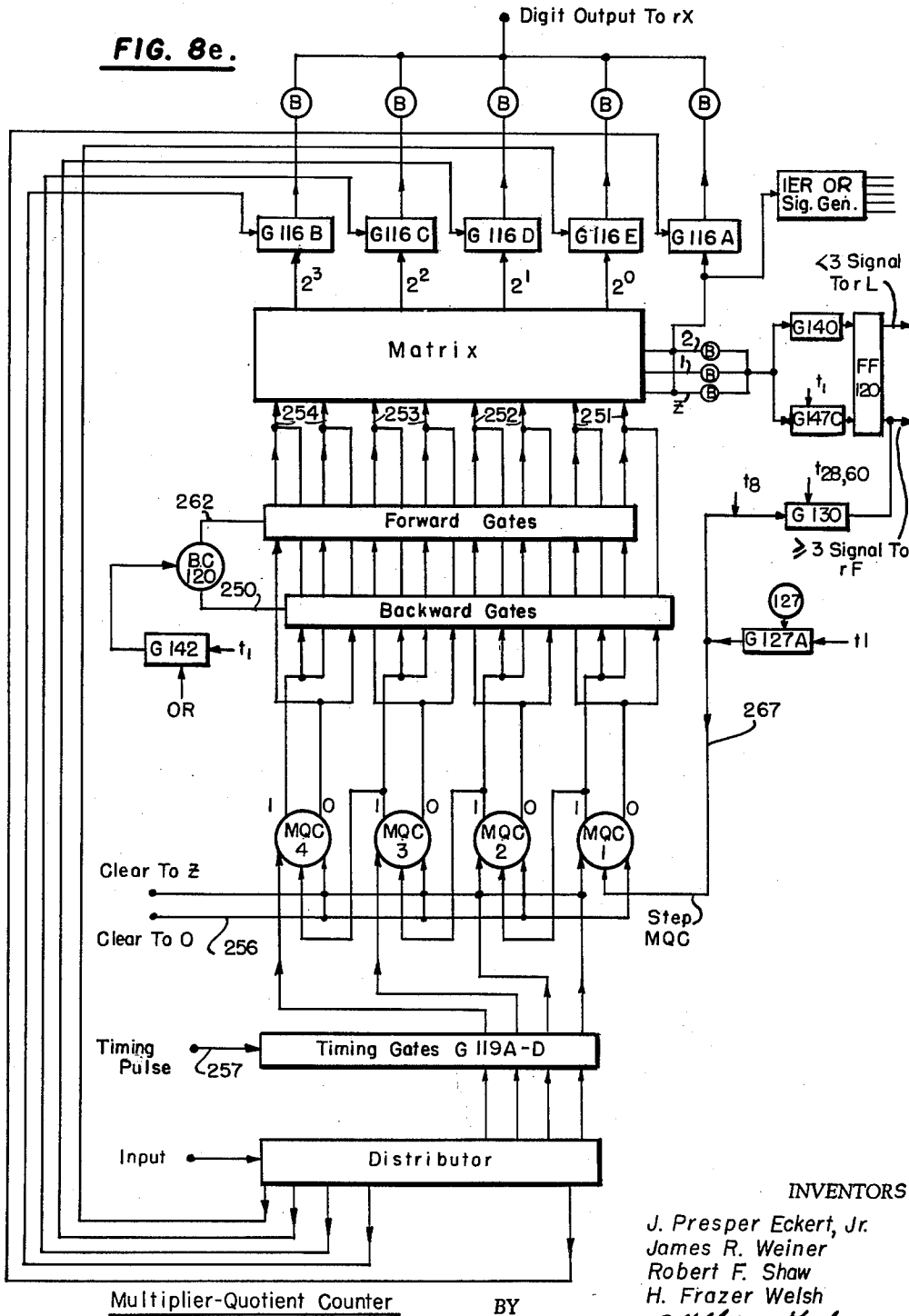
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FIG. 8e.



Multiplier-Quotient Counter

BY

INVENTORS

J. Presper Eckert, Jr.
James R. Weiner
Robert F. Shaw
H. Frazer Welsh

William Sholman
ATTORNEY

May 12, 1964

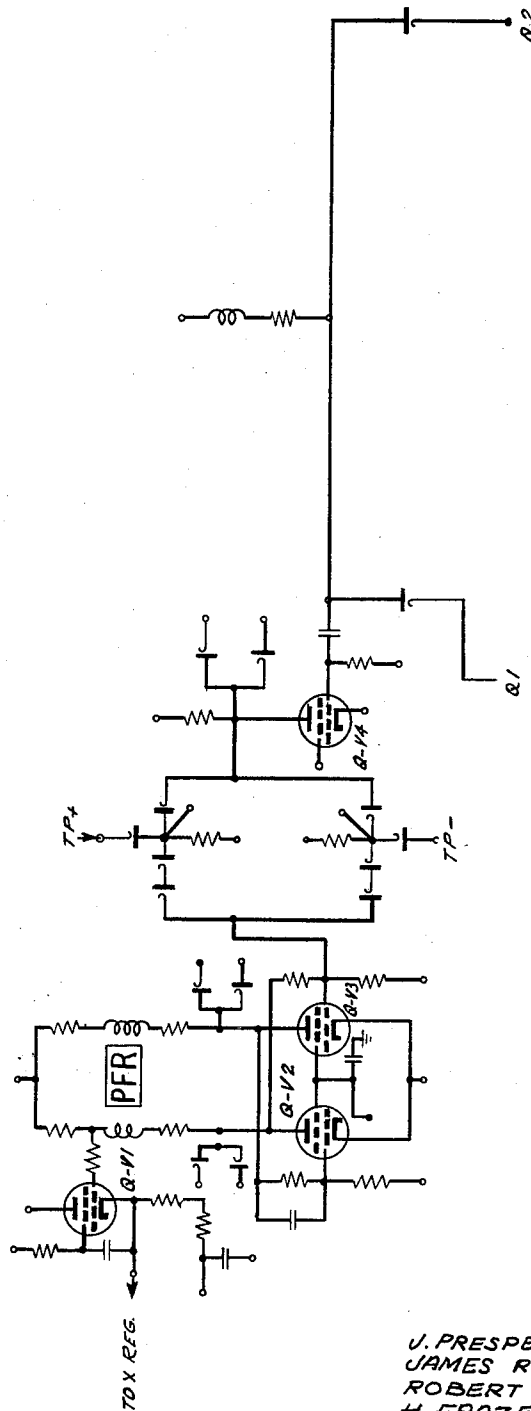
J. P. ECKERT, JR., ETAL
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110 Sheets-Sheet 26

FIG. 9a



INVENTORS
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BY *George F. Feltz* ATTORNEY

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J. P. ECKERT, JR., ETAL
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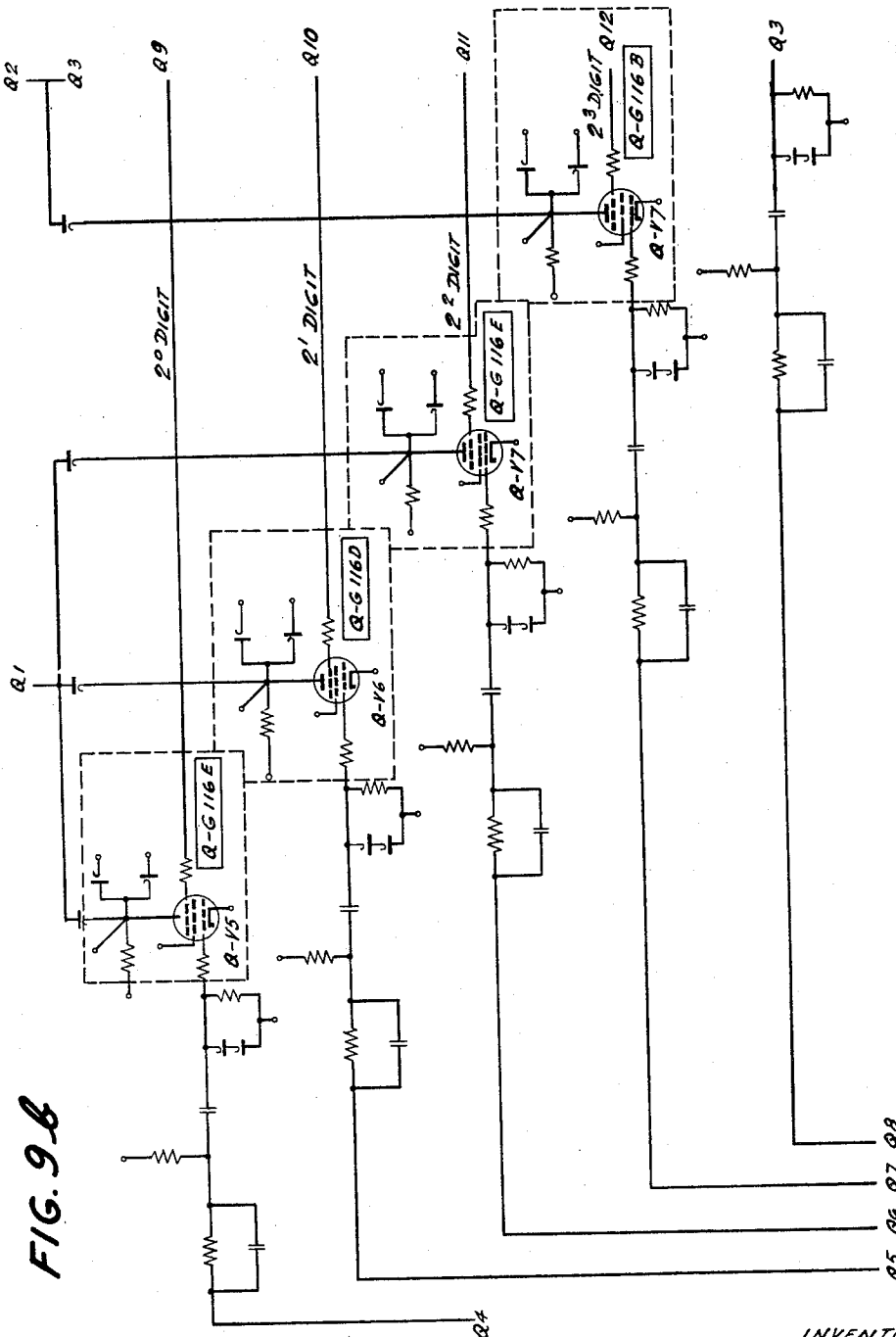


FIG. 9b

INVENTORS
J. PERSER ECKERT, JR.
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ROBERT F. SHAW
H. FRAZER WELSH

By *George P. Kelly*
ATTORNEY

May 12, 1964

J. P. ECKERT, JR., ETAL
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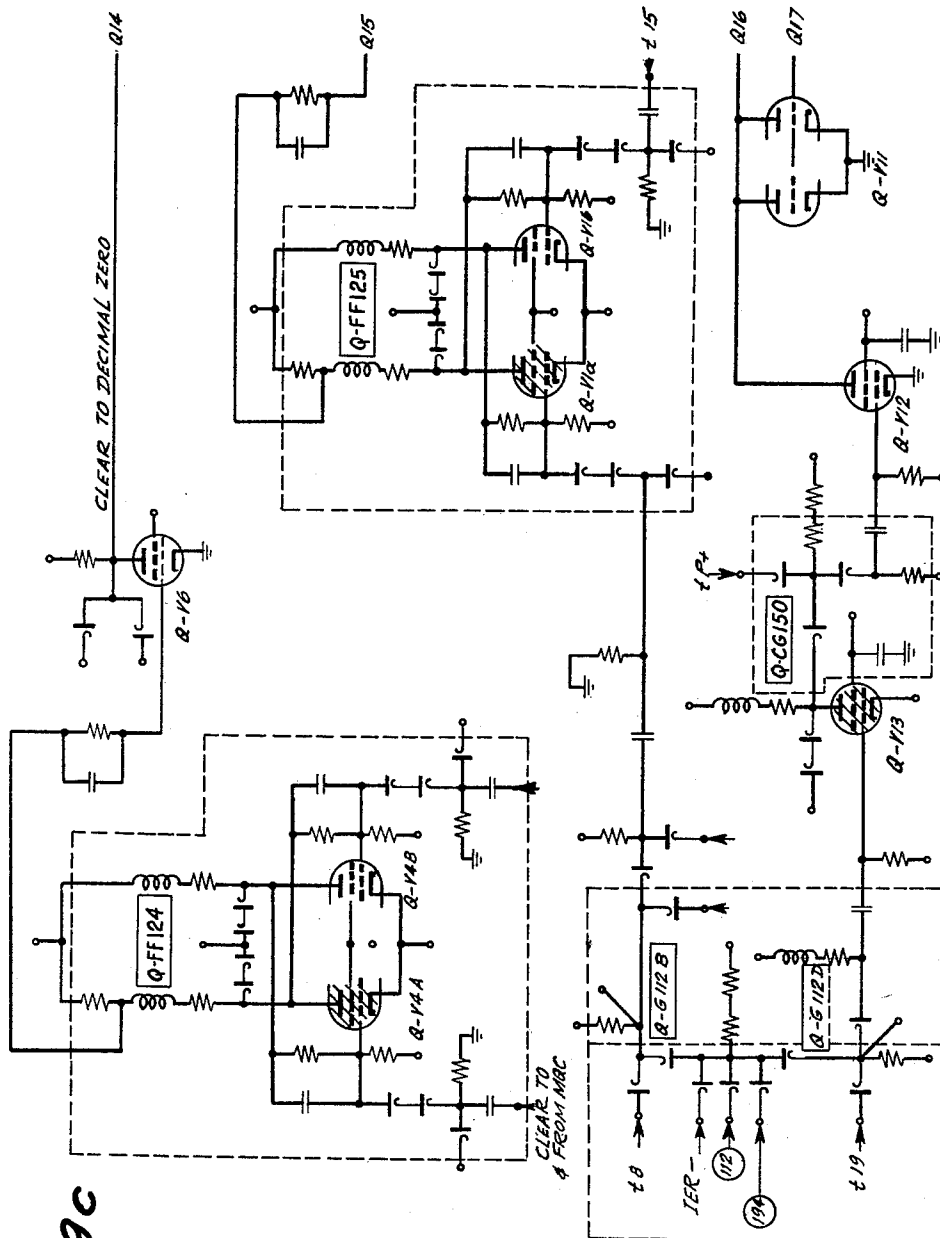


FIG. 9C

INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George F. Ritz*
ATTORNEY

May 12, 1964

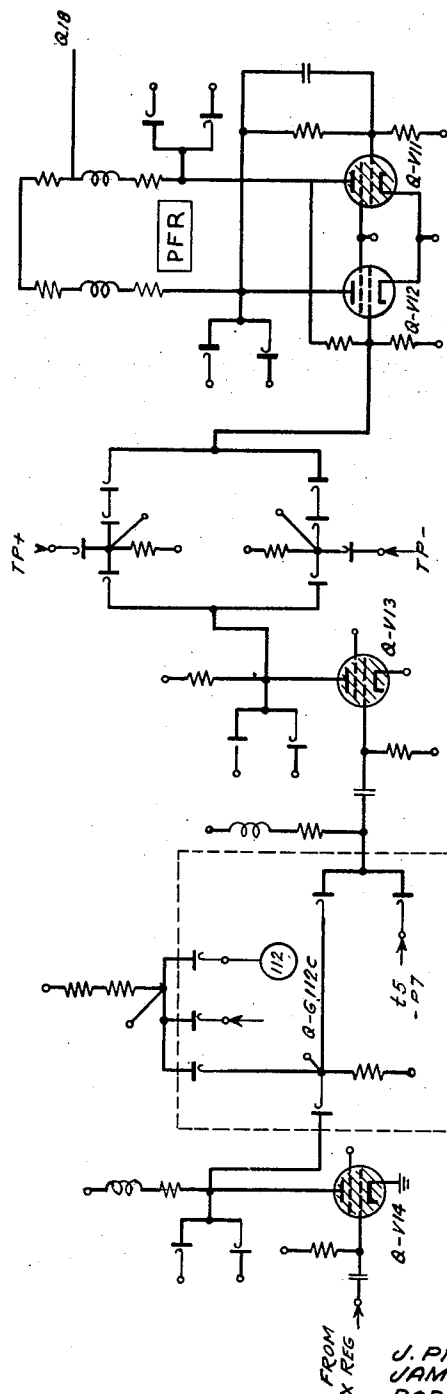
J. P. ECKERT, JR., ETAL
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110 Sheets-Sheet 29

FIG. 9d



INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *Ingert G. Roth* ATTORNEY

May 12, 1964

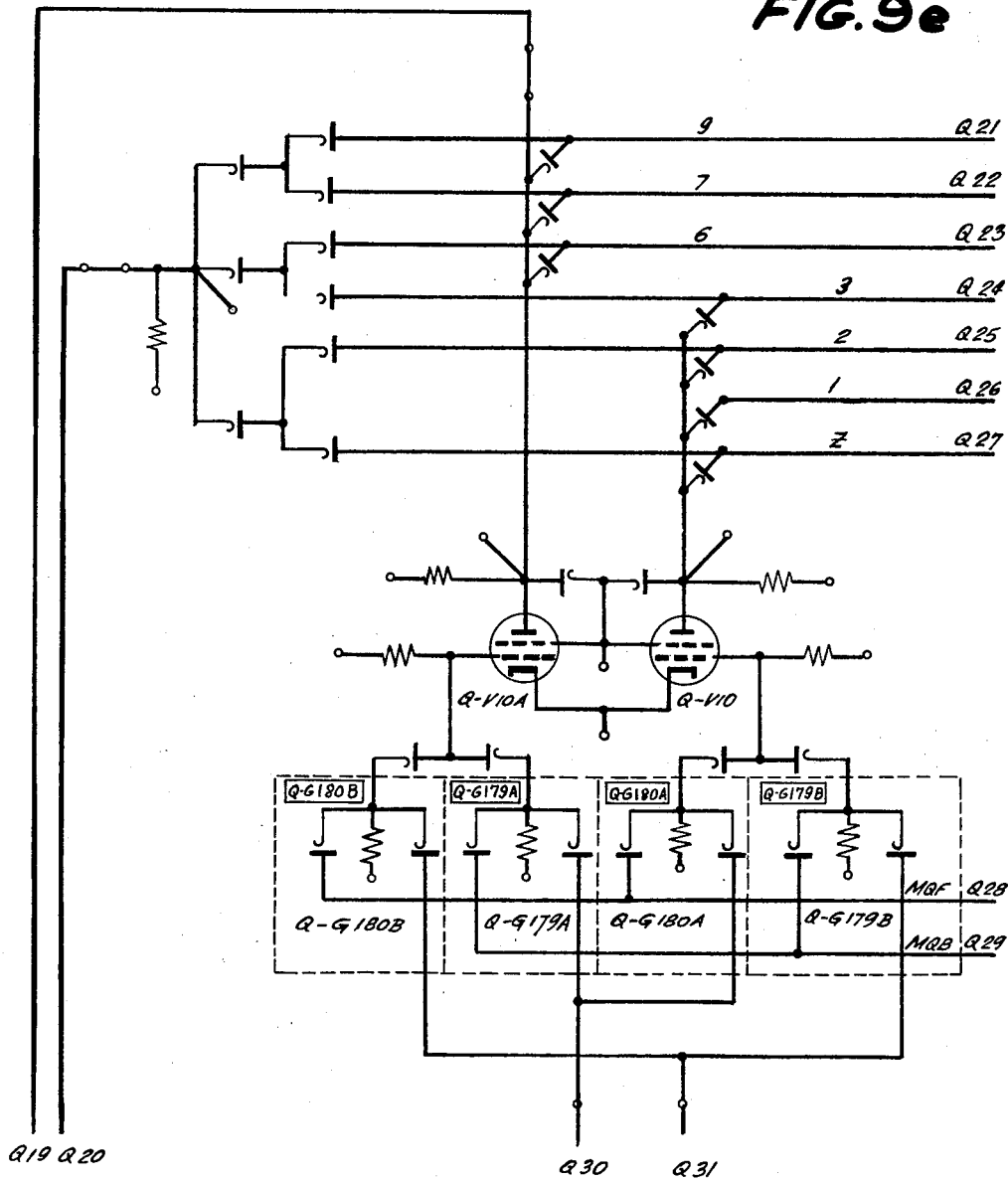
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110 Sheets-Sheet 30

FIG. 9e



INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George R. B. B. B.*
ATTORNEY

May 12, 1964

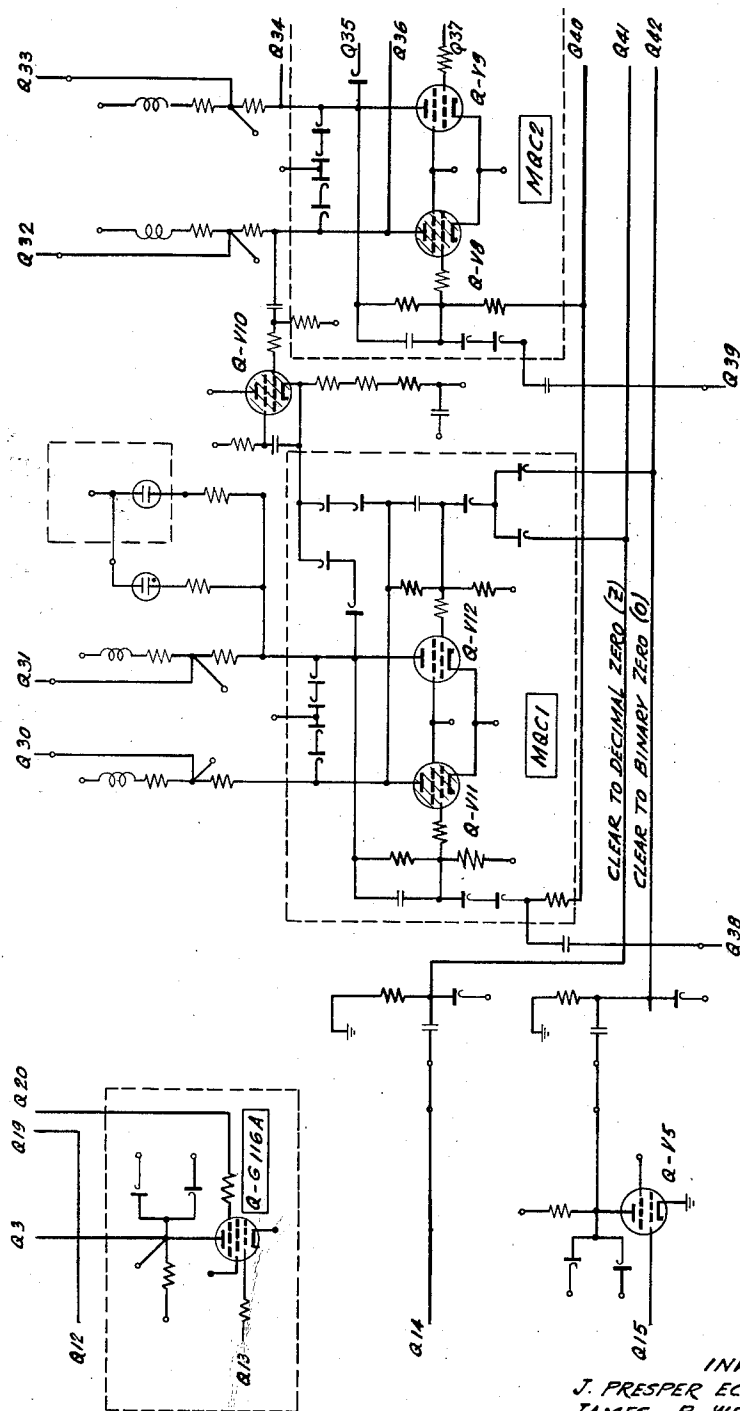
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FIG. 9f



INVENTORS
J. PERSPER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

BY *George V. Roth*
ATTORNEY

May 12, 1964

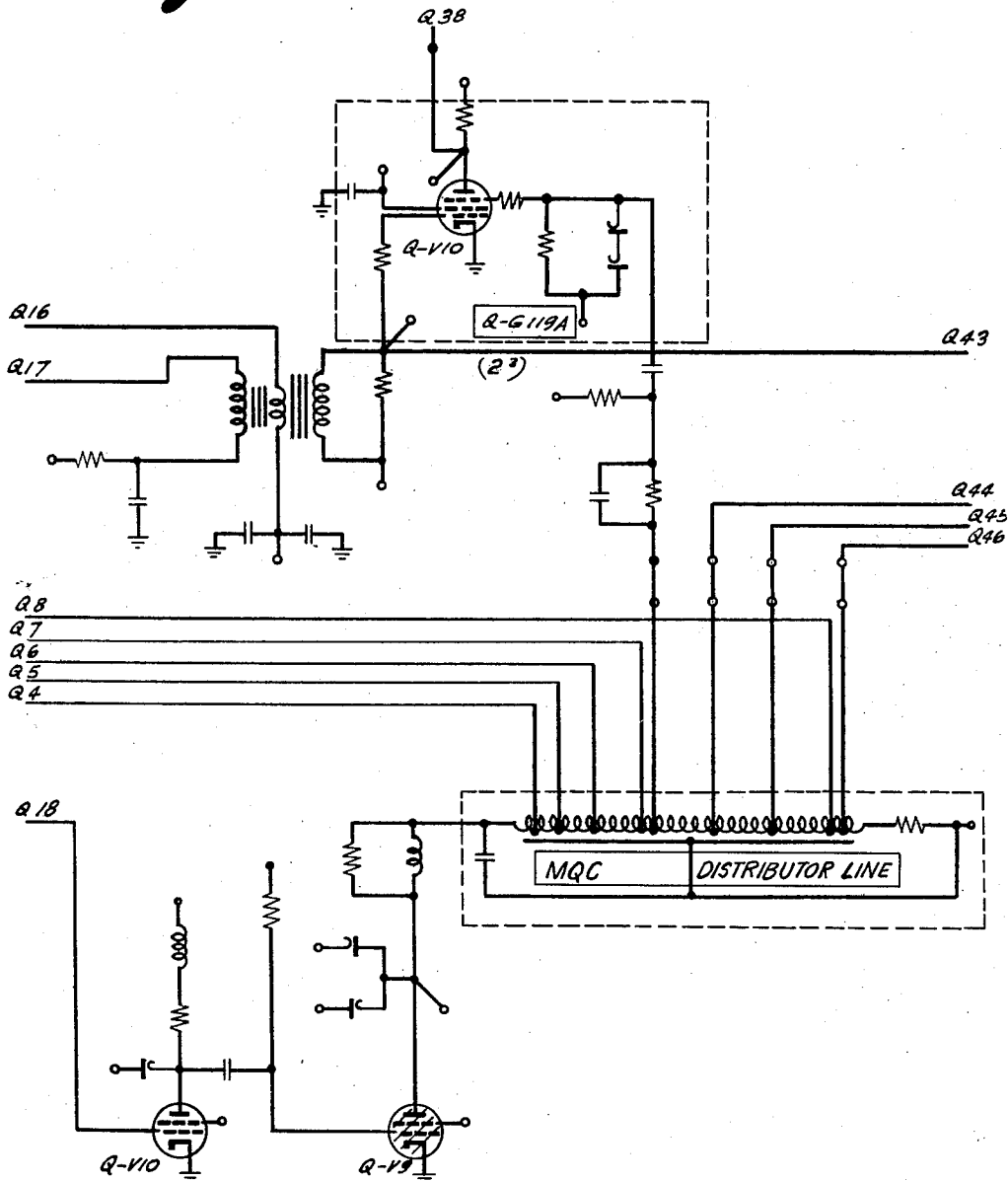
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110 Sheets-Sheet 32

FIG. 9g



INVENTORS
J. PRESER ECKERT, JR.
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H. FRAZER WELSH
BY *George Feltz* ATTORNEY

May 12, 1964

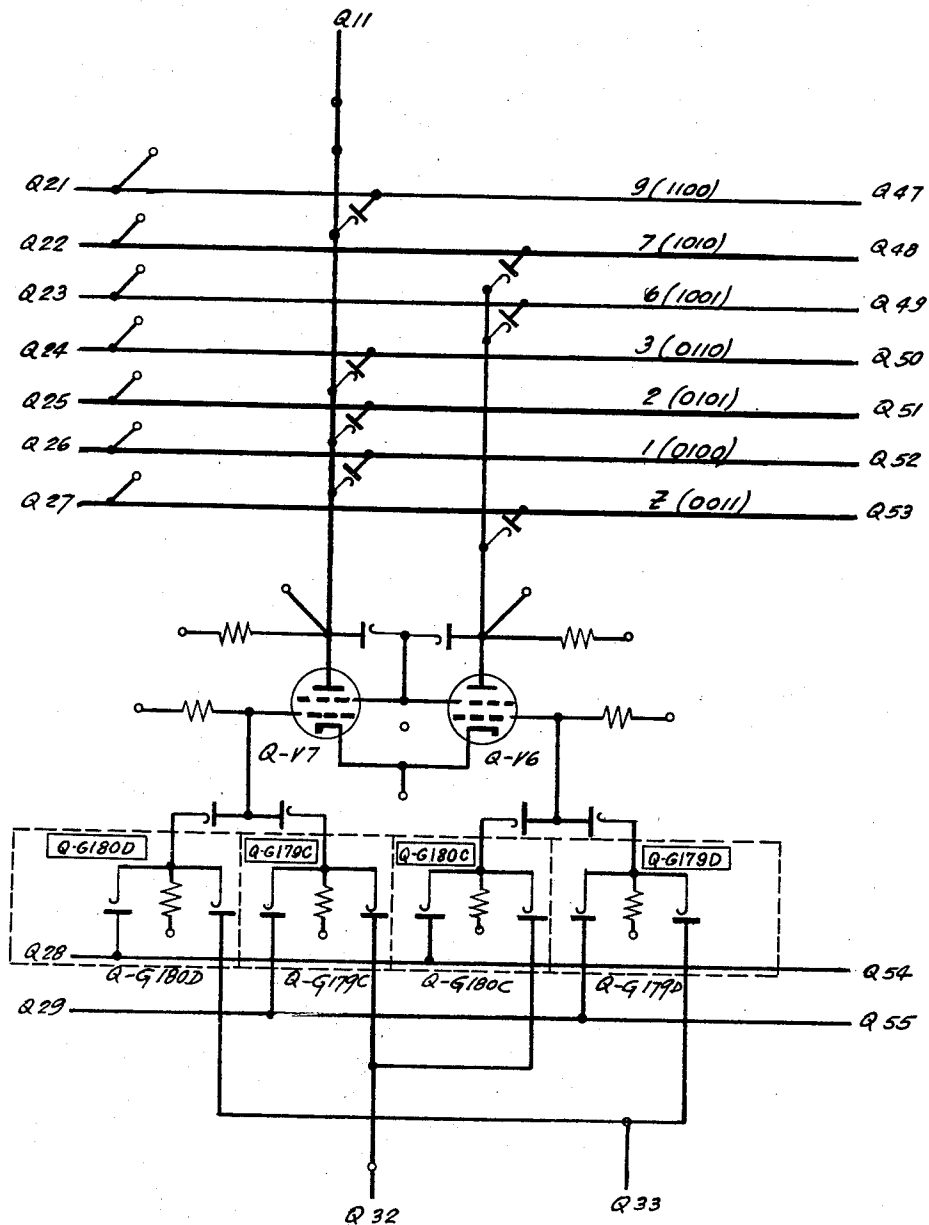
J. P. ECKERT, JR., ETAL
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FIG. 9h



INVENTORS

J. PRESER ECKERT, JR.

JAMES R. WEINER

ROBERT F. SHAW

H. FRAZER WELSH

BY *George Veltz*
ATTORNEY

May 12, 1964

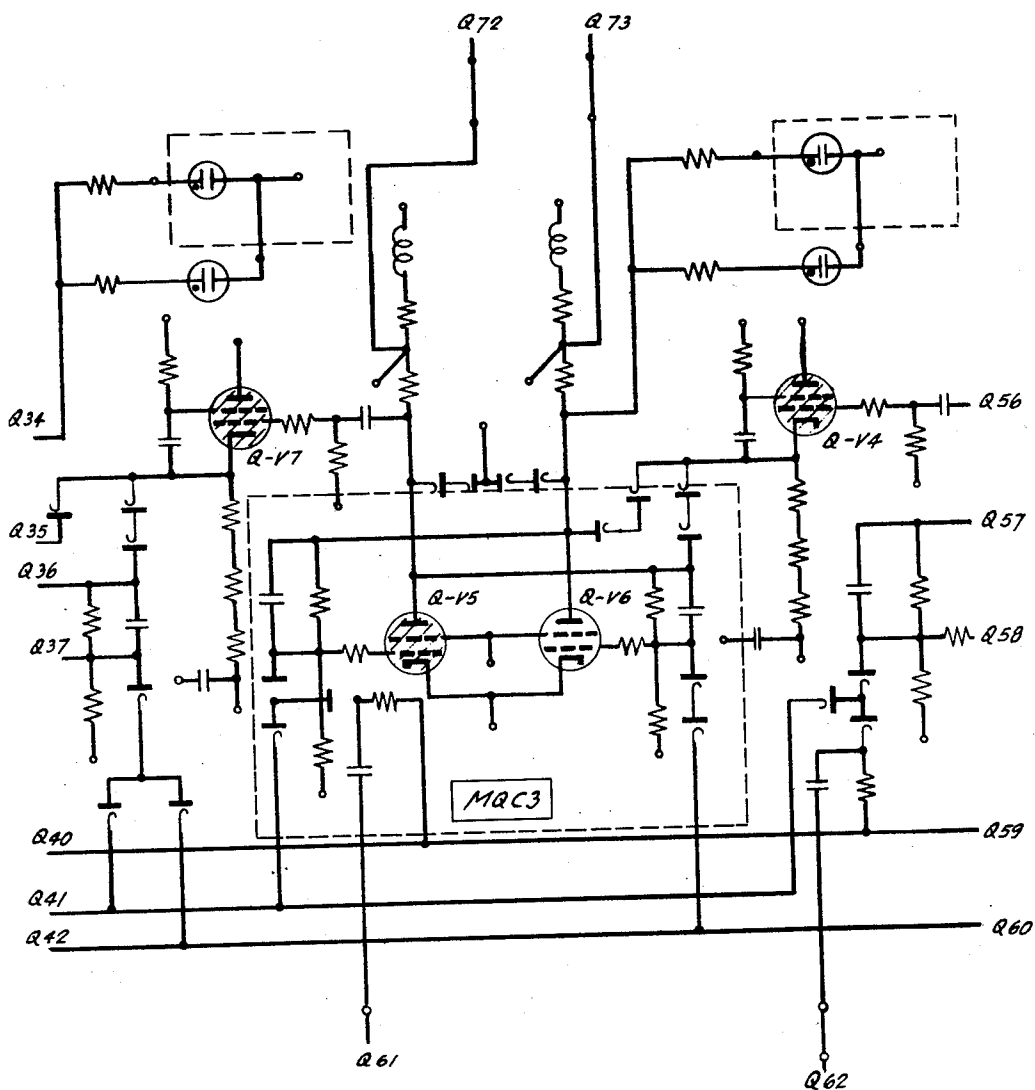
J. P. ECKERT, JR., ETAL
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110 Sheets-Sheet 34

FIG. 9i



INVENTORS
J. PRESER ECKERT, JR.
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H. FRAZER WELSH
BY *George P. Kelly*
ATTORNEY

May 12, 1964

J. P. ECKERT, JR., ET AL
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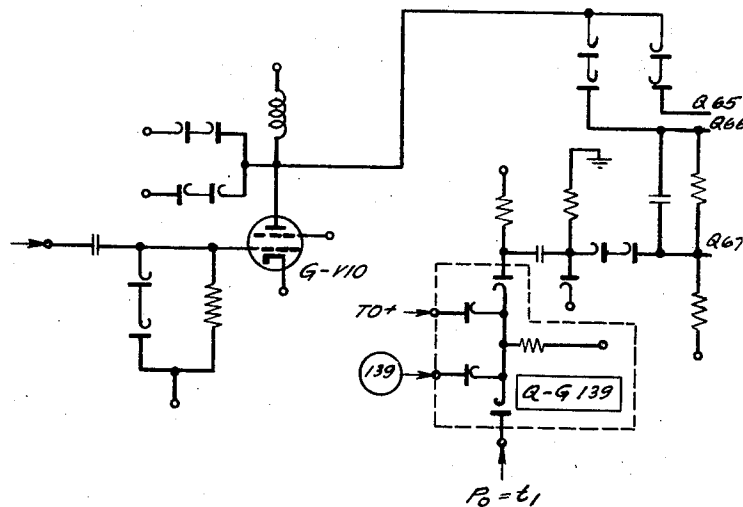
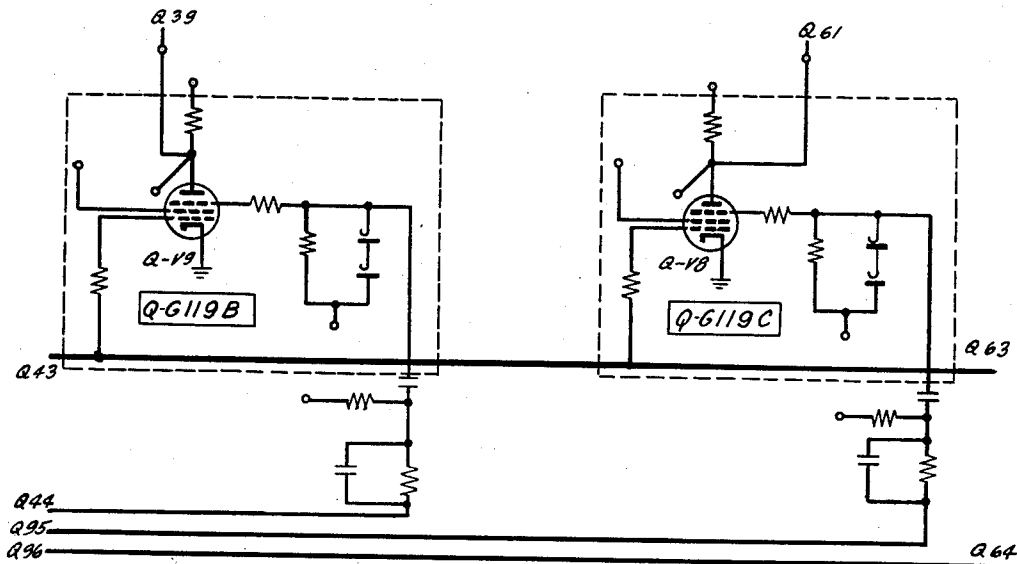


FIG. 9j

INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George P. Kelly*
ATTORNEY

May 12, 1964

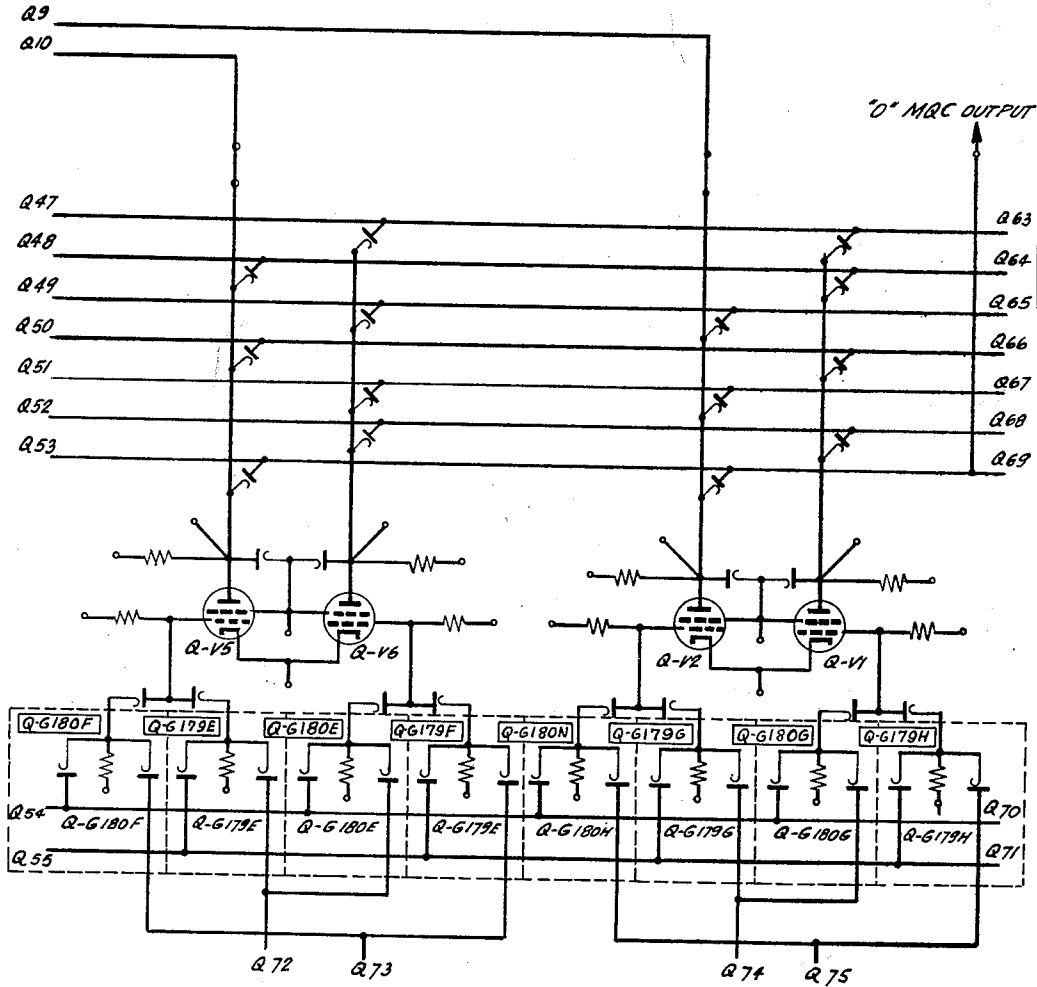
J. P. ECKERT, JR., ETAL
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110 Sheets-Sheet 36

FIG. 9A



INVENTORS
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H. FRAZER WELSH
BY *[Signature]* ATTORNEY

May 12, 1964

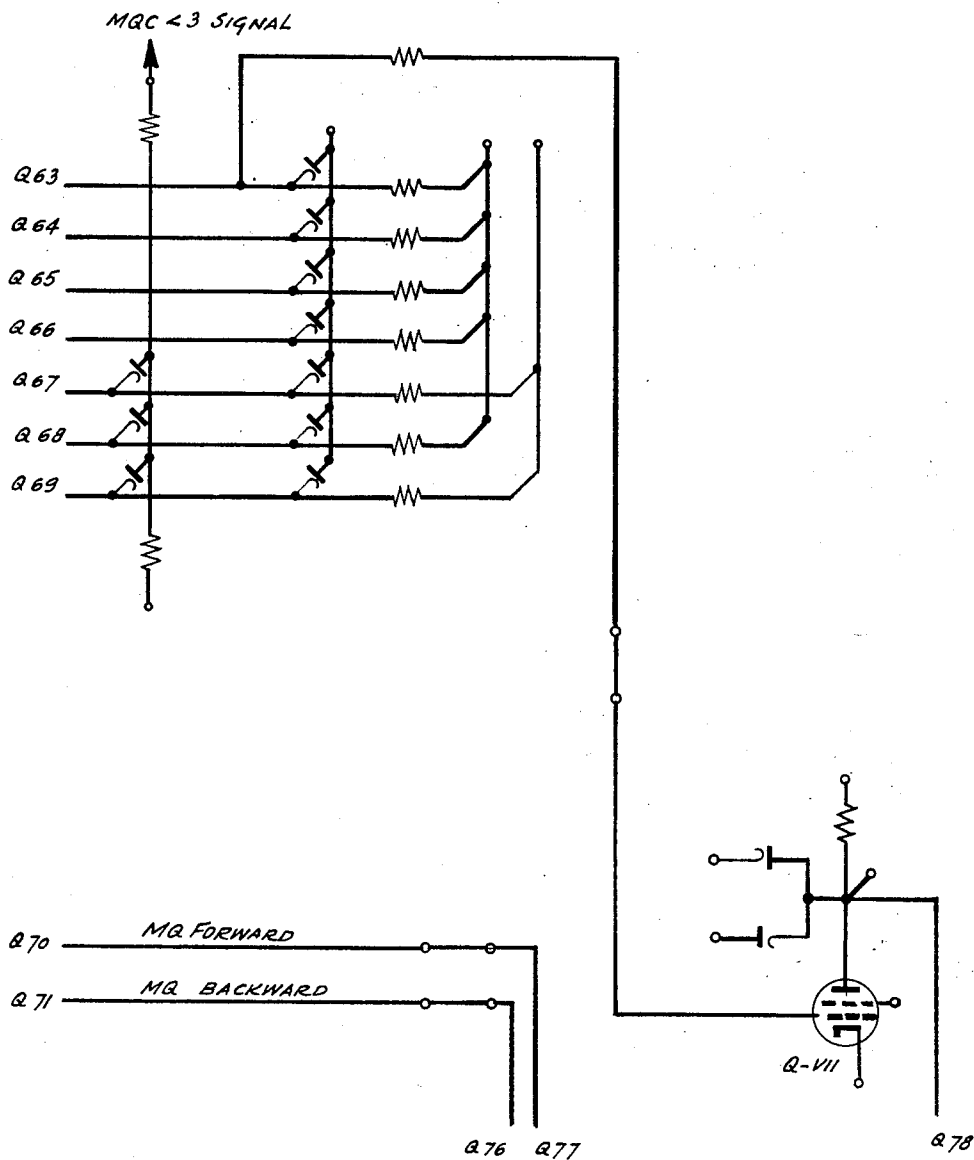
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FIG. 9e



INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George R. R. R.*
ATTORNEY

May 12, 1964

J. P. ECKERT, JR., ETAL
UNIVERSAL AUTOMATIC COMPUTER UTILIZING
BINARY CODED ALPHANUMERIC CHARACTERS

3,133,190

Filed March 31, 1952

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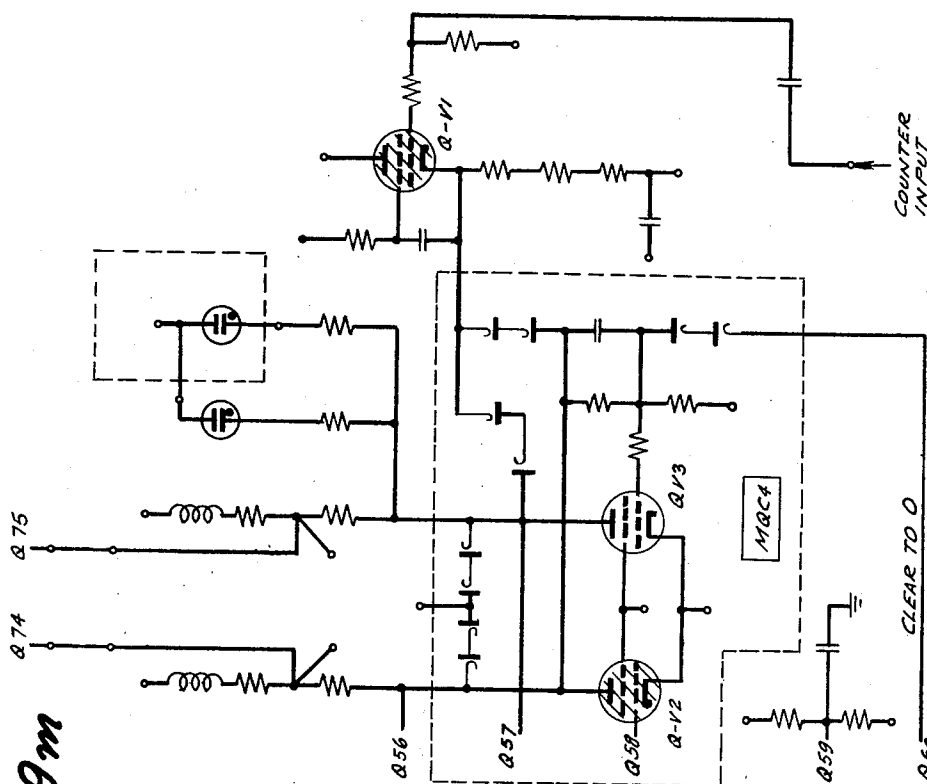
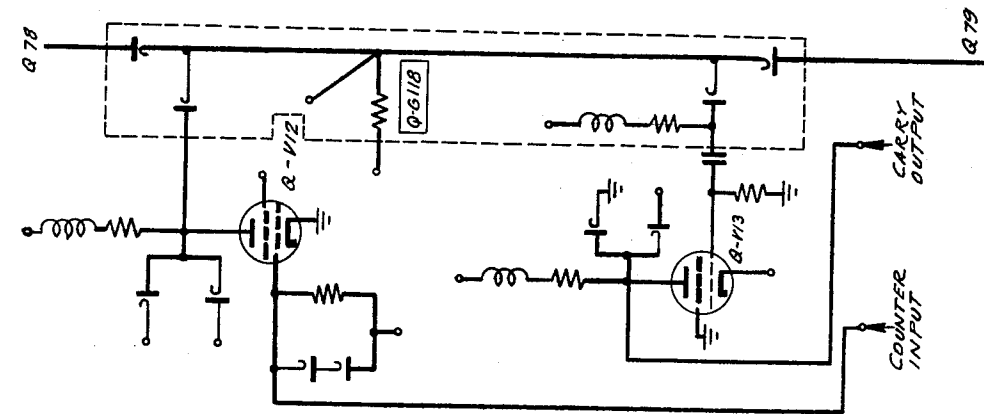


FIG. 9m

INVENTORS

J. PRESPEER ECKERT, JR
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

ROBERT F. SHAW
H. FRAZER WELSH

BY *George B. Elliott*
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May 12, 1964

J. P. ECKERT, JR., ETAL
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BINARY CODED ALPHANUMERIC CHARACTERS

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Filed March 31, 1952

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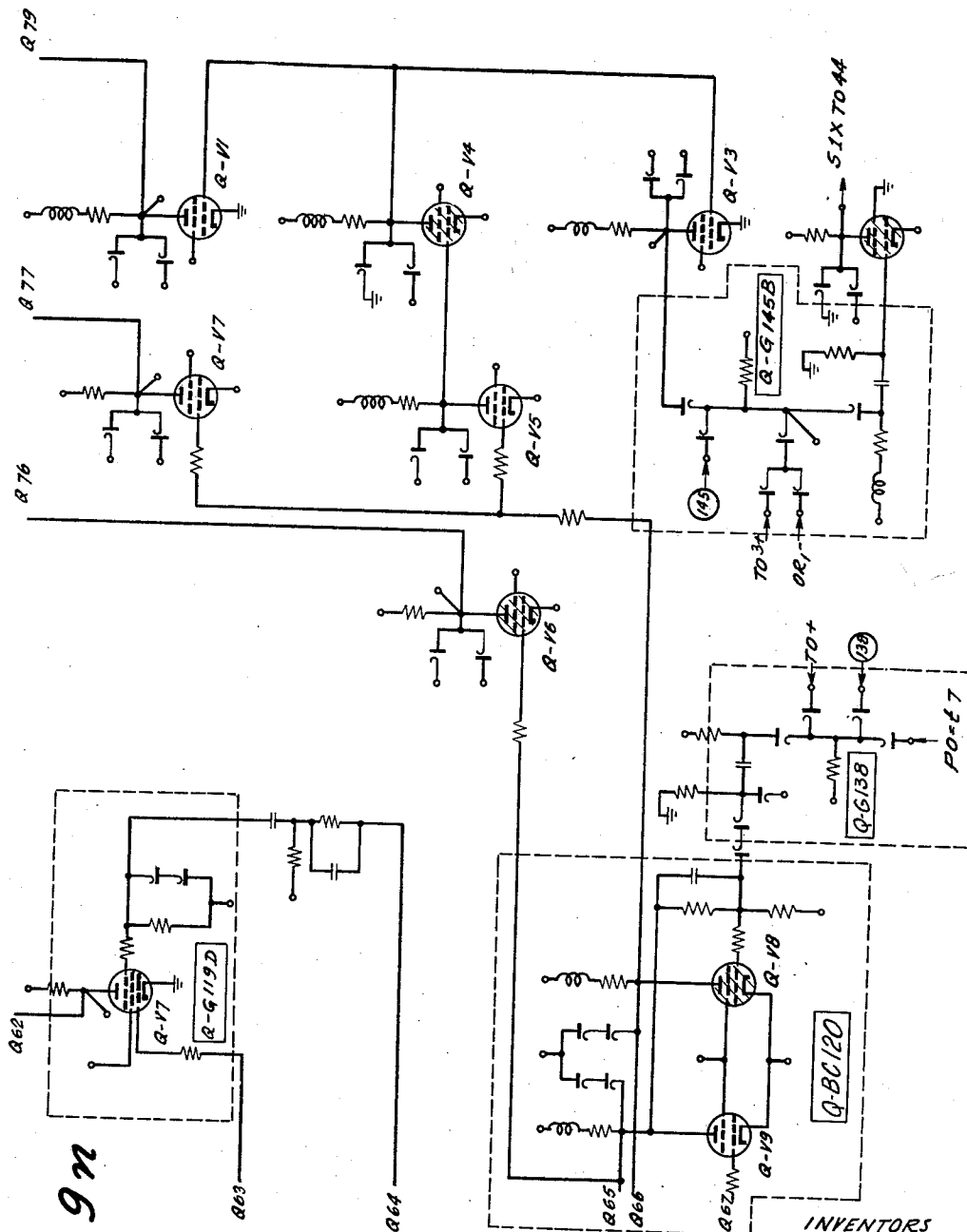


FIG. 9n

INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

BY *George B. Ritz*
ATTORNEY

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110 Sheets-Sheet 40

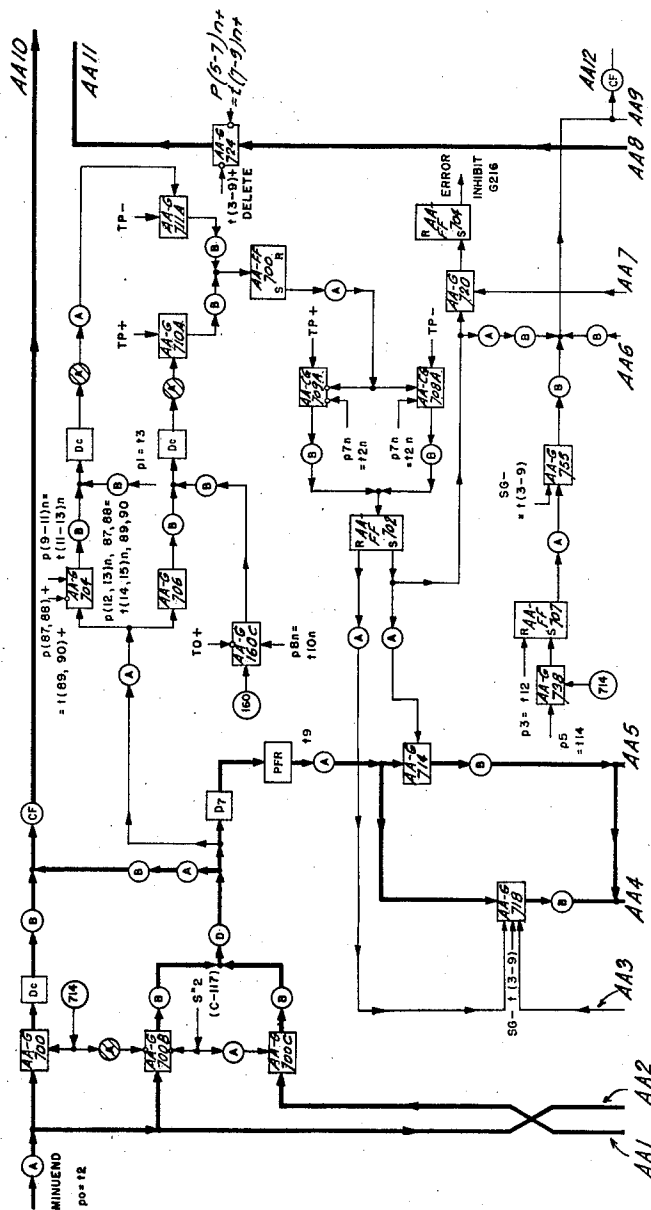


FIG. 10a

J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

H. FRAZER WELSH
George V. Elyroth
ATTORNEY

May 12, 1964

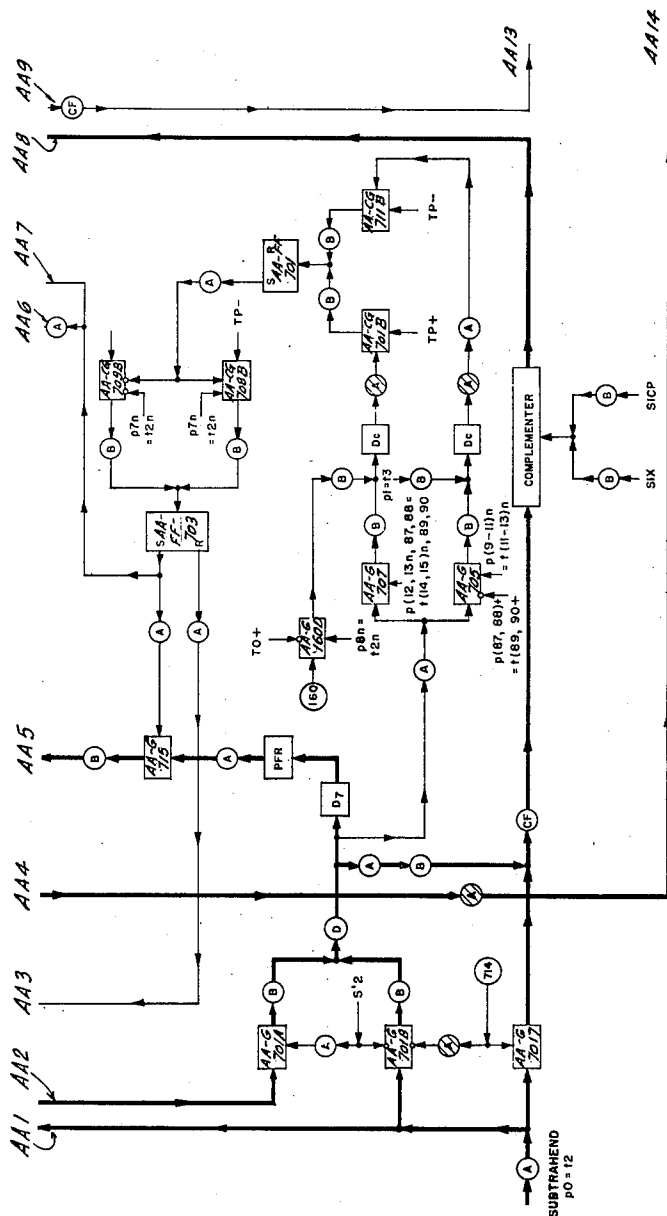
J. P. ECKERT, JR., ETAL
UNIVERSAL AUTOMATIC COMPUTER UTILIZING
BINARY CODED ALPHANUMERIC CHARACTERS

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FIG. 10b



INVENTORS

J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

BY

George V. Elgorth
ATTORNEY

May 12, 1964

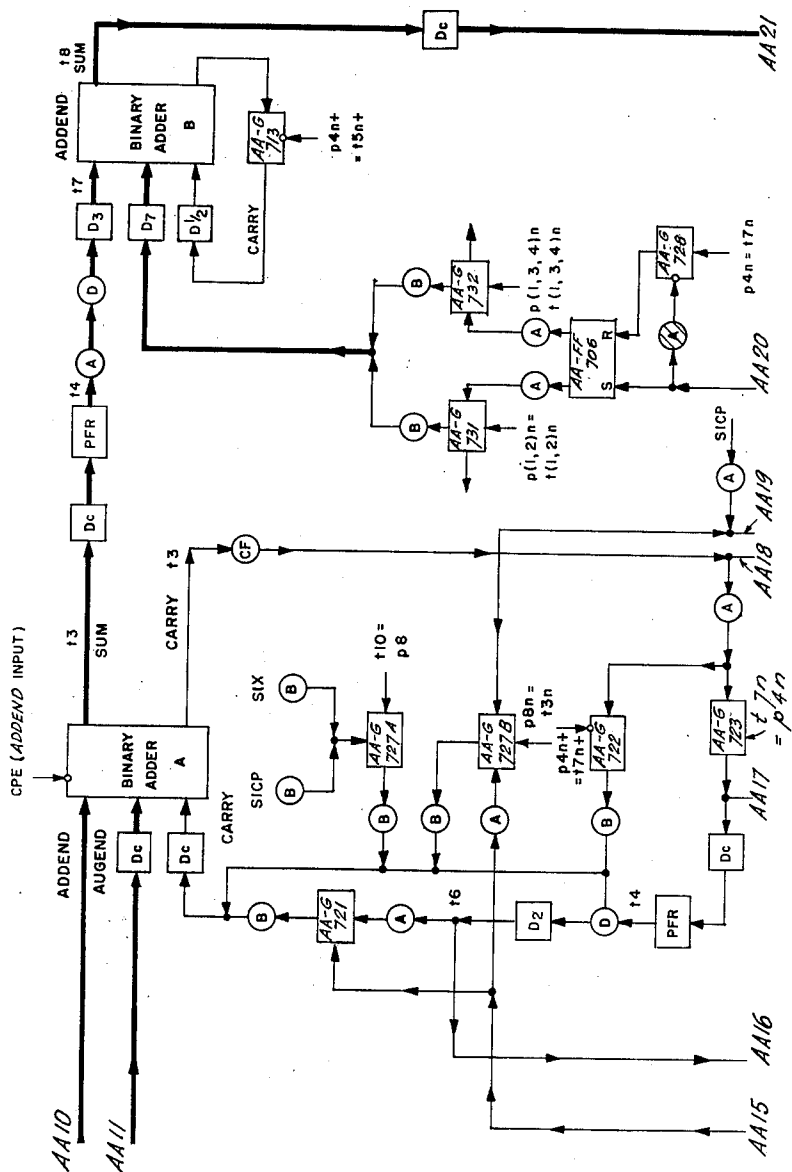
J. P. ECKERT, JR., ETAL
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BINARY CODED ALPHANUMERIC CHARACTERS

3,133,190

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110 Sheets-Sheet 42

FIG. 10c



BY

INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
George V. Retzger
ATTORNEY

May 12, 1964

J. P. ECKERT, JR., ETAL
UNIVERSAL AUTOMATIC COMPUTER UTILIZING
BINARY CODED ALPHANUMERIC CHARACTERS

3,133,190

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110 Sheets-Sheet 43

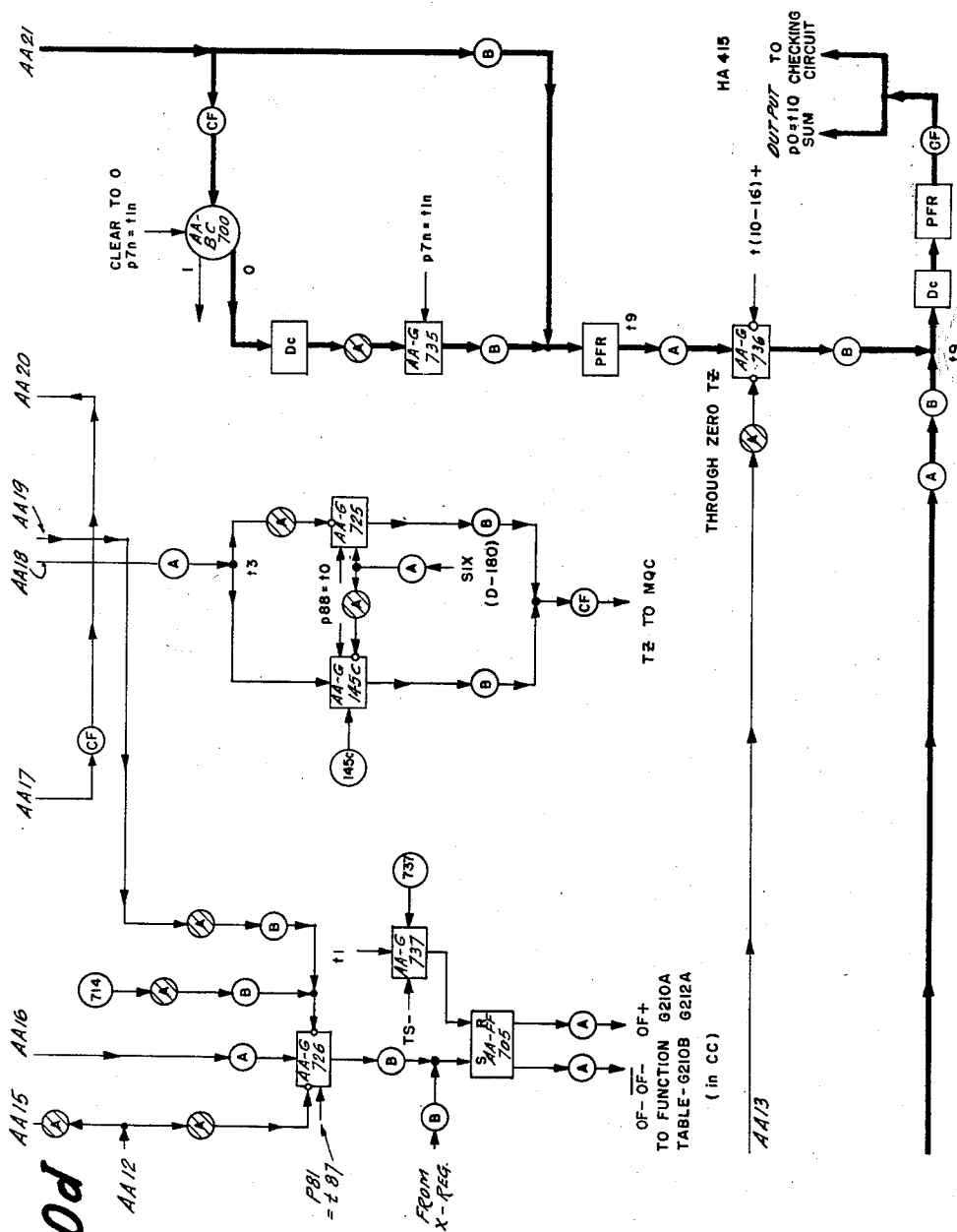


FIG. 10d

INVENTORS

J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

BY

H. FRAZER WELSH
George V. Elyroth
ATTORNEY

May 12, 1964

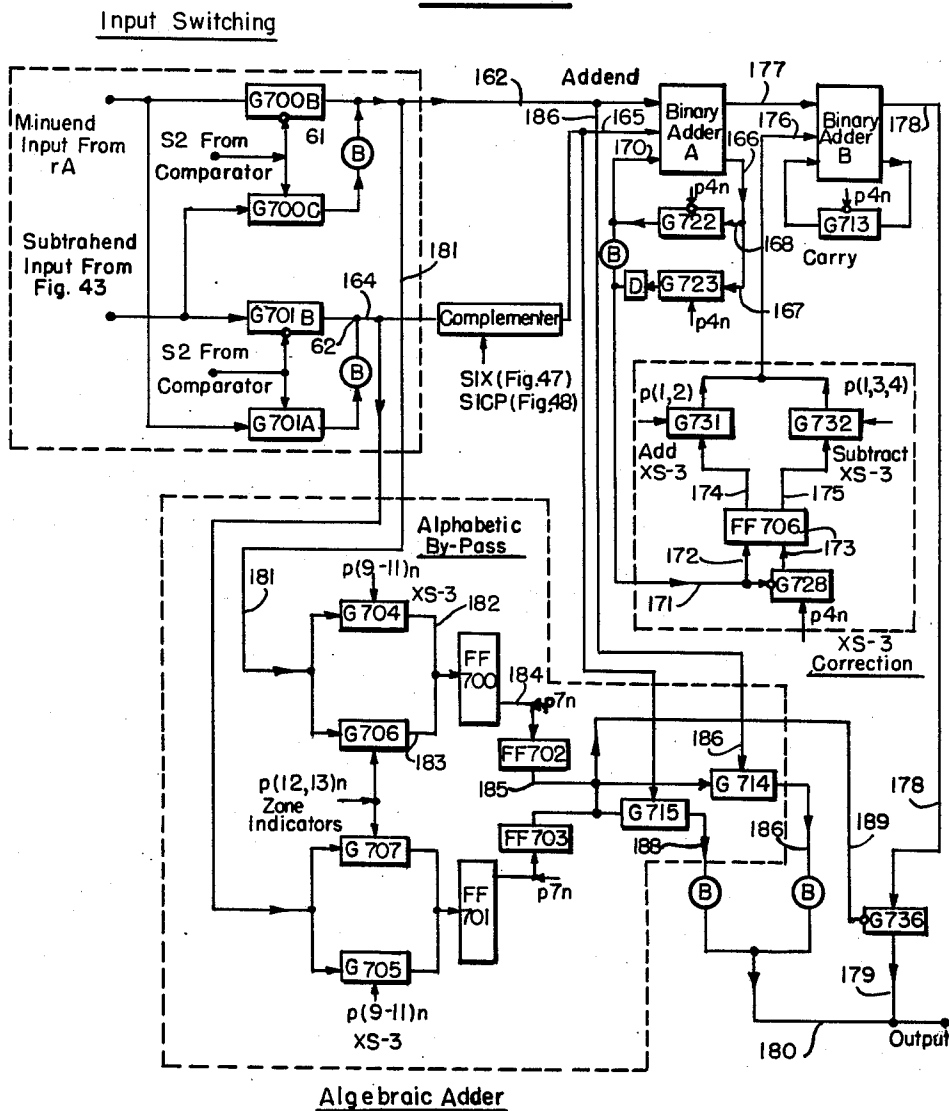
J. P. ECKERT, JR., ETAL
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BINARY CODED ALPHANUMERIC CHARACTERS

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FIG. 10e.



INVENTORS

J. Presper Eckert, Jr.
James R. Weiner
Robert F. Shaw
H. Frazer Welsh

BY

William Hobman
ATTORNEY

May 12, 1964

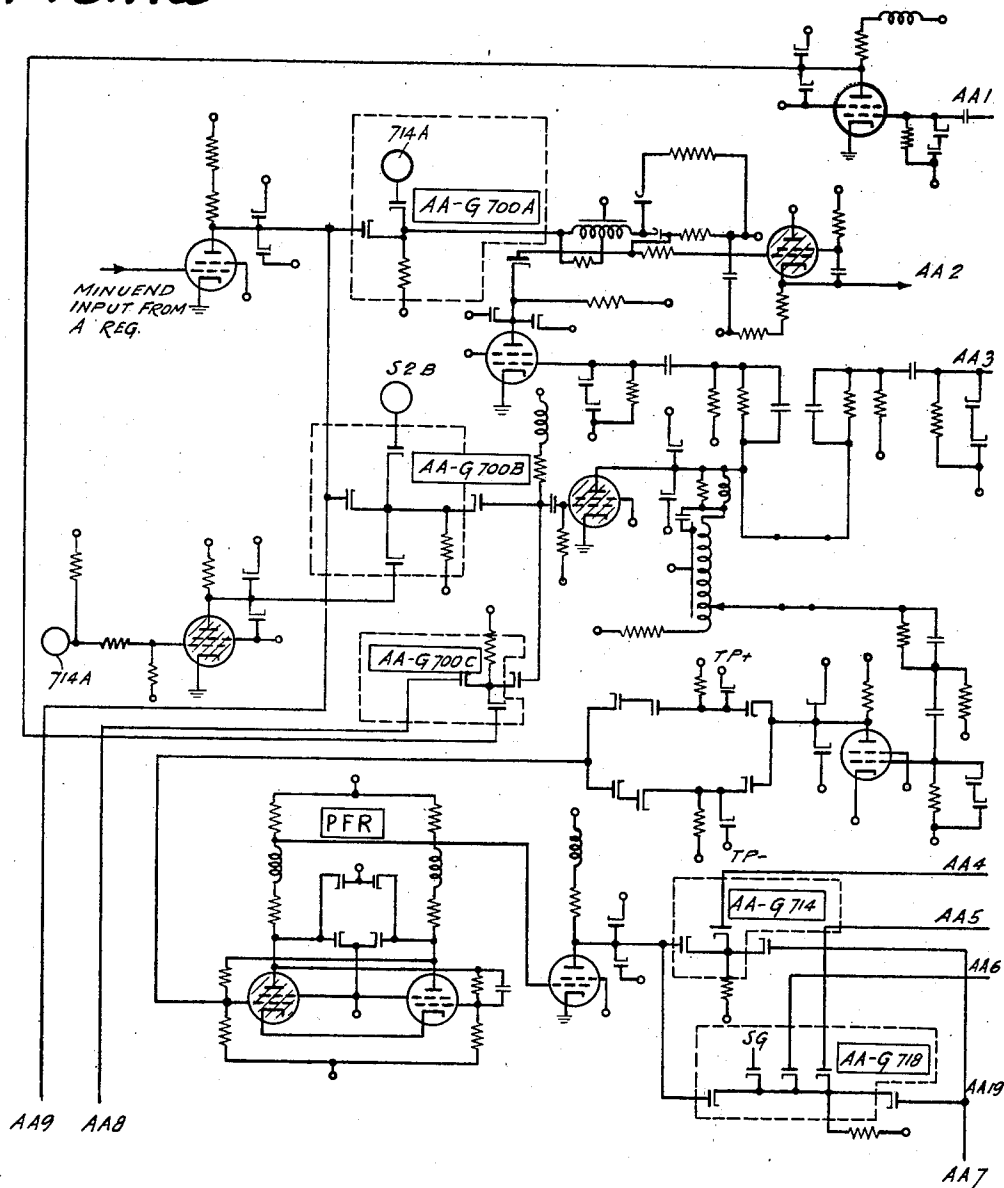
J. P. ECKERT, JR., ETAL
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BINARY CODED ALPHANUMERIC CHARACTERS

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FIG. 11a



INVENTORS

J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

BY *Lawrence R. Wilk*
ATTORNEY

May 12, 1964

J. P. ECKERT, JR., ETAL
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BINARY CODED ALPHANUMERIC CHARACTERS

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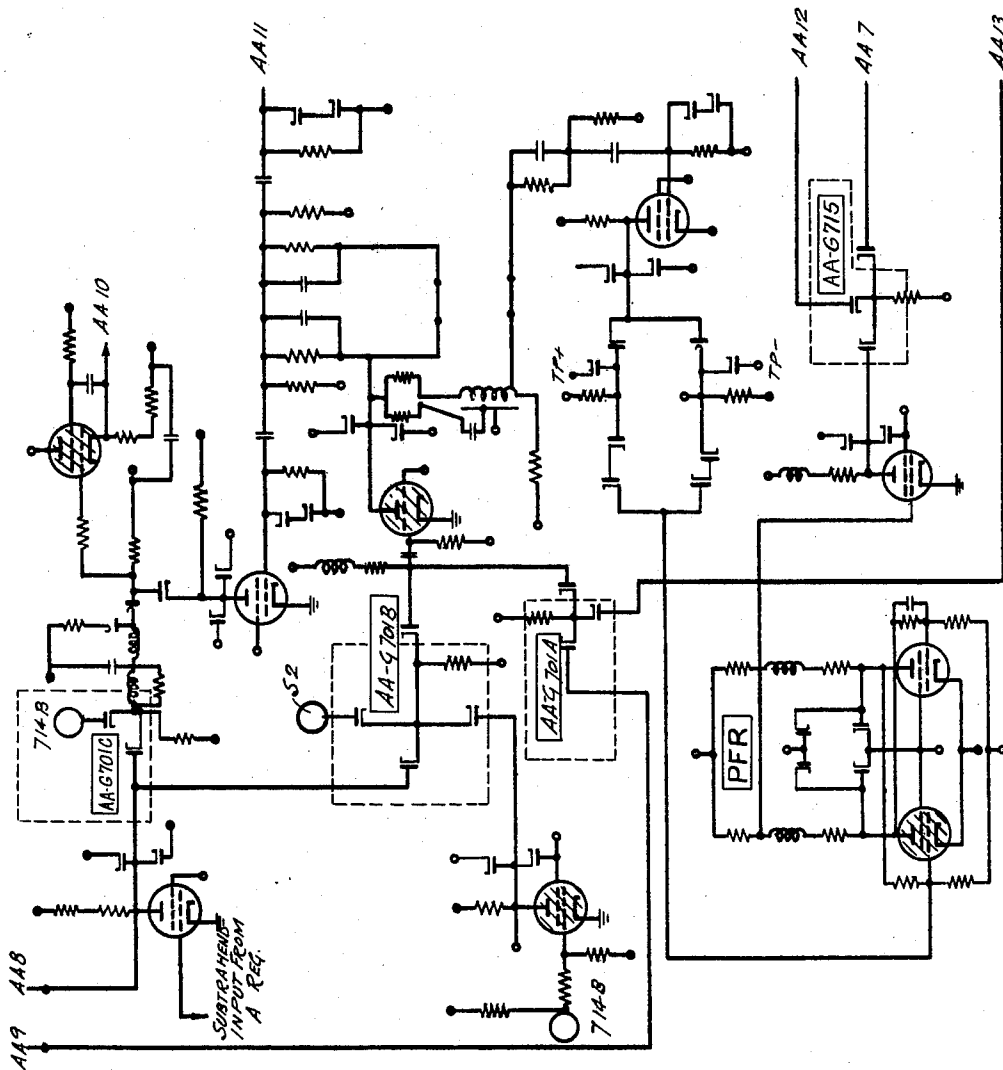


FIG. 11b

INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George R. Rytz*
ATTORNEY

May 12, 1964

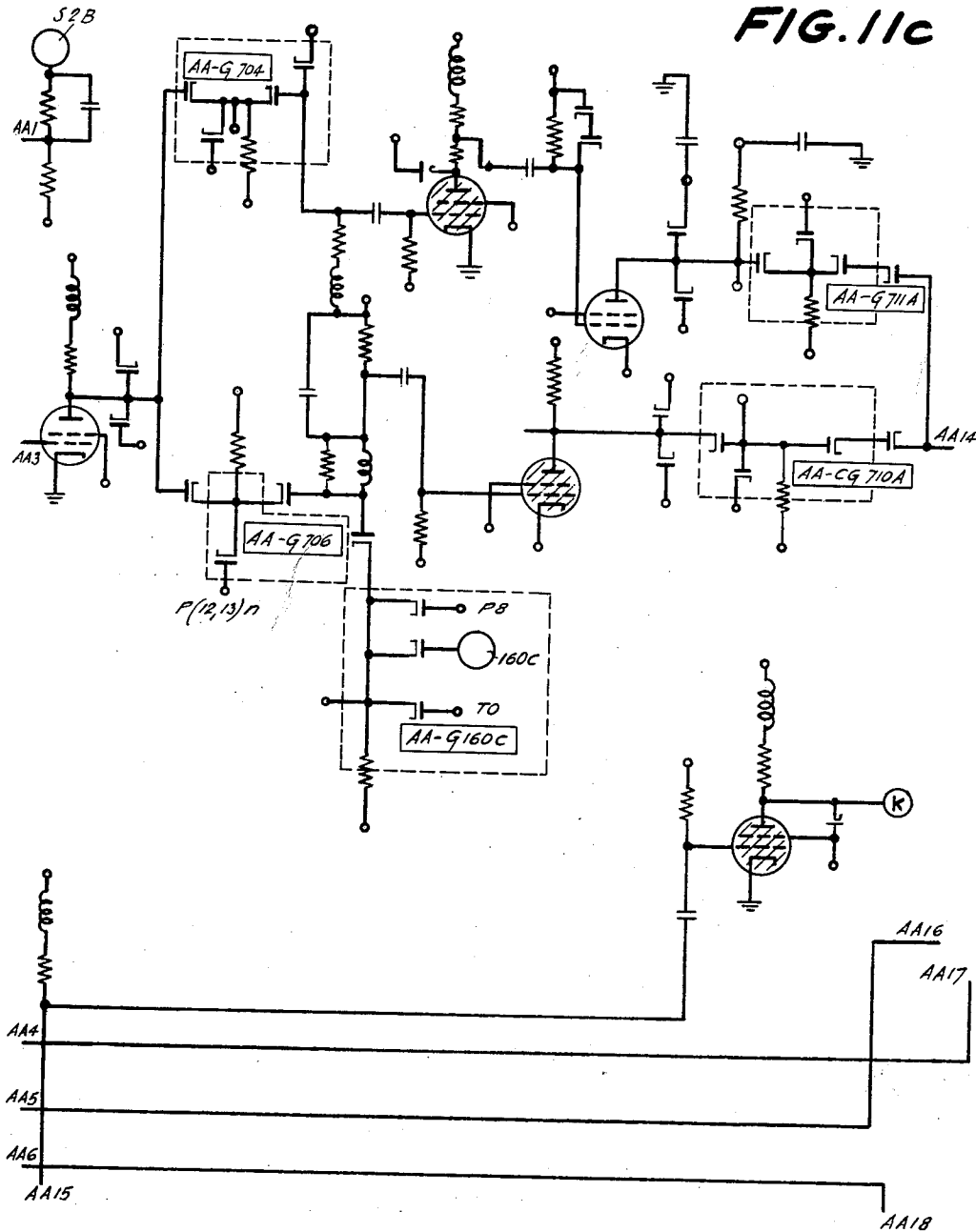
J. P. ECKERT, JR., ET AL
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BINARY CODED ALPHANUMERIC CHARACTERS

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Filed March 31, 1952

110 Sheets-Sheet 47

FIG. 11c



INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George V. Wright*
ATTORNEY

May 12, 1964

J. P. ECKERT, JR., ET AL
UNIVERSAL AUTOMATIC COMPUTER UTILIZING
BINARY CODED ALPHANUMERIC CHARACTERS

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110 Sheets-Sheet 48

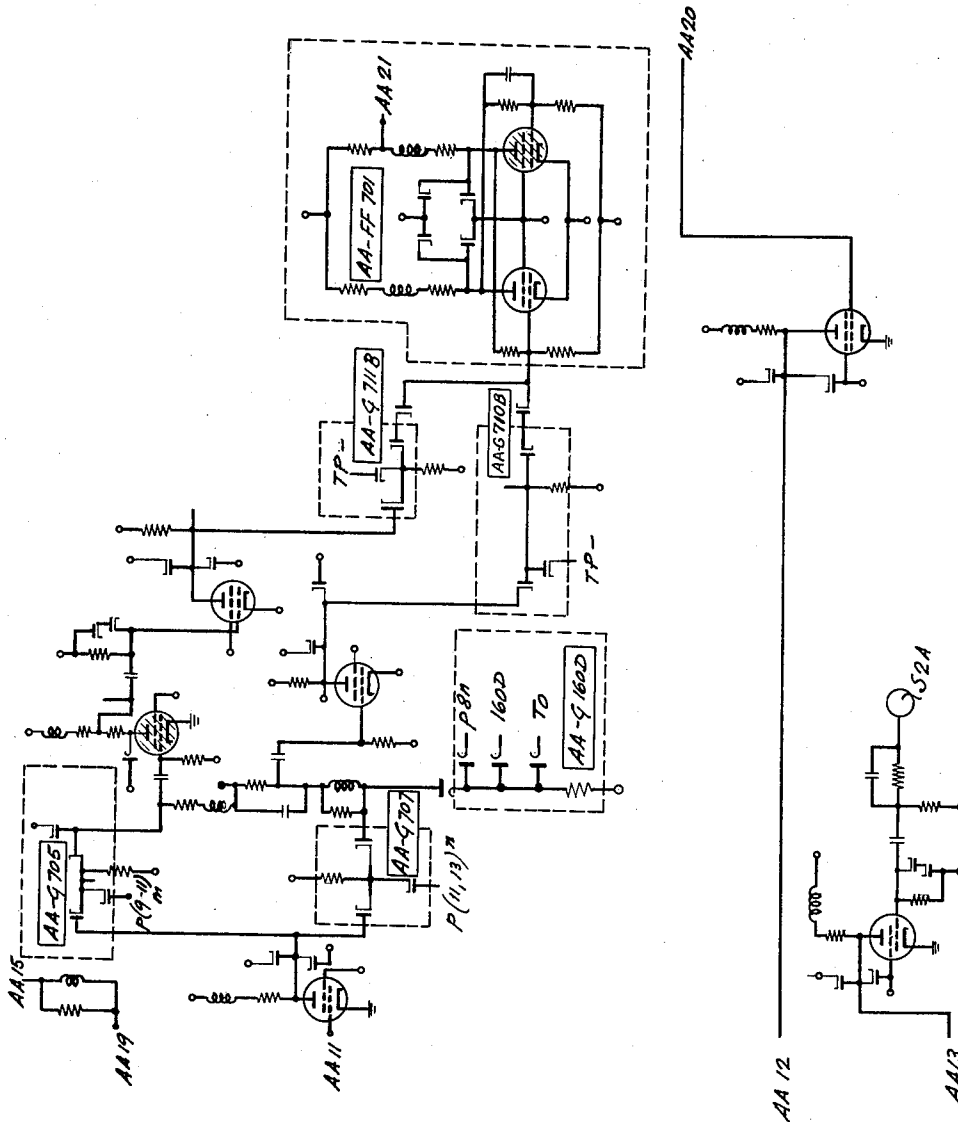


FIG. 11d

INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *Lawrence R. Welch*
ATTORNEY

May 12, 1964

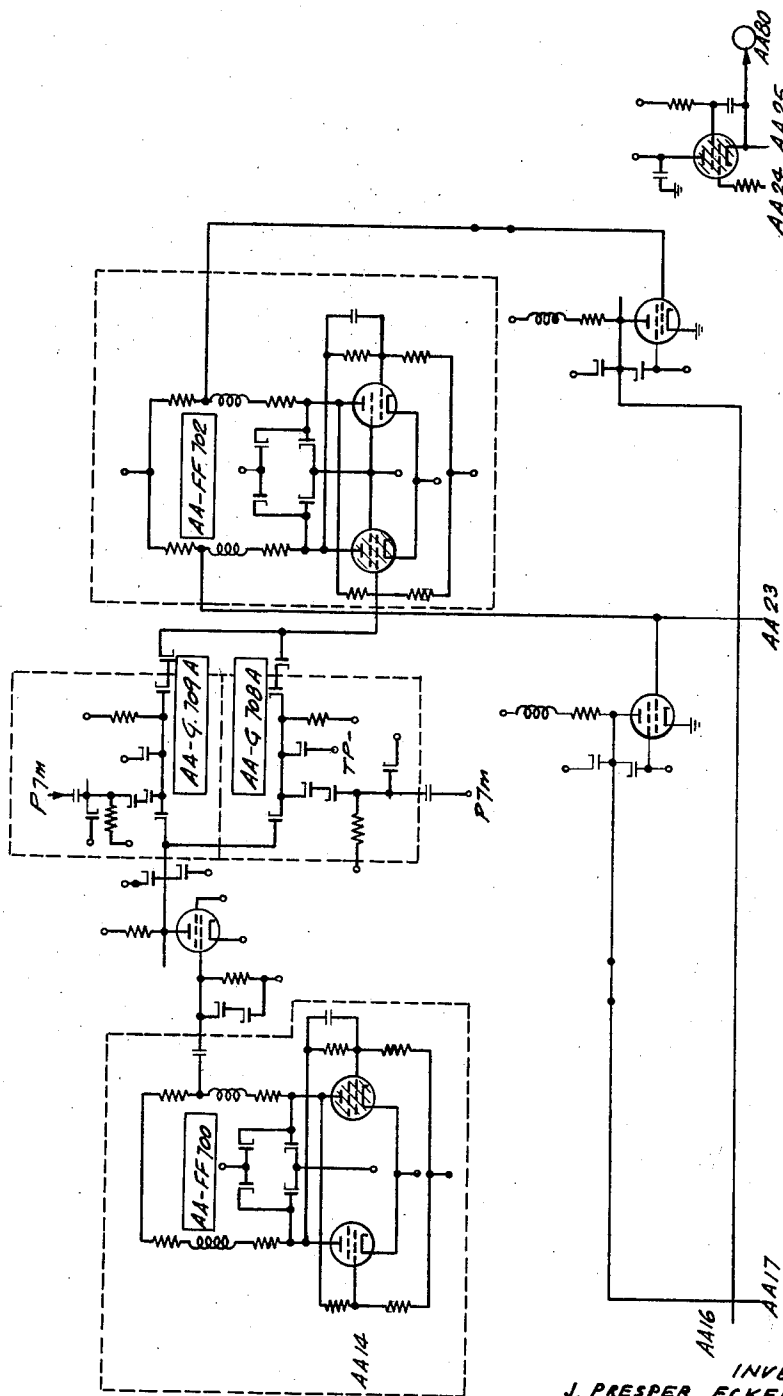
J. P. ECKERT, JR., ETAL
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110 Sheets-Sheet 49

FIG. 11e



INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

BY

George V. Kelly
ATTORNEY

May 12, 1964

J. P. ECKERT, JR., ETAL
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BINARY CODED ALPHANUMERIC CHARACTERS

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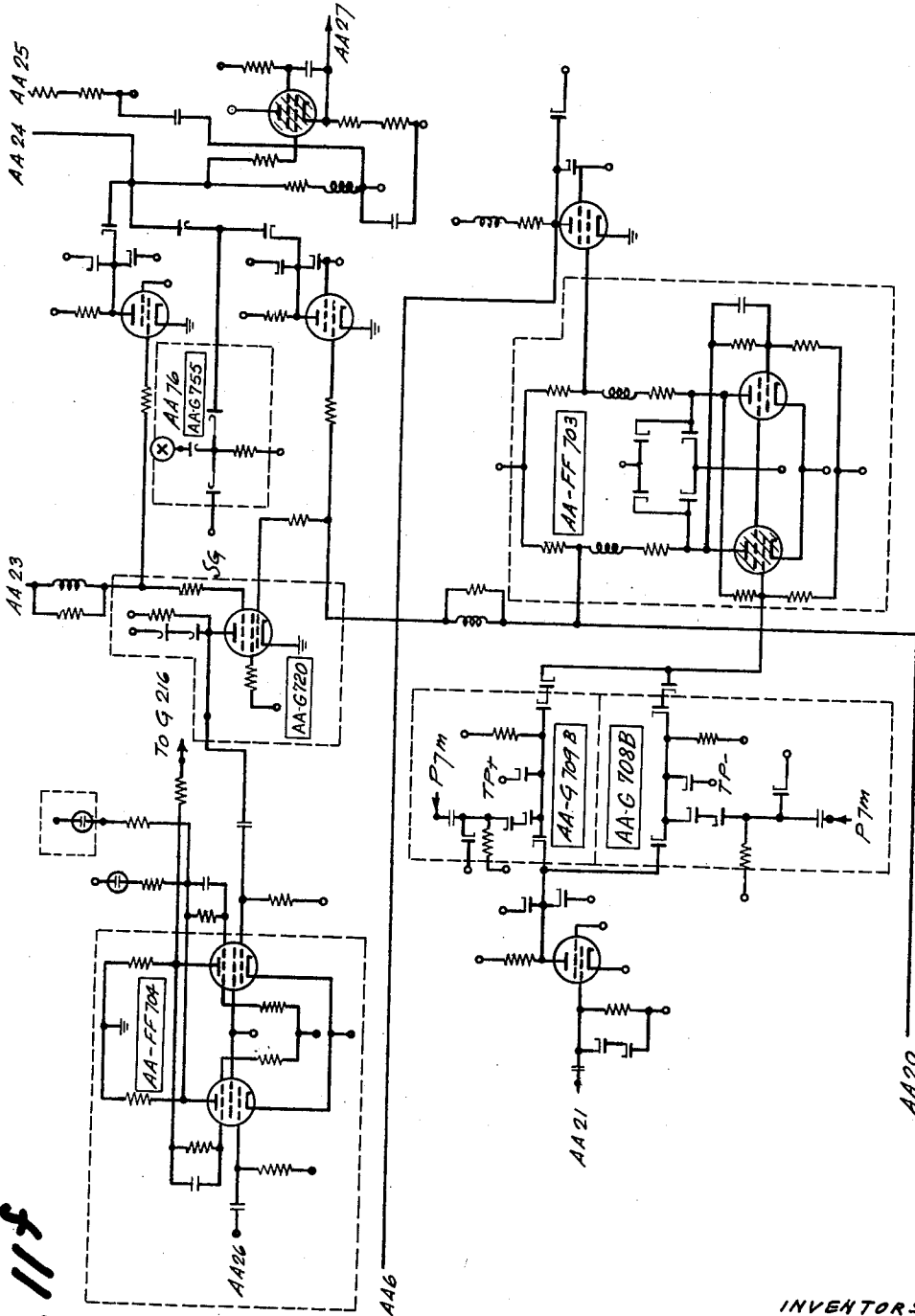


FIG. 111f

INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

BY

George P. Peltz
ATTORNEY

May 12, 1964

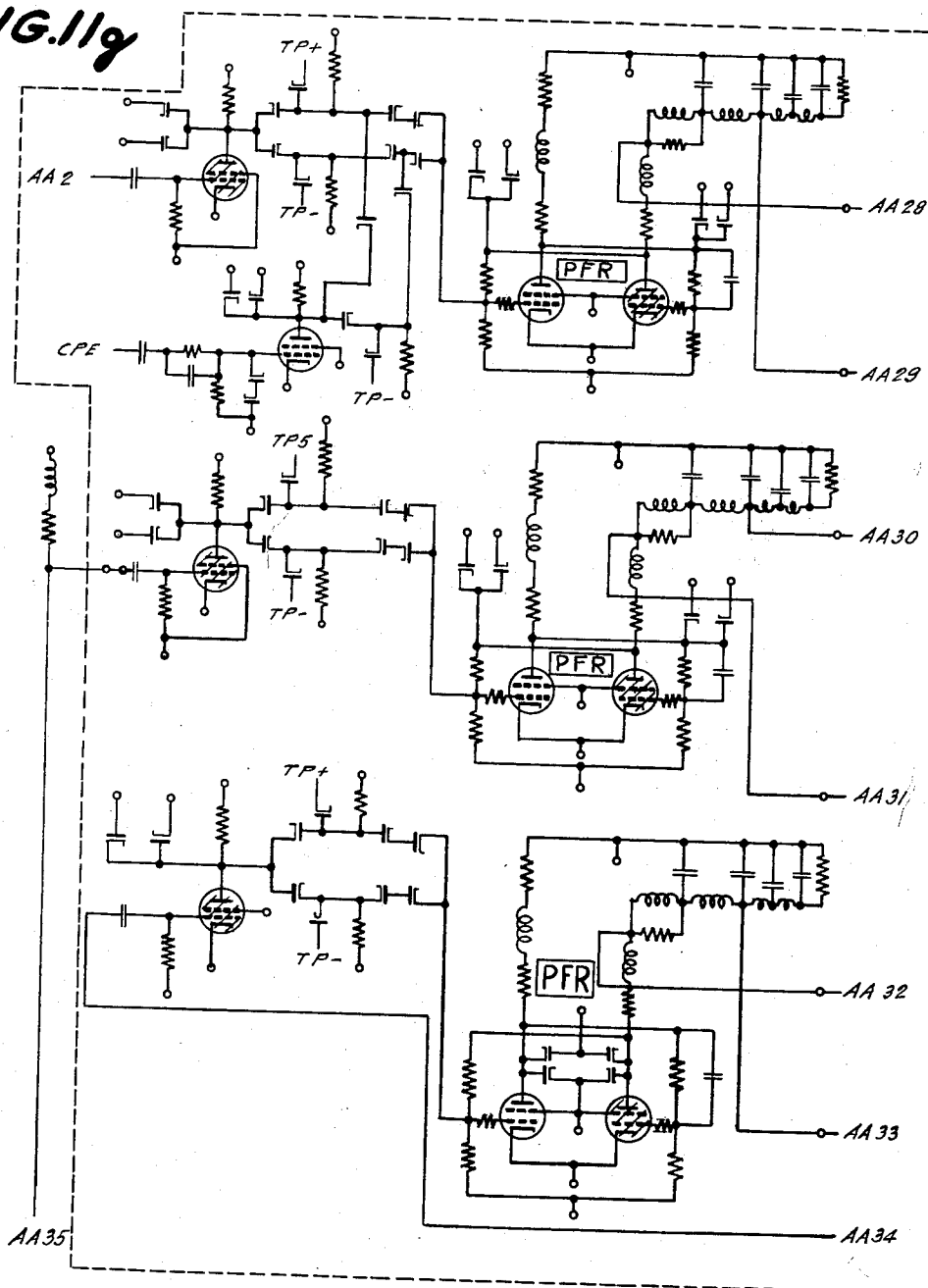
J. P. ECKERT, JR., ET AL
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3,133,190

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110 Sheets-Sheet 51

FIG. 11g



INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George R. Elgert*
ATTORNEY

May 12, 1964

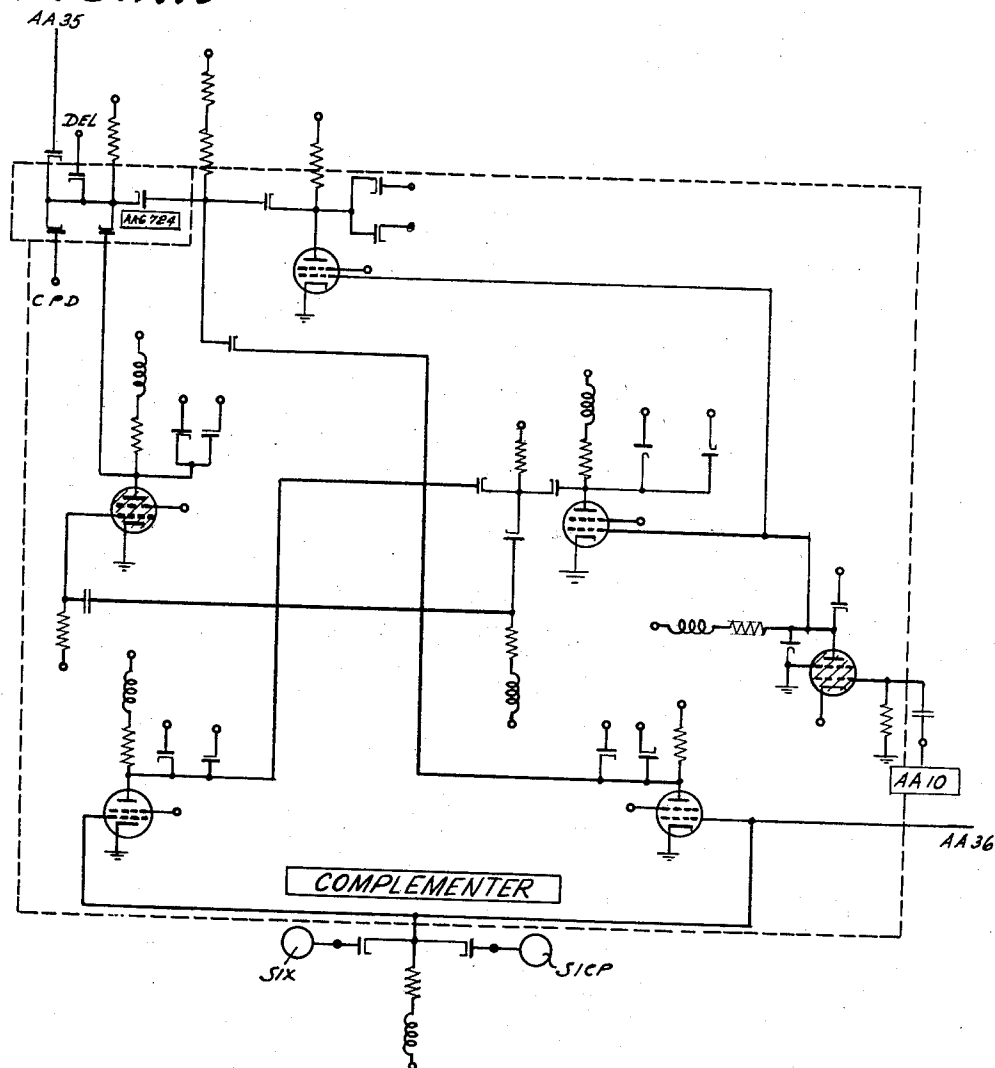
J. P. ECKERT, JR., ET AL
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BINARY CODED ALPHANUMERIC CHARACTERS

3,133,190

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110 Sheets-Sheet 52

FIG. 11h



INVENTORS
J. P. ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *Henry Veltz*
ATTORNEY

May 12, 1964

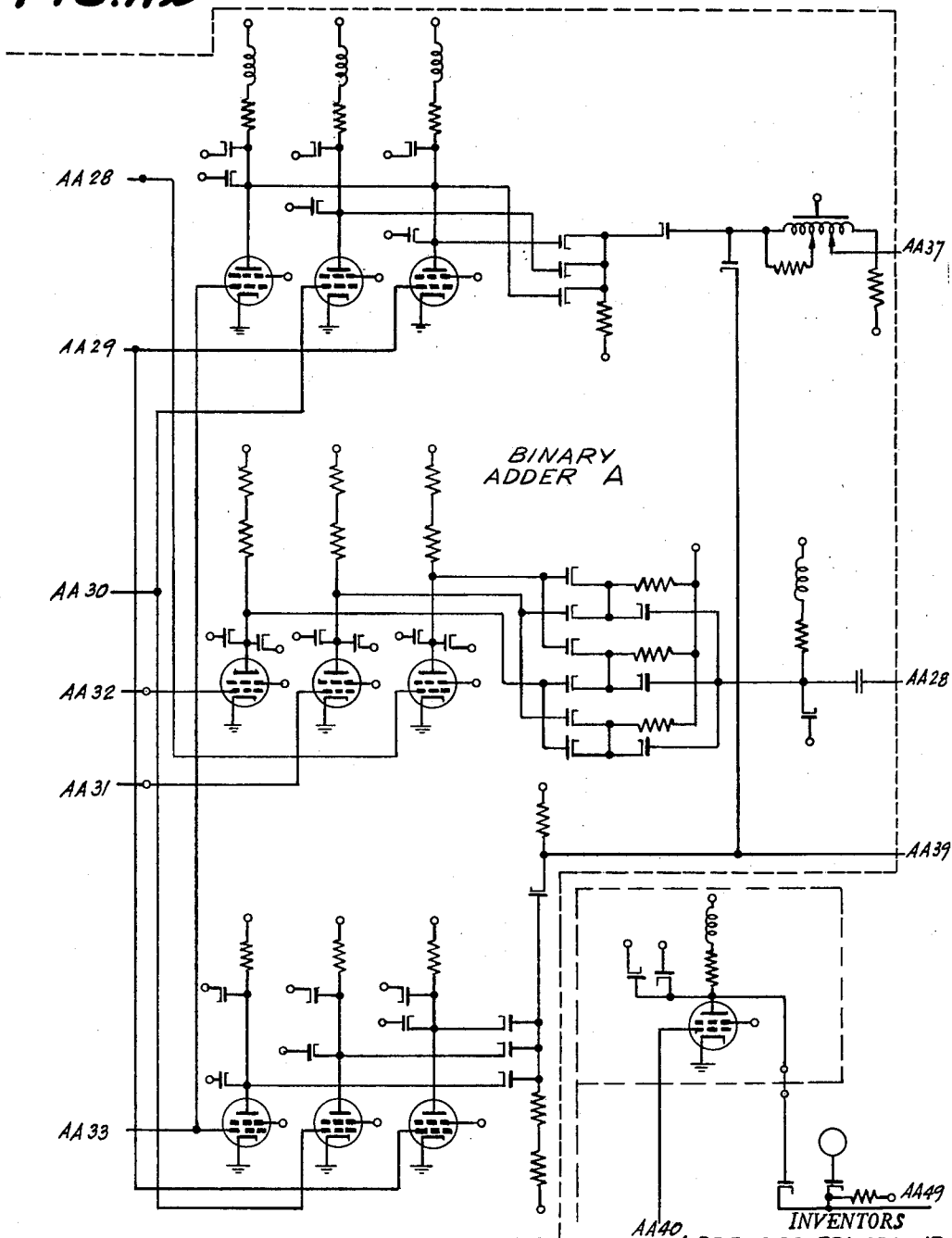
J. P. ECKERT, JR., ETAL
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FIG. 11i



INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George W. Little*
ATTORNEY

May 12, 1964

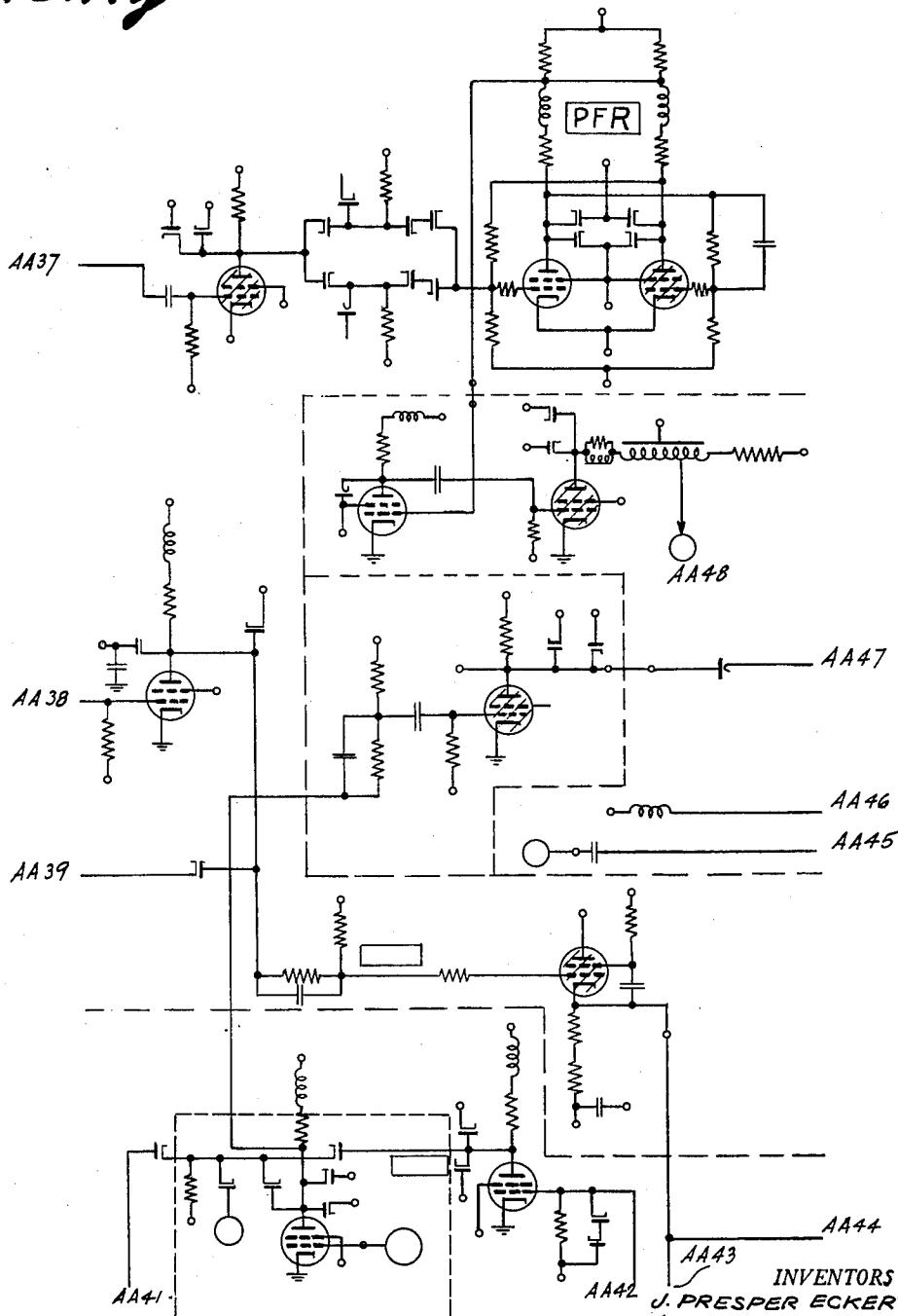
J. P. ECKERT, JR., ET AL
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3,133,190

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FIG. 11j



INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George V. Elgert*
ATTORNEY

May 12, 1964

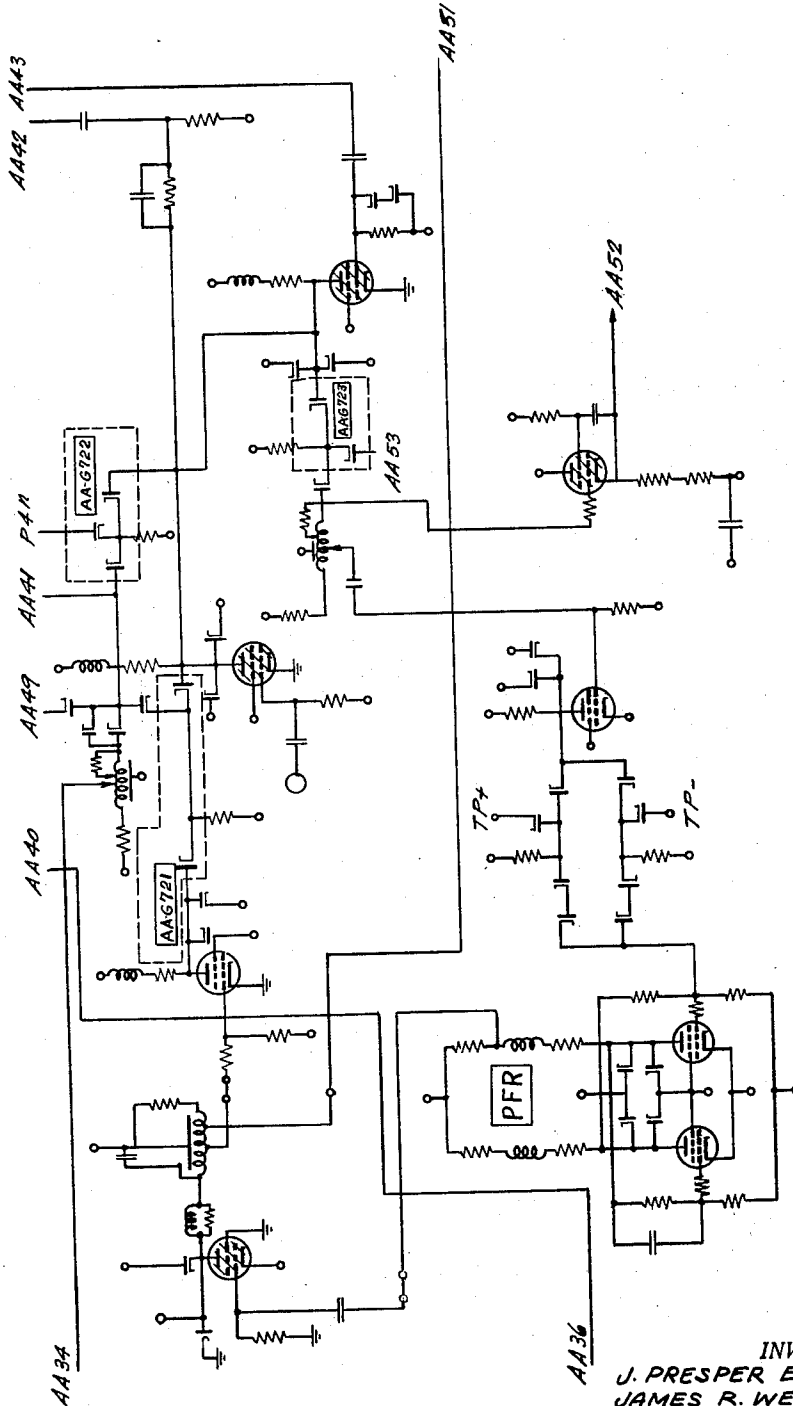
J. P. ECKERT, JR., ET AL
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BINARY CODED ALPHANUMERIC CHARACTERS

3,133,190

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110 Sheets-Sheet 55

FIG. 11K



INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George W. Elgert*
ATTORNEY

May 12, 1964

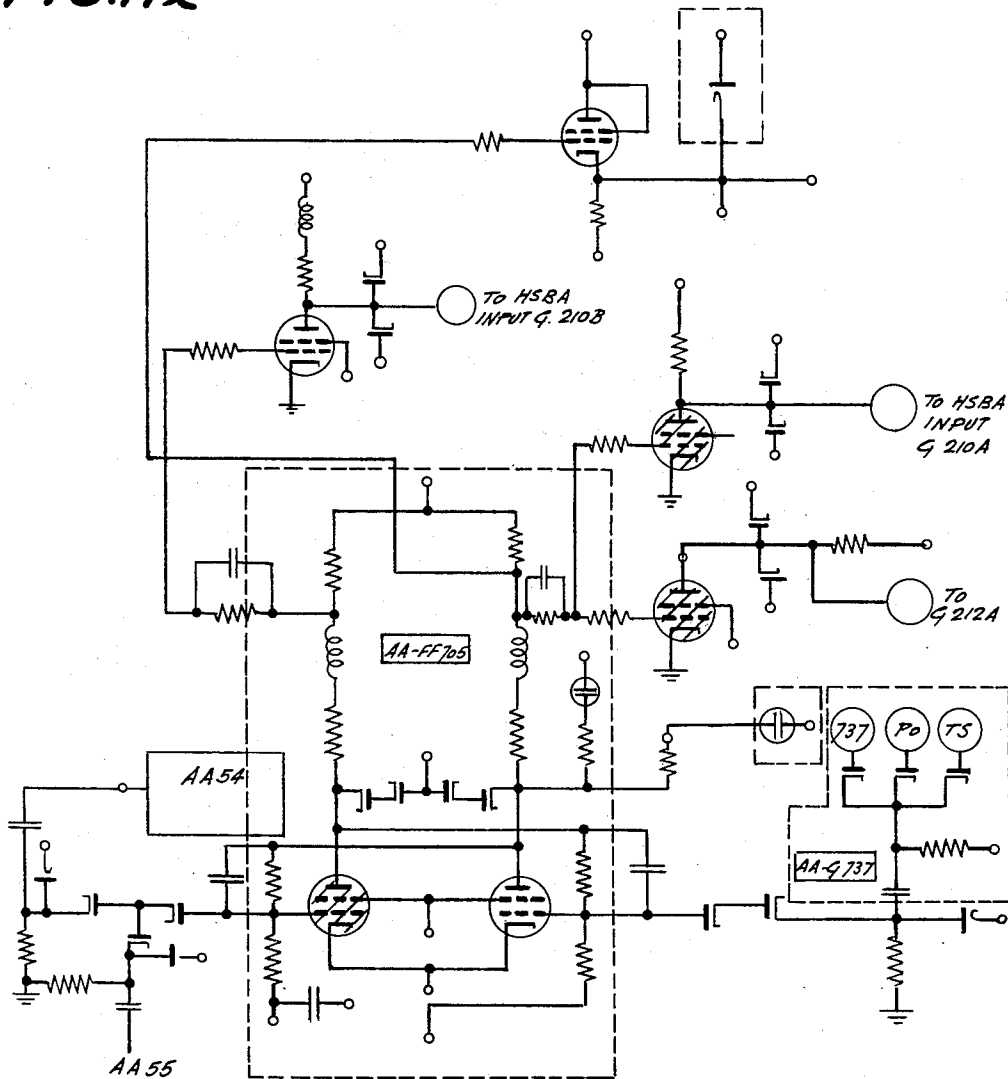
J. P. ECKERT, JR., ETAL
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BINARY CODED ALPHANUMERIC CHARACTERS

3,133,190

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FIG. 112



INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *Harvey W. Blythe*
ATTORNEY

May 12, 1964

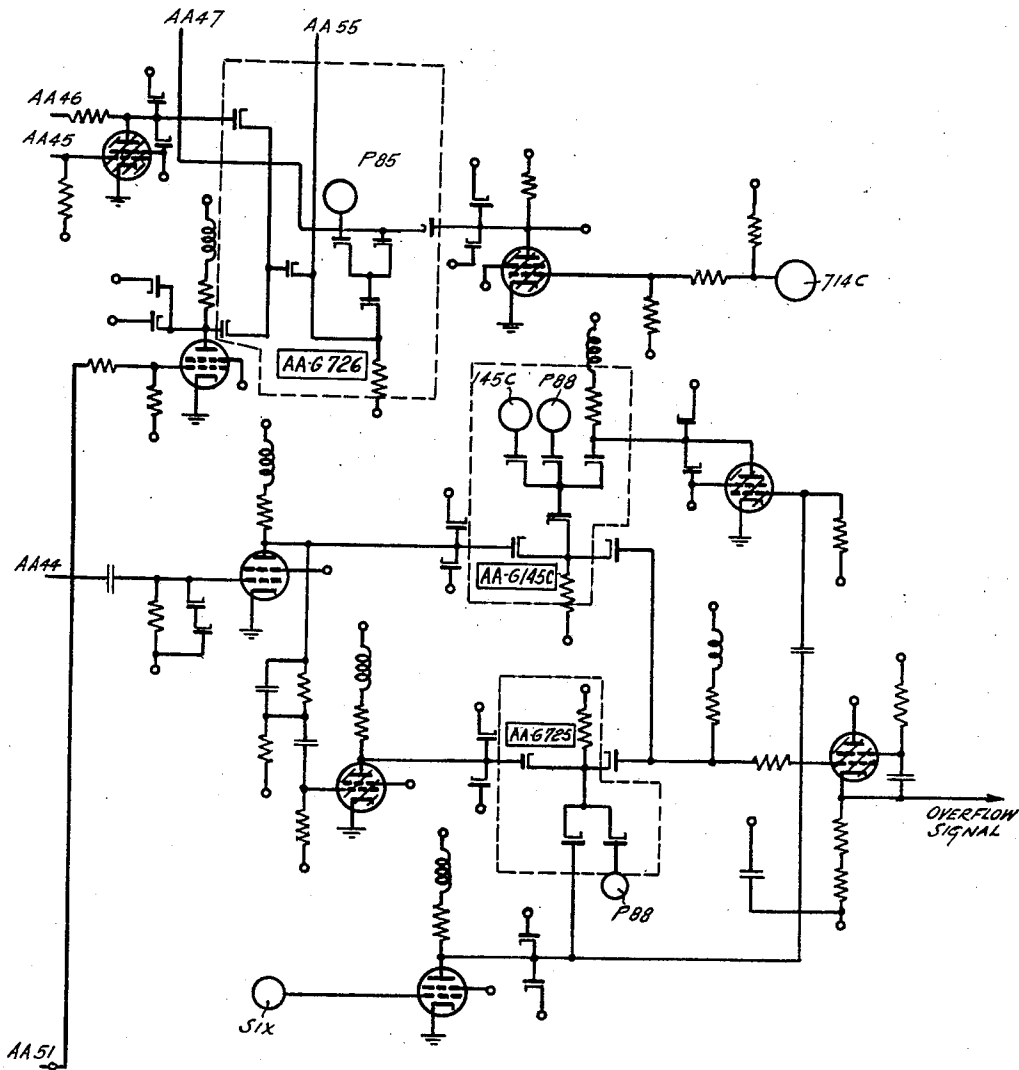
J. P. ECKERT, JR., ETAL
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BINARY CODED ALPHANUMERIC CHARACTERS

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110 Sheets-Sheet 57

FIG. 11m



INVENTORS
J. PRESPEER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George Feltz*
ATTORNEY

May 12, 1964

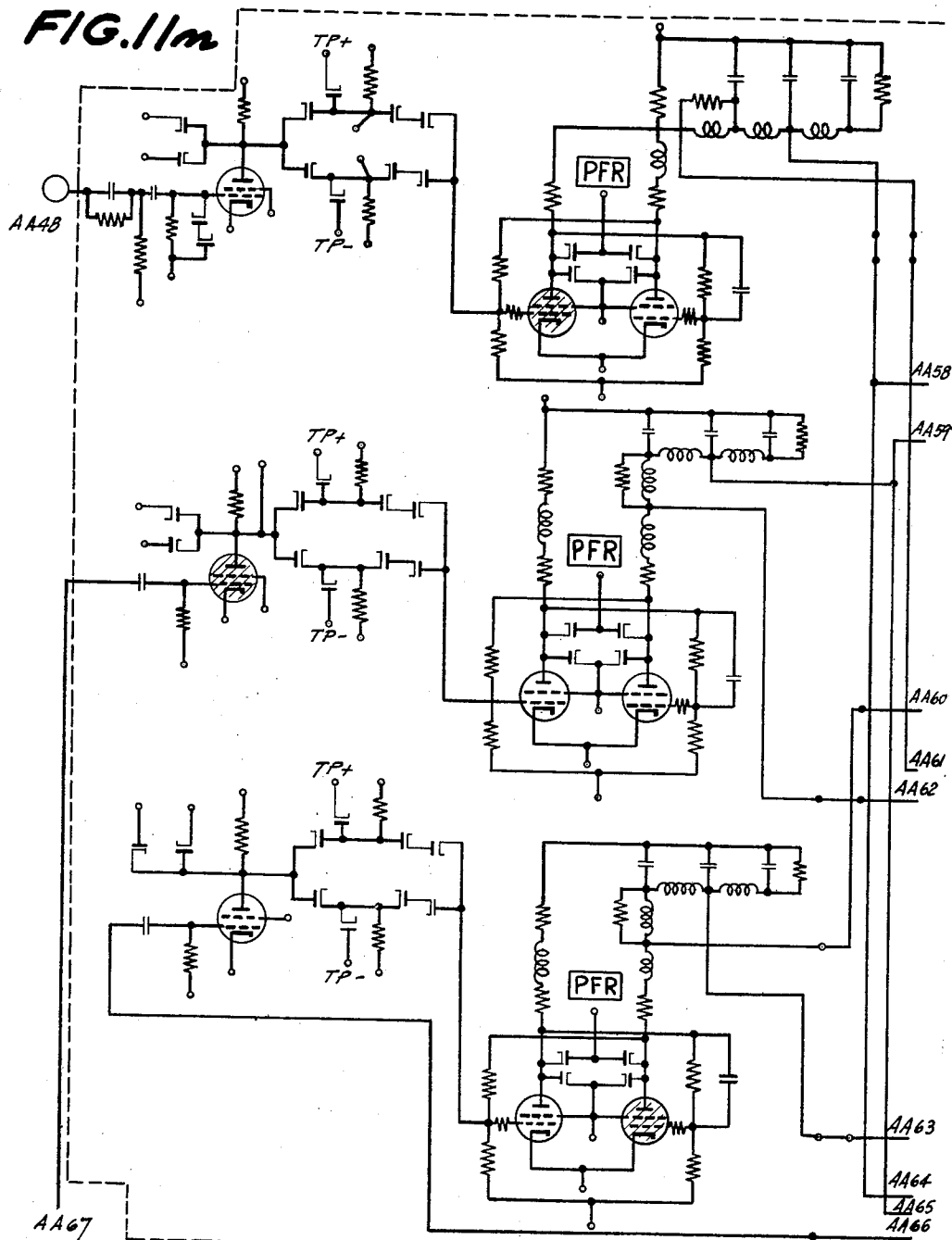
J. P. ECKERT, JR., ETAL
UNIVERSAL AUTOMATIC COMPUTER UTILIZING
BINARY CODED ALPHANUMERIC CHARACTERS

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110 Sheets-Sheet 58

FIG. 11m



INVENTORS
J. PERSPER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George R. Galt*
ATTORNEY

May 12, 1964

J. P. ECKERT, JR., ETAL
UNIVERSAL AUTOMATIC COMPUTER UTILIZING
BINARY CODED ALPHANUMERIC CHARACTERS

3,133,190

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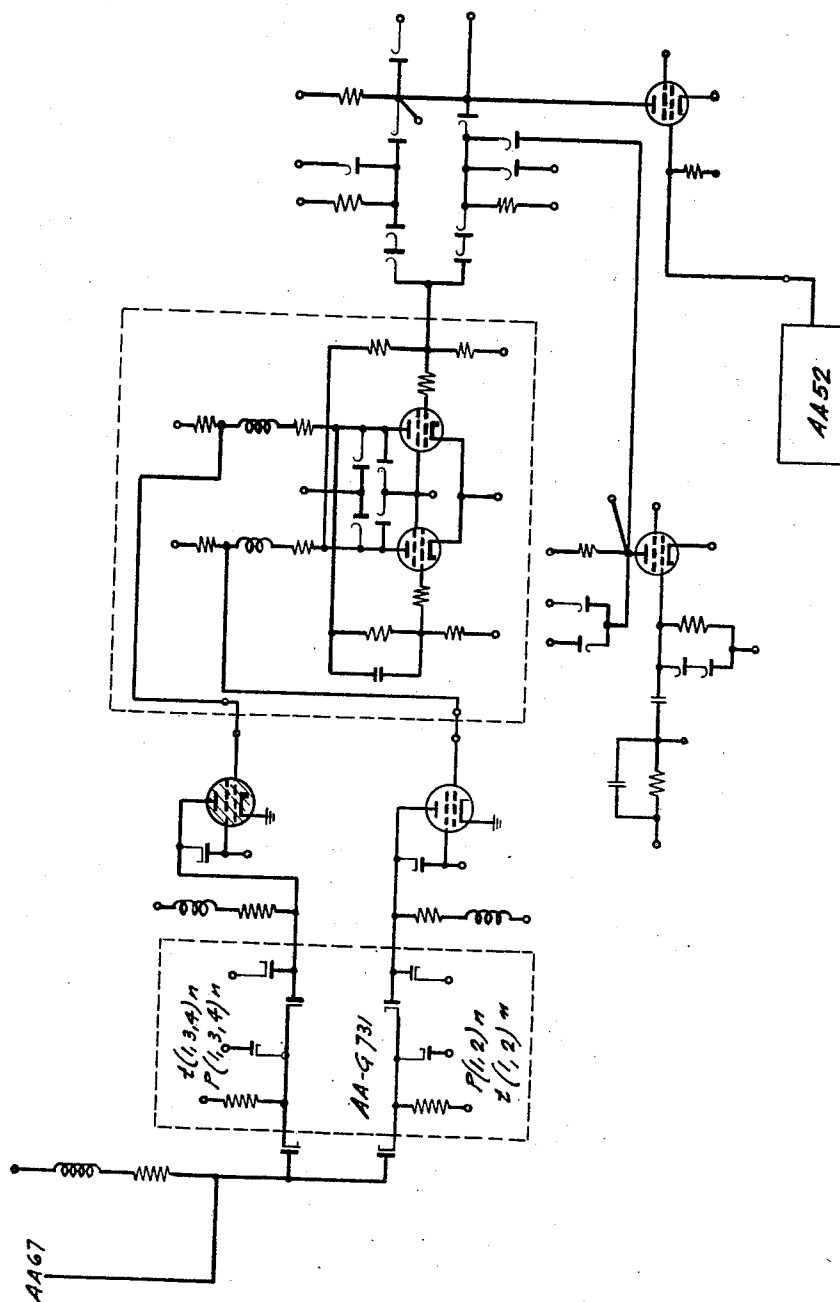


FIG. 110

INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *Samuel H. Smith*
ATTORNEY

May 12, 1964

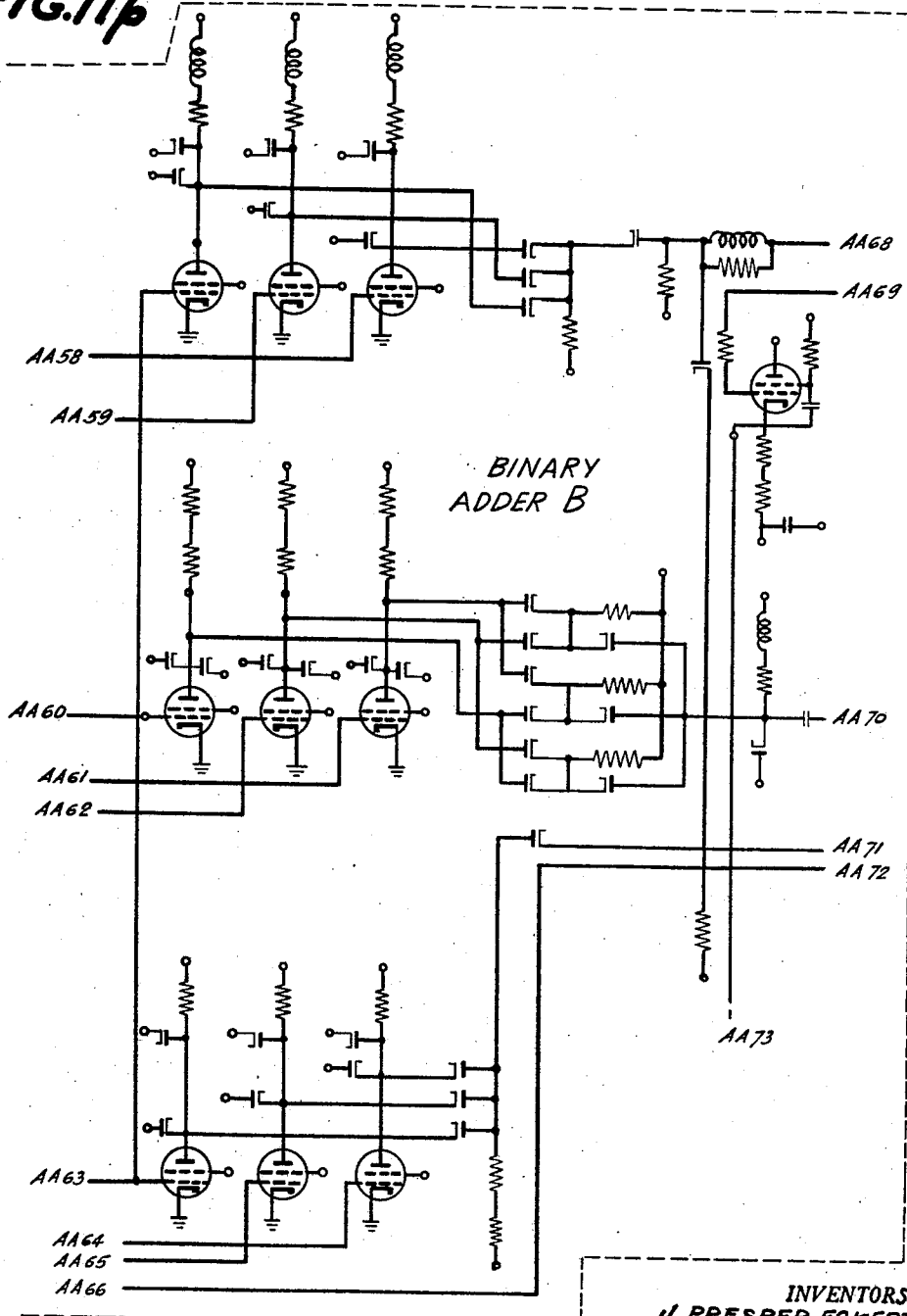
J. P. ECKERT, JR., ET AL
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BINARY CODED ALPHANUMERIC CHARACTERS

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FIG. 11p



INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *Samuel R. Galt*
ATTORNEY

May 12, 1964

J. P. ECKERT, JR., ETAL
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BINARY CODED ALPHANUMERIC CHARACTERS

3,133,190

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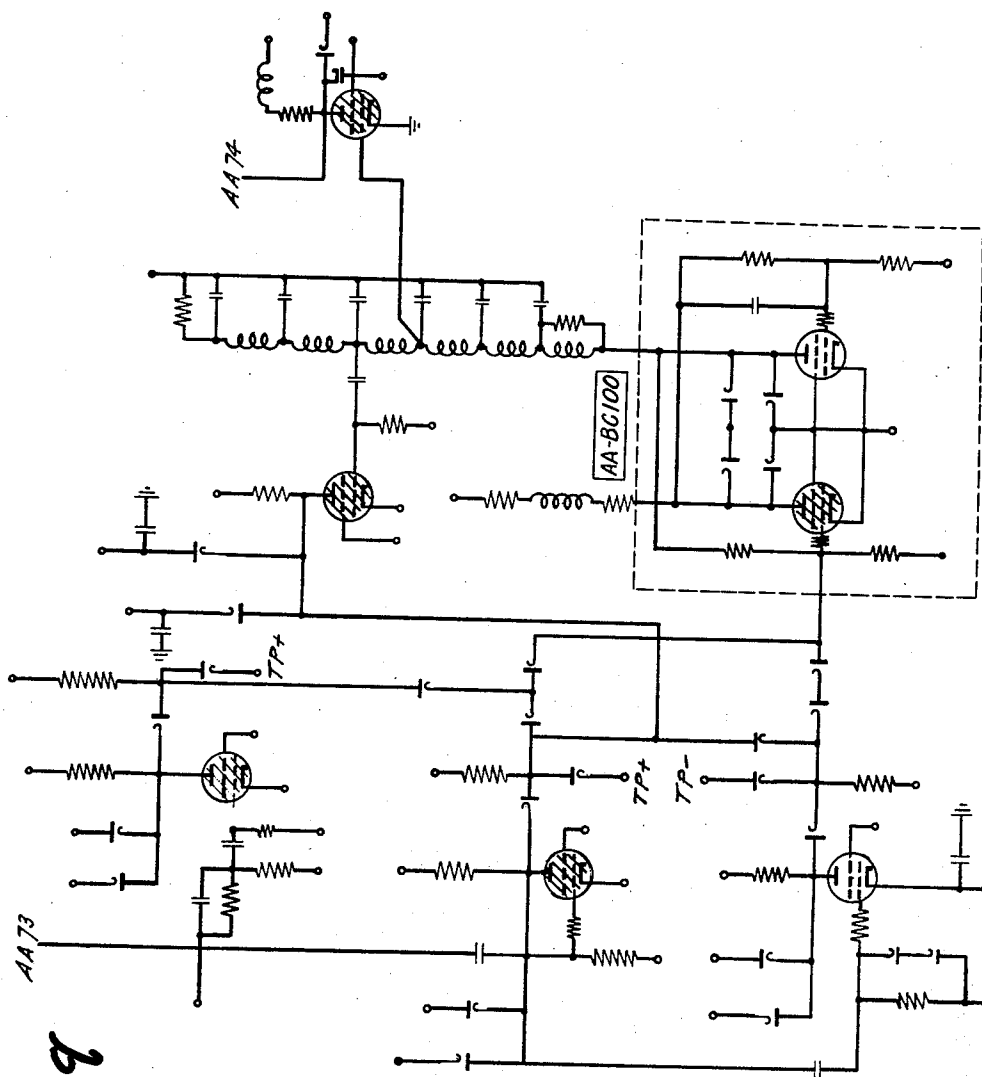


FIG. 119

INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH

BY *Samuel D. Bell*
ATTORNEY

May 12, 1964

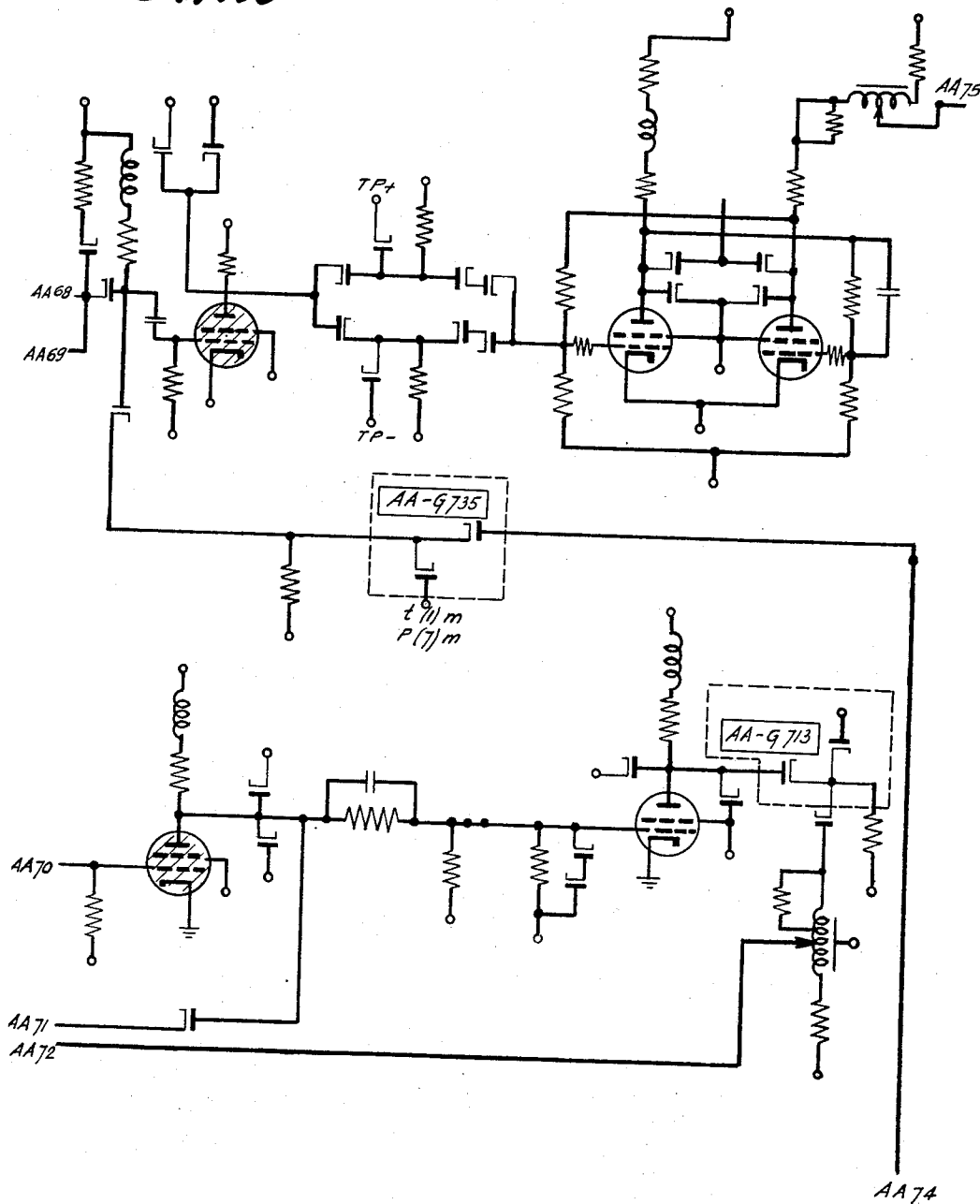
J. P. ECKERT, JR., ETAL
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BINARY CODED ALPHANUMERIC CHARACTERS

3,133,190

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110 Sheets-Sheet 62

FIG. 11a



INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George W. H. H. H.*
ATTORNEY

May 12, 1964

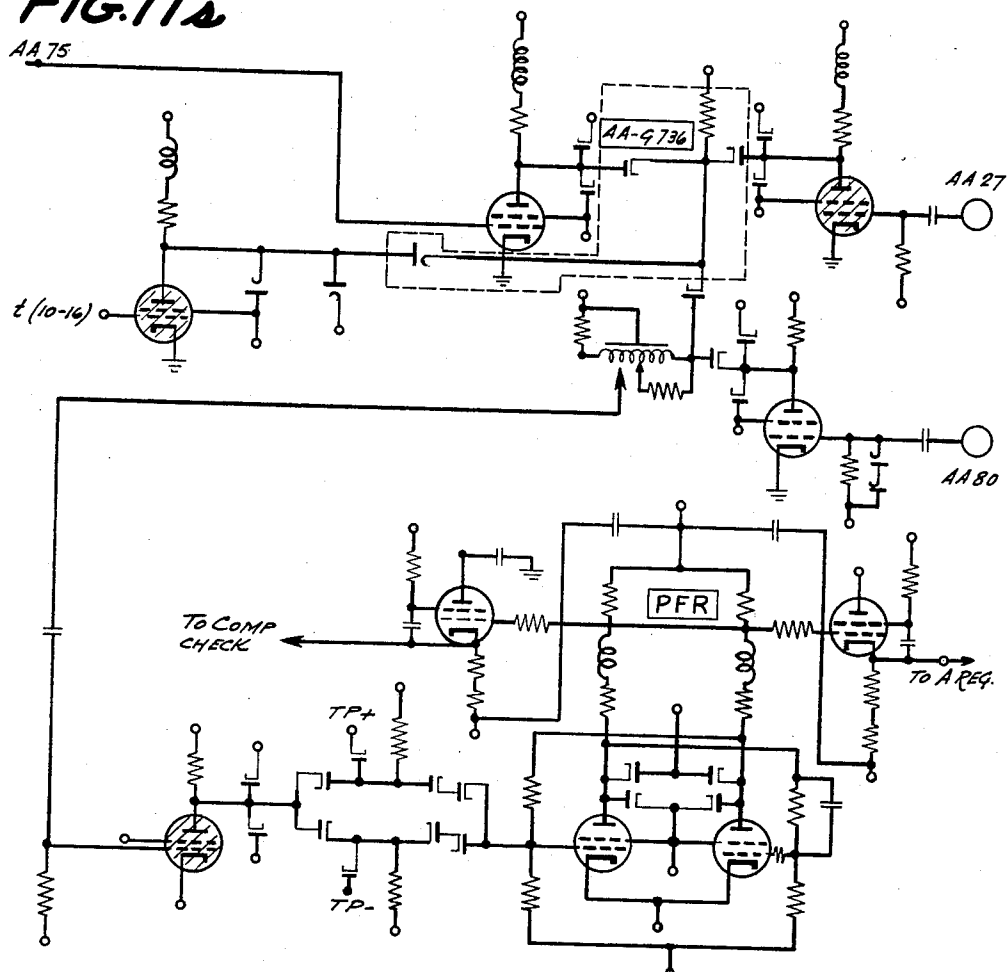
J. P. ECKERT, JR., ETAL
UNIVERSAL AUTOMATIC COMPUTER UTILIZING
BINARY CODED ALPHANUMERIC CHARACTERS

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FIG. 11A



INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George Feltz*
ATTORNEY

May 12, 1964

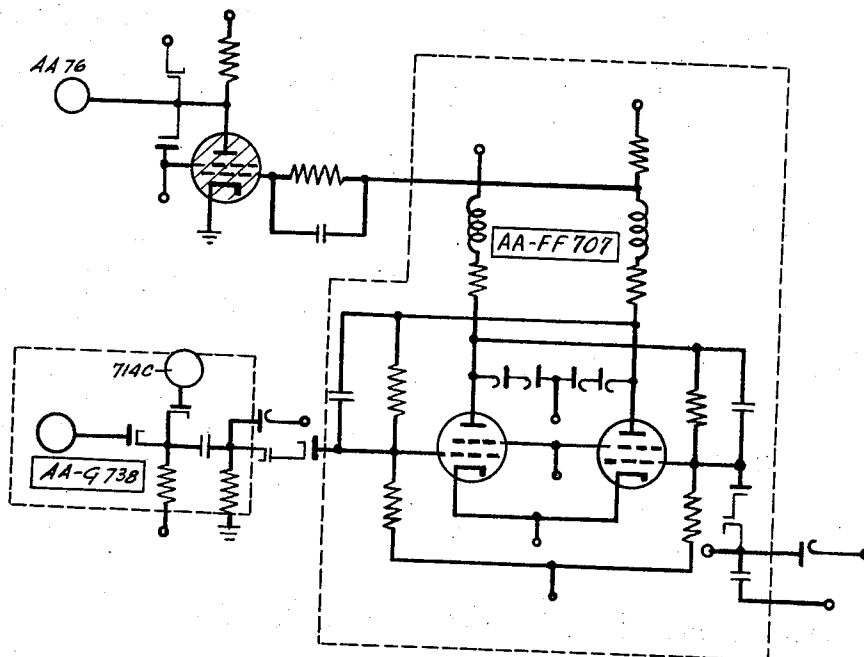
J. P. ECKERT, JR., ET AL
UNIVERSAL AUTOMATIC COMPUTER UTILIZING
BINARY CODED ALPHANUMERIC CHARACTERS

3,133,190

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110 Sheets-Sheet 64

FIG. 11a



INVENTORS
J. P. ECKERT, JR.
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ROBERT F. SHAW
H. FRAZER WELSH
BY *George F. Feltz*
ATTORNEY

May 12, 1964

J. P. ECKERT, JR., ETAL
UNIVERSAL AUTOMATIC COMPUTER UTILIZING
BINARY CODED ALPHANUMERIC CHARACTERS

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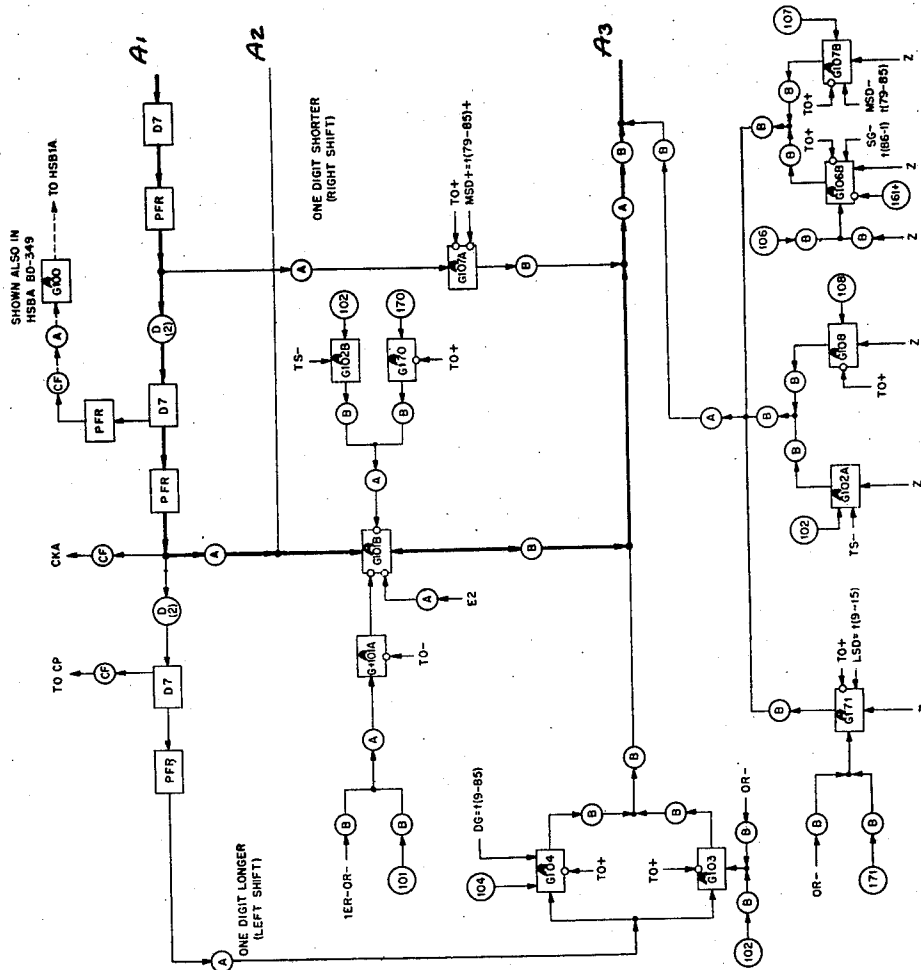


FIG. 12a

INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George Veltz*
ATTORNEY

May 12, 1964

J. P. ECKERT, JR., ETAL
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BINARY CODED ALPHANUMERIC CHARACTERS

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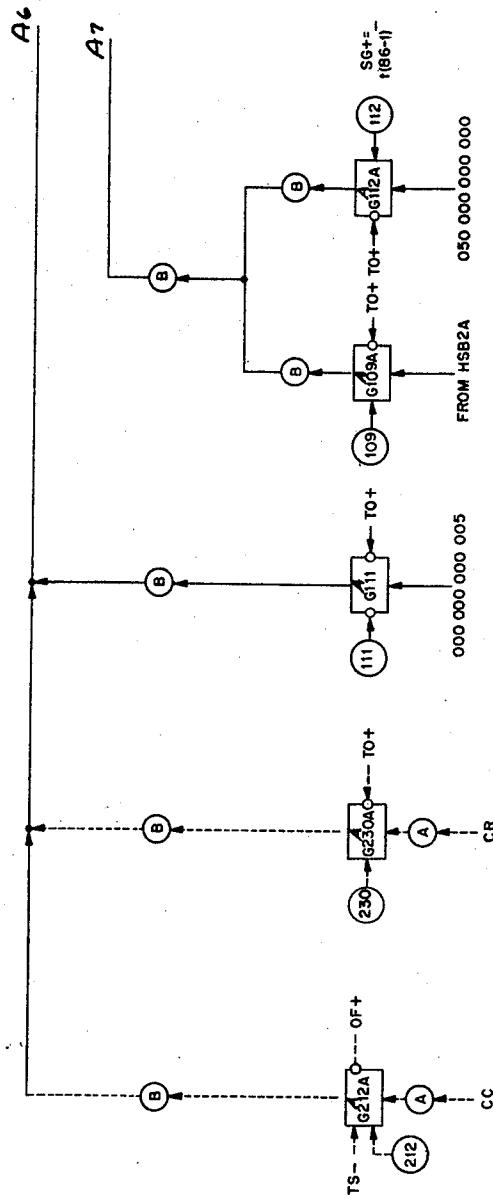


FIG. 12b

INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George W. Elgorth*
ATTORNEY

Filed March 31, 1952

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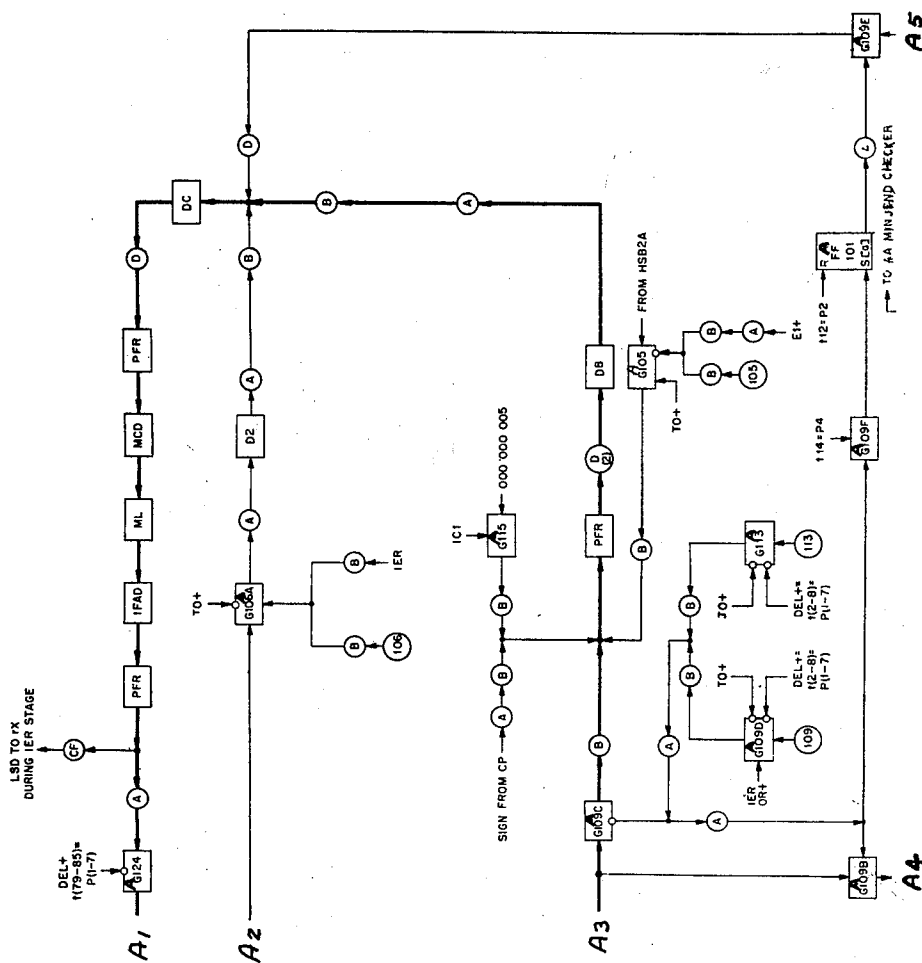


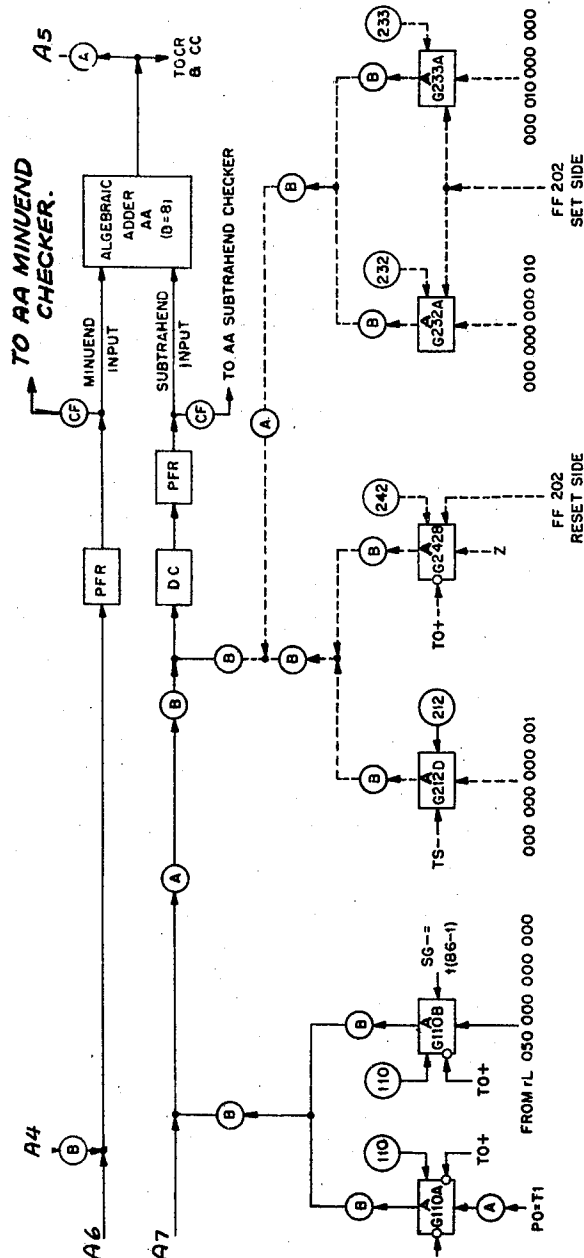
FIG. 12c

INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George F. [Signature]*
ATTORNEY

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INVENTORS
J. PRESPEER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George Feltz*
ATTORNEY

FIG. 12d

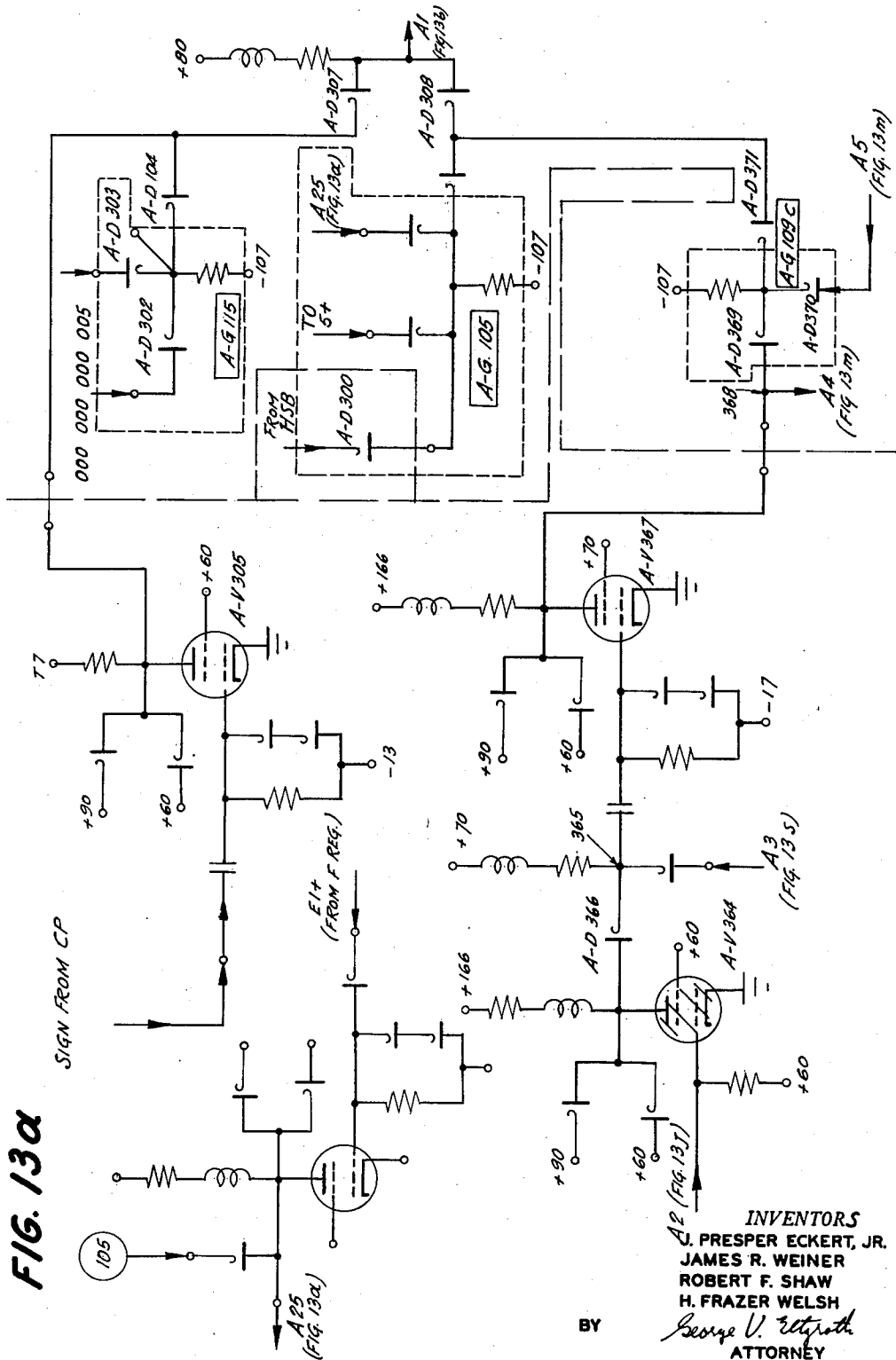
May 12, 1964

J. P. ECKERT, JR., ETAL
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BINARY CODED ALPHANUMERIC CHARACTERS

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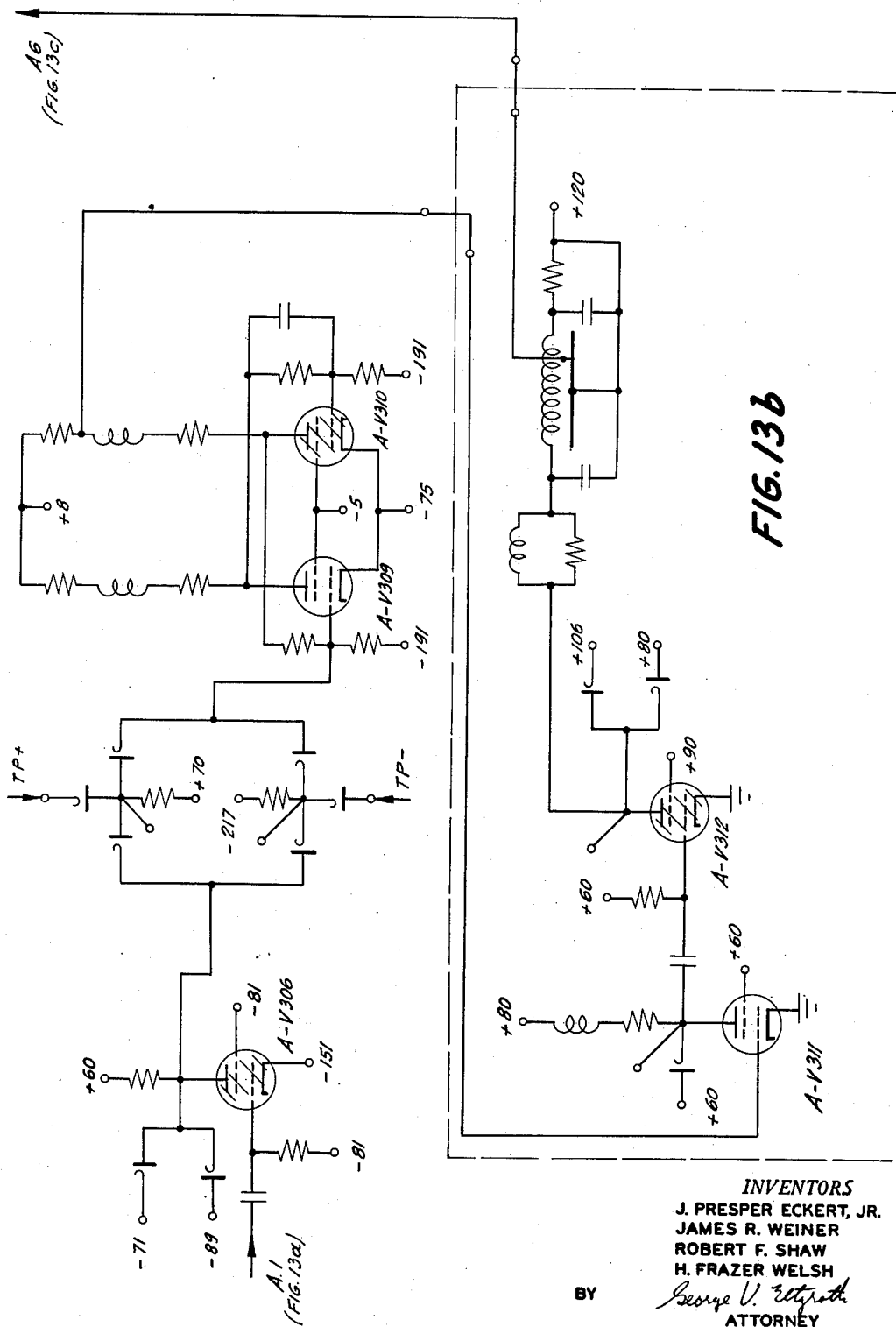
May 12, 1964

J. P. ECKERT, JR., ET AL
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BINARY CODED ALPHANUMERIC CHARACTERS

3,133,190

Filed March 31, 1952

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INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George V. Zitzroth*
ATTORNEY

May 12, 1964

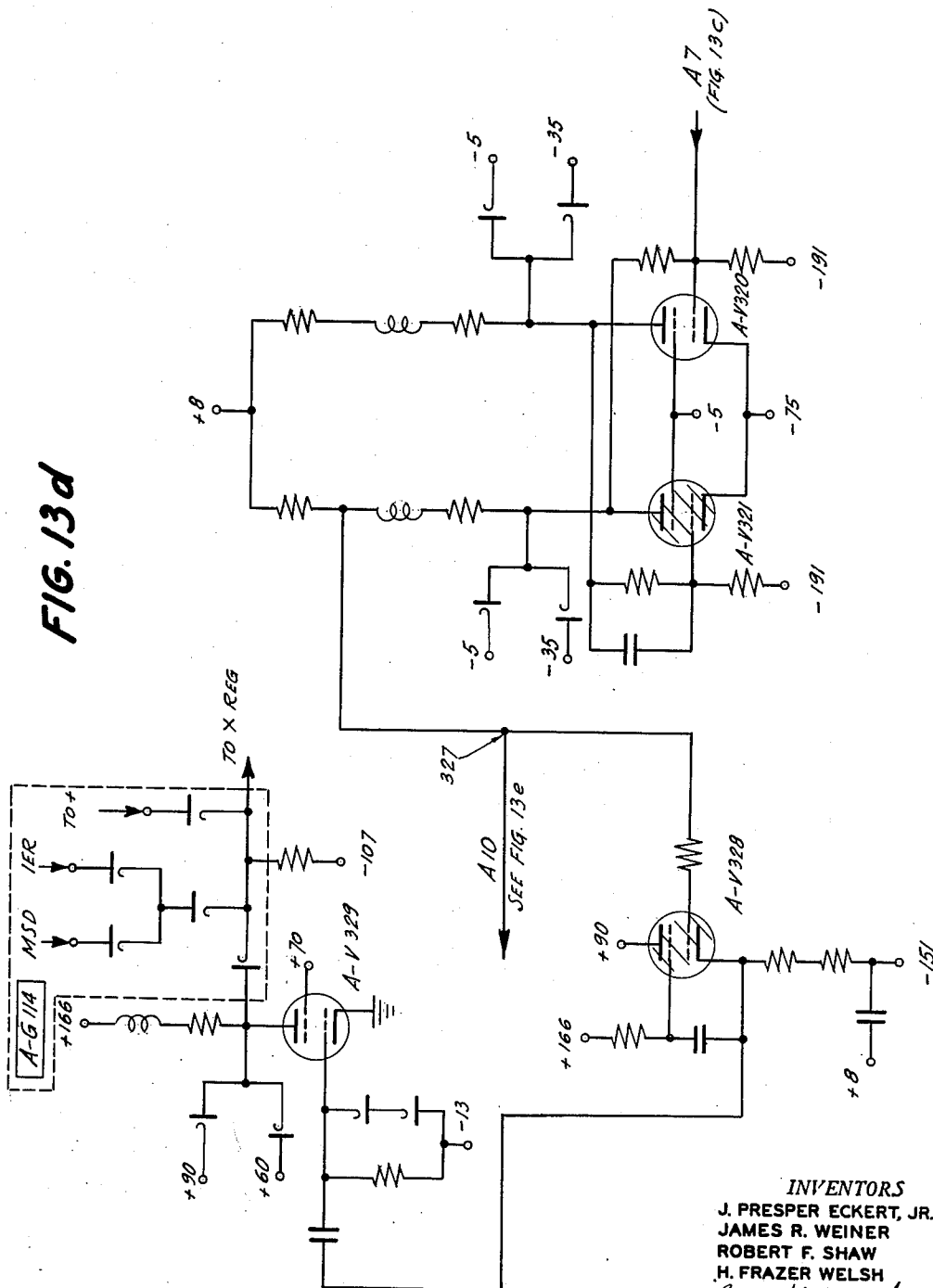
J. P. ECKERT, JR., ET AL
UNIVERSAL AUTOMATIC COMPUTER UTILIZING
BINARY CODED ALPHANUMERIC CHARACTERS

3,133,190

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FIG. 13d



INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George V. Zettrath*
ATTORNEY

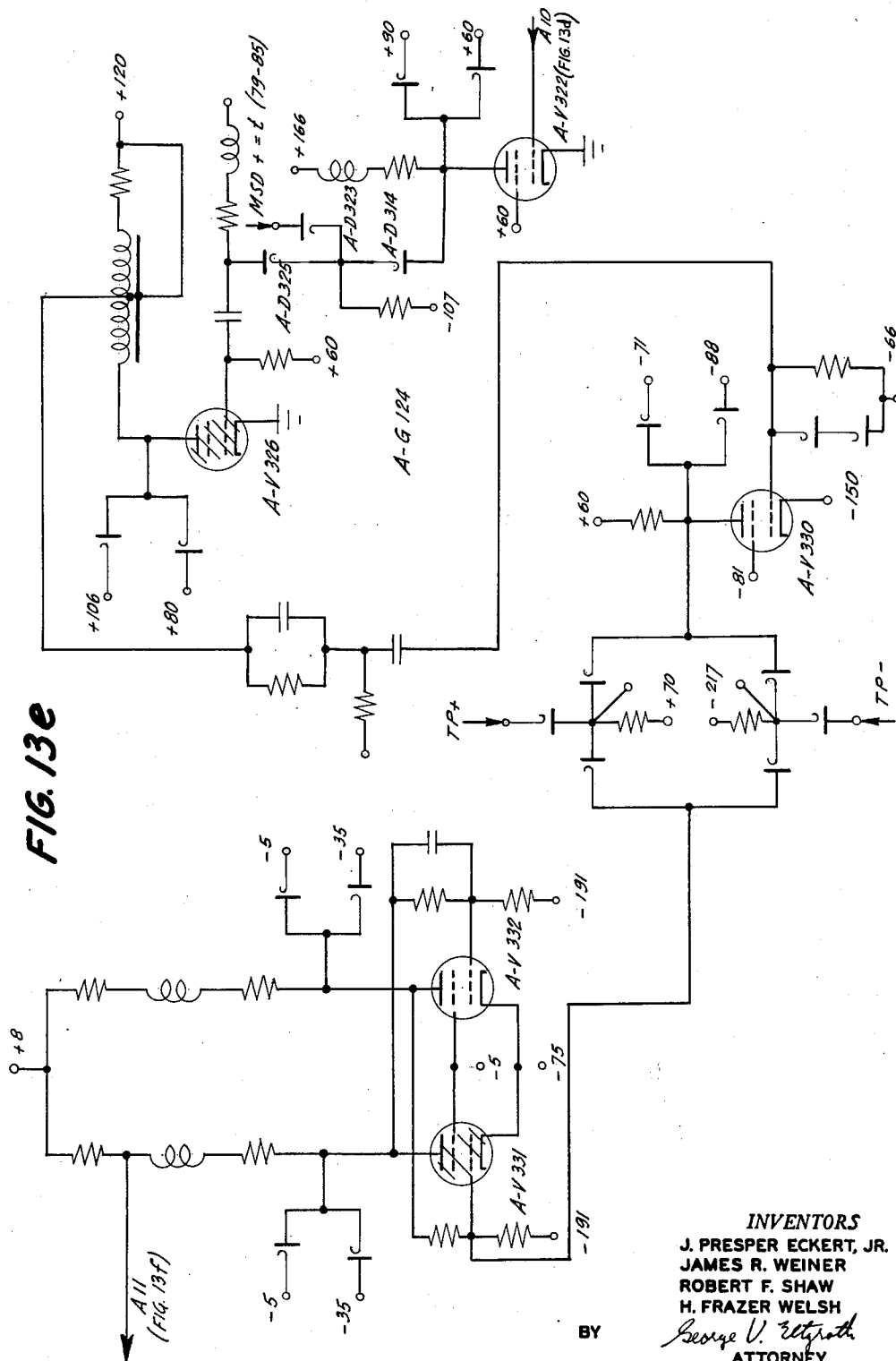
May 12, 1964

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BINARY CODED ALPHANUMERIC CHARACTERS

3,133,190

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INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George V. Retzger*
ATTORNEY

May 12, 1964

J. P. ECKERT, JR., ETAL
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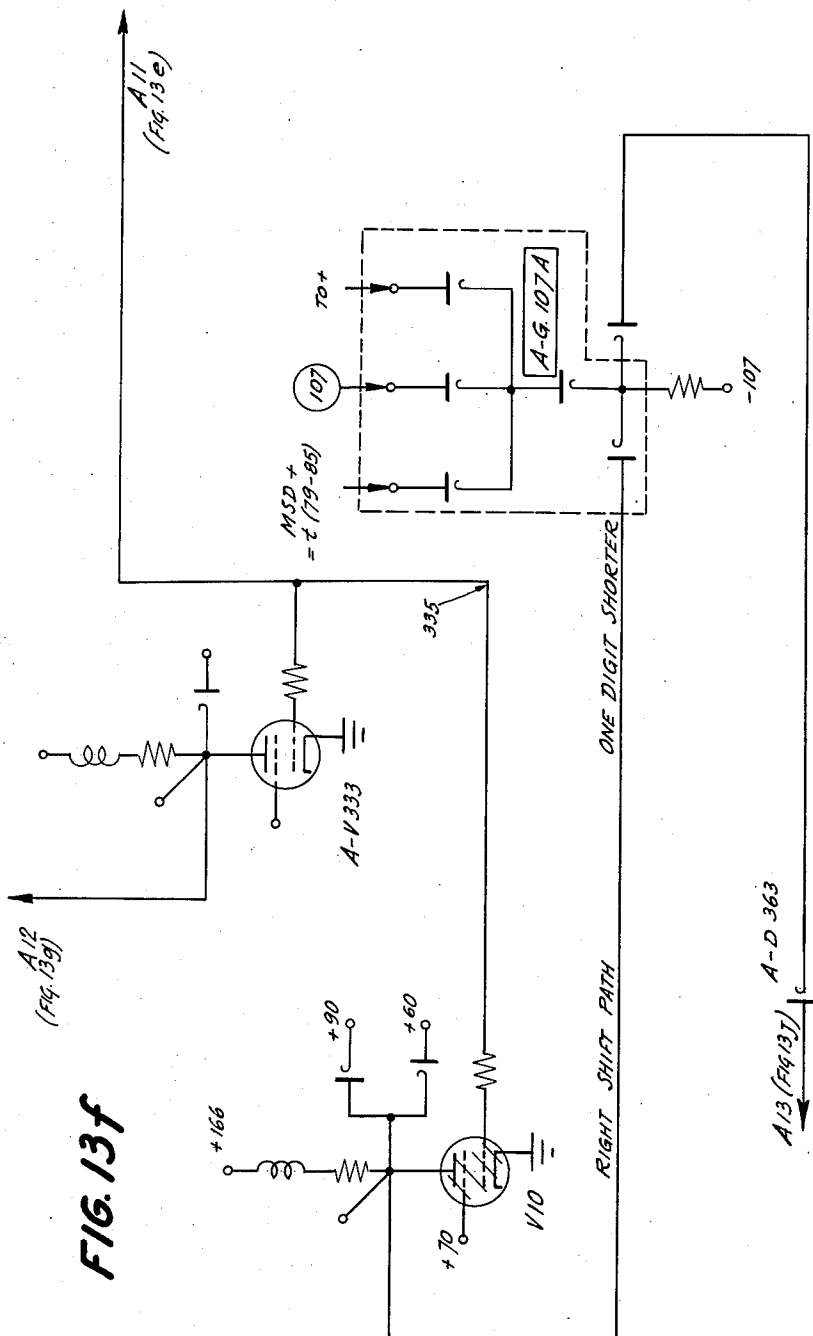


FIG. 13f

INVENTORS
J. PRESER ECKERT, JR.
JAMES R. WEINER
ROBERT F. SHAW
H. FRAZER WELSH
BY *George V. Zettrath*
ATTORNEY

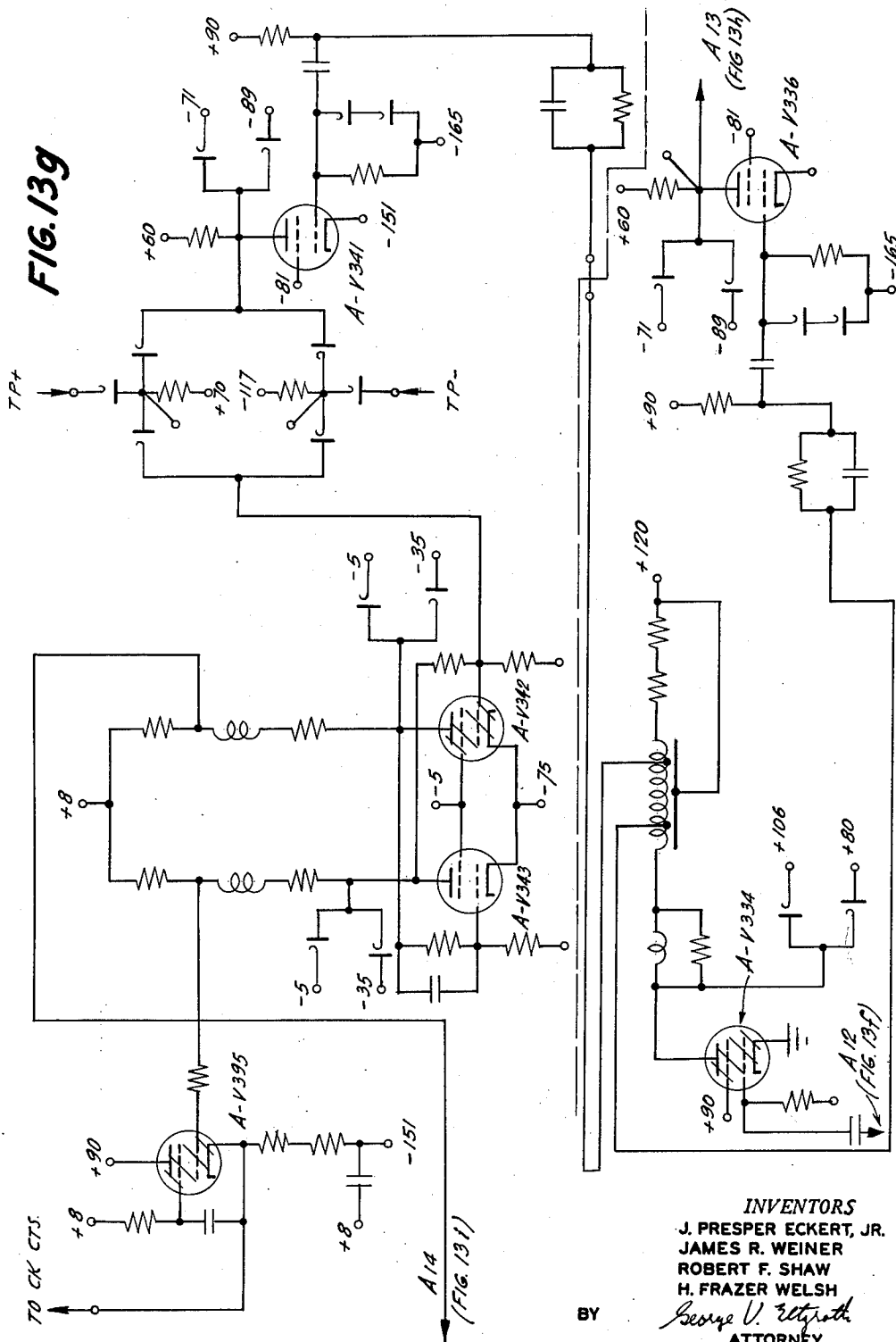
May 12, 1964

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BINARY CODED ALPHANUMERIC CHARACTERS

3,133,190

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May 12, 1964

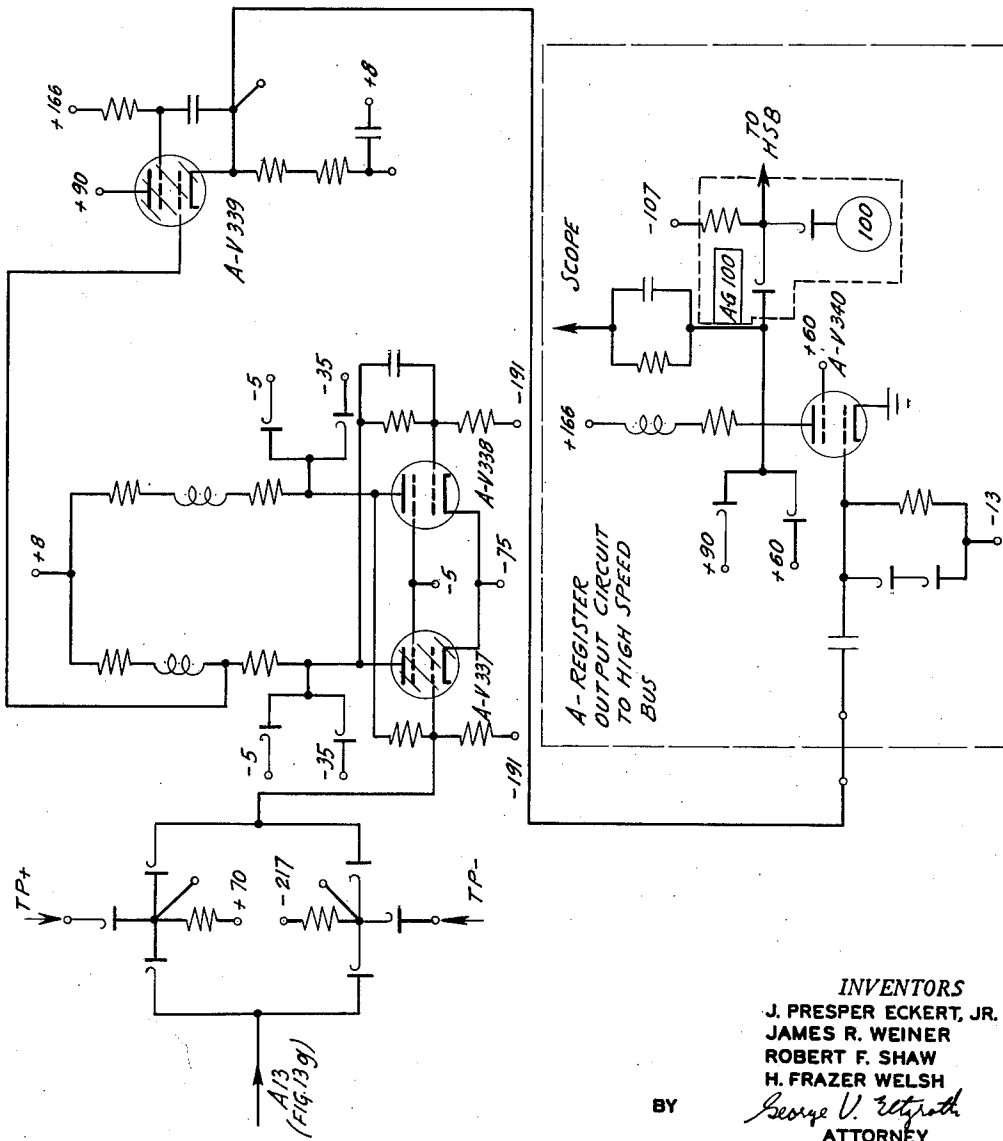
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FIG. 13h



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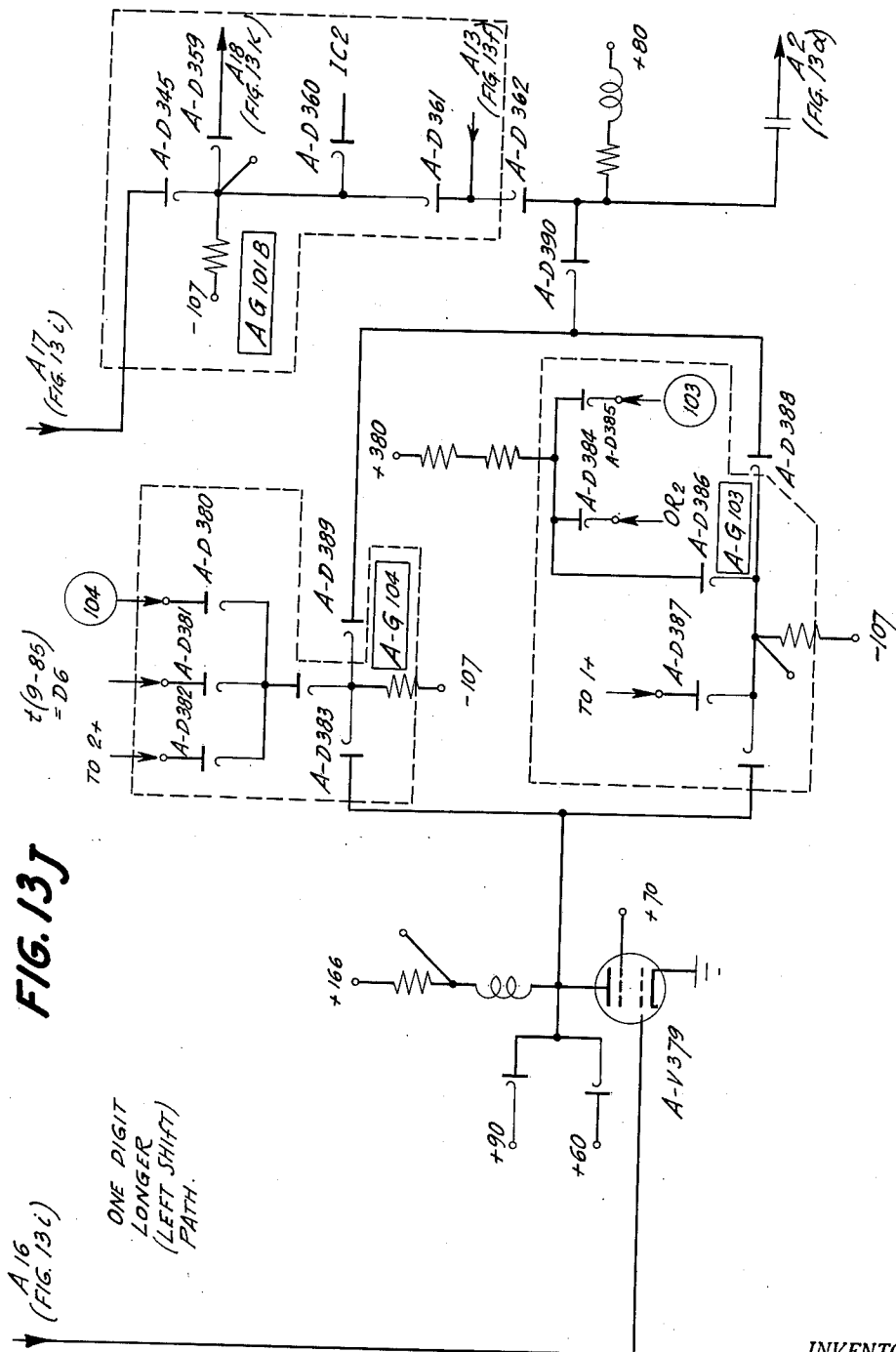
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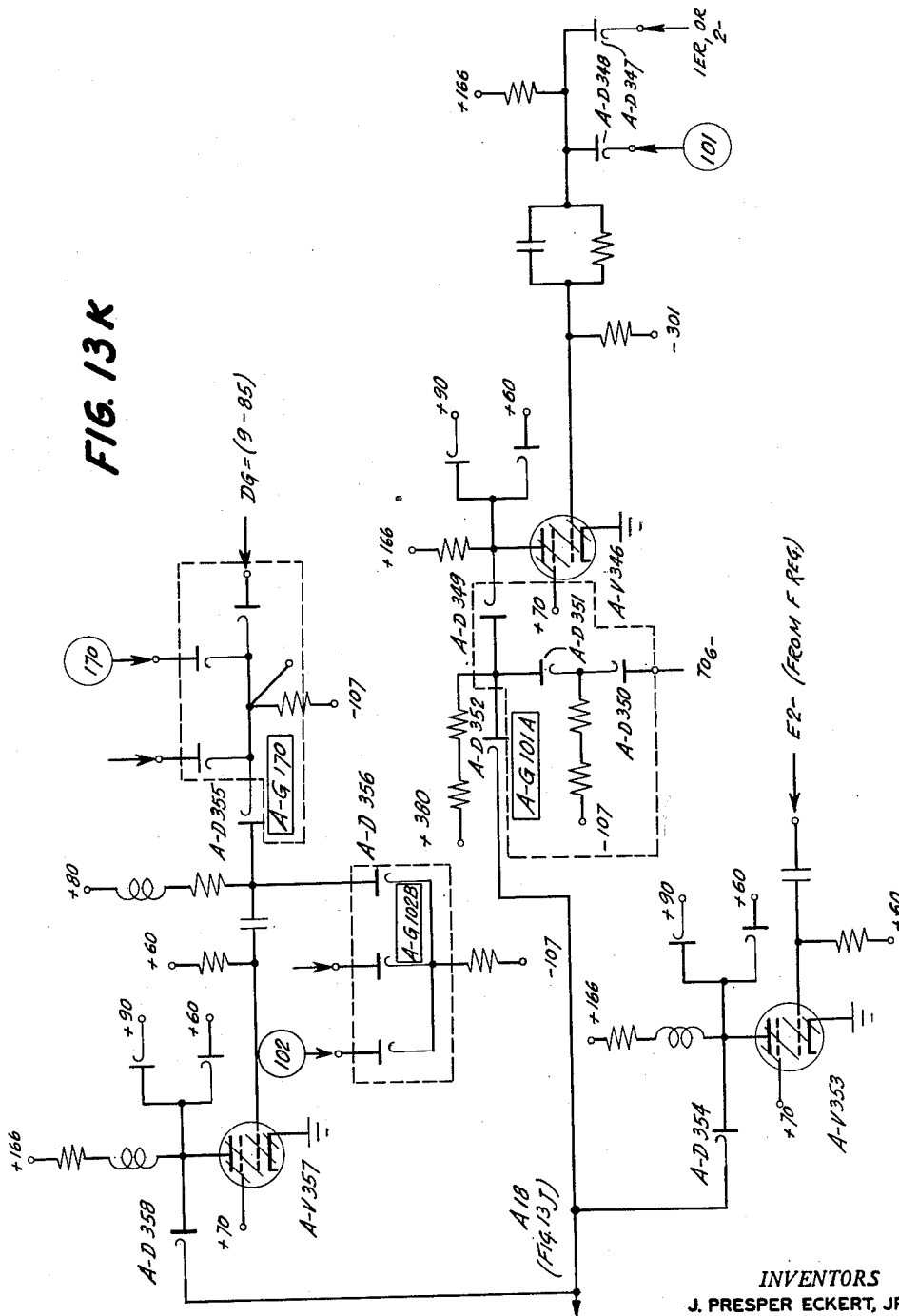
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FIG. 13K



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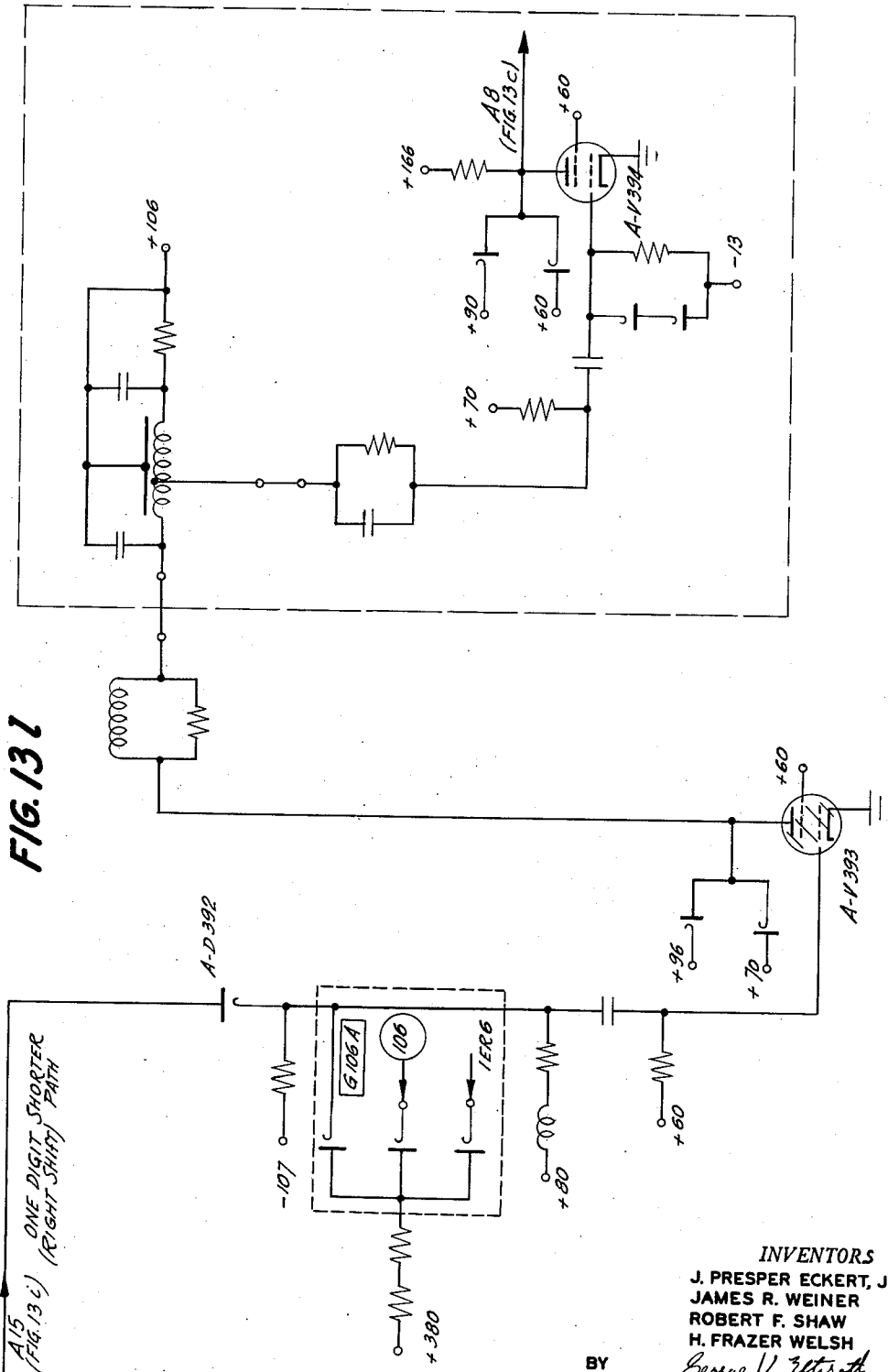
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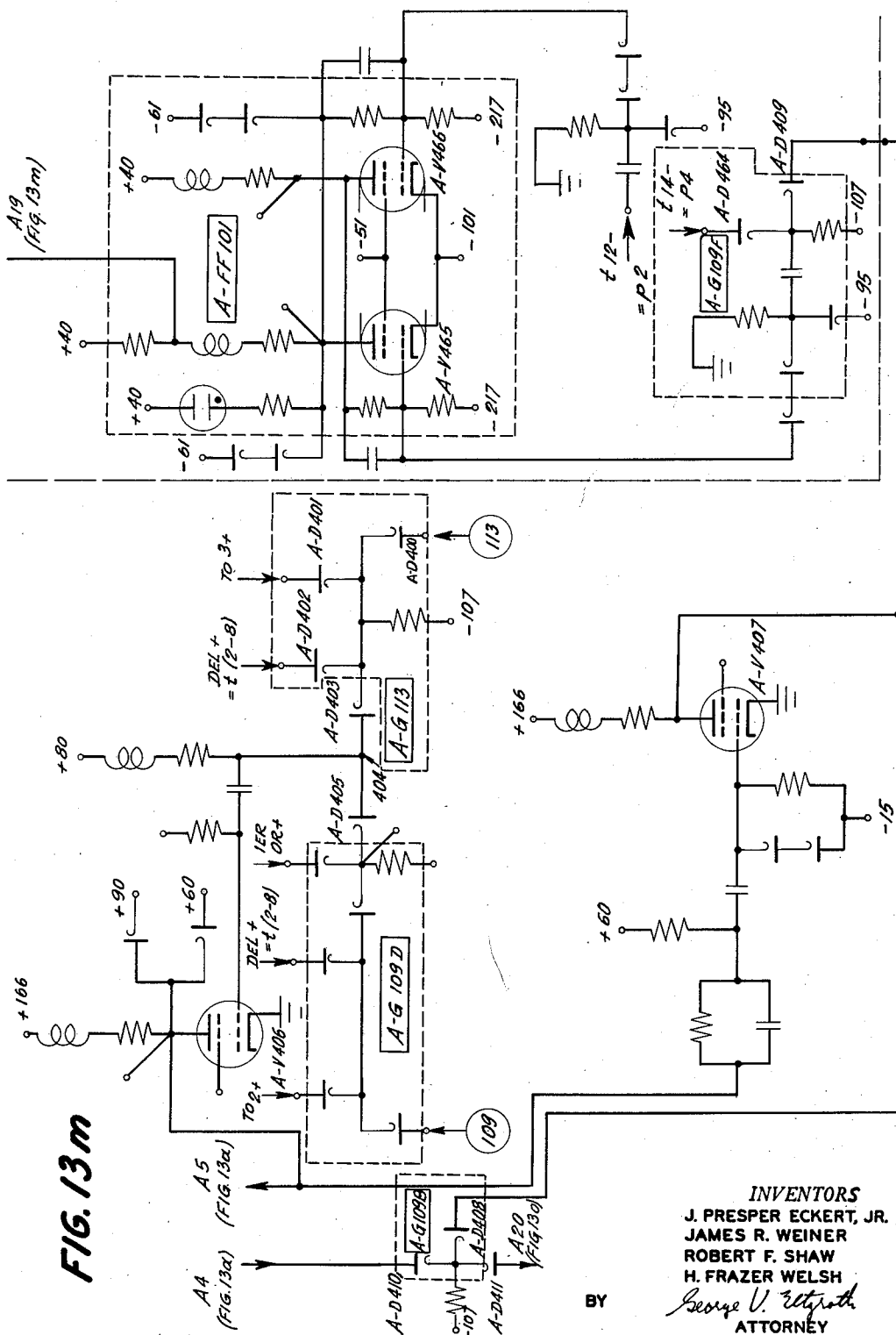
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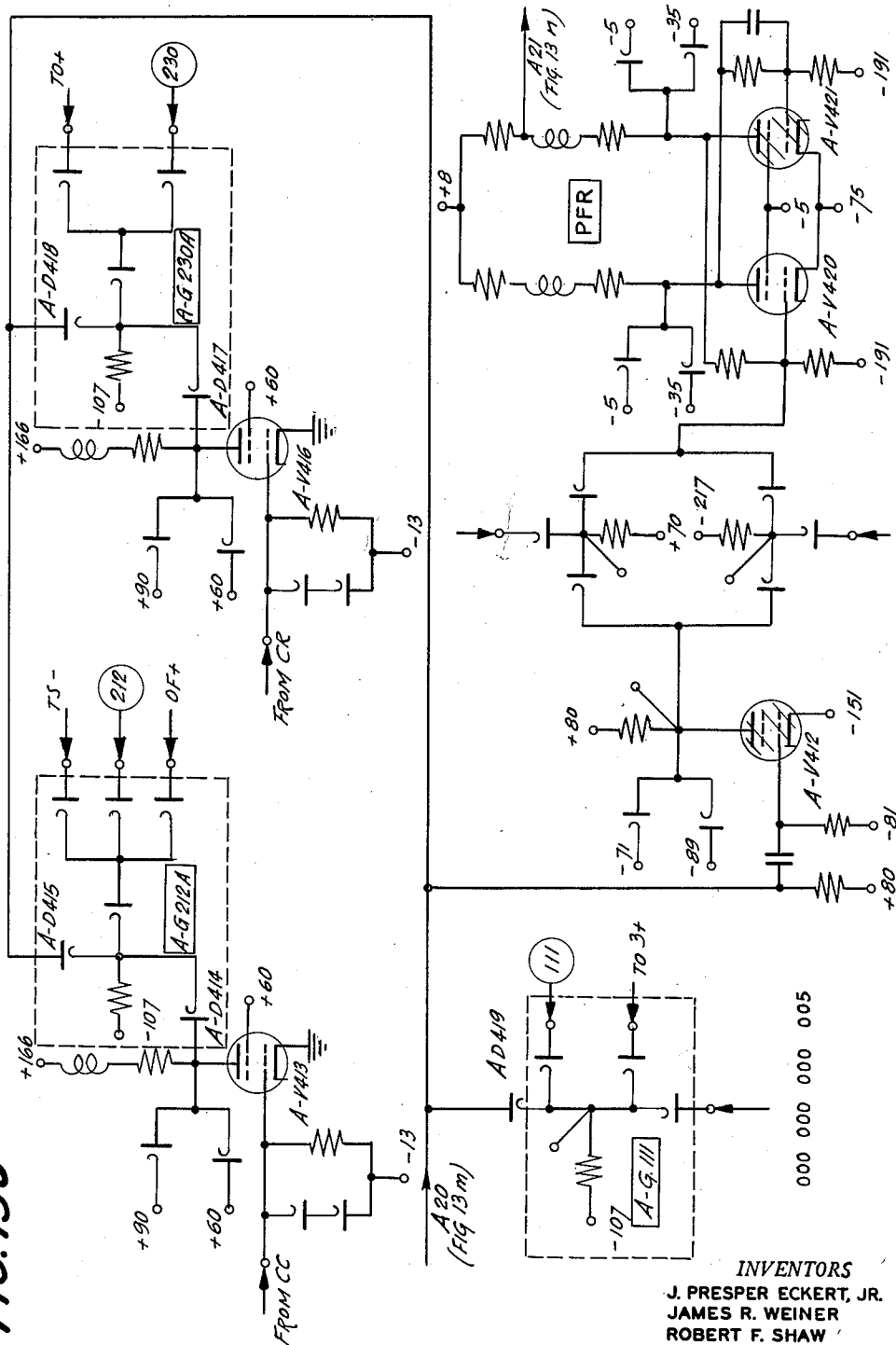


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FIG. 130



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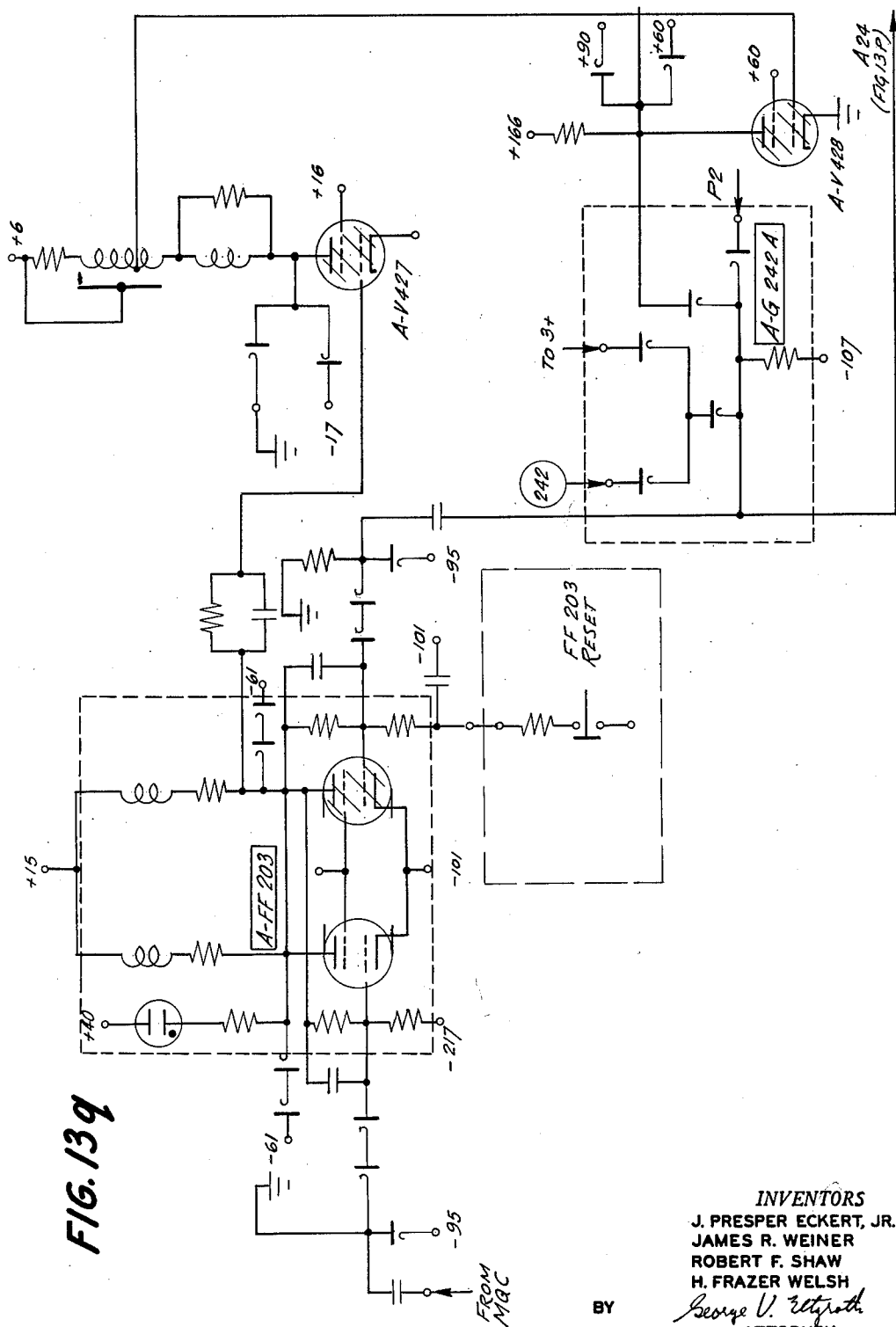


FIG. 13q

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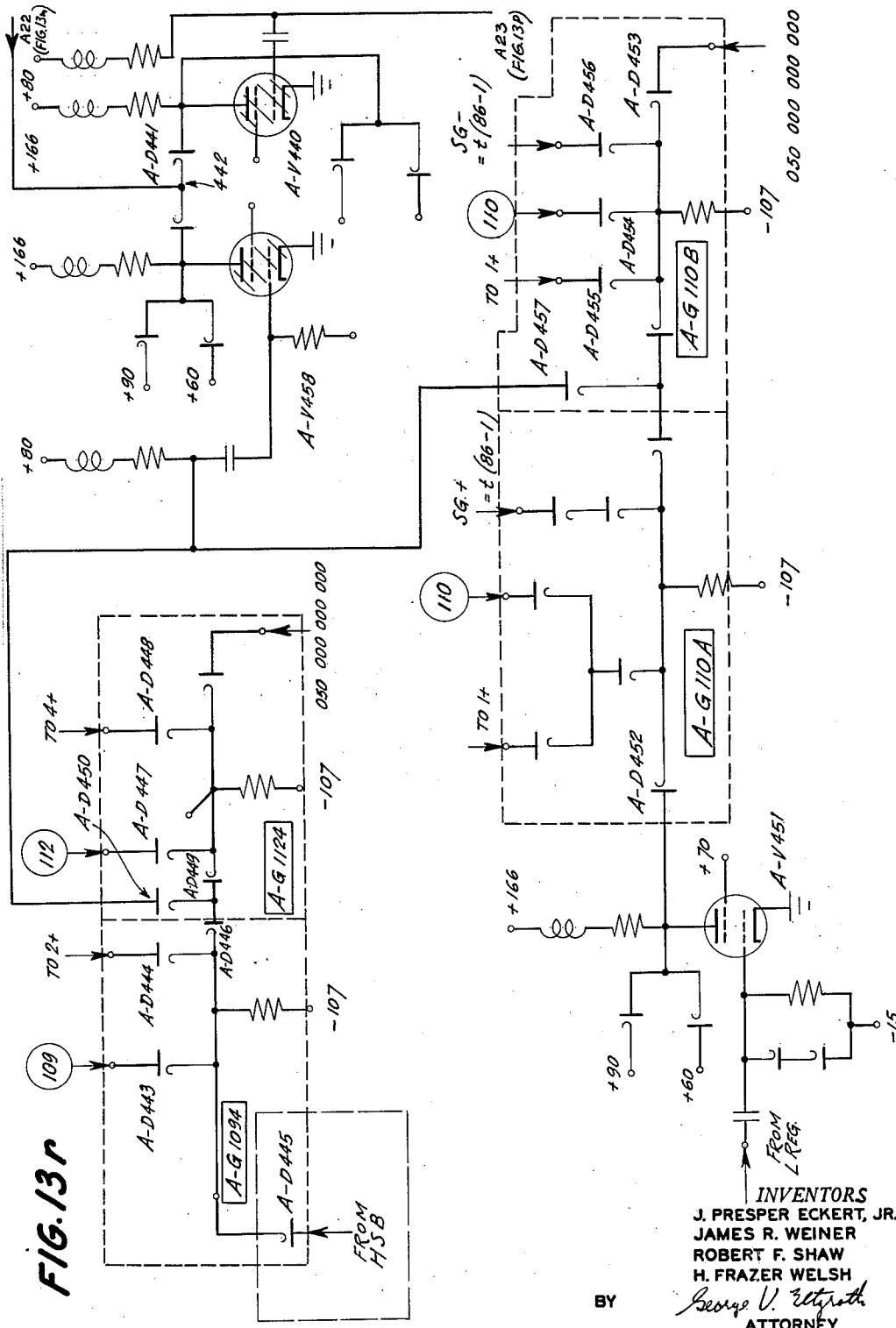
May 12, 1964

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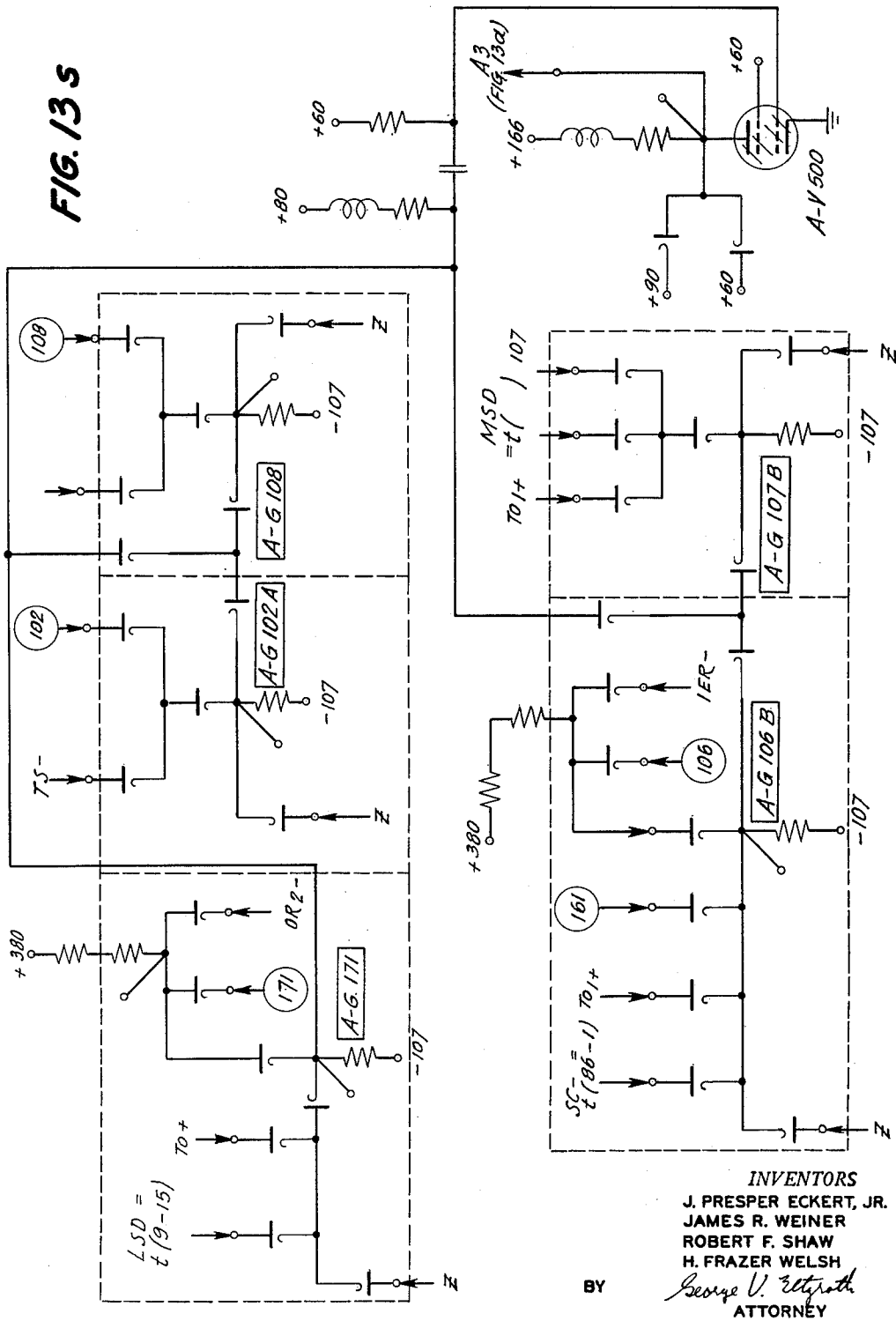
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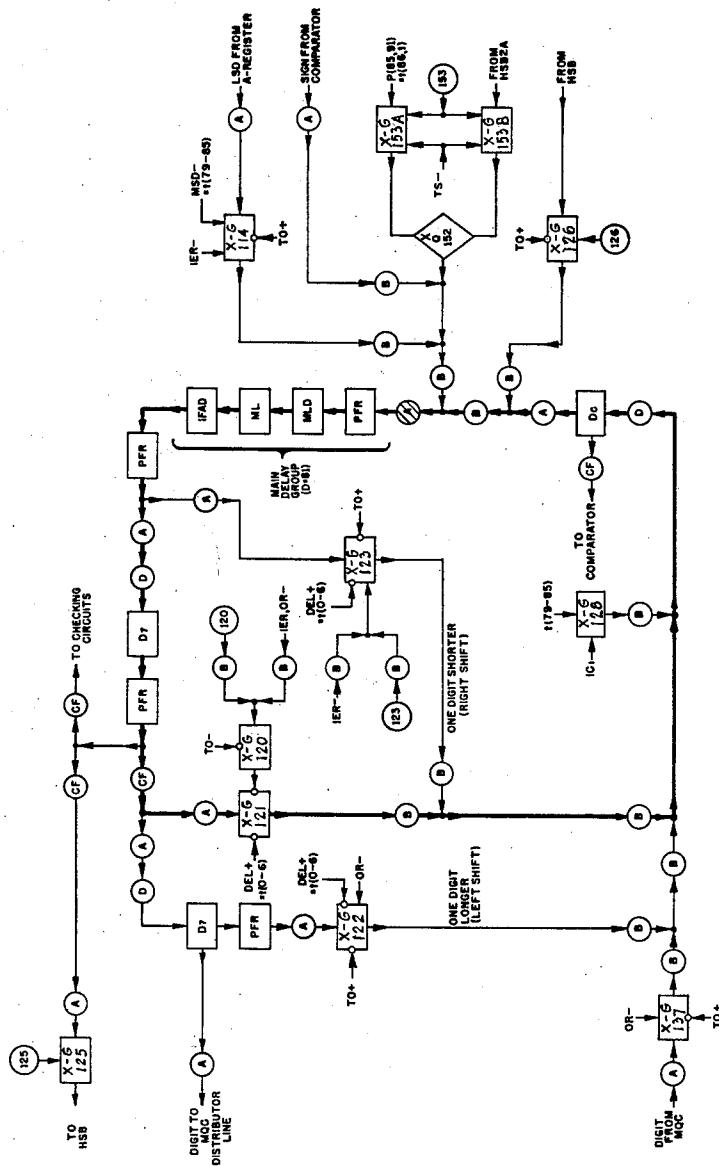
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FIG. 14



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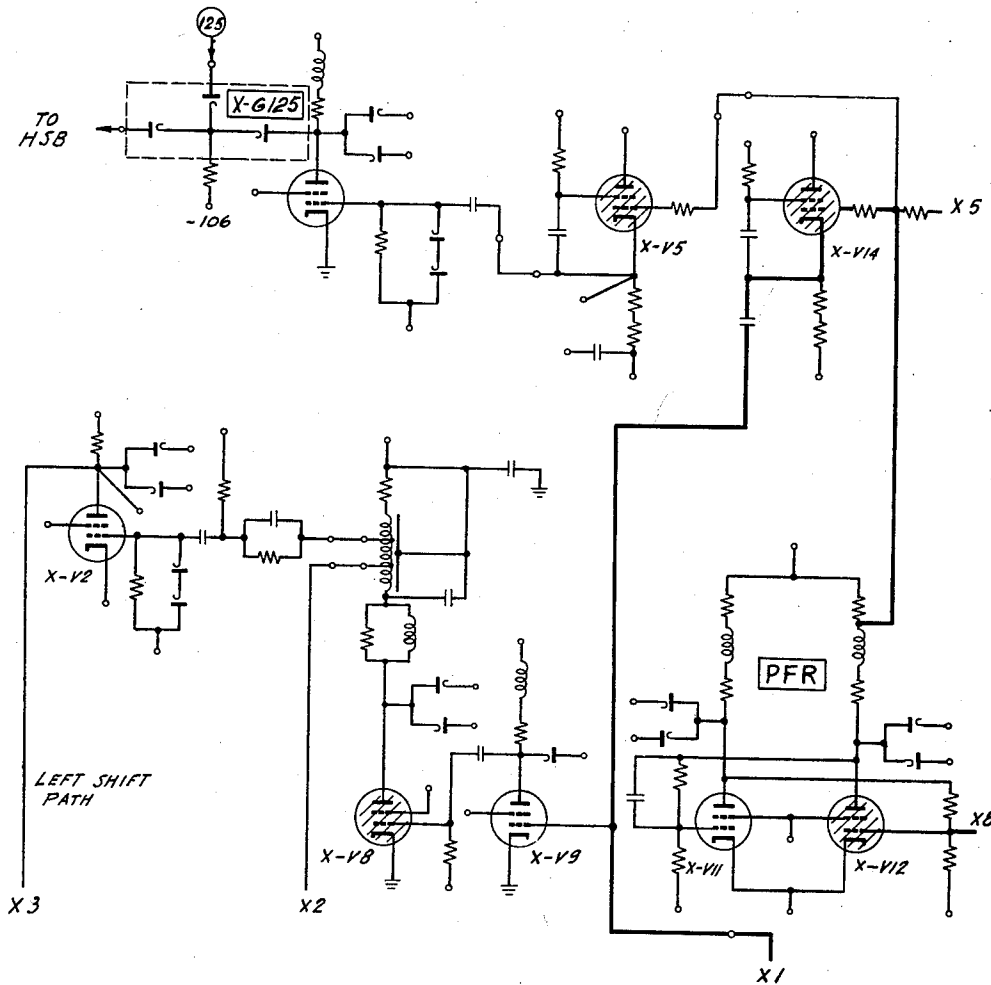
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FIG. 15a



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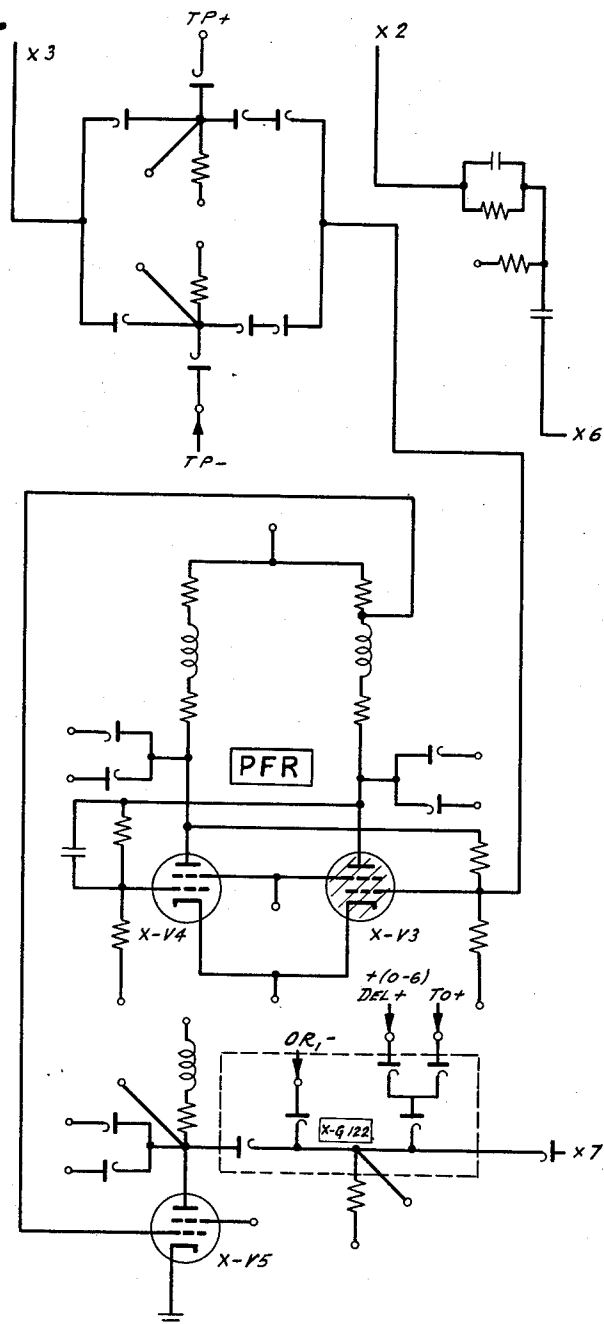
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FIG. 15b



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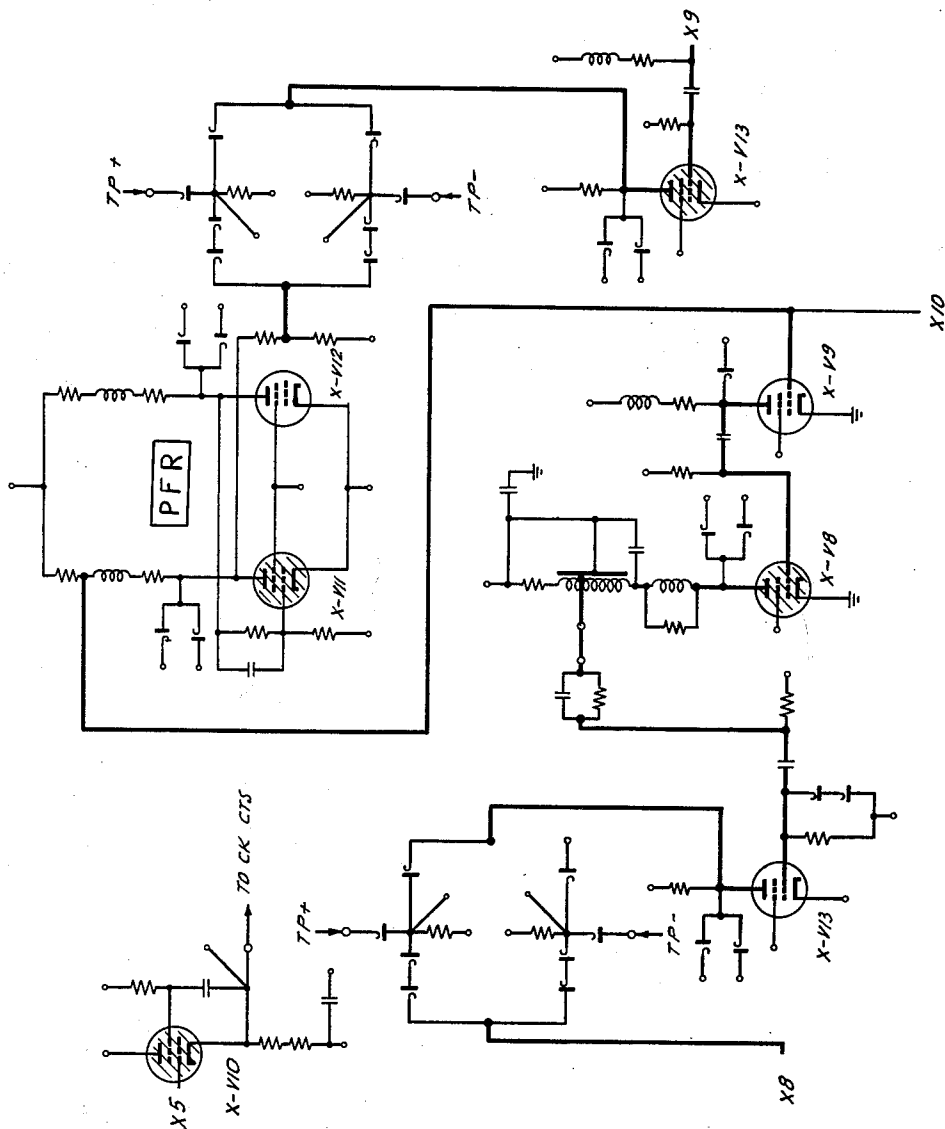


FIG. 15c

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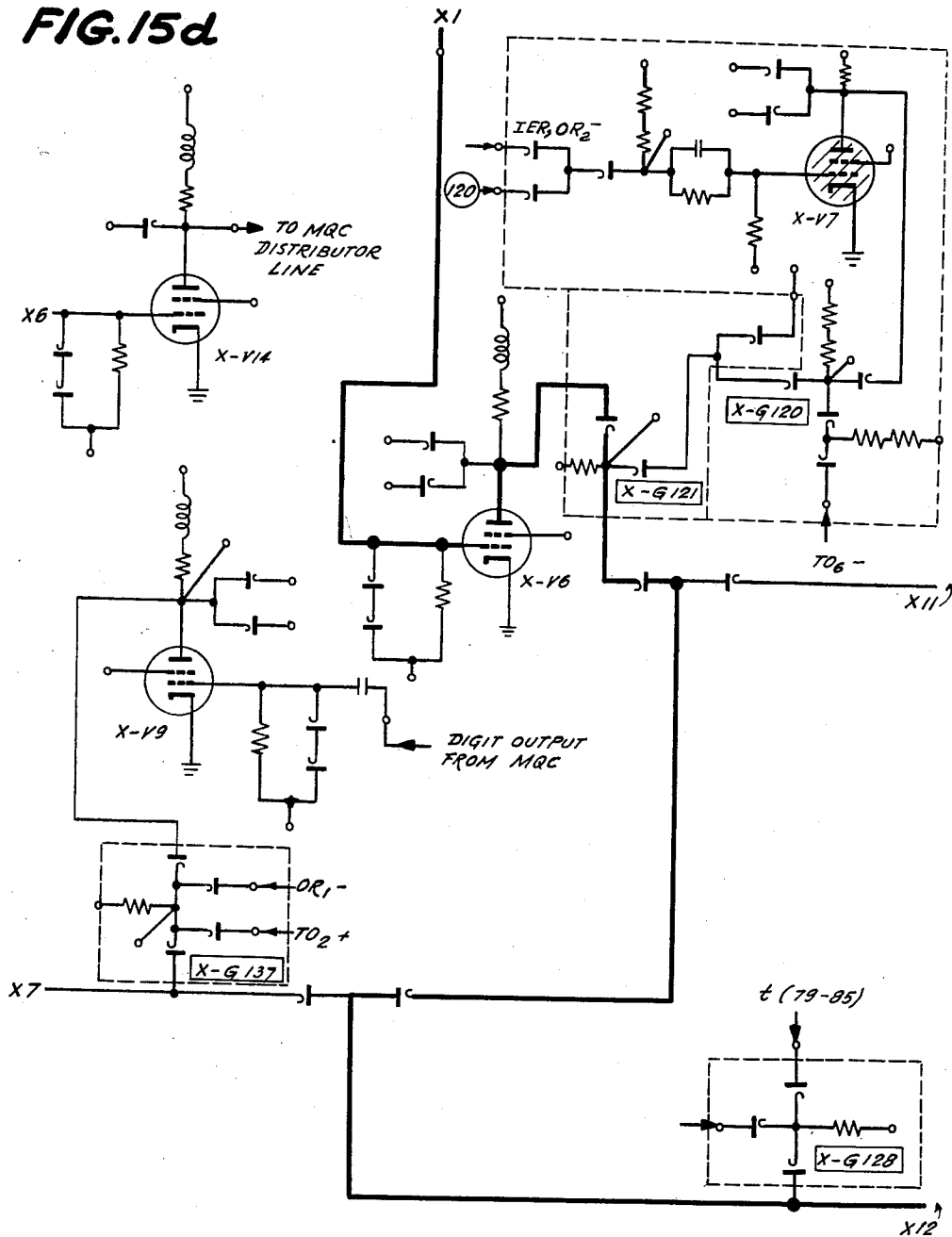
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FIG. 15d



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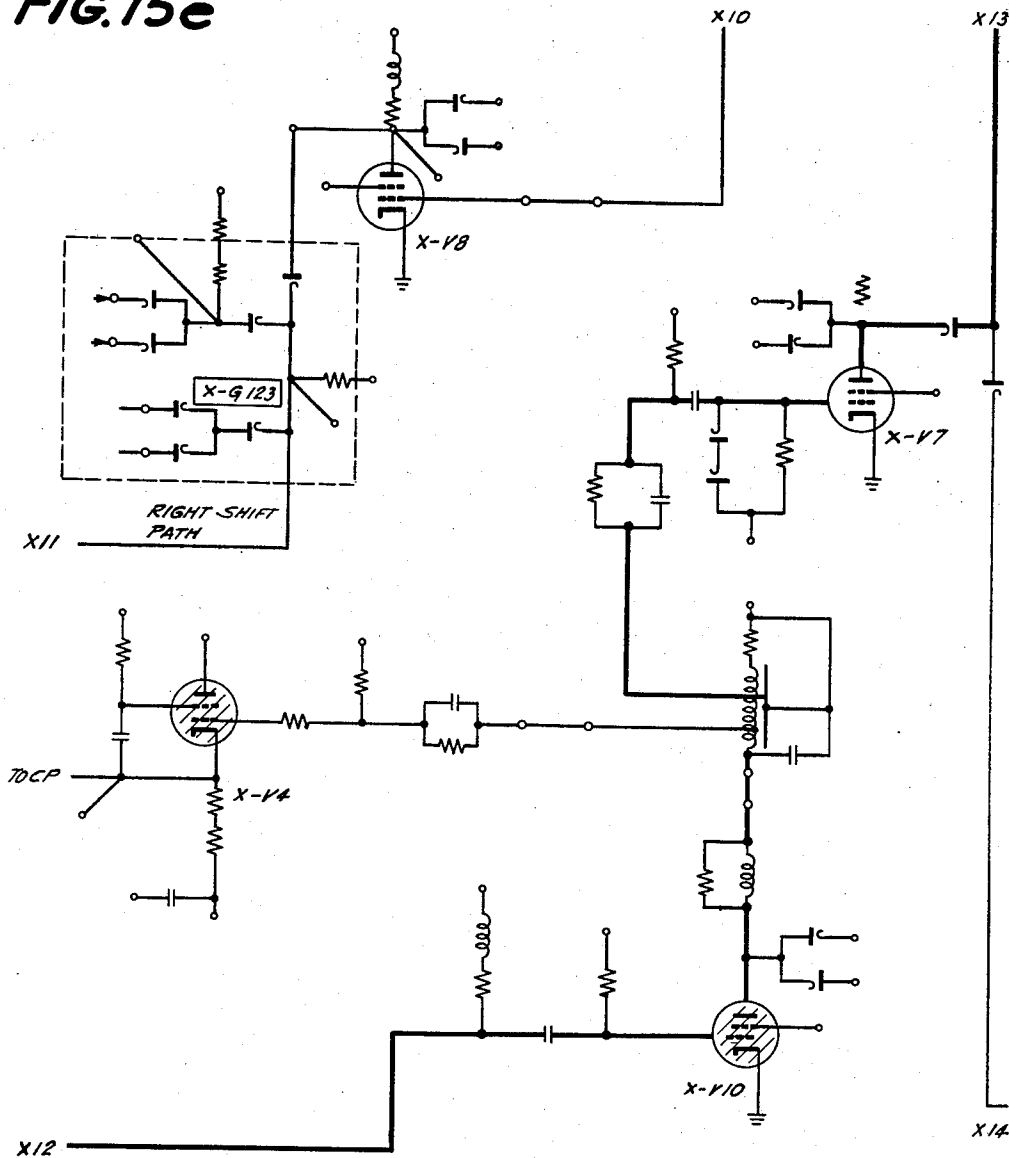
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FIG. 15e



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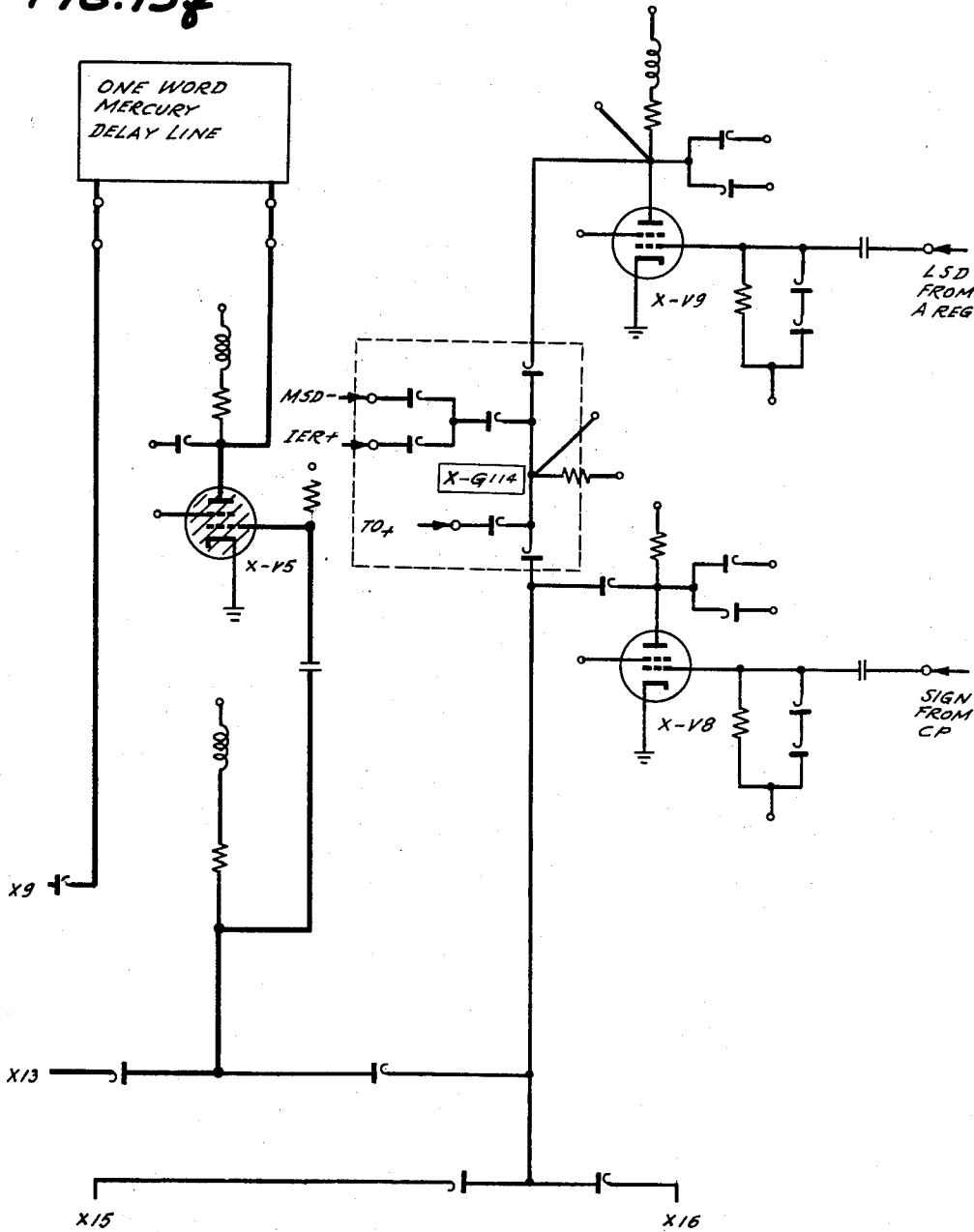
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FIG. 15f



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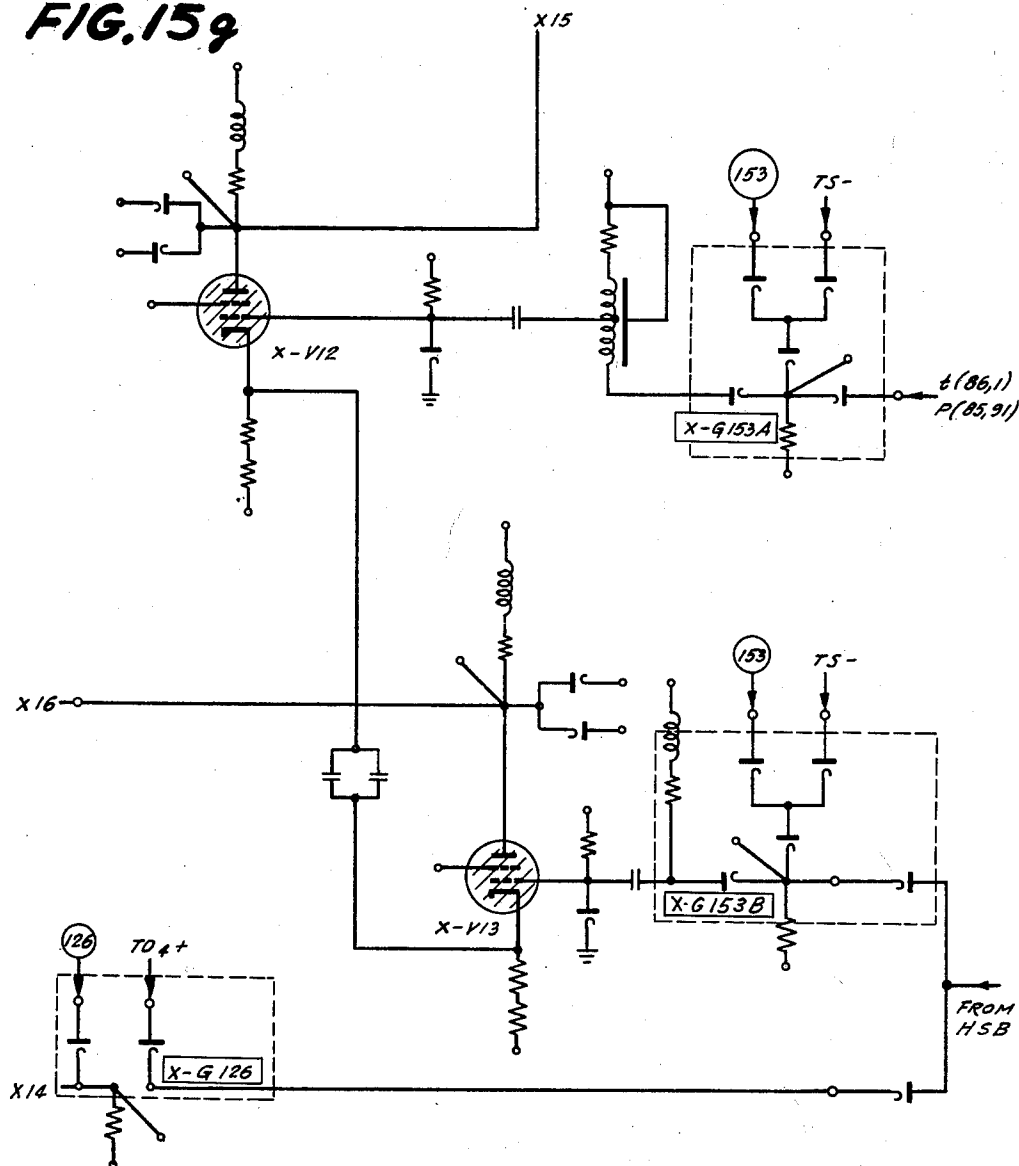
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FIG. 15g



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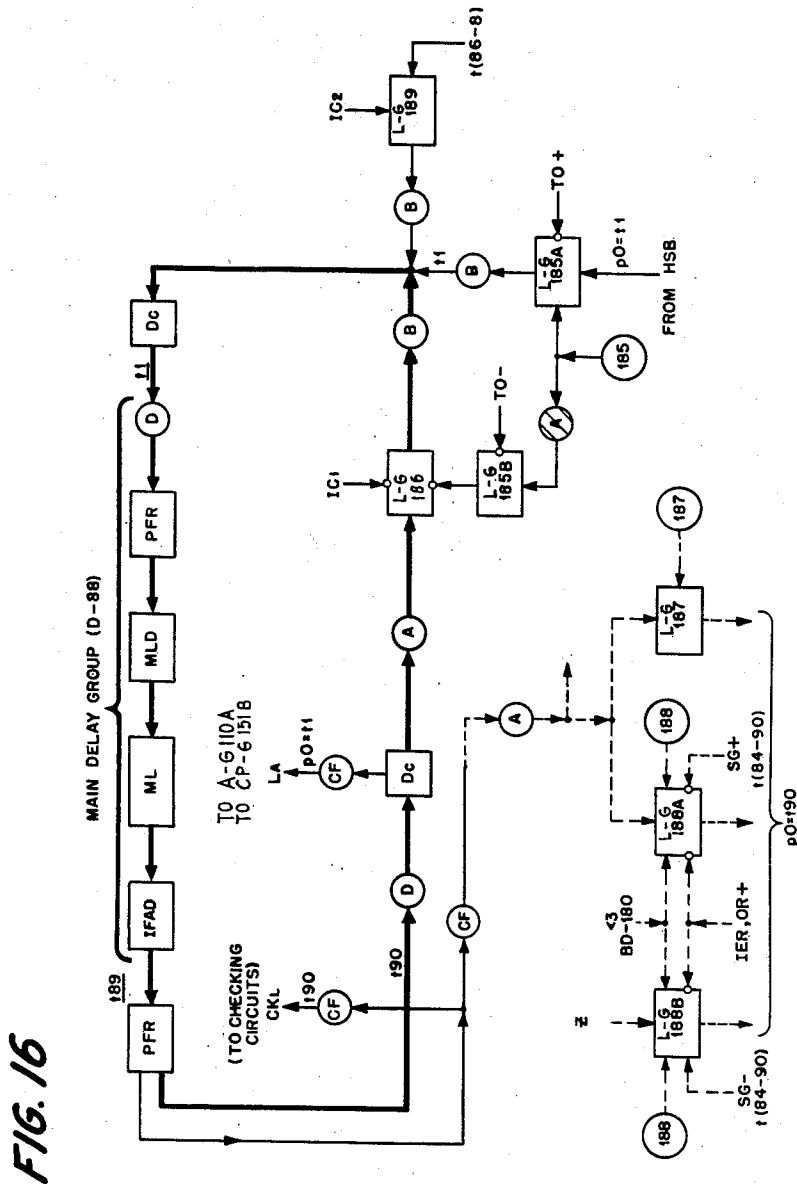
May 12, 1964

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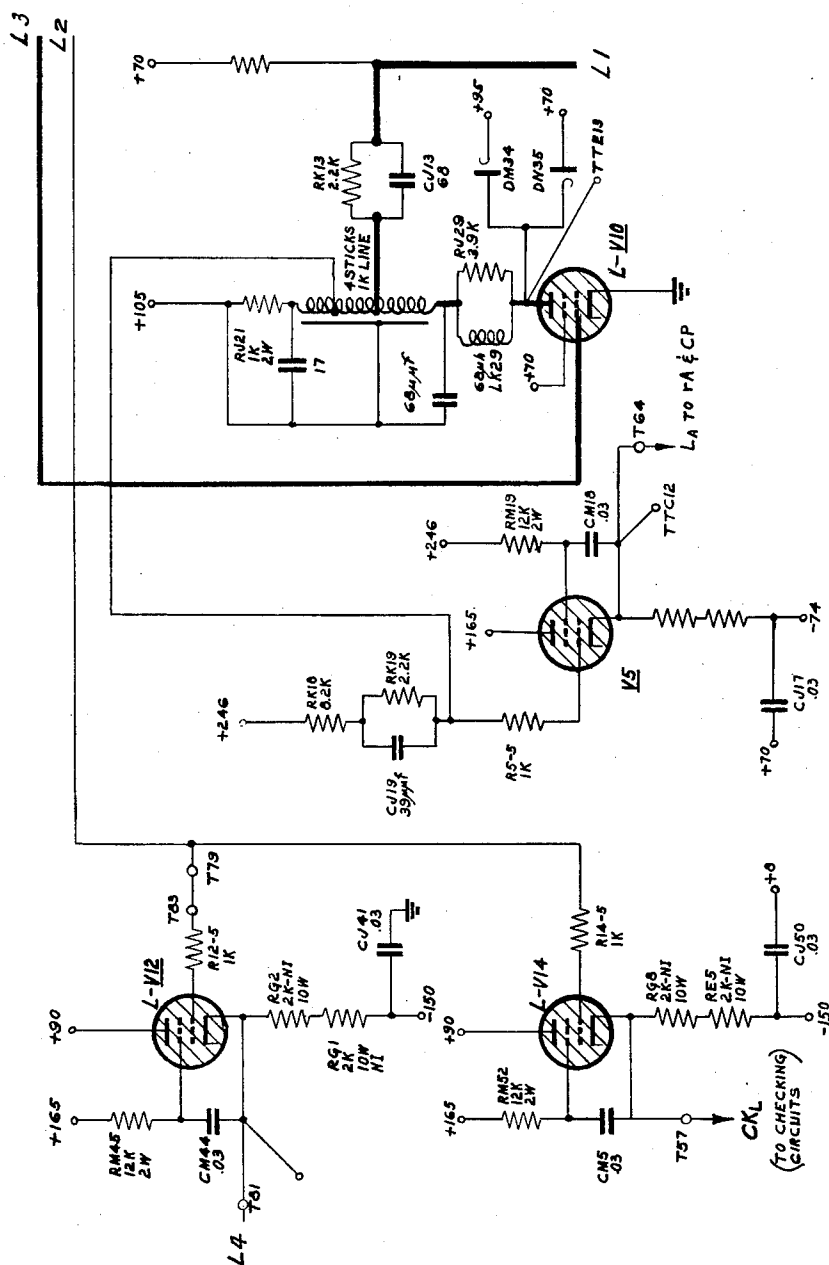


FIG. 17a

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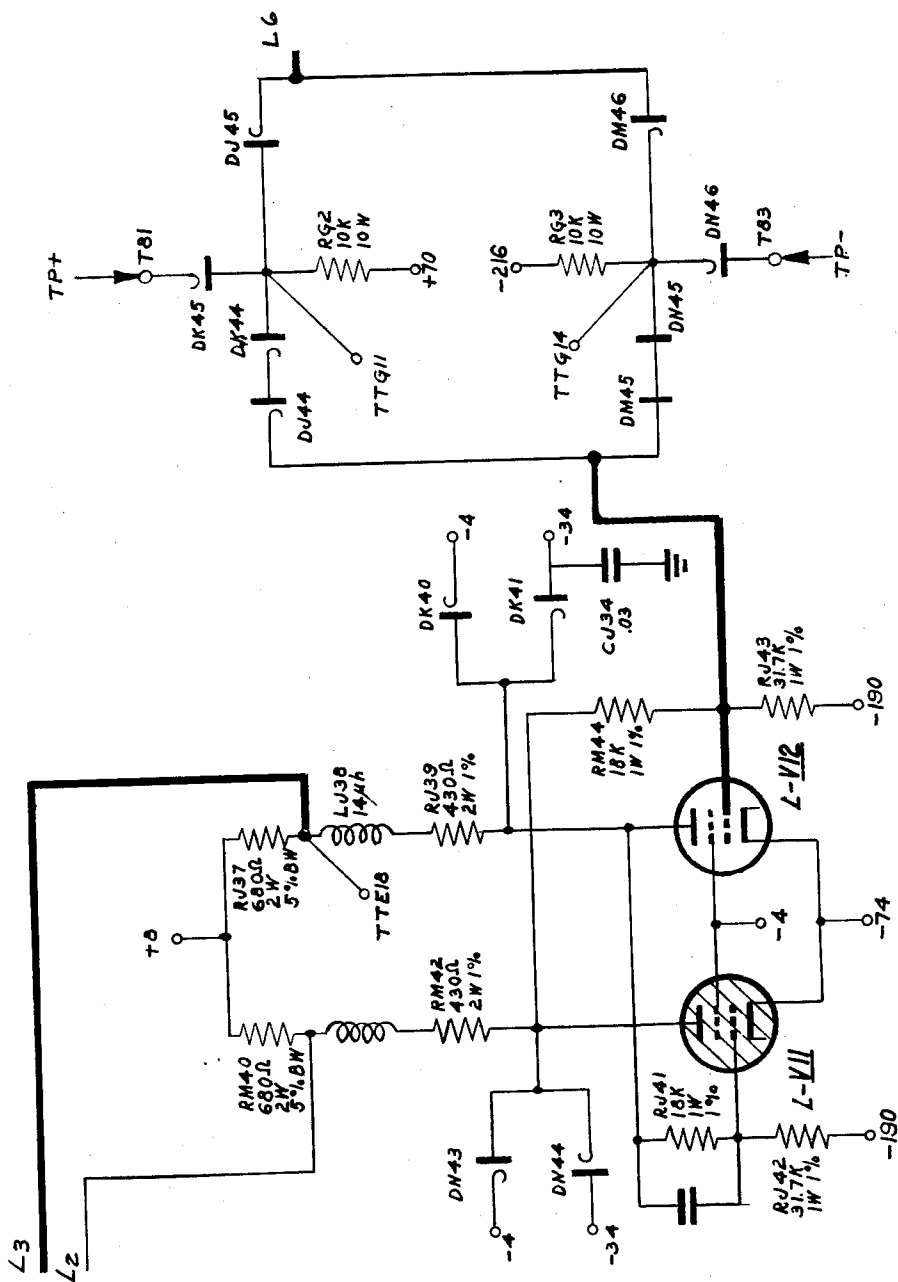
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FIG. 17b



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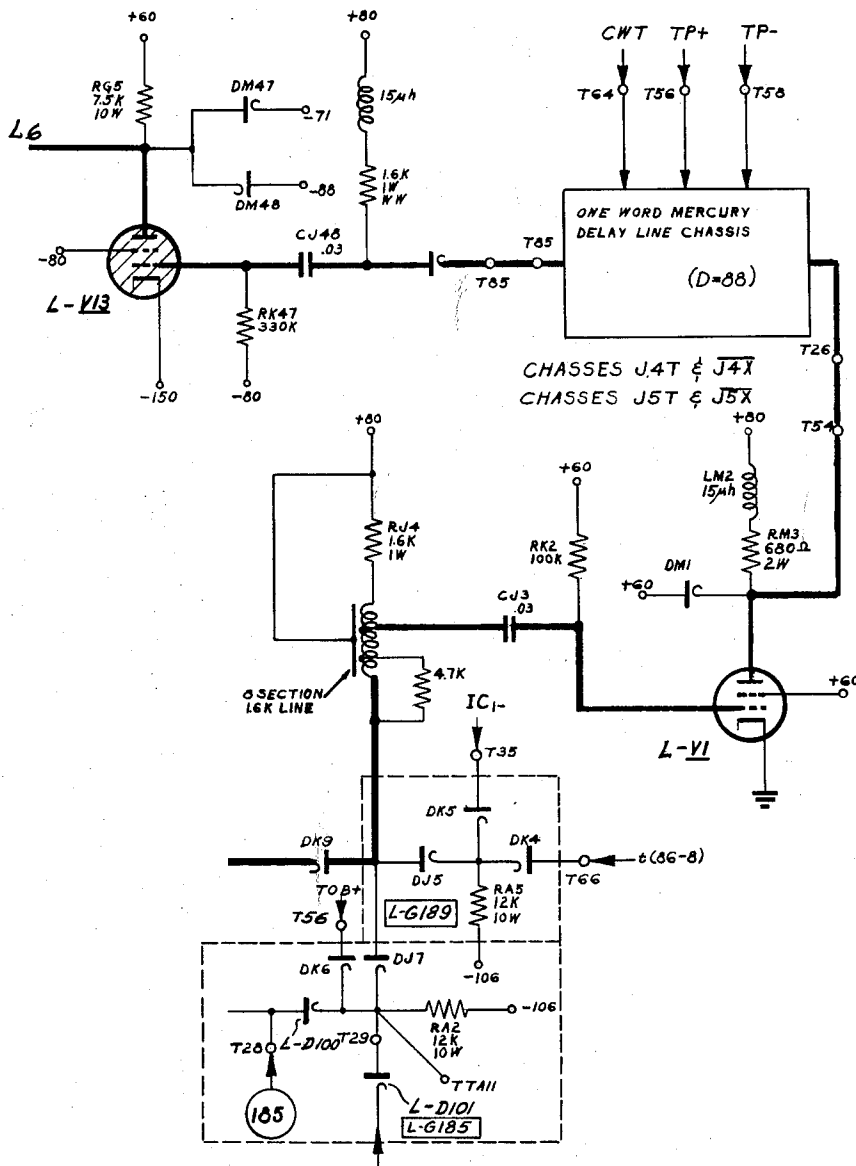
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FIG. 17c



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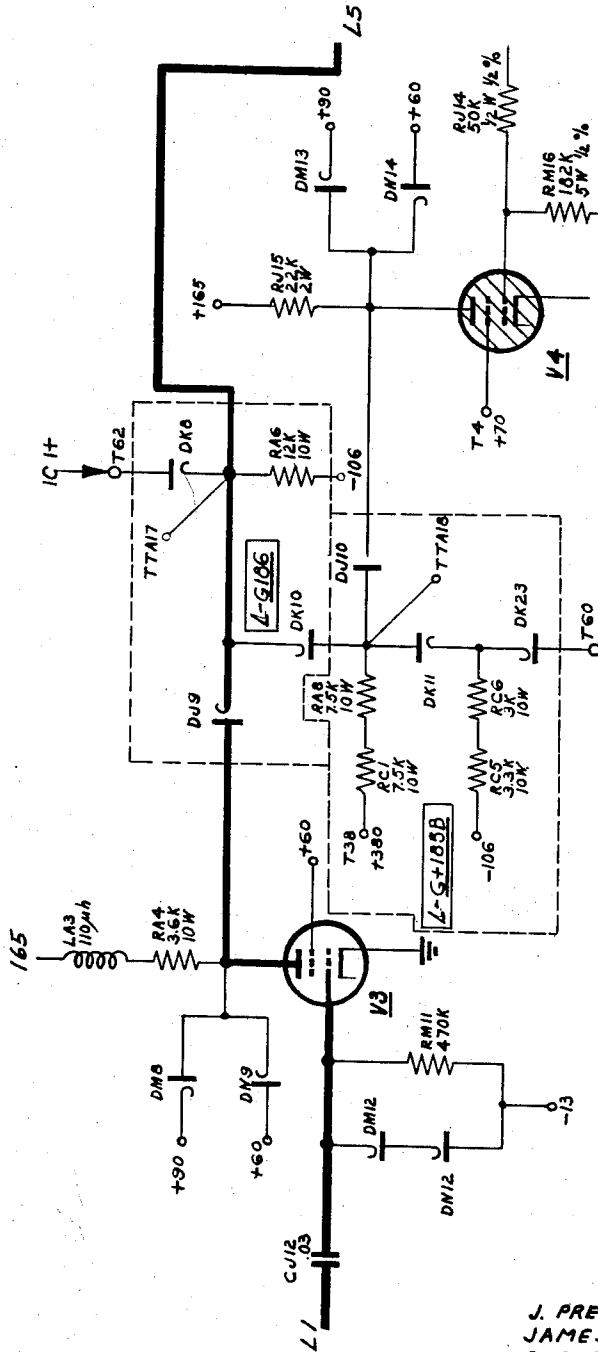


FIG. 17d

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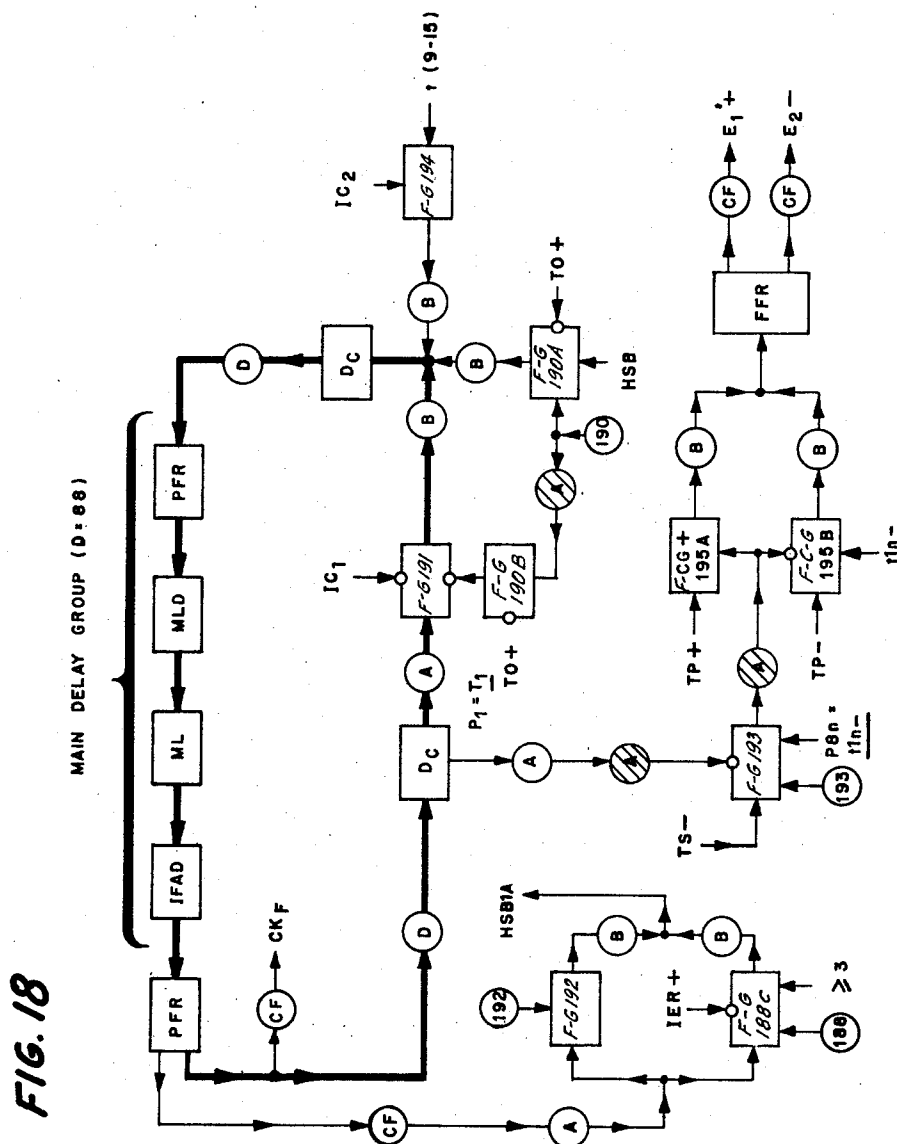
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FIG. 17e

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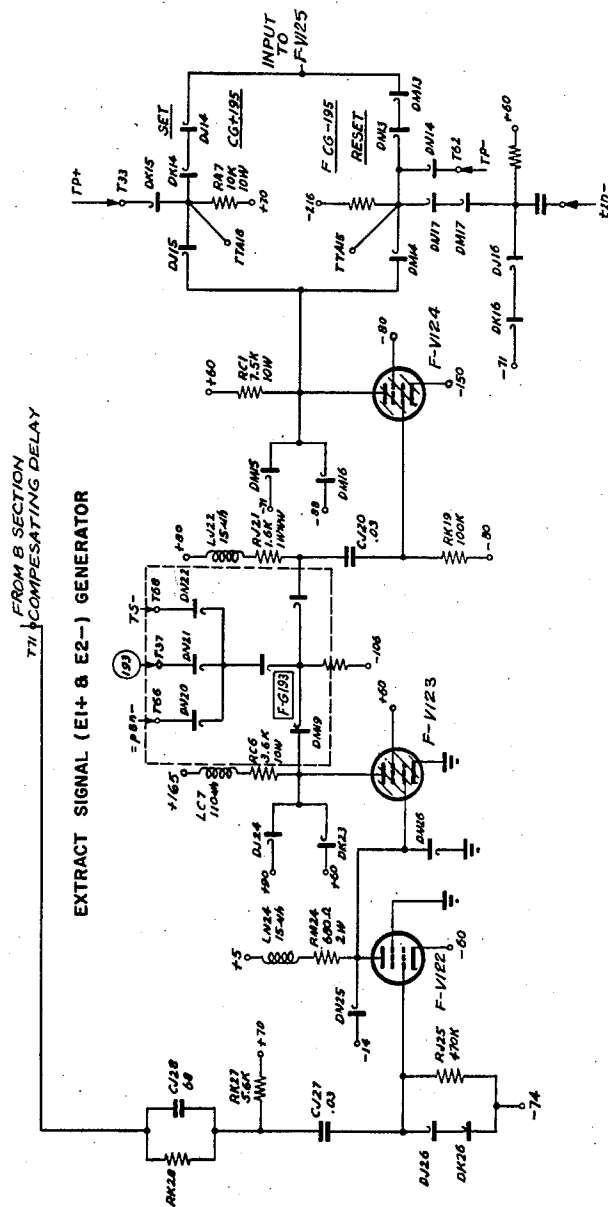
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FIG. 19b



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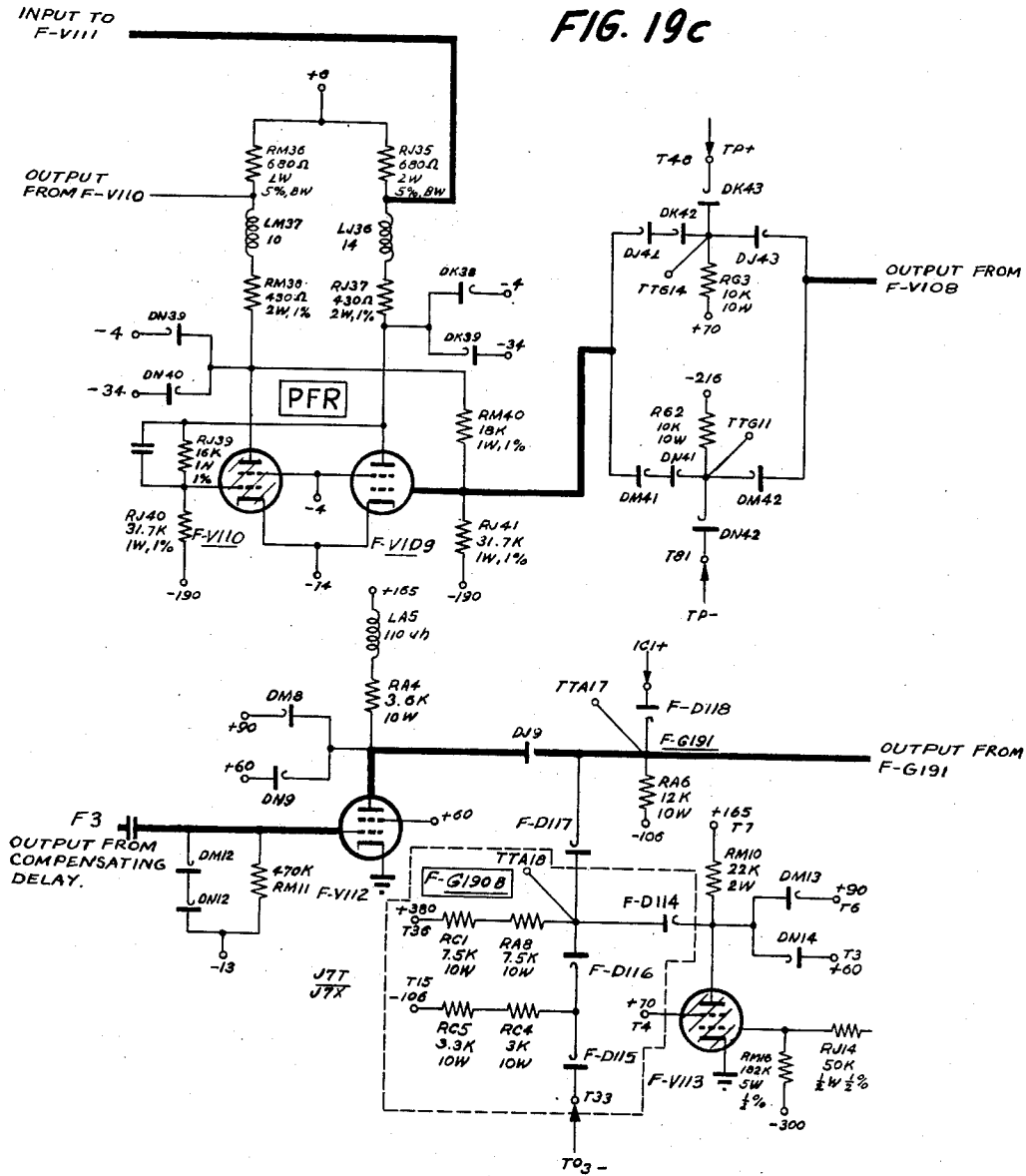
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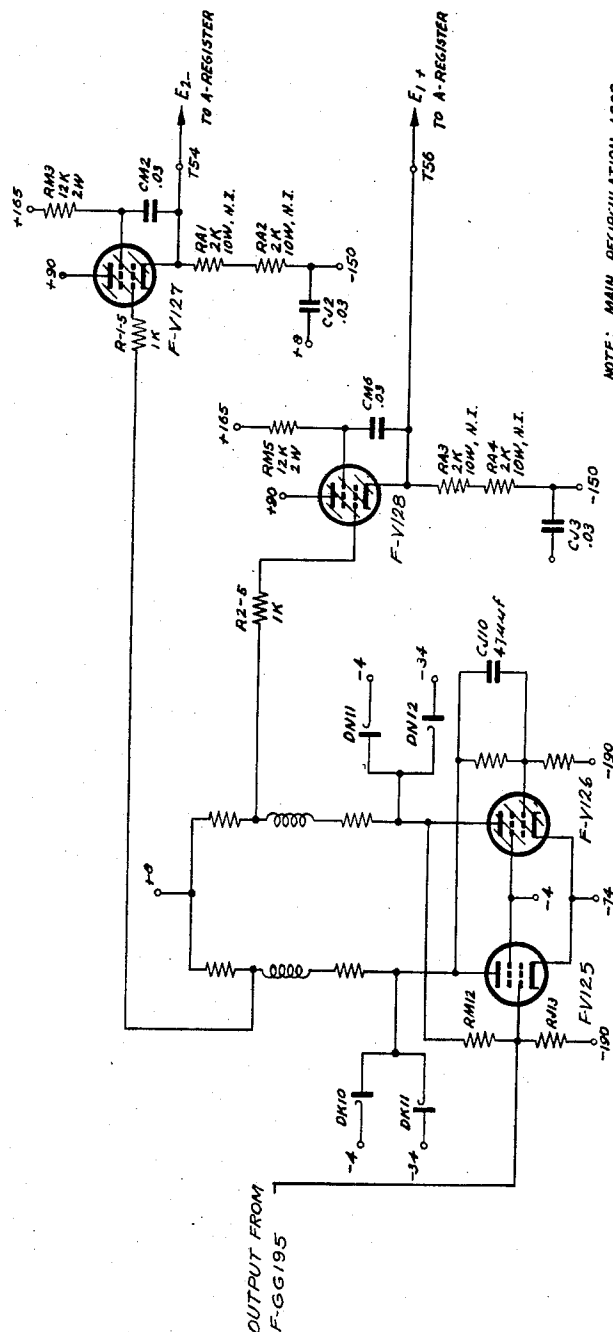
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FIG. 19d



NOTE: MAIN RECIRCULATION LOOP
INDICATED BY HEAVY LINE

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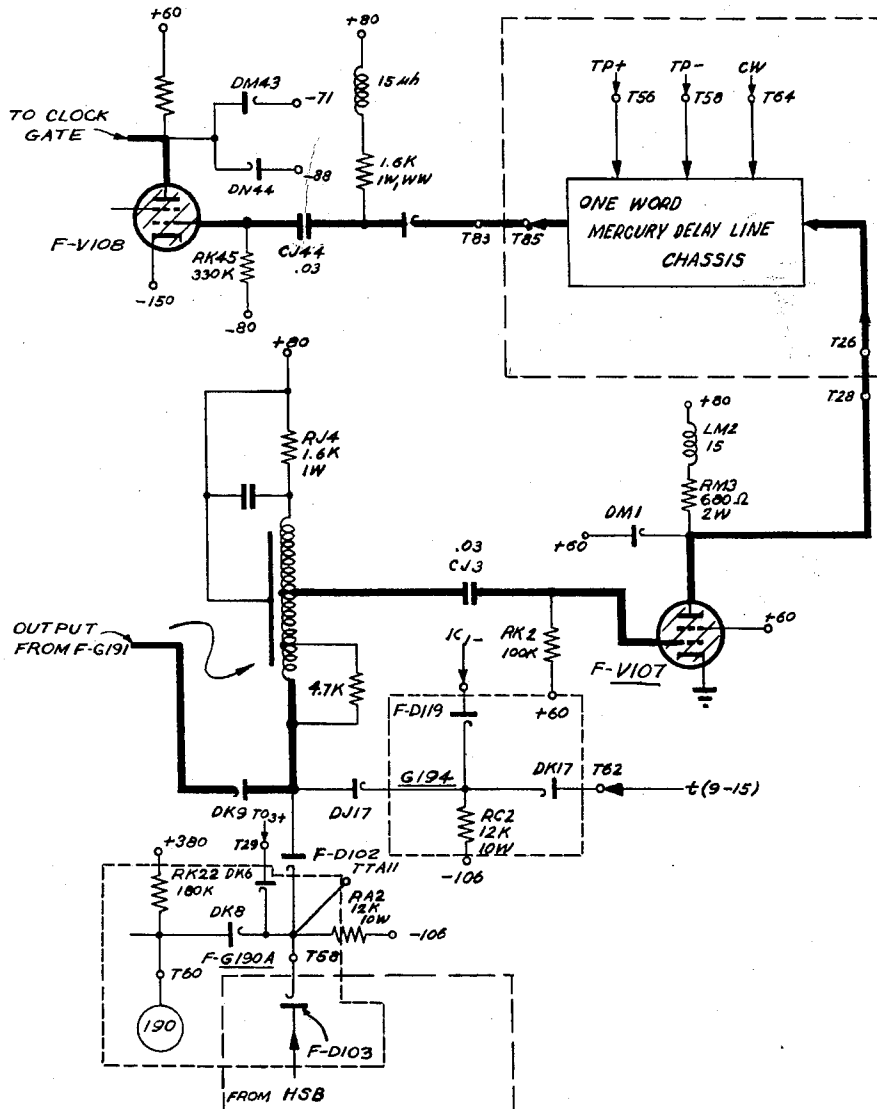
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FIG. 19e



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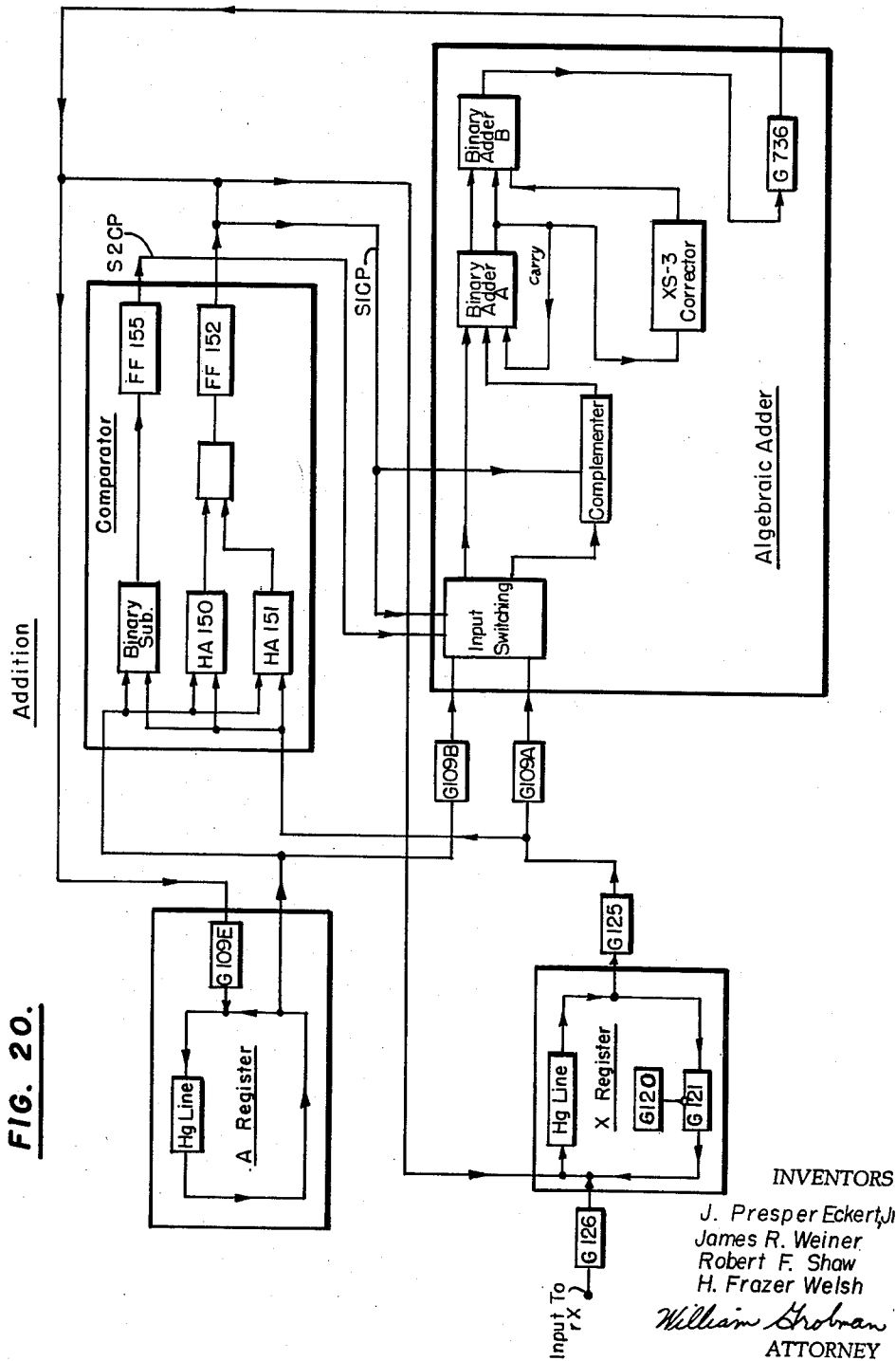
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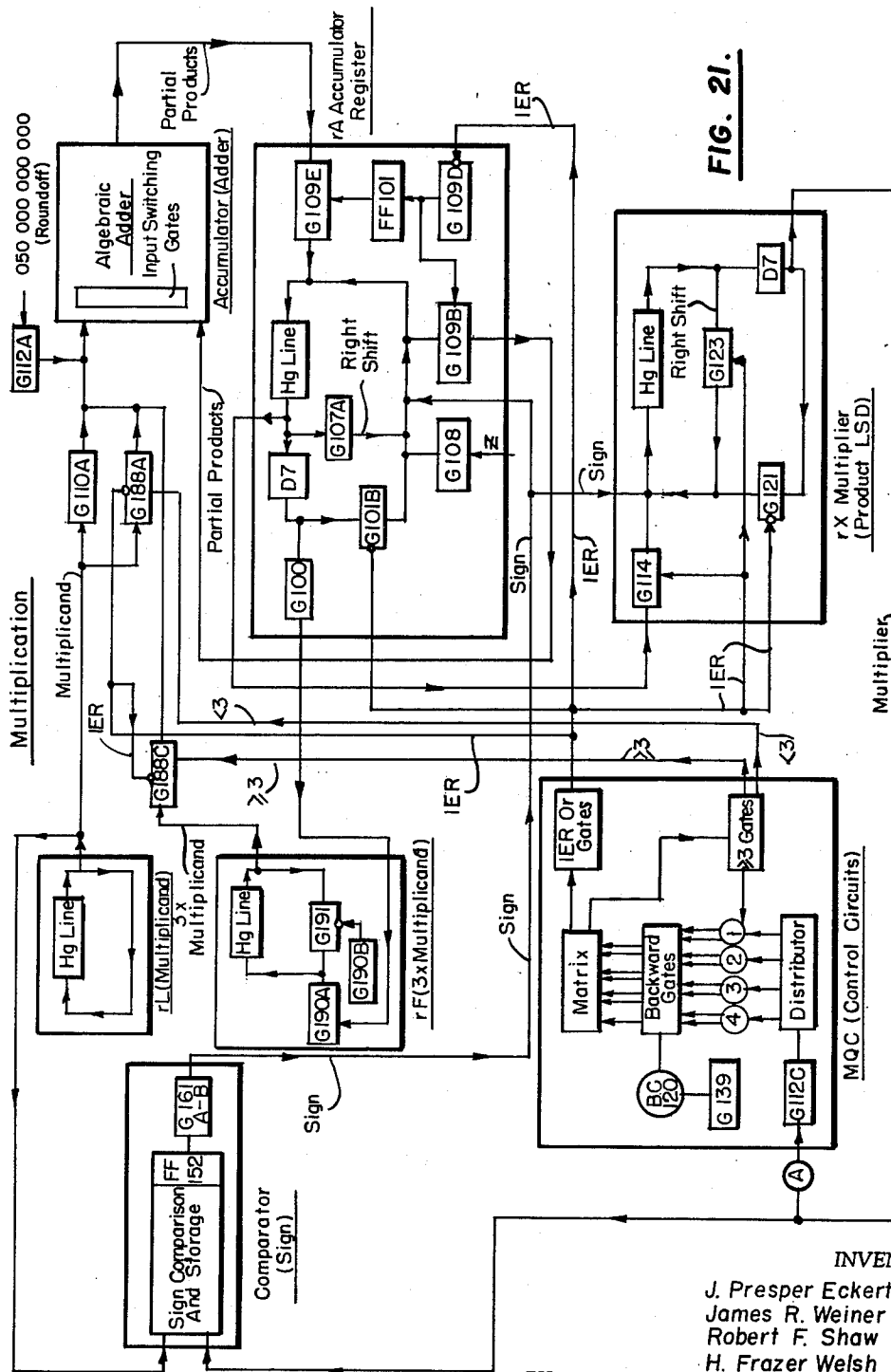


FIG. 21.

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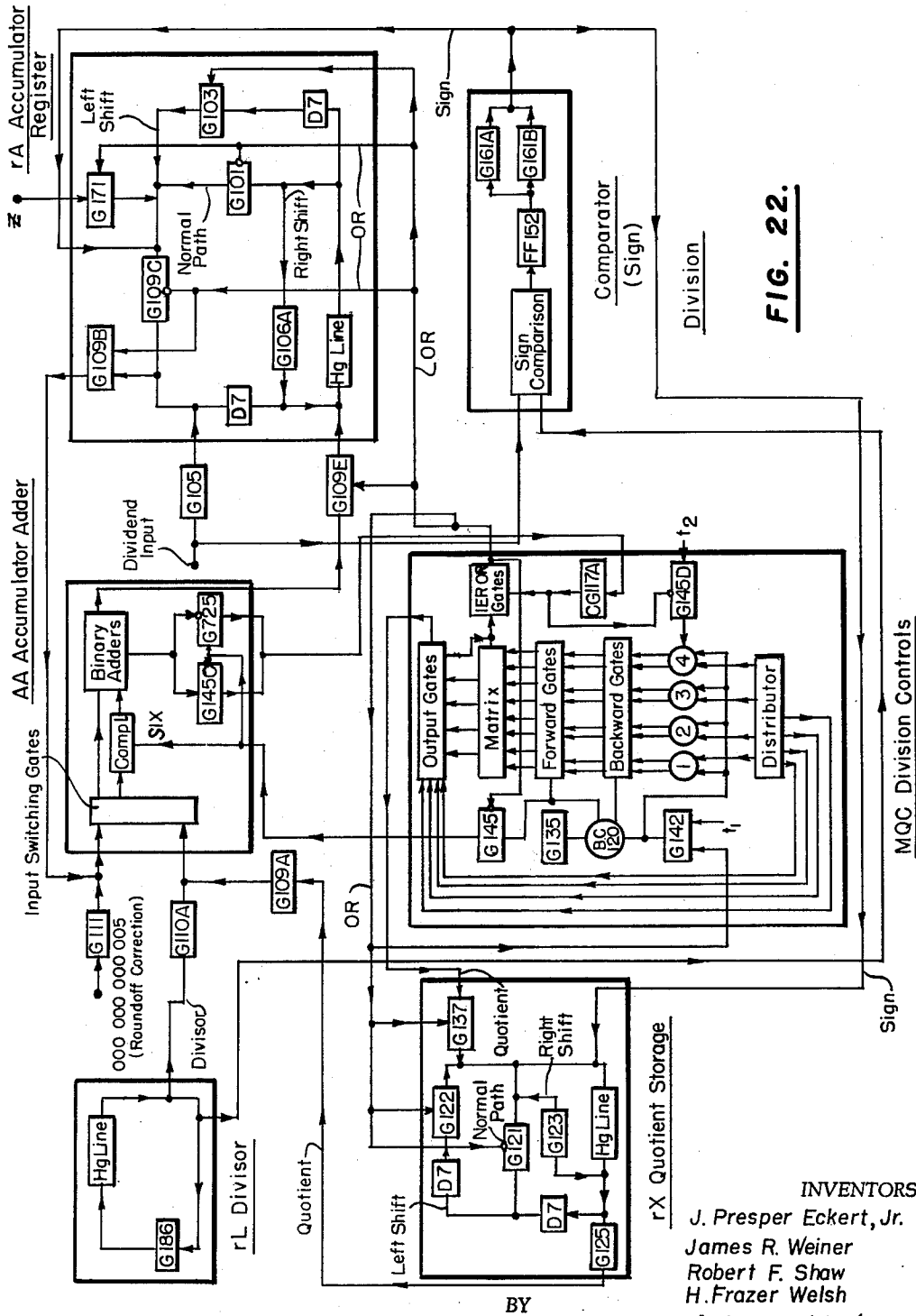


FIG. 22.

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3,133,190

UNIVERSAL AUTOMATIC COMPUTER UTILIZING BINARY CODED ALPHANUMERIC CHARACTERS

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Filed Mar. 31, 1952, Ser. No. 279,713
34 Claims. (Cl. 235-159)

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INTRODUCTION

The present invention relates to an electronic system for use with an automatic sequenced electronic digital computer of the general purpose type wherein the digits are expressed in binary form. More particularly, the present invention is directed toward arithmetic circuits adapted for use in such a computer.

There are many mathematical problems which may be more or less readily solved by mathematicians in general terms, but which can be solved in specific terms only at the cost of large outlays in time and labor because of the sheer volume of the iterative arithmetical processes involved.

Different types of computers have been devised to solve such problems in specific terms. Thus, there are general purpose computers which are adapted to solve a wide range of problems in specific terms and there are special purpose computers which are adapted to solve a narrow range of problems in specific terms. Furthermore, any computer may be either of the analog or of the digital type. An analog computer operates on physical quantities which can be measured: angular positions of shafts, voltage magnitudes, etc. A digital computer operates on numbers or digits which can be counted and hence which can only assume discrete values.

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A digital computer is capable of performing any or all of the following operations:

- Algebraically adding two quantities together and determining the sum;
- Algebraically subtracting one quantity from another and determining the difference;
- Algebraically multiplying one quantity by another and determining the product;
- Algebraically dividing one quantity by another and determining the quotient;
- Comparing one quantity with another to determine whether the compared quantities are equal or unequal;
- Extracting selected digits of a first quantity in accordance with the requirements of a second quantity and placing these extracted digits of the first quantity into corresponding digital positions of a third quantity. (This operation is sometimes called logical multiplication.)

Hence before a computer is to solve a problem, a mathematician must first analyze the problem and determine, in terms of allowable computer operations, the steps by which the problem is to be solved. From these steps, the mathematician must prepare a program; i.e., a sequential list of operations for supplying information to the computer.

In general, all computer operations are performed automatically. However, the sequence of operations may be manually or automatically controlled. In other words, a computer may be manually sequenced or automatically sequenced. In a manually sequenced computer an operator must supply sufficient information to the computer to initiate each operation. In an automatically sequenced computer, after one operation has been completed, the computer automatically proceeds to perform the succeeding operation.

The operation of an automatically sequenced computer may be regarded as sequential, synchronous, or synchronous-sequential in nature. If sequential, an operation may be performed within a variable period of time but the succeeding operation begins immediately after the preceding operation is completed. If synchronous, an operation must be performed within a fixed period of time, and the succeeding operation begins after the expiration of this fixed period. If synchronous-sequential, an operation must either be performed within a fixed period of time or an integral multiple of this fixed period, and the succeeding operation begins either after the expiration of the fixed period or the integral multiple of this period.

If an automatically sequenced computer is digital in type, its operation may further be regarded as either serial or parallel in timing. If the operation is serial in timing, the digits of any quantity operated upon by the computer are operated upon in succession while if the operation is parallel in timing, all the digits of this quantity are operated upon simultaneously.

A more complete description of an electronic computer of the type under discussion will be found in copending application S.N. 279,710. The computer is adapted to operate on purely numeric quantities or on purely alphabetic characters or on mixed alphabetic characters and numeric quantities.

Such a computer must contain the following basic components: a storage device (generally called a memory) in

which the program is entered and from which the ultimate solution of any problem is taken, an arithmetic unit wherein the computer operations are performed, and control circuits which operate in the triple capacity of sequencing the computer operation such that the program is executed sequentially, interpreting the instructions to produce control signals and controlling the sub-steps of any multiple step operation.

Parenthetically, it will be noted that no mention has been made of apparatus for entering the program into the memory or for removing the eventual problem solution from the memory. Such apparatus, the input-output circuits, are described in the aforesaid copending application S.N. 279,710.

The memory may be considered analogous to a structure constituted by a plurality of individual cells numbered 0, 1, 2, etc. Information corresponding to the first step in the program is stored in cell 0, that corresponding to the second step in cell 1 and so on. The information stored in each cell remains there until the cell is cleared or emptied of the information.

The control circuit has built into it a counting device called a control counter. This counter has the location of memory cell 0 stored in it before computer operation begins. When the computer has completed the operation called for by the information stored in cell 0, the counter then stores the location of cell 1. In other words, the counter stores the memory location of the next computer step called for by the program, and the control circuit automatically acts on the information contained in this memory location.

The arithmetic unit is the subject of this invention.

Objects

It is an object of this invention to provide an arithmetic unit adapted to perform operations on alphabetic characters or on numeric quantities or on mixed alphabetic characters and numeric quantities.

Still another object of this invention is to provide an arithmetic unit which can discriminate between alphabetic characters and numeric quantities.

Yet another object of this invention is to provide an arithmetic unit which can sort and arrange alphabetic characters.

Still a further object of this invention is to provide an arithmetic unit which may initiate a shift of control by the control circuits after comparison of alphabetic characters or numeric quantities.

Yet a further object of this invention is to provide electronic comparison apparatus for comparing either alphabetic characters or numeric quantities.

Another object of this invention is to provide improved electronic apparatus for detecting computation errors.

Other objects and advantages of this invention will in part be disclosed and in part be obvious when the specification is read in conjunction with the accompanying drawings in which:

Short Description of Drawings

FIGURE 1a diagrammatically illustrates a typical instruction word;

FIG. 1b diagrammatically illustrates a typical data word;

FIGURE 1c diagrammatically illustrates a typical computer digit;

FIGURE 2 shows the keyboard coding of numbers, alphabetical characters and other non-numeric symbols;

FIGURE 3 is a block diagram showing the present invention as a component of an information handling system;

FIGURE 4a is a block diagram of a typical flip-flop;

FIGURE 4b is a block diagram of a typical gate;

FIGURE 4c is a block diagram of a typical buffer circuit;

FIGURE 4d is a block diagram of a typical comparator;

FIGURE 4e is a block diagram of a typical half-adder;

FIGURE 5 is a block diagram of a typical full-adder;

FIGURES 6a-6d comprise a block diagram of the comparator according to this invention;

FIGURES 7a-7k comprise a schematic diagram of the comparator according to this invention;

FIGURES 8a-8d comprise a block diagram of the multiplier-quotient counter;

FIGURES 9a-9n comprise a schematic diagram of the multiplier-quotient counter of this invention;

FIGURES 10a-10d comprise a block diagram of the algebraic adder of this invention;

FIGURES 11a-11f comprise a schematic diagram of the algebraic adder;

FIGURES 12a-12d comprise a block diagram of an A register;

FIGURES 13a-13s comprise a schematic diagram of the A register;

FIGURE 14 is a block diagram of an X register;

FIGURES 15a-15g comprise a schematic diagram of the X register;

FIGURE 16 is a block diagram of an L register;

FIGURES 17a-17e comprise a schematic diagram of the L register;

FIGURE 18 is a block diagram of an F register; and

FIGURES 19a-19e comprise a schematic diagram of the F register.

Code Structure

Both from the standpoint of simplicity and reliability in the various computer components and from the standpoint of ease in computer operation, it has been determined that the computer functions most successfully when the digits are expressed in binary form. More specifically, each digit takes the form of a pulse train wherein pulses are present and absent in a coded arrangement which identifies each particular digit. The binary one denotes the presence of a pulse; the binary zero denotes the absence of a pulse. Both binary ones and binary zeros are generated in identical time intervals.

Since the computer can operate on alphabetic characters as well as numeric quantities, it is necessary to devise a binary coding system so that the computer may distinguish therebetween. (The term "alphabetic character" refers not only to letters of the alphabet but, also, to non-numeric symbols, such as punctuation marks.)

Any decimal digit (including decimal zero) may be expressed in terms of four binary digits. Any letter of the alphabet or any punctuation mark may be expressed in terms of six digits. Therefore, all such quantities are expressed by a six binary digit pulse train. The fifth and sixth digits of this train (called zone indicators) are always binary zeros when the quantity represents a decimal digit; at least one of these zone indicators is always a binary one when the quantity represents an alphabetic character.

A seventh binary digit, the checking digit, is always added to each sixth digit train. If the total number of binary ones in the first six binary digits is odd, the seventh binary digit is a binary zero. If the total number of binary ones in the first six digits is even, the seventh binary digit is a binary one. Hence, this seventh digit ensures that the total number of binary ones is the seven digit train is always odd. Frequent checks are made throughout the various computer circuits to ensure that this condition holds for each seven digit train. Such a seven digit train is called a computer character. FIGURE 1c illustrates a typical computer character.

Thirteen computer characters constitute a computer word; i.e., a pulse train of ninety-one binary digits. The second through thirteenth characters represent alphabetic characters or numeric quantities, and the first character, called the space-between-words, always consists of all binary zeros. FIGURE 1b illustrates a typical word. This space-between-words is required to maintain a time space between the last quantity of one word and the first

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quantity of the succeeding word in order to ensure proper timing for switching operations.

When a word represents a numeric quantity, the second through twelfth computer digits represent decimal characters arranged in increasing order of significance with respect to the first computer character (which is the space-between-words). The thirteenth computer character represents the algebraic sign of the quantity. The computer, being serial in timing, operates on one computer character at a time and operates in the sequence set forth above, the least significant decimal digit being operated upon first, and appearing first in time at any point in the computer.

When a word represents alphabetic characters, the second through thirteenth computer characters represent alphabetical letters or other nonnumerical quantities, and the first computer character represents the space between words. The order in which the computer operates on these characters, however, does not differ from the numerical case; i.e., the first computer digit, not the thirteenth computer character, is operated on first.

A word may contain both alphabetic characters and numeric quantities but, again, the order of computer operation does not change. Words and computer characters may be stored either statically or dynamically in the computer depending on the particular use to which the digit or word is being put. If a word is statically stored, the entire contents of the word (the binary digit train) may be available at a selected instant of time or may be made available serially, whereas a dynamically stored word becomes available only as its serially arranged binary digits reach the point of readout. If a word is dynamically stored, only a single binary digit of the word may be made available at this selected instant in time.

In the computer, a statically stored word is represented by steady state direct current signals while a dynamically stored word is represented by transients.

Components of System

A counter device can store a word statically as the reading of the device represents the entire word. An electrical or acoustical delay line placed in the form of a closed loop, provided that the pulses are continuously regenerated, can store a word dynamically because the binary digits of the word pass any selected point in the loop in sequence. The time interval required for an entire word to pass the selected point is called a minor cycle.

In dynamic storage, the digital order within the word is such that the least significant digit precedes the next more significant digit and so on. It is important to understand at this point that if the information contained within a dynamically stored word is to be properly transferred, the transfer must be so timed that the least significant digit is transferred first. Furthermore, if a word is dynamically stored as, for example, circulating within a closed loop, it is possible momentarily to connect a conductor to this closed loop and transfer the word, a digit at a time, to some other point in the computer while the word continues to circulate within the loop and, hence, continues to be stored. It is equally possible, of course, to open the loop at a point beyond the connection point of the conductor to the loop in the direction in which the word travels, thus deleting the word after it has been transferred. In the latter case, the loop is said to be cleared.

The memory is a dynamic storage device; the intermediate storage registers contained in the arithmetic circuit are either dynamic or static storage devices. The majority of these intermediate registers utilize dynamic storage.

Since the computer operation is synchronous sequential in nature, it is necessary to accurately time all computer operations, including those in which words are stored and removed from storage. These operations are timed by means of timing signals produced within the control cir-

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cuit. The timing signals also serve to actuate devices which will restore the original wave form to words or computer digits whose original pulse pattern has become distorted due to pulse degeneration. The actual apparatus for producing these signals is constituted by a timing pulse generator which produces pulses at the frequency at which binary digits are generated and a cycling unit which subdivides this frequency to produce pulses at frequencies corresponding to the rate at which words are generated and to the rate at which computer characters are generated. This apparatus is described in detail in co-pending patent application S.N. 279,710.

Arithmetic Operations

In order to describe the arithmetic circuits completely, it will first be necessary to explain how these circuits function when the computer solves a purely numeric problem and when it solves a purely alphabetic problem.

In solving a numeric problem, the computer operations may be any or all of the following: addition, subtraction, multiplication, division and comparison extraction. These operations will be described below.

In the addition operation, that section of the arithmetic circuits called an accumulator is used. The accumulator is constituted by a dynamic storage register called the A register and a device called an algebraic adder. The output of the adder is connected to the input of the A register and the output of the A register is connected to one of three inputs to the adder. Consequently, the adder is effectively inserted in the dynamic storage loop of the A register to form a composite storage loop. If a quantity has been stored in the A register, this quantity circulates in the closed path formed by the A register and the adder. The adder is so named because in the condition that a first quantity is circulating through the composite loop, if a second quantity is supplied to the second input of the adder in such timing that the two quantities arrive at corresponding inputs at the same time, the resultant quantity leaving the output of the adder (and thus circulating in the composite loop) has been so modified as to represent the sum of the first two quantities. After this quantity has circulated once through the loop, the connections between the adder and the A register are broken, and the resultant quantity circulates in the A register only until the next operation.

In the event that successive addition operations are required, the sum of the two quantities being added in any addition step before the final addition step may be a twelve digit number; hence a carry digit will be produced. This carry digit must be added in the next addition step. For this purpose, the adder is provided with a third input, the carry digit input.

Consequently, the addition process consists of first storing the augend in the accumulator, then supplying the addend to the adder with the timing described above, thus producing the sum which then circulates in the accumulator. The accumulator has a storage capacity of one word. In the addition process, therefore, the augend, the addend and the sum may only represent eleven digit algebraic numbers; the twelfth computer digit representing the space-between-words and the thirteenth computer digit representing the algebraic sign. The technique of sign manipulation in connection with the algebraic operations of the computer will be described when the comparison operation is discussed.

The addend may either be supplied from the memory or from a second dynamic storage register, the X register, depending which instruction is called for.

In the subtraction operation, the accumulator section of the arithmetic circuits is used in conjunction with a complementor. Since the adder is only capable of addition, the computer does not subtract the subtrahend from the minuend but rather adds the tens complement of the subtrahend to the minuend and ignores the most significant digit in the resultant sum, it is first necessary

to complement the subtrahend before supplying it to the adder (the minuend has been inserted in the accumulator by some previous operation).

The complementer is a device whose output yields the nines complement of whatever quantity is supplied to its input. Thus, the subtrahend is supplied from the memory through the complementer to the second input of the adder with such timing that the complemented subtrahend and the minuend arrive at corresponding inputs of the adder at the same time. Since the complemented subtrahend is the nines complement, it is necessary to convert the nines complement to the tens complement. This is accomplished by supplying the digit 1 to the third input of the adder with such timing that it is added to the least significant digit of the nines complement, thus effectively adding the tens complement of the subtrahend to the minuend. Neither the circuit for generating this digit 1 nor the means by which the most significant digit in the sum is ignored will be discussed at this point.

Since the computer is designed to produce only uncomplemented quantities as a result of any computer operation, the subtrahend must be a smaller quantity than the minuend. If the subtrahend is larger than the minuend, the result will be the complement of the difference.) Thus the minuend, must always be the larger quantity and must always enter the first input of the adder. This problem is discussed at greater length in the detailed description of the computer operation.

Any multiplication operation may be performed through repeated steps of addition as multiplication is a shortcut method for repetitive addition operations. The computer multiplication operation is performed by additions and shifts. Thus, in the first step, the multiplicand is added to itself repeatedly; the number of repetitions being equal to the last significant decimal digit in the multiplier. The decimal digits in the resultant sum (this sum is called a partial product) are then shifted one decimal digit to the right and in the second step, the multiplicand is repeatedly added to this partial product, the number of repetitions being equal to the next least significant multiplier digit. The new partial product is again shifted and the process is repeated until the number of additions indicated by every digit in the multiplier has been accomplished in this manner and the final product has been obtained. The final product may be rounded off, if desired, by adding the digit five to the least significant decimal digit in this product.

In order to reduce the number of additions required in the multiplication process, each multiplier digit immediately before being used to initiate a step of addition is tested to determine whether it is less than, or equal to or greater than three.

If the original digit is less than three, the multiplicand is added repeatedly to the appropriate partial product, each addition initiating a process whereby the original multiplier digit is reduced by one until the original digit equals zero. Each time the multiplier digit is reduced, the multiplier digit is tested again. When the multiplier digit is reduced to zero, the appropriate partial product is shifted one decimal digit to the right and the entire process is repeated for the next least significant multiplier digit.

If the original multiplier digit is equal to or greater than three, a quantity equal to three times the multiplicand is added to the appropriate partial product and the original multiplier digit is reduced by three and tested again. This process continues until the original digit is reduced to zero and the shifting occurs as before.

In multiplication, the computer makes use of the accumulator, the X register, two additional dynamic storage registers (the L and F registers), and a device called the multiplier quotient-counter. This counter stores each multiplier digit successively in static form, tests this digit to determine if it is less than, or greater than or equal to three, and initiates the shifting operation.

The multiplicand is stored in the L register; the multiplier is stored in the X register. After the algebraic sign of the product has been determined (as will be explained later), the multiplicand is transferred three times from the L register to the accumulator and the resultant quantity (three times the multiplicand) is transferred from the accumulator to the F register. The accumulator is then cleared.

At this point, the least significant multiplier digit is transferred from the X register to the multiplier quotient-counter which produces one of three signals.

If the multiplier digit is equal to or greater than three, the ≥ 3 signal is produced; if the digit is equal to one or two, the < 3 signal is generated; and if the digit is a decimal zero, the shift signal is produced. The ≥ 3 signal causes the contents of the F register to be added to the contents of the accumulator and also admits three pulses to step the multiplier-quotient counter three times, thus reducing by three the number in the counter. The < 3 signal causes the contents of the L register (less the algebraic sign) to be added to the contents of the accumulator and admits one pulse to step the counter once, thus reducing by one the digit in the counter. When the original digit is reduced to decimal zero, or when the original digit is a decimal zero, the shift signal is produced, causing the contents of the accumulator and the X register to be shifted one digit to the right.

The right shift in the accumulator is, of course, logically required for the multiplication operation as described above. The right shift in the X register is required, because each multiplication step (due to the synchronous-sequential operation of the computer) must be performed in an equal time interval. Consequently, if each decimal digit transfer from the X register to the multiplier-quotient counter is to take place at the same point in the X register (as is the case here), a right shift is required to maintain this time interval.

The shifting operation, as will be explained in more detail later, effectively removes a delay equal to one computer character time, in the appropriate register during one complete circulation for a right shift. The least significant digit in the partial product stored in the accumulator must then either be deleted or transferred to the X register, where it can occupy the space made vacant by the transfer to the multiplier-quotient counter of the least significant multiplier digit when twenty-two-place multiplication has been called for.

Since the multiplier and the multiplicand are both eleven-digit quantities, the product may have a maximum of twenty-two digits. If all of the digits of the product are required for a subsequent operation each time a shifting operation takes place, the least significant decimal digit in the partial product is not deleted but is transferred into the X register so that after the multiplication operation has been completed, the accumulator stores the eleven most significant digits and the X register stores the remaining least significant digits. In the event that only an eleven-digit product is desired, the least significant digit in the partial product is always deleted during the first circulation in the accumulator following a shift operation. In eleven-digit multiplication, a number five is added to the least significant digit of the product after the multiplication has been completed to round off the product. The mechanism for rounding off will be described later.

Both in multiplication and division the computer considers the decimal point to be placed immediately to the right of the algebraic sign position within the word. Thus, all quantities, x , are treated as falling within the range 2^{-1} to 2^{-30} .

Consequently, in computer division, the dividend must always be less than the divisor.

The computer performs division by a series of subtractions and additions, the so-called "non-restoring" method. In this method, the dividend is first shifted one decimal

digit to the left and the divisor is repeatedly subtracted from the shifted dividend until the remainder goes through zero. (In essence, this means that the remainder changes from a positive to a negative quantity, although the algebraic sign is not used in this process.) The number of subtraction steps, not counting the step in which the remainder goes through zero, becomes the most significant digit in the quotient.

The remainder resulting from this uncounted step is shifted one decimal digit to the left and the divisor is repeatedly added to the shifted remainder until the remainder again goes through zero. The nines complement of the quantity representing the number of addition steps, not counting the step in which the remainder goes through zero, then becomes the second most significant digit in the quotient. This sequence of repeated subtractions and additions is continued until twelve quotient digits have been determined. At the end, a round-off correction is added and the quotient is shifted right to become the rounded eleven-digit quotient.

The computer performs subtraction by complementing the subtrahend and adding. Hence, each subtraction step in division is performed by addition of complements. For purposes of each subtraction step, the divisor is regarded as if it were a twelve-digit number with a zero as the most significant digit and the remaining eleven-digit divisor. The complemented divisor used in each subtraction step is the tens complement of this twelve-digit number. During the subtraction sequence of division, the step in which the remainder passes through zero is indicated by the absence of a carry digit produced by addition of the most significant digits in the remainder and the complemented divisor. In addition sequence in division, the step in which the remainder passes through zero is indicated by the presence of such a carry digit.

The division operation requires the use of the accumulator, the multiplier-quotient counter, and the X and L registers. The divisor is stored in the L register; the dividend is stored in the accumulator. The dividend is then shifted a digit to the left. The complement of the divisor is transferred from the L register into the accumulator as many times as is required for the subtraction sequence described above. The multiplier-quotient counter counts each transfer except the transfer in which the remainder passes through zero. The number thus generated in the counter is transferred to the X register as the most significant decimal digit in the quotient. Then the remainder in the accumulator is shifted one decimal digit to the left and the divisor is transferred from the L register into the accumulator as many times as is required for the addition sequence described above. The nines complement of the number digit generated in the counter (by counting each addition step except the step in which the remainder again passes through zero) is then transferred to the X register as the second most significant decimal digit in the quotient and the process continues as outlined in the preceding paragraphs.

Before an addition or subtraction operation can be performed, the signs of the operands must be compared. Furthermore, since the subtraction operation is performed by complementing the smaller quantity (the subtrahend) and adding the complement to the other operand (the minuend), a magnitude comparison of these two quantities must be made. The comparator is a device which compares both the signs and the magnitude of these quantities.

The adder has a switching arrangement in its input system such that a first signal generated by the comparator can interchange the minuend and subtrahend inputs to the adder if the results of the comparison operation so indicate. The adder passes the quantity supplied to the minuend input with sign unchanged and suppresses the sign of the subtrahend. Thus the difference quantity produced by the subtraction operation has the correct sign. This switching operation also occurs during addi-

tion but since the signs of the two quantities to be added are the same, their sum must have the correct sign.

The complementor, as we have seen, is associated with the subtrahend input of the adder and does not operate unless a second signal for the comparator is present. The comparator only generates this second signal when the signs of the two quantities to be compared are different and hence a subtraction is called for.

Hence, for either the addition or subtraction operation, the two quantities must be supplied to the comparator before being supplied to the adder.

In the multiplication and division operations, the comparator must only compare the signs of the operands; if the signs are the same, the product or quotient must have a plus sign, while if the signs are different, the quotient or product must have a minus sign. The comparator, having determined the sign of the quotient or product, stores this sign statically while the division or multiplication operation is carried out with the absolute values of the operands. After the appropriate operation is carried out, this sign is transferred into the appropriate register to become attached to the quotient or product.

In the extraction operation, the computer extracts characters from a word in the A-register and replaces them with the corresponding characters from the word in a specified memory location. The selection of the characters to be replaced is accomplished by means of an "extractor word" in the F-register. The characters in the extractor word which correspond to the characters to be replaced contain a binary zero in their least significant pulse space. The presence of the zero is detected in the F-register which then develops the extract signals which control the extraction operation.

As an example, assume that the word in the A-register is a numerical quantity +34576953210. It is desired to extract the eighth through eleventh characters from this word so that the word produced by the extraction process will be +04576000000.

Therefore, the quantity +00000000000 is stored in the specified memory location. The extractor word is stored in the F-register and is so coded (as described above) that the instruction implicit in the F-register is: delete the second through seventh characters and the twelfth digit in the A-register word and replace these deleted digits by the second through seventh characters and the twelfth character in the word stored in the specified memory location.

In solving an alphabetic problem, the computer operations may be either comparison or extraction or both comparison and extraction. The extraction operation is basically the same whether extraction is performed on numeric quantities or alphabetic characters, and will not be described again.

The comparison operation is performed by the comparator which compares two quantities either alphabetic or numeric and determines equality or comparative magnitude. Since, as will be apparent from FIGURE 2 (which illustrates the algebraic and numeric coding system used herein), the alphabetic code combinations are arranged in numeric order, the comparator effectively subtracts corresponding characters in the two words and learns from the resulting difference the alphabetic precedence of the two words. Thus, the comparator is effectively an alphabetizer as well as a numerical comparator.

The basic alphabetical problem is one of collation or sorting; i.e., one of arranging a series of random items into a sequence according to one or more key digits. This may be done by examining the first two items, placing them in proper order to form a string of two in sequence, and then successively examining every other item to determine whether it should be placed in that string.

The simple example below indicates how a group of items may be processed to form a sequence in alphabetical order. Each item is represented by a word formed by twelve alphabetic characters, the first alphabetic charac-

ter representing the key digit. All succeeding alphabetic characters within the word are not material in the sorting operation. The arrangement of data before the beginning of the first sorting step is shown in the left hand column. Only the key digits are shown; actually, of course, the data is in the form of words.) Rows of dots mark off the groups of items which are to be formed into a string during any sorting step.

Original Data	Sorting Step 1	Sorting Step 2	Sorting Step 3
S.....	S.....	S.....	S.....
X.....	X.....	V.....	T.....
Y.....	V.....	X.....	U.....
V.....	Y.....	Y.....	V.....
T.....	T.....	T.....	W.....
Z.....	Z.....	U.....	X.....
W.....	U.....	W.....	Y.....
U.....	W.....	Z.....	Z.....

At the beginning of the first sorting step S is compared with X. No arrangement of the items is necessary since S as coded is smaller than X and already appears first. Then Y is compared with V. These items must be rearranged to form a string in ascending order. To collate the next pair, no inversion is needed. In the last pair, W and U are interchanged. At the end of the first step, there are four strings of two items each.

During the second sorting step, the first item of the first string is compared with the first item of the second string. As S is smaller than V, S becomes the first entry in the new string being formed. The next comparison is between X and V. This time, V is the smaller and therefore, V is transferred. The next item in the second two-item string is Y. When Y is compared with X, it is found that X should be transferred first, followed by Y. This completes the first string of four items. The second string of four is arranged by similar techniques. The items are compared in the order (T, U), (U, Z), and (W, Z).

In the third sorting step, the two strings formed during the second sorting step are collated into a single string of eight items. The order in which the pairs of key digits are drawn and compared is (S, T), (T, U), (U, V), (V, W), (W, X), (X, Y), and (Y, Z). Collation is then complete.

The preceding discussion has described the computer operations in rather general terms. Before proceeding to a more detailed description, it will be necessary to discuss the binary coding system used in this computer. Each decimal digit is not represented by its binary equivalent, but rather each decimal digit is represented, in binary form, by its original value plus three. This system is called an excess-three (XS-3) system. Its main advantage over the usual binary coding system is in the ease of complementing as well as seen below.

FIG. 2 illustrates the excess-three coding system. It will be seen for example, that a decimal two is represented by a binary 0101. (Because of the zone indicators and the check digit, this decimal is represented by 1 00 0101. Note that the order in which this computer decimal digit is operated on in the computer is such that the checking digit is in the seventh and last binary digit position.)

In the excess-three system the binary equivalent of the nines complement of any decimal digit is obtained by substituting zeros for ones and ones for zeros in the binary equivalent of this decimal digit. In other words, the nines complement expressed in binary terms of any binary number in the excess-three system is obtained by interchanging zeros and ones in this binary number.

When two decimal digits are added and do not produce a tens carry, the corresponding binary addition of their excess-three representations will exceed the correct sum in the excess-three system by another excess-three; i.e., sums

too great by an excess-three correction. Hence, if no carry occurs when two digits are added, an excess three must be subtracted (complement of excess three, 1101, added) in that column to produce the correct sum. In performing excess-three corrections, no carry is permitted from decimal column to decimal column.

When two decimal digits are added that produce a ten's carry, the corresponding binary addition of their excess-three representations will produce a sixteen's carry from the fourth binary digit position. Thus the excess-three correction is missing from the sum digit; i.e., sums deficient by an excess-three correction. Hence, if a carry occurs when two digits are added, an excess three must be added to that column to produce the correct sum in the excess-three system.

In the subtraction operation, excess-three differences are obtained by adding the complement of the quantity, smaller in absolute magnitude to the larger, and appending the sign of the larger.

FIGURE 3 is an overall block diagram of the system described in copending application S.N. 279,710. All of the elements shown are contained within the central computer casework except the Supervisory Control desk (SC) and the Uniservos, to which the lines in the upper right section of the diagram connect. The Supervisory Control, in addition to all the necessary control switches and indicator lights, contains an input keyboard. Also cabled to the Supervisory Control is a typewriter which is operable by the main computer. By means of these two units, limited amounts of information can be inserted or removed either at the will of the operator or by programmed instructions.

The input-output circuits operate on all data entering or leaving the computer. The input and output synchronizers properly time the incoming or outgoing data for either the Uniservos or the Supervisory Control devices. The input and output registers (rI and rO) are each 60 word (720 characters) temporary storage registers which are intermediate between the main computer and the input-output devices.

The high speed bus amplifier is a switching central through which all data must pass during transfer between any arithmetic register and the main memory or between the memory and the input-output registers.

The arithmetic registers are shown along the bottom of the diagram, each connected to the high speed bus system. The L-, F-, X- and A-registers are each one word capacity and are directly concerned with the arithmetic operations.

The Y- and V-registers are 2 and 10 word capacity, respectively. They are used solely for multiple word transfers within the main memory.

Associated with the arithmetic registers are the algebraic adder (AA), comparator (CP), and multiplier-quotient counter (MQC).

The basic operating cycle of the system is founded upon single address instructions which specify the memory location of one word. In the case of the arithmetic instructions which require two operands, one of the operands must be moved into the proper position by some previous instruction. In order to control the sequence of instructions a special counter, called the control counter (CC) retains the memory location from which the succeeding instruction word is to be obtained. Each time a new instruction word is received from the memory, the quantity in the control counter is passed through the adder, where a unit is added to it. Therefore, the normal sequence is to refer to numerically successive memory locations for successive instruction words. Initially the control counter is cleared to zero and the first group of instructions must therefore be paced in memory locations from zero upward. A transfer of control instruction enables the programmer to change the control counter reading whenever desired and thus shift from one sequence to another. After a transfer of control takes

place, the new number in the control counter is increased by unity each time a new instruction word is obtained from the memory.

The transfer of control instructions are of three types, the unconditional transfer which changes the control counter reading without question, and two conditional instructions which require that either equality or a specific inequality exists between the words in the A-register and the L-register. In the former case, the quantities must be identical for transfer of control to occur and in the latter, the quantity in the A-register must be greater than the quantity in the L-register for the control counter reading to be changed.

Since the system can handle alphabetic as well as numerical data, these conditional transfer instructions are as useful to alphabetizing as they are to determine if a certain iterative arithmetic process has been performed often enough to come within specified numerical tolerances.

Since six characters (intermixed alphabetic and numerical) are sufficient to specify an instruction, and there are 12 characters per word, each instruction word can represent two independent instructions. (FIGURE 1a illustrates a typical instruction word). A one word register called the control register (CR) has been provided, which stores each instruction word as it comes from the memory. Thus one memory referral is sufficient for a pair of instructions and the control register stores both halves so that the second instruction is available as soon as the first has been completed.

Control Operations

The controls circuit include all those elements which work together to process the instruction routine. As each instruction word reaches the control register, the first half of it is passed immediately into the static register (SR). The static register drives the main function table and memory switch. The instruction digits are translated by the function table into the appropriate control signals for the instruction called for. The memory switch selects the location called for by the memory location digits and opens the proper memory channel to the high speed bus system at the proper time. Since the memory is constructed of 100 channels, each holding 10 words, the memory switch is a combination of spatial and temporal selection.

Implicit within each instruction, as translated by the function table is an ending signal which causes the computer to move on to the next instruction. The key to this sequence is the cycle counter (CY), which is advanced by the ending pulse. The cycle counter is a two stage, four position counter, which is connected into the function table. By virtue of this relation, it develops signals in addition to those developed by the instruction, which, for example, can cause the control register to transfer the second half of the instruction word into the static register when the first half has been completed. Similarly, after the second half instruction is finished, the cycle counter causes the reading of the control counter to pass into the memory location section of the static register and thus cause the next instruction word to be transferred from the memory to the control register. When the word reaches the control register, the cycle counter also causes the control counter reading to be increased by unity. The four cycles are designated by the first four Greek letters α (transfer CC to SR), β (transfer memory to CR) γ (perform first instruction) and δ (perform second instruction).

The multistage instructions such as multiplication, are guided through their various steps by the program counter (PC). The program counter has four stages or 16 positions. All multistage instructions can be performed within this number of steps.

The checking circuits are provided for the system of

two main types, odd-even checkers and duplicated equipment with comparison circuits. Odd-even checker depends upon the design of the pulse code used within the computer. This code provides seven pulse positions for every character. Six of the seven positions are significant as the actual code while the seventh is the odd-even check position. If the number of pulses or ones within the first six positions of any character is even, a one is placed in the seventh position to make the total odd. Thus, the total number of ones in the seven positions is always odd. By means of a binary counter and a few gates, an odd-even checker has been constructed which examines every group of seven pulse positions which passes through the HSBA. In this connection, mention must be made of the periodic memory check which interrupts operation every five seconds to pass the entire contents of the memory over the high speed bus system and, consequently, through the odd-even checker. Any discrepancy is immediately signaled to the supervisory control and further operation ceases. The duplicated equipment type of checking consists of duplicating the most essential parts of the arithmetic circuits and their controls and producing simultaneously independent results, which can then be compared for equality. For this type of checking, the A-, F-, X- and L-registers, algebraic adder, comparator, multiplier-quotient counter, and high speed bus amplifier are duplicated. The memory is not duplicated, but is checked by the periodic memory check mentioned above. Various sections of the control circuits are duplicated such as the program counter and cycle counter.

The timing pulse generator and cycling unit (CU) are the source of the basic timing signals throughout the computer and are described in copending application S.N. 279,156. The timing pulses occur at 2.25 megacycles per second. The cycling unit subdivides this rate into the character rate and computer word rate. The character rate is one seventh of the basic pulse rate since there are seven pulses for each character. There are twelve characters per word but space for a thirteenth character is included in a word time and is called the space between words. This time is used for switching purposes. The cycling unit, therefore, develops the word time signals at $\frac{1}{7} \times \frac{1}{13}$ or $\frac{1}{91}$ of the basic pulse rate. Within the cycling unit are numerous duplications and comparisons to ensure complete reliability.

Input-Output Operations

The operation of the input-output system is dovetailed as efficiently as possible with the operation of the arithmetic circuits. Whenever possible, parallel operations are allowed to proceed so as to minimize the time lost on internal operation while the slower input-output operations are taking place. The principal input-output instructions are handled in a manner identical to that for the internal operations as far as the function table. The Function Table (FT) develops signals which bring the input-output control circuits into operation. The information supplied to the input-output control circuit by the Function Table includes the following:

- (1) Which Uniservo, of the ten possible, is being called on.
- (2) Whether it is a read or write, i.e., an input or output operation.
- (3) If it is "read," the direction in which the tape is to move.

The input-output control circuits begin by testing whether or not the Uniservo indicated is now in use. If it is already in use, everything else waits until the Uniservo is free. Next, the input-output control circuits to determine whether the Uniservo selected previously moved backward or forward. If the previous direction does not agree with the new direction called for, the input-output control circuits generate the proper

signals to prepare the Uniservo to move in the opposite direction. If the instruction is to rewind a Uniservo, the input-output controls then direct the center drive of the selected Uniservo to rewind the tape to the beginning and stop.

As soon as the instruction has proceeded to the point where the input-output control circuits need no further information from the Function Table (FT), the instruction ending signal is generated and the internal circuits proceed to the next instruction, even while the reading, writing or rewinding continues.

The system according to the present invention can process an input, an output and several rewind operations while simultaneously carrying on internal computation.

The method by which the words are transferred from the I-register to the memory is combined with certain read instructions. There are two instructions which read from the tape to the I-register, one causing the tape to move forward, the other causing it to move backward. There are two other input instructions similar to those just mentioned, but they have the additional operation of first reading from the I-register to the memory and then reading a new group of 60 words from tape into the I-register. Thus the first type of input instruction reads from tape to the I-register only. It must be followed by the second type of instruction in order first to clear the I-register and then read in the second block of 60 words. The output instructions do not operate in this way but instead read directly from memory to the O-register and then to the tape as one instruction.

A third type of checking circuit occurs in the input-output circuits and counts the number of characters transferred from the tape in each block. Since there must always be 720 characters per block, the 720 checker signals any discrepancy to the supervisory control.

The other phase of the input-output operation concerns the two types of Supervisory Control input-output instructions. One type permits a single word to be typed in from the input keyboard and the other causes a single word to be typed out automatically.

The keyboard controlled tape recorder serving as the type hereinbefore mentioned is specifically described and claimed in co-pending application S.N. 279,712, now Patent No. 2,860,325.

The tape controlled printer already mentioned is specifically described and claimed in co-pending application S.N. 279,711, now Patent No. 2,860,756.

Each of the components contained in the arithmetic circuit make use of certain basic elementary circuit components. These components will be discussed below. The first elementary circuit component is called a flip-flop (abbreviated as FF) and is shown in block form in FIGURE 4a. The flip-flop is a device which has two stable states, one of which may be represented by "1" and the other by "0." These two states are indicated by set (S) and restore (R). Its use is sufficiently broad that the binary notation is not always appropriate. For example, it can, in a binary computer, store the sign digit, i.e., either a plus which is equivalent to one, or a minus which is equivalent to zero. The flip-flop is also useful for converting from a pulse to a static signal. For example, one pulse may indicate when a static signal is to start and another pulse when it is to stop. The flip-flop can be used for generating such a static signal. The duration of the signal is fixed by the interval between pulses. When a pulse is supplied to the set input, the flip-flop is said to be set; when a pulse is applied to the restore input, the flip-flop is said to be restored or cleared.

TYPICAL CIRCUITS

Flip-Flop

A flip-flop may be modified internally so that there is no restore input. In this case, each time a pulse is supplied to the set input, there is a change of state. In other words, one pulse will set this modified flip-flop to one

stable state, and the succeeding pulse will set this modified flip-flop to the other stable state. Such a modified flip-flop is called a binary counter and is abbreviated as BC.

A binary counter resembles a flip-flop in that it has two stable conditions. However, it differs from the flip-flop in its basic logical significance. The flip-flop is put into either state without specific knowledge of its previous state, while the binary counter cannot be so controlled by its main input.

Gate

The next elementary circuit component is called a gate (and is abbreviated as G). Gates are the chief form of switching used herein. The typical gate is shown in block form in FIGURE 4b. As the name implies, a gate permits or prohibits the passage of signals from one point to another. Referring to FIGURE 4b, it will be seen that the signal being gated (S) appears at the left. The various control signals are indicated as 1, 2 and 3. In order for signal S to pass through gate G, signals 1 and 2 must be present and signal 3 must be absent. Any other arrangement of signals is sufficient to prohibit signal S. Signal 3 is often called an inhibiting signal (note the small circle at the point of connection) while signals 1 and 2 are called permissor signals (without the circle connections).

Buffer

Another elementary circuit component is called a buffer (and is abbreviated as B). The buffer is indicated in block form in FIGURE 4c. The purpose of buffering is to combine several signal sources into a single line without interaction among the sources; thus signal 1 cannot pass into S2 but only through its buffer B into output O. Either signal S1 or signal S2 can pass into the output O.

Binary Comparator

The next elementary circuit component is called a binary magnitude comparator and is shown in block form in FIGURE 4d. This comparator is a simple combination of gates and flip-flops. Its purpose is to compare the magnitude of two unsigned binary combinations. First, it is important to realize how to compare two binary quantities. Suppose the two quantities are:

$$A = 0110110111$$

$B = 1110101001$ with the least significant digits shown on the right. Begin by comparing the least significant digits. They are both ones, therefore, the numbers so far are equal. Compare the second digits, A has a one, B has a zero; therefore, A is now larger. The third comparison repeats this conclusion. The fourth comparison reverses the conclusion in favor of B, etc., until the most significant digit is reached when the decision finally falls to B. B is assumed larger than A unless proven otherwise; therefore, the restoring pulse removes the $A > B$ before the comparison starts. As the first or least significant digit pulses of A and B reach their respective inputs, both gates G1 and G2 are closed by the opposite input. No pulse reaches the flip-flop. On the second pair of digits, the pulse on A inhibits G2 and passes through G1 to set FF. A now is greater than B. The third pair of digits follows the same procedure. When the fourth pair of digits arrive, the pulse in B inhibits G1 but passes through G2 to restore the flip-flop, etc. When the most significant digits are compared the flip-flop is left in restored condition and the fact is determined that A is not greater than B.

Suppose the quantities A and B had been equal; no pulses would have reached the flip-flop and it would have remained restored. Therefore, the comparator only indicates two conclusions, $A > B$ and $A \leq B$; but cannot distinguish between $A < B$ and $A = B$.

Half Adder

Still another elementary basic circuit component is called a half adder and is indicated in block form in FIG-

URE 4e (and is abbreviated as HA). The half adder combines the pulses of two words and produces either sum or carry pulses according to the laws of binary arithmetic. These rules are as follows: $0+0=0$, $0+1$ or $1+0=1$ (sum pulse), $1+1=0$ (sum pulse) and 1 (carry pulse). In FIGURE 4e, the two inputs are marked addend and augend. If no pulses enter either input, no pulses are emitted. If a pulse appears on either input, it reaches G1 and also passes through the delay D and a buffer to G2. (This delay is an electrical delay and its purpose will become apparent at a later point in this discussion.) Since G1 had only one input signal, it did not open and, therefore, did not inhibit G2. Therefore, a sum pulse was produced.

If two pulses are applied to a half adder, one to each input simultaneously, then G1 does operate. The two pulses become one pulse in G1. The output of G1 becomes carry pulse and also inhibits G2. The two input pulses pass through the delays and buffers to G2 but are prevented by G2 from passing to the sum output. The two delays are inserted in the path to G2 in order to delay the pulses for the amount of time required for G1 to develop its inhibition on G2 if both inputs of G1 have been excited. The half adder thus follows all the rules laid down for it above. Of course, the missing operation is the transfer of the carry pulse back to the input of the adder so that it can be combined with the next digit pair entering the adder. First, such a device would require a one pulse delay between the carrier output and the input of the adder. However, there is still another problem in that the half adder only has two inputs: the carry pulse could not be buffered into one of the two present inputs because the carry pulse would be lost if another pulse should occur as a digit of the word entering that word. Therefore, a third input must be devised to provide for the triple input condition when there is a one in both the addend and augend inputs and also a carry pulse to be added in from the previous addition. For this operation a full binary adder is required. This full binary adder will be described later.

The half adder can be used for another purpose in binary computing. The rule of the half adder is that two ones produce a zero on the sum output and that a one and zero in either order on the inputs produce a one. Now examine the binary complement. By definition, the complement when added to the original quantity should produce all zeros except a final carry in the place beyond the most significant digit. Thus consider the following:

quantity=1101100011101,
the complement=0010011100011,
the sum being 10000000000000,

and the upper quantity is represented in complementary form by the lower quantity. Note that the complement is formed by interchanging ones for zeros and zeros for ones in the original quantity except for the least significant digit. The particular complement given in the illustration is called a tens complement. The complement by interchanging ones and zeros without correction of the least significant digit position is called a nines complement. The tens complement is used more frequently than the nines complement. The nines complement may always be converted to a tens complement by adding a one to the least significant digit.

Consider now the nines complement and the half adder. If a binary quantity is added to a string of ones, the nines complement is obtained since the half adder has no carry over circuit. Thus, only the individual sums are obtained for each pair of corresponding digits. By means of the half adder the nines complement may be formed by adding the original quantity to a string of ones. The ten's complement can be obtained by adding a one to the least significant digit. Thus, the half adder is also a complementor. When so used, the carry output of the complementor is ignored. Note that if a quantity is sup-

plied to one input of the complementor and no quantity is supplied to the other input, the complementor yields the original quantity unaltered.

If two pulse strings are identical and are applied simultaneously to the two inputs, the sum output of a half adder should emit no pulses. The combinations which produce no sum pulses are two zeros or two ones. Thus, the half adder can be used as a comparator. If the two input quantities are equal, no sum pulses occur. If either quantity contains a one where the other has a zero, the sum output emits a pulse which signals the lack of identity.

Full Adder

The half adder, therefore, may perform two very useful functions for a serial binary computer; it may complement and it may compare for identity. The last elementary circuit component to be discussed herein is called a full adder. The full adder is shown in block form in FIGURE 5. As will be seen in FIGURE 5, the inputs A, B and C pass through delays Da, Db and Dc and are buffered together into G5. The three inputs also meet in G4. Each pair (three in all) of inputs meet in gates G1, G2 and G3.

A single pulse on any input produces a sum pulse. A combination of two ones and a zero meet in some one of the three gates G1, G2 or G3. This situation produces a carry pulse which inhibits G5 as in the half adder. The carry pulse, however, also passes into a one pulse delay, D1. The output of the delay is connected to the carry (C) input. If one occurs at all three inputs then, G4 operates. The pulse from G4 bypasses G5 to become a sum pulse. Meanwhile, all three gates G1, G2 and G3 open to produce a carry pulse which, incidentally, inhibits G5. The action in G5 is insignificant since G4 opened in this case and bypassed G5. However, the carry pulse is significant because it enters the delay D1, for combination with the next digit combination. When the operation of the various components in the arithmetic circuit are described in detail, references will be made to signals which are generated elsewhere in the computer. The apparatus wherein these signals are generated is described in copending application S.N. 279,710. However, it will be necessary to give a brief description of what these signals are and what they are intended to do.

Function Table

One type of these signals consists of those signals which are supplied from a function table. In general, a function table is an arrangement of data which is entered with an argument and which yields, as a result, the value of function corresponding to the argument. The function table (FT) in the central computer is analogous to the mathematical function table just described. The function table in the computer is an array of lines which translates the instructions set up in the computer in accordance with the allowable computer operations into appropriate gating signals which establish and break connections between the components of the arithmetic circuit and also within these components themselves. The input or exciting lines are interconnected with the output or excited lines through diodes. The arguments of the function table are the binary digit combinations of the instruction code and the functions of the various combinations of gating signals unique for each computer operation.

When a computer operation causes the function table to emit function table signals, a finite time is required for the function table to reach equilibrium before these signals can be produced. This time is called switching time. The switching time allowed for the main function table signal is one minor cycle even though they reach equilibrium in less time. The control signal on certain gates must only change during the space between words. To insure that during the switching time, undesirable computer operations do not occur, certain apparatus in the

computer described in copending application S.N. 279,710 is used to generate time-out signals which are supplied to the various computer components to prevent this undesirable type of operation. Function table signals are abbreviated hereafter as FT signal; time-out signals are abbreviated as TO signals.

Timing Pulses

The standard timing pulses which are generated by the timing pulse generator at the frequency at which binary digits are generated may be either of positive or negative polarity and are abbreviated as TP+ and TP—.

The timing pulses generated at word and computer character frequencies by the cycling unit are indicated as px or tx where the letter x may be any number from 0 to 90. (Sometimes the number 91 appears; in this case, it should be considered equivalent to 0.) The symbol px designates a given pulse position within the word. Its significance is positional. (See, for example, FIGURE 2b which indicates the pulse positions within the word.) The symbol tx also designates a given pulse within a word, but its significance is temporal. When it is necessary to gate a specific px in a circulating register, a certain tx is supplied to the gate. If it is necessary to gate a specific px to two or more different points within a register, and these points are different in time within the register, different tx 's will be required at these points.

When the term pxn or txn appears, it indicates that the particular px or tx is repeated once every computer digit. For example, $p1n$ would mean that $p1$, $p8$, $p15$ and so on, are applied to the same point.

Sometimes the letter t will be followed by a bracket containing two numbers, for example $t(69-72)$. This expression has one of two meanings. The first meaning is that the pulses corresponding to $t69$, $t70$, $t71$ and $t72$ have been buffed together to produce a composite pulse which is present over the entire time interval $t69-t72$. The second meaning of this expression is that these corresponding pulses are present in sequence. The particular meaning the expression as used in the text will be apparent from the context. In either case, the term indicates that signals are present during the pulse times indicated by the numbers within the brackets.

Another signal which is supplied to the arithmetic circuit from another component in the computer is called the time selector signal (abbreviated as TS). This signal is generated when words are transferred into or out of the memory. A detailed description of this signal as well as the other signals will be found in the aforesaid co-pending application S.N. 279,710.

High Speed Bus

Word transfer within the arithmetic circuit and, for that matter, within the computer proper is not accomplished by transferring the words directly from, for example, one register to another but rather by routing all signals through a central switching apparatus called a high speed bus amplifier (abbreviated as HSBA). The high speed bus amplifier is the main route by which information is transferred from one point to another within the computer. The high speed bus then is in reality no more than a switching central which receives signals from the many registers and other elements and sends these signals out over various lines to their destination. The high speed bus amplifier is described in detail in copending application S.N. 279,710.

Checking Circuits

The checking circuits of the arithmetic circuit are of two main types; odd-even checkers and duplicated equipment with comparison circuits.

Odd-even checkers depend on the design of the pulse code used within the computer. This code provides seven pulse positions for every character. Six of the seven positions are significant as to the actual code while the seventh is the odd-even position. If the number of pulses

or ones within the first six positions of any character is even, a pulse is placed in the seventh position to make the total odd. Thus the total number of pulses in the seven positions is always odd. By means of a binary counter and a few gates, an odd-even checker has been constructed which examines every group of seven pulse positions which passes through the high speed bus amplifier.

The duplicated equipment type of checking consists of duplicating the most essential parts of the arithmetic circuit and producing simultaneous independent results which can then be compared for equality. For this type of checking, the A, the R, the X and the L-registers, the algebraic adder, the comparator, the multiplier-quotient counter and the high speed bus amplifier are all duplicated.

The test for oddness of a dynamic pulse train can be made without interrupting normal operation by a simple combination of binary counters. A binary counter has two stable states called zero and one and changes its state whenever a pulse is supplied to it. Suppose a binary counter is cleared to zero and a pulse train of data is supplied to it, after the first decimal digit, the binary counter should be advanced an odd number of times and therefore, should be set to one. After the second decimal digit, it should be set to zero. Suppose another binary counter is added to the circuit which is initially cleared to zero and advanced once each decimal digit, the settings of the two binary counters should agree after each decimal digit. This device is a common odd-even checker.

In order to provide a check on arithmetic operations without interrupting computation, the circuits are duplicated. In this way, the computation is performed simultaneously but independently in two separate units. The results from each of the two duplicated circuits are compared, any discrepancy indicating an error.

This type of comparison is made by a half adder. A half adder, as we have seen, produces no pulses on its sum output when there is a signal on both inputs. The pulse trains from the duplicated units are supplied to the half adder which provides a constant check. As soon as there is any discrepancy, there is a sum output from the half adder to indicate an error. This type of checker is called a like-unlike or comparison checker.

MAJOR COMPONENTS, BLOCK DIAGRAMS

In the following discussion, wherein the comparator, the multiplier-quotient counter, the algebraic adder (including the complemeter), the A-register, the X-register, the L-register and the F-register are described in detail individually, all flip-flops, gates, and other basic electronic components are numbered. In order to identify the location of each of these components, an alphabetic character will precede the designation of the particular component concerned. This character will indicate in what major unit of the arithmetic circuit this electronic component is located. Thus, components in the A-register will be designated by the letter A; those in the X-register by the letter X; those in the L-register by the letter L; those in the F-register by the letter F; those in the comparator by the two letters CP; those in the multiplier-quotient counter by the letter Q; those in the algebraic adder by the letters AA. The same letters with an overline refer to the duplicated unit. Thus A refers to the A-register and $\bar{A}$ refers to the duplicated A-register. In the procedure which will be followed, the block diagram of each of these major units in the arithmetic circuit will be described first and then the schematic diagram associated with this block diagram will be described immediately thereafter. Certain material in the following discussion deals with operations which are performed by the arithmetic circuit in conjunction with units external to the arithmetic circuit. In this situation, reference may be made to copending application S.N. 279,710 for any further information desired.

When more than one sheet is required for the showing

of a block or schematic diagram of any of the arithmetic units, connections between such sheets are indicated by a code making use of the unit letter designations described above. For example, if an output line from a gate shown on one A-register sheet must be connected to the input line to a gate shown on a second A-register sheet, both lines will be labeled A1. The letter "A" indicates the A-register; the number "1" indicates that both lines are really one line. Because of the large number of interconnections among the various components of this system, it would be impossible to show them all upon a reasonable number of sheets of drawings. To avoid undue complexity of the drawings, the connections from one component of the system to the others are shown as arrows, pointing out from the component if it is an output connection and pointing toward the component if it is an input connection, appropriately labeled with the component to which it is connected.

Comparator

The comparator is illustrated in FIGS. 6a-e in which FIGS. 6a, b, c and d comprise a detailed block diagram of the entire comparator and FIG. 6e is a simplified block diagram of the comparator.

Referring first to FIG. 6e, the comparator is therein illustrated in simplified form utilizing, as much as possible, the same blocks and reference characters found in FIGS. 6a-d so that the correlation between the simplified and the detailed block diagrams is clear.

The comparator has three main functions which it performs either simultaneously or individually. The comparator determines which of two words is the larger to control the inputs to the algebraic adder so that the subtrahend input always re-receives the smaller quantity. In addition, the comparator determines when two inputs are equal or are not equal for the conditional transfer operation. Further, the comparator compares the signs of two inputs to the algebraic adder, determining whether they are similar or different, and, from this, deriving the sign of the result.

To perform these functions, the comparator has five inputs as shown in FIG. 6e. There is an input from the A register and an input from the L register, which two inputs are combined together into a single line. There is also an input from the high speed bus amplifier and from the X register, which two inputs are also buffed together into a second line. In addition to these, a minus sign is also supplied to the sign detector and the equality detector portions of the comparator.

Considering first the magnitude detector which determines which of two words is the larger, a word from the A or the L register is applied to one input of the magnitude detector and a second word from the X register or the high speed bus is applied to a second input of the magnitude detector. The magnitude detector comprises a binary subtracter which is made up of two cross-connected gates and a flip-flop as is better illustrated in FIGS. 6a and c and which will be described in detail hereinafter. One of the primary functions of the magnitude detector is to control the input gates of the algebraic adder to ensure that the larger quantity is always applied to the minuend input, and a signal is obtained from the magnitude detector only when the input from the A register is greater in absolute magnitude than the input from the X register or from the high speed bus, which may provide a word from the L register. The output of the magnitude detector is applied to the magnitude memory, flip-flop FF154, to set that normally restored flip-flop. The setting of FF154 applies a signal to the conditional transfer gates which control the condition of the conditional transfer storage, FF155. When FF155 is restored, it generates the S2CP signals which are applied to the gates of the algebraic adder to reverse the inputs. But the output of the magnitude memory causes FF155 to be set. Thus, when the absolute magnitude of the con-

tents of the A register are greater than the absolute magnitude of the X or L register, no S2CP signal is generated.

The comparator also compares the signs of the two words being operated upon by the algebraic adder and determines the sign of the result which is applied to the X register. A minus sign is applied, during the sign portion of the word, to the input of the equality detector, which is a pair of cross-connected gates where the inhibitory input to one is the permissive input to the other. If the contents of the X register (or the L register through the high speed bus) is negative, the equality detector generates no output signal at that time; but, if the contents of the X (or L) register is positive, then a carry is generated and applied to FF150 immediately after that flip-flop had been restored by a t86 pulse. Thus, the condition FF150 is an indication of the sign of the information of the subtrahend.

The minuend is applied to the sign detector, which is a half-adder, HA151, just as the equality detector, together with the minus sign. Again, if the minuend is negative, there is no output from HA151, but if the minuend is positive, the carry out put from the minuend is applied to the sign storage, FF151, to set that flip-flop. The two outputs, set and restored, are applied to the inputs of gates G157 and G158 together with the two outputs of FF150. If the two signs are positive, both flip-flops are restored and G157 and G158 are inhibited to prevent the passage of a p91 pulse. The result sign storage then remains restored, and the sign gates G161A and B pass a positive sign to the X register. If the contents of both minuend and subtrahend are negative, then the two flip-flops FF150 and FF151 are set, again inhibiting both gates G157 and G158. If the signs of the minuend and the subtrahend are different, then a minus sign must be applied to the result. In that case one of the two flip-flops FF150 and FF151 will be set and the other will be restored, opening one or the other of the gates G157 or G158 to pass a p91 to set FF152. The sign gates will then pass a minus sign to the X register. In addition, the output of the sign storage will also generate the S1CP signal which is applied to the complementer in the algebraic adder to render it operative. This is necessary, since when the two signs are different, a subtraction takes place, and subtraction is performed in this system by the addition of the complement of the subtrahend to the minuend and ignoring the overflow from the last place.

Actually, the magnitude detector produces an output whenever the absolute value of the contents of the A register is either greater than or equal to the absolute value of the contents of the X or L register. This is all that is necessary to control the algebraic adder input gates. But in one conditional transfer operation when the transfer of control from one series of instructions to another series is affected, it is necessary to determine the equality between the contents of the A and the X registers and between the contents of the A and the L registers. The equality detector is used for this as well as for determining the sign of the contents of the A register. During the first twelve digit times, the equality detector is used for the determination of equality, but during the time of the sign digit, the equality detector determines the value of a sign. This is accomplished by using appropriate timing pulses to open or close gates so that the desired portion of the word passes, the proper gate at the proper time.

As mentioned above, the equality detector is a half adder, HA150, which comprises two cross-connected gates in which the permissive, or opening, signal on one gate is an inhibitory, or closing, signal on the other. When there is no equality between the inputs to HA150, an output carry occurs. This carry is applied to the input of the equality storage, flip-flop FF153, to set that normally restored flip-flop. The two outputs from FF153 are

applied to the conditional transfer gates and, together with the signals from the magnitude detector and FF150, determine the condition of the conditional transfer storage. As explained in detail below, there are 12 possible conditions which can exist between the contents of the A and the L registers. The contents of either register can be positive or negative and either can have the larger value. Under only five of these 12 possible conditions is there to be a transfer of control. The conditional transfer gates are so arranged that the various individual outputs from the magnitude memory, the magnitude detector, the equality storage, and FF150, condition the gates to allow the conditional transfer storage to be set only under the proper conditions.

The inputs to the comparator are shown on the left side of FIGS. 6a and 6b. As shown the uppermost input to the comparator is applied to CP-G151A and comes from a seven-pulse delay (shown in the upper left portion of FIG. 12a) in the main recirculation path of the A register. A second input to the comparator is applied to CP-G151B and comes from the output of the L register (shown in the lower middle portion of the recirculation path approximately in the center of the drawing). On FIG. 6a an input to the comparator at CP-G152C is shown coming from the high speed bus. The high speed bus is a complicated switching central for the computer and, as such, is not considered a portion of the arithmetic circuits. Because of this, it is not shown in detail in this application but reference is made to the copending application S.N. 279,710. An input from the X register to the comparator is shown in FIG. 6b at CP-G152D. In the main recirculation path of the X register, which is shown toward the right side of FIG. 14, is a compensating delay D_c from which the input to the comparator is taken. The comparator has two inputs from the X register as shown on FIG. 6b, both inputs being the same in time, $p0=t1$. Also shown in FIG. 6b is a second input to the comparator from the high speed bus. This input is to CP-G152A and will not be discussed in greater detail herein, for the reasons given above.

It should be apparent that the interconnections among the various elements of the arithmetic circuits form a rather complex arrangement of lines, and to avoid complexity in the drawings, the actual connections among the various elements have not been shown as continuous lines, but will be referred to and described by indicating the outputs of each figure which connect to the inputs of each other figure.

During multiplication, the sign of the multiplier which is stored in the X-register is compared with the sign of the multiplicand which is stored in the L-register. During division, the sign of the dividend, which is stored in the L-register, is compared with the sign of the divisor as it arrives from the memory.

The multiplication comparison requires only one FT signal, FT151. When this signal is present, the input gate from the L-register, CP-G151B (see FIGURE 6a), is open and the input gates from the X-register, CP-G152B and CP-G152D (see FIGURE 6b) are also open because FT152 is not present.

These three input gates are closed during the check pulse time by the check pulse eliminator signal (abbreviated as CPE), since the check pulse does not follow the laws of binary magnitude observed in the other six channels.

The signs are detected by CP-HA150 and CP-HA151. (See FIGURES 6a and 6b.) The entire word in the L-register (through CP-G151B) is applied to one input of the CP-HA150. (See FIGURE 6a.) The word from the X-register is applied to the other input of CP-HA150 (through CP-G152D) but with the sign deleted. During the sign digit time a minus sign (p86) is supplied through the X-register input to the CP-HA150. During the first eleven digit times, pulses are applied to the CP-FF150. However, at t86, which is just before the minus sign pulse t88 reaches CP-HA150 (through CP-CG144B), a p84

pulse is applied to the CP-FF150. If the sign of the word from the L-register is minus, the sum output of the half adder, CP-HA150 emits no pulses during the sign digit time since the input signals are identical, and FF150 remains restored. If, however, the sign of the word from the L-register is positive (a plus sign is represented by zero equals 1 00 0011 but with the check pulse eliminated), then the minus sign pulse is matched in the half adder by the pulse in the next to the least significant position of the + sign, giving no output, but the pulse in the least significant digit position of the plus sign digit becomes a sum pulse and, passing through the CP-CG141B, sets CP-FF150. (The letters CG indicate that the particular gate referred to is a clock gate, i.e., a gate which retimes, by means of the standard timing pulses, incoming pulses which are subject to undesirable phase displacement. A further description of a clock gate will be found in the discussion of the schematic diagram of the comparator, FIGURES 7a to 7k.) Thus CP-FF150 registers the sign of the word from the L-register: if the sign is plus, this flip-flop is restored, if the sign is minus, the flip-flop is set.

The word from the X-register enters a circuit composed of CP-HA151 and CP-FF151 via CP-G152B. (See FIGURE 6b.) CP-HA151 and CP-FF151 operate in identical fashion as CP-HA150 and CP-FF150. Thus CP-FF151 remains restored if the quantity in the X-register is positive, and is set if negative.

There are two possible conclusions which can be made: if the signs are the same, that is, both plus or minus, then the product is plus; if the signs are opposite, then the product is minus. CP-G157 and CP-G158 (see FIGURE 6b) generate the proper conclusion in the absence of FT-159. If CP-FF150 and CP-FF151 are both set or both restored, then CP-G157 and CP-G158 each receive only one signal which is inadequate for either gate to open. However, if the signs are different, then the two flip-flops are in opposite states. Thus if CP-FF150 is set and CP-FF151 is restored, CP-G157 is open; if the opposite situation holds, then CP-G158 opens. In either case, a p91 is gated by one or the other gate, which pulse sets CP-FF152. (See FIGURE 6d.) CP-FF152 therefore indicates that the sign of the product is plus if it remains restored, and that the sign is minus if it is set. CP-FF152 is set by a p91, the same pulse as is gated by CP-G157 or CP-G158; however, there is a two pulse delay between the gates and the set input of CP-FF152. During the fourth through fifteenth steps of multiplication, the FT159 inhibits CP-G157, CP-G158 and CP-G159 to prevent the p91 from changing the state of CP-FF152.

If the sign of the product is negative, then CP-G161A (see FIGURE 6d) can gate a minus sign (p86) to the A and X-registers when the other signals (FT161 and IER) are applied to CP-G161A. (The IER signal is supplied from the multiplier-quotient counter as will be described hereinafter.)

If the sign of the product is positive, then CP-G161B can gate a plus sign (indicated as a decimal zero, abbreviated as Z) to the A and X-registers when the other signals are applied. Since the Z signal is available during every digit time (decimal zeros are continuously generated in units external to the arithmetic circuit), CP-G161B has the additional signal, the sign gate signal, applied to it which allows only that Z pulse group which occurs during the sign digit time to be gated. The other signals (IER and FT161) are identical to those on CP-G161A. FT161 is produced during the last multiplication step as described in the discussion of the multiplier-quotient counter; both CP-G161A and CP-G161B are inhibited during the preceding time out.

During the multiplication sign comparison, the words entering the comparator are applied to various other elements in the comparator but such operations are trivial. For example, both the words are supplied to the binary

subtractor but no significant actions result from this operation.

The division sign determination is similar to that of multiplication. The divisor appears in the high speed bus and enters the comparator through CP-G152A and CP-152C during the first step of division. (See FIGURES 6b and 6a.) The dividend enters at the comparator from the L-register and arrives via CP-G151B. FT151 is present during this division step to open CP-G151B. FT152 is also present simultaneously to open CP-G152A and CP-G152C and to inhibit CP-G152B and CP-G152D. All gates carry the check pulse eliminator signal to delete the check pulses. Furthermore, the sign gating signal through CP-G152G deletes the sign digit of the divisor at CP-G152C. As in the case of multiplication, the passage of the word through CP-G152C is trivial. The signs are determined by CP-HA150 and CP-HA151. The results are stored in CP-FF150 and CP-FF151 respectively, and the final sign is stored in the CP-FF152. During further steps in division FT159 is present to inhibit CP-G157, CP-G158 and CP-G159 to prevent p91 from altering the state of CP-FF152. During the last step of division FT106 and FT161 are present to gate the sign of the quotient from CP-FF152 to the A and X-registers. (See FIGURE 6d.)

Before an addition or subtraction operation can be performed, the signs of the operands must be compared. In addition, like signs indicate an actual addition while unlike signs actually call for a subtraction. In subtraction, the same rules can apply since the algebraic sign of the subtrahend is always reversed before the sign comparison operation.

In actual subtraction, whether it is the algebraic addition of two quantities of unlike sign or an algebraic subtraction of quantities with like signs, is performed by complementing the smaller quantity and then adding the complement to the other operand. In this way all additions and subtractions produce an uncomplemented result with an algebraic sign. In order to determine which is the smaller quantity, a magnitude comparison is required.

The algebraic adder has a switching arrangement on its input system such that a signal (S'2 and S''2) from the comparator can interchange the minuend and subtrahend inputs if the results of the magnitude comparison so indicate. This action occurs even for an actual addition: the smaller quantity always enters the subtrahend input of the algebraic adder.

The complementer is associated with the subtrahend input of the algebraic adder. The complementer does not operate unless a signal (S1CP) from the comparator is present. The S1CP signal indicates that the signs are different and that an actual subtraction must be performed.

The sign of the result is determined by the familiar algebraic rules. In addition (which implies the same sign), use the same sign; in subtraction use the sign of the larger quantity. Since the larger quantity always enters the minuend input, its sign is allowed to pass through the algebraic adder unchanged while the sign of the subtrahend is suppressed in the algebraic adder.

The minuend from the A-register (the terms minuend and subtrahend are here intended to include the equivalent operands for addition) enters the comparator through CP-G151A. (See FIGURE 6a.) This gate requires no function table signal but carries a check pulse elimination signal. The subtrahend enters the comparator through CP-G152D and CP-G152B. (See FIGURE 6b.) The words entering through CP-G152D are applied to CP-HA150 but this action has no significance unless the two quantities are identical. The signs of both the subtrahend entering through CP-G152B and the minuend through CP-G151A are determined by the respective half adders and stored correspondingly in CP-FF150 and CP-FF151. The parity of the signs (that is, whether they are like or unlike) is stored in CP-FF152. (See FIGURE 6d.) CP-FF152 controls the complementer by means of signal

S1CP which is developed only if the signs are unlike. The set input of CP-FF152 indicates unlikeness and its signal is, therefore, gated to the complementer by CP-G160A as the S1CP signal. FT160 is present during the addition and subtraction instructions.

The minuend, through CP-G151A and the subtrahend through CP-G152B are also applied simultaneously to the binary subtracter. This subtracter consists of two gates, CP-CG154A and CP-CG154B, and a flip-flop. The flip-flop CP-FF156 (see FIGURE 6c) is initially restored to indicate that the subtrahend is greater than or equal to the minuend. This flip-flop is then set each time the minuend contains a pulse and the subtrahend contains a zero, and is restored each time the opposite condition holds. Furthermore, this flip-flop is left unaltered each time a pair of ones arrive simultaneously. Therefore, the final state of the flip-flop indicates which quantity contained the binary one of the final one-zero combination. Incidentally, one-one and zero-zero combinations can occur after the final one-zero combination without altering the conclusion.

Because the absolute magnitudes exist in the first eleven positions only (that is, the first eleven positions after the space between words) and since the absolute magnitudes must not include the sign (which is the twelfth position) CP-FF156 is sampled at p84 before the sign digit has entered the subtracter. If CP-FF156 is set, CP-G172C is opened and passes a p84 (t87) pulse to set CP-FF154. (See FIGURE 6a.) CP-FF154 remembers which of the absolute quantities is greater until after the signs have been inspected, then it is restored by a t8 pulse. CP-FF154, when set, opens a gate, CP-G167 which passes a p91 (t3) pulse to set CP-FF155. (See FIGURE 6d.) Since CP-FF155 is also reset at t3, the pulse from CP-G167 passes through a two pulse delay.

CP-FF155 indicates whether or not the algebraic adder inputs are to be interchanged. It is normally restored, and in this condition, the output of this flip-flop is applied to CP-G160B. During the addition and subtraction operations, FT160 opens CP-G160B when the time out period has ended and the signal from the restore output of CP-FF155 passes through to generate the S'2 and the S''2 signals. These signals interchange the algebraic adder inputs. To prevent CP-FF155 from interchanging the inputs, a signal from the binary subtracter, or from some other source, must set this flip-flop.

If the minuend and subtrahend are equal in absolute magnitude and different in sign, the difference in sign will generate the S1CP signal and cause the algebraic adder to subtract the two numbers. The result would be a string of decimal zeros signed with the sign of the minuend input. But it is conventional that a string of zeros be signed positive, i.e., with another zero, therefore, in this unique case, the positive quantity must enter the algebraic adder on the minuend input.

First, the two quantities are applied to CP-HA150 (see FIGURE 6a) to test for equality. If the two quantities are not identical, the output of CP-HA150 is passed through gate CP-G156B to set CP-FF153. (See FIGURE 6c.) A sign gating signal inhibits CP-G156B to prevent a difference in sign from effecting CP-FF153. If the absolute quantities are equal, there is no output pulse from CP-HA150 and CP-FF153 (which is restored at t5) remains restored. The restored output of CP-FF153 inhibits a gate CP-G172A.

The signs are then tested in the binary subtracter. Because the quantities are equal, CP-FF156 is restored. (See FIGURE 6c.) If the signs are the same, or if the subtrahend is plus and the minuend minus, CP-FF156 remains restored. If the minuend is plus and the subtrahend is minus CP-FF156 is set and opens CP-G172A. When CP-G172A is opened, it passes a p91 (t3) pulse through CP-G167 to set CP-FF155 and prevent the interchange of the algebraic adder inputs.

When the comparator is comparing two quantities dur-

ing addition and subtraction, the comparisons are made during the time out period. If either of these operations require transfers from the memory to the various registers before the actual addition or subtraction is accomplished, the comparisons are made in the time out period just after these memory transfers have been accomplished. In the event that no memory transfers are required, the comparison operation takes place in the time out period just before the operation is performed.

No function table signals are required to operate the comparator input gates for addition and subtraction since the operands are always supplied to the comparator from the X-register and the A-register and the input gates from the X-register and the A-register (CP-G151A, CP-G152B, CP-G152D, CP-G156A) are normally open. (See FIGURES 6a and 6b.) The time out signal inhibits CP-G151C and CP-G152E and CP-G152F in order to isolate the associated gates from the function table and thus prevent the function table signals from effecting the input gates from the X-register and the A-register while information is passing therethrough. The function table signals which are required by the comparator during the addition and subtraction instruction are not used until after the time out minor cycle referred to above.

Certain computer operations require that the comparator compare two words to determine whether they are equal or unequal. These computer operations are called for by the Q and T instructions. These instructions are discussed in more detail in copending application S.N. 279,710; the Q instruction calls for a transfer of control if the comparator finds the contents of the A-register and the L-register to be equal. The T instruction calls for a transfer of control if the comparator finds the contents of the A-register greater than the contents of the L-register. Hence, the Q instruction calls for a test of equality, and the T instruction calls for a test of inequality. (It is important to understand at this point that the comparator can perform either comparison with both alphabetical and numerical data. If the data is numerical, the comparator takes the sign into consideration and compares the numbers algebraically.)

During the test for equality, the word from the A-register passes through CP-G151A to CP-HA159. (See FIGURE 6a.) FT152 meanwhile inhibits CP-G152B and CP-G152D, the inputs from the X-register, and opens CP-G152C, the input from the high speed bus amplifier. The word from the L-register is transferred to the comparator through the high speed bus and enters through CP-G152C. FT156 inhibits CP-G152G, CP-G156D and prevents the sign digit signal from passing to inhibit CP-G152C. Therefore, the entire word from the L-register passes to CP-HA150. FT156 also inhibits CP-G156A which would otherwise superimpose a minus sign on one input to CP-HA150.

The two words, including signs, are compared in CP-HA150. If these words are not identical, the sum pulse for CP-HA150 is passed through CP-G156B and sets CP-FF153. FT156 is applied to CP-G156E and prevents the sign gating signal from inhibiting CP-G156B. If the words are equal (the Q instruction), CP-FF153 remains restored. The restored output of CP-FF153 controls a gate CP-G156C which has been alerted by FT156. CP-G156C passes a p91 (r3) pulse to set, CP-FF155. (See FIGURE 6d.) When set CP-FF155 generates the CT+ and CT- signals which effect the transfer of controls by transferring the three least significant digits from the control register to the control counter. (The use of these CT signals as well as a description of the control register and the counter will be found in copending application S.N. 279,710.)

The word from the L-register enters the comparator through CP-G152A which is opened by FT152, and is applied to CP-HA151. (See FIGURE 6b.) The words from the A-register and the L-register are both applied to the binary subtractor but in both cases the presence

of these quantities in these units is trivial as no output from the binary subtractor may set CP-FF155, FT156 inhibiting CP-G167.

In the test for inequality (the T instruction), FT152 opens the input gates from the high speed amplifier and closes the input gates from the X-register in the same manner as described above. The complete words from the A-register and from the L-register are supplied through corresponding gates CP-G151A and CP-G152A to the binary subtractor. At the output of the binary subtractor, FT172 inhibits CP-G172C and opens CP-G172A. The condition of CP-FF156 is sampled by a p91 (r3) pulse at CP-G172A. At r3, all digits of the two words have been entirely compared, including the signs, if present. If CP-FF156 is set, thus indicating the quantity from the A-register is greater than the quantity from the L-register, CP-G172A passes a pulse through CP-G167 thus setting CP-FF155 and generating the CT signals which have been previously discussed.

There are twelve possible conditions which the comparator may encounter in making algebraic comparisons of signed, numerical quantity. First, the absolute quantities may compare in three ways:

- I. $|A| > |L|$
- II. $|A| < |L|$
- III. $|A| = |L|$

Second, in each of these three conditions, there are four possible sign combinations:

- (a) A+ L+
- (b) A+ L-
- (c) A- L+
- (d) A- L-

Table 1 below lists the twelve possible conditions versus the proper results of algebraic comparison. An asterisk on the table indicates the carry output from the binary subtractor in that condition. The chart also summarizes the gating system connecting the output of the binary subtractor with CP-FF155.

TABLE 1

A>L	A<L
I(a) *CP-G172A and CP-G167 I(b) *CP-G172A and CP-G167 II(b) *CP-G172A and CP-G167 II(d) CP-G172B III(b) CP-G172A and CP-G167	I(c) I(d) *CP-G172D II(a) II(c) III(a) III(c) III(d)

In conditions I(b), II(b) and III(b), the positive quantity in the A-register is always greater than the negative quantity in the L-register. When the binary subtractor compares the sign digits it finds the zero greater than the minus sign and develops a carry output to cause a transfer.

The opposite is true of conditions I(c), II(c) and III(c), where the quantity in the A-register is negative and the quantity in the L-register is positive. CP-FF156 in the binary subtractor is reset and no carry pulse is produced. (See FIGURE 6c.)

In conditions I(a), II(a) and III(a), where both signs are plus, the comparison is made on the basis of the absolute quantity. The binary subtractor, unaffected by the like signs, develops a carry output only if $|A| > |L|$ as in condition I(a). The two conditions of complete equality III(a) and III(b) produce no carry output nor is a transfer supposed to occur in such cases.

In conditions I(d) and II(d), where both signs are minus, the binary subtractor, unaffected by the like signs, compares on the basis of absolute quantity. But in the case of two negative numbers, the number with the lesser absolute quantity is the greater algebraically. Therefore, in condition I(d) the binary subtractor emits a carry out-

put pulse but a CP-G172D prevents this pulse from setting CP-FF155. (See FIGURE 6d.) Inversely, in condition II(d) the binary subtractor does not produce a carry output where one is required. In this case, CP-G172B generates a substitute pulse to set CP-FF155.

Certain control signals are necessary to operate CP-G172D and CP-G172B during I(d) and II(d) conditions. Both gates are controlled by FT172 which is present only during the inequality test. Both gates are operated also by two other signals which indicate that the quantities being compared are both negative numerals.

If these three signals are present, CP-G172D passes a pulse to inhibit CP-G167, preventing any binary subtractor output from setting CP-FF155.

CP-G172B requires two additional signals to insure that it generates a pulse only in II(d) conditions. A signal from the set output of CP-FF153, indicating that the two absolute quantities are not equal is applied to CP-G172B. In III(d) conditions, this signal is not present and CP-G172B cannot open; thus CP-G172B is prevented from generating a signal in I(d) conditions by the carry output of the binary subtractor, which inhibits CP-G172B through CP-G172A.

The sign digits are inspected by CP-HA150 and CP-HA151, to determine when two minus signs are present. The word from the A-register and the word from the L-register are applied to CP-HA150. The sign digit is deleted from the word in the L-register, however, and a minus sign is inserted in its place. In this way, CP-HA150 checks both for equality in the absolute magnitudes (in conjunction with CP-FF153) and for the sign of the word from the A-register. The presence in the sign digit of any character other than minus, such as a plus sign or an alphabetic character, causes the CP-HA150 to generate a sum output which resets CP-FF150. If the sign of the word from the A-register is minus, CP-FF150 which is set at p84 (186) remains set. Similarly, the sign of the word from the L-register is tested in CP-HA151 and is stored in CP-FF151. The set outputs of both CP-FF150 and CP-FF151 alert CP-G172D and CP-G172B. (See FIGURE 6c.)

The comparison always takes place during the first step of one of the conditional transfer instructions. During the second step, for either the Q or T instruction, the FT159 inhibits CP-G167 to prevent any change in the setting of CP-FF155. The setting of CP-FF155 is subject to the control of the conditional transfer switch, a three position non-locking switch. (See FIGURE 6d.) This switch is described in detail in copending application S.N. 279,710. In the normal position, this switch has no effect on operation. In the transfer position, the switch jams CP-FF155 in the set position independently of the comparator circuits. In this case, every Q or T instruction causes the transfer of control regardless of the results of the comparison. In the no transfer position, the switch jams CP-FF155 in the reset position and prevents transfer of control regardless of the results of the comparison.

The comparator is duplicated. However, there is no comparison checker associated with the comparator. Most of the signals from the comparator go to duplicated units and are effectively checked by the comparison checkers of these units. The conditional transfer signal, however, does not go to a duplicated unit and so requires a special checker. This special checker is described in detail in copending application S.N. 279,710.

Algebraic Adder

The algebraic adder is illustrated in FIGS. 10a, 10b, 10c, 10d, and 10e in block form. FIGS. 10a-d forms a detailed block diagram of the algebraic adder and FIG. 10e is a simplified block diagram utilizing as much as possible the elements and logic of the more detailed diagram.

FIG. 10e should be considered first since it sets forth in a simplified manner what is illustrated in more detail in the other figures. The algebraic adder comprises three major components. It contains the actual mechanism for adding comprising a binary adder A, wherein the information supplied to the minuend and to the subtrahend are added to produce the sums, and a second binary adder B with a correction network by means of which the XS-3 correction is achieved during addition. Further, the algebraic adder comprises, in its input circuitry, switching networks for ensuring that the smaller value input word is applied to the subtrahend line for transmission to the complementer. As explained earlier, the input switching operates in conjunction with the comparator.

The algebraic adder also contains, within its confines, networks which detect information which is non-numeric in character and which provide means for insuring that alphabetic and symbolic information is transmitted to the output of the algebraic adder in unmodified form.

As can be seen from FIG. 10e there is a minuend input from the A-register and a subtrahend input as shown in FIG. 12. The minuend input supplies a gate G700B and a second gate G701A; and the subtrahend input supplies a gate G700C and gate G701C. Gate G700B and gate G701C both have the S2CP signal from the comparator supplied as an inhibitory, or closing, signal, and gates G700C and G701A have the S2CR signal supplied thereto as a permissive, or opening, signal. Assuming that no S2CP signal is present from the comparator, gates G700B and G701C will not be inhibited, and the input information will pass therethrough. At the same time, gates G700C and G701A are not opened by the S2 signal, and information supplied thereto will not pass. Thus, the minuend input information will pass through gate G700B and will be applied to the addend input of the binary adder A, and the subtrahend input will pass through gate G701C, through the complementer which may or may not be operative to complement, and be applied to the augend input of the binary adder A. In addition, the addend and the augend inputs to the binary adder A are supplied to gates G714 and G715 respectively to bypass the binary adders should the information contained therein prove to be alphabetic or symbolic in nature. When the comparator determines that the information supplied to the subtrahend is greater in absolute magnitude than the input to the minuend, an S2CP signal will be generated and will be applied to the input gates in the algebraic adder. Upon receipt of this signal, gate G700B will be inhibited and gate G701C will be opened; and gate G701B will be inhibited and gate G701A will be opened. Since gates G700B and G701B are closed, information applied to the minuend and the subtrahend inputs will no longer pass through the same routes that they took before, but information from the minuend will pass through the now open gate G700A and be applied through the complementer to the augend input of the binary adder A, and the information applied to the subtrahend input will pass through gate G700C and will be applied to the addend input of binary adder A. From this it can be seen that a determination made by the comparator that the information supplied to the subtrahend input of the algebraic adder is greater in absolute magnitude than that supplied to the minuend input will cause a switching operation to take place and will open and close the appropriate gates to insure that the larger signal is always applied to the addend input of the binary adder A. The reason for this will become evident when it is considered that the complementer is found only in the augend input to the binary adder A. Since subtraction, in this system, is performed by adding the complement of the smaller quantity, it is necessary that only the smaller valued number be complemented, and it must be assured that the smaller valued number is always supplied to the augend input. As explained above, the comparator also determines when a subtraction is to take

place by comparing the relative signs of the inputs to the algebraic adder. When it has determined that the signs are different and that an algebraic subtraction is required, it generates an S1CP signal which is applied to the complementer and causes the complementer to become operative. The complementer, as will be explained in more detail hereinafter, comprises two lines of amplifiers and appropriate means to direct the information through one line or the other. One of the lines of amplifiers contains an even number of stages and merely amplifies the information in the same phase relation it originally was, whereas the other line contains an odd number of stages and produces information which is 180° out of phase from that applied to it. Since, in the XS-3 system of notation, a complement of a digit may be obtained merely by substituting a pulse where there was no pulse originally and deleting pulses from the positions which originally contained them (inverting), the information may be complemented merely by passing it through an odd number of amplifier stages.

Information supplied to the addend and the augend inputs of the binary adder A is added therein in accordance with the standard rules of binary arithmetic. This means that if a zero is added to a 1, the sum is 1 with no carry; if a 1 is added to a 1, then a 0 is generated as the sum and a 1 is carried. The sum output of binary adder A is applied by lines 177 to the addend input of a second binary adder, B, and the carry output of binary adder A is applied through line 166 to a pair of gates G722 and G723. The carry is normally passed through gate G722 to the carry input of binary adder A, through line 170 and is added to the augend and addend inputs thereto. However, a $p4n$ pulse closes gate G722 and opens gate G723 to prevent the addition of the carry during the times of the zone and check pulses. If there is a carry during this time, this carry should be applied to control the XS-3 correction circuit including gate G728 and flip-flop FF706, and should indicate whether the XS-3 correction will contain an XS-3 signal or an XS-13 signal.

In the XS-3 numerical system, a number is represented by the binary notation of the value which is actually three counts higher than the number. Thus the decimal number 4 is represented by 0111, which is the binary representation of 7. When two such numbers are added together, some correction must be made to maintain this XS-3 relation constant. If two numbers are added together and their total is less than ten, there will be an additional XS-3 in the total over and above what is actually desired. Thus, if the two decimal numbers 4 and 4 are added together, a decimal 8 which is less than 10 is obtained. In the XS-3 system, the sum should be 11, the binary representation of which is 1011. Now, since each decimal 4 is represented by a 7 in the XS-3 numerology and the binary 7 is 0111, the sums of the two 7's comes out to be 1110 which is the binary representation of 14. Thus, this sum contains two XS-3's rather than just one, and this must be corrected. To properly correct for an additional XS-3 it is necessary to subtract 3, or, to add its 16's complement which is 13. If we add the 13 to the 1110, the sum then becomes 1011 (the carry is ignored), which is 11 in binary form, and that is the correct XS-3 sum for the two decimal numbers 4 and 4. Following the operation of the actual circuit, two binary 7's, 0111, are presented to the addend and augend inputs of binary adder A, and the binary value 1110 is transmitted through line 177 to the input of binary adder B. In the last position there is no carry and no signal is applied to lines 171 and 172 to close gate G728. Therefore, a $p4n$ pulse is applied to gate G728 to restore FF706 and apply a permissive signal to line 175 and gate G732. When gate G732 is opened, pulses $p1$, $p3$ and $p4$ pass therethrough to be successively added as the subtrahend input of binary adder B to correct the digit applied thereto by the proper amount. The corrected sum is applied through line 178 to output gate G736.

However, if two numbers whose total is greater than 10 are added, there results from their sum in the last position a carry which produces a different result. Take for example, the two decimal numbers 6 and 8, which total a decimal 14. The XS-3 representation of 14 would be 17. But when the two XS-3 numbers are added together they are $9+11$ and their total is 20. In the machine, the two XS-3 numbers would be 1001 which is added to 1011 and the total would be 10100, producing a carry from the last position. To correct this for XS-3, it is necessary to add 3 rather than to subtract 3, since the carry represents 10 and actually removes two extra 3's from the digit. When we add 3 to the sum of 0100 the total becomes 0111 which is 7, and that, with the carry which represented 10, is the number 17 which was expected. In operation, the two numbers are applied to the addend and augend input of binary adder A and a carry is produced from the highest position. At time $p4n$ gate G722 is closed and gate G723 is opened, so that the final carry is delayed through the delay in line 167 sufficiently long to be presented through line 170 to the first input signal of the next succeeding digit, and, at the same time, the carry is applied to line 171 and line 172 to set FF706 and to close gate G728. Flip-flop FF706 then opens gate G731 to allow the pulses $p1$ and 2 to pass therethrough and add a 3 to the quantity from binary adder A, which is presented along line 177 to binary adder B. The total output is then applied to line 178 to gate G736.

Under ordinary circumstances gate G736 would not be closed, and the output from binary adder B would then be applied to the output of the algebraic adder. However, if the information supplied at the minuend input or the subtrahend input was alphabetic in character, only garbled data would result from the processing of such information, and to prevent erroneous information from passing through the algebraic adder, G736 must be closed. To accomplish this each digit presented to either the minuend input or to the subtrahend input is carefully examined to determine its content. Consider the operation of the upper alphabetic bypass circuit which examines the minuend input. The digits are applied through line 181 to the inputs of gates G704 and G706. Gate G704 is opened only during the pulse times $p(9-11)n$, and gate G706 is opened only during pulse times $p(12 \text{ and } 13)n$. All numerical information contain pulses in the $p(9-11)$ pulse positions, and therefore, all numeric information will pass a signal through gate G704 and line 182 to set FF700. In addition, alphabetic or symbolic information contains information in pulse positions $p(12-13)n$, and this information is not present in the purely numerical digits. Thus, if an alphabetic or symbolic digit is applied to the algebraic adder at the minuend input, pulses will pass through gate G706 to line 183 to restore FF700 and produce an output signal on line 184. Flip-flop FF702 is set by that signal, and it applies a signal to gate G714 to open that gate and allow the minuend signal to be applied from the addend input of the binary adder A to gate G714 and lines 186 and 189, to the output terminal, and closes gate G736 to prevent any processed information coming from the binary adder B to be presented at the output terminal. Thus, it can be seen that if alphabetic information is applied through the minuend input of the algebraic adder, it is detected in gates G704 and G706 to close gate G736 and prevent erroneous information from being supplied to the rest of the machine, while, at the same time, allowing that information to bypass the arithmetic portions of the circuit and to pass out of the algebraic adder unchanged. The lower alphabetic bypass circuit, apparatus G707, G705, flip-flop FF701 and FF703, operates the same as that described for the minuend input but examines, instead, the digit applied at the subtrahend input of the algebraic adder. Thus, either information which is alpha-

betic in nature operates the appropriate alphabetic bypass circuit to accomplish the desired results.

The algebraic adder is the principal arithmetic unit for the arithmetic circuits and is duplicated. It performs the additions and subtractions called for by the computer operations of addition, subtraction, multiplication and division as well as additions for instructions $3n$, $4n$, $5n$ and $7n$ wherein the values of n must be augmented by 10 for each of the memory tanks concerned. In like manner, the adder also augments the memory locations by 10 for the memory tanks in the periodic memory check and memory clear and also increases the control counter reading by unity during the β cycle.

The algebraic adder is equipped with special detecting circuits which enable it to handle words containing a mixture of alphabetic and numerical digits in various ways for the several computer operations. The block diagram of the algebraic adder is shown in FIGURES 10a, 10b, 10c and 10d.

For the addition and subtraction operations, the algebraic adder performs eleven place addition. The input gates (see FIGURES 10a and 10b) are controlled for these instructions by the $S'2$ and $S''2$ signals from the comparator. If the minuend and subtrahend are in proper order, there is no $S'2-S''2$ signal. The subtrahend word, therefore, enters the adder through gate AA-G701B (see FIGURE 10b) and the minuend enters through gate AA-G700B (see FIGURE 10a). If the minuend and subtrahend are found to be in the opposite order, the comparator generates the $S'2$ and $S''2$ signals which permits the subtrahend to enter the minuend input via AA-G700C and the minuend to enter the subtrahend input via AA-G701A by inhibiting AA-G701B and AA-G700B alerting AA-G700C and AA-G701A. The input to the algebraic adder will be discussed in greater detail hereinafter in conjunction with FIGS. 12a-d.

The outputs of AA-G700B and AA-G700C are buffed together and applied to the addend input of binary adder A. (See FIG. 10c.) Similarly, the outputs of AA-G701A and AA-G701B are buffed together and applied to the input of the complementer. (See FIG. 10b.) If the comparator has determined that a subtraction should take place, the S1CP signal is present to excite the complementer and the nines complement of the subtrahend is produced. If an addition has been indicated, the subtrahend word passes uncomplemented, through the complementer.

The check and the zone indicator pulses are deleted from the output from the complementer by the signal $p(89-0)n+ = t(0-2)n+$, applied to AA-G724. This signal inhibits AA-G724 during the three most significant binary digit positions of each decimal digit. Gate AA-G724 is also inhibited during the space-between-words by the DEL signal.

The zone indicator positions of any digit which is applied to binary adder A contain no pulses, since only numbers are so applied, unless the digit is complemented. Since the method of complementing, substituting pulses for no pulses and deleting pulses from those positions in which they originally appeared, inserts pulses into the zone indicator positions of numbers and into the space-between-words, these pulses must be eliminated before the information is applied to binary adder A. They do not convey binary information and do not obey the laws of binary computation.

The binary adder A (see FIGURE 10c) inhibits the check pulse position of the addend word by means of the check pulse eliminator signal. The reason for the difference between deleting only the check pulse of the one word and the check pulse and the zone pulses of the other word is not of significance for the computer operations of addition and subtraction. In each case, however, the check pulse must be eliminated since the check pulses do not obey the laws of binary addition.

The output of the complementer is applied to the augend input of binary adder A. The timing of the inputs of the binary adder A is a delayed $p0(t2)$, i.e., this pulse has been delayed by one-half pulse. The timing at the algebraic adder inputs is $p0=(t2)$. There is a half pulse delay encountered, therefore, between either algebraic adder input and the binary adder A inputs. Each path contains a compensating delay to adjust this timing since the binary adder A contains a PFR which must receive pulses at the underscored timing. The output of the binary adder is, therefore, $p0=t3$.

The carry system of the binary adder A considers three different conditions during normal addition and subtraction. The first condition is a simple binary carry within the first four binary digits of each decimal digit. Whenever a carry pulse of this type develops, it is passed around the carry pulse loop through AA-G722 (see FIGURE 10c). The total delay through this loop is one pulse time including the delay in the binary adder.

AA-G727A (see FIGURE 10c) is a complement correction gate. If the complementer is operating, the least significant digit must be increased by unity in order to produce a tens complement. Therefore, in the presence of the S1CP signal supplied from the complementer, AA-G727A passes a $p8=(t10)$ pulse in order to perform the complement correction.

The second condition covered by the binary adder A carry loop is the carry pulse from the fourth and most significant digit of the numerical part of each decimal digit. This pulse must be carried over the zone and check positions and added to the least significant digit of the next decimal digit. Each such pulse appears simultaneously at AA-G722 and AA-G723 (see FIGURE 10c). AA-G722 is inhibited in each such case by the $p4n=(7n)$ pulse, which is the first zone pulse, while AA-G723 is open only during $p4n=(t7n)$. Thus, every carry from one decimal digit to another is prevented from passing through the short loop and is allowed to pass around the longer loop. The total delay around the AA-G723 loop is four pulse times including the delay in the binary adder A, thereby avoiding the pulse times of the zone and check pulses and delaying the carry pulse until the first pulse time of the following digits.

The third condition carried by the carry loop is the excess three correction process. In excess three arithmetic, a carry pulse from a fourth binary digit calls for adding an excess three to the result, while no carry indicates that an excess three should be subtracted from the result. The significant carry for this operation is the one which is gated through AA-G723. Therefore, just following AA-G723, a tap (see FIGURE 10c) is taken off to drive the excess three correction circuit.

The excess three correction circuit includes AA-FF706, AA-G728, AA-G731, AA-G732 and the binary adder B. (See FIGURE 10c.) If a carry pulse passes AA-G723, it sets AA-FF706 indicating that an excess three is to be added. When AA-FF706 is set, it opens AA-G731 to pass a $p(1,2)n$ into the augend input of binary adder B. Meanwhile, the sum of binary adder A is applied to the addend of binary adder B through a four pulse delay. The $p(1,2)n$ is the 0011 combination which is called excess three or decimal zero. The AA-FF706 is restored by a $p4n=(t7n)$ but this is the same pulse that sets AA-FF706 if it were gated by AA-G723. Therefore, a pulse on the set input is also applied to AA-G728 to inhibit the restoring pulse. If no carry pulse occurs, then no signal is applied through AA-G723 to inhibit AA-G728; AA-FF706 is restored by $p4n=(t7n)$; and the complement with respect to ten of excess three, 1101, is passed by AA-G732 into the augend of binary adder B. The complement, 1101, is created by the signal $p(1,3,4)n=t(1,3,4)n$.

The binary adder B is constructed like binary adder A. Since the purpose of binary adder B is to add in the excess three or its complement, the carry circuit only

operates during the first four binary digits. By the rules of excess three arithmetic, any carry pulses to the fifth place are suppressed. For this reason, AA-G713 is inhibited during $p4n=(t5n)$ in order to delete each such carry pulse.

The corrected sum of the first eleven digits (the first eleven digits following the space between words) of the two quantities which originally entered the algebraic adder appear at the sum output of binary adder B with the timing $p0$ ($t8$). The outputs then pass through a half pulse delay and are buffed into a PFR (see FIGURE 10d). The timing after the PFR is $p0$ ($t9$).

The other signal buffed into this pulse former is the new check pulse. Binary counter AA-BC700 (see FIGURE 10d) is cleared by a $p7n$ ($t1n$) to binary zero. If an odd number of pulses within a decimal digit enters this counter from binary adder B, the counter is left in state one which leaves the check pulse as zero. However, if an even number of pulses within a decimal digit is applied to AA-BC700, it is left in state zero. The zero output of AA-BC700 is applied to the check pulse gate AA-G735 through a compensating delay D (see FIGURE 10d), this delay being required in order to permit AA-BC700 to be cleared to zero by the same pulse as is gated by AA-G735. The counter must be cleared during the check pulse position, since that is the only free pulse position within a word leaving the adder. (Certain considerations for alphabetic digits allows zone pulses to pass this point as will be shown later.) Therefore, the delay is inserted in order to extend the last state of AA-BC700, before being cleared, long enough to gate or not gate a check pulse as the case may be.

Some of the signals from the cycling unit which appear in the adder may occur during the space between words; for example, the $p7n$ applied to AA-G735. Any such pulses are deleted at AA-G736 by the $t(10-16)$ signal which clears the space between words.

The final output passes through AA-G736, a delay and a pulse former, to the algebraic adder output (see FIGURE 10d). The timing at this point is $p0=(t10)$. The total delay to the algebraic adder is, therefore, eight pulse times. The algebraic adder comparison checker for comparing the output of the algebraic adder with the duplicate algebraic adder is tied in at this point. There are two other odd-even checkers in the adder inputs which have been discussed previously.

Adding and subtraction may be performed on the numerical parts of words which also contain alphabetic digits. Moreover, the problem of affixing the proper sign to the result of an addition or a subtraction operation is handled in a different manner than the processing of the eleven numeric digits.

Each word entering the algebraic adder is applied to alphabetic detecting circuits. The two circuits, one for each input, are symmetrical. The word entering either AA-G700B or AA-G700C, for example, passes immediately to a pair of gates AA-G704 and AA-G706 (see FIGURE 10a).

The outputs of these gates are applied to a flip-flop AA-GG700. At the end of each computer digit (seven pulse times) the state of AA-FF700 is examined. If it is set, the digit is alphabetic; if it is restored, the digit is numerical.

AA-FF700 is maintained in the restored condition by a $p1=t3$ (introduced just following AA-G704) applied every minor cycle. However, during the minor cycle of an addition, the FT160 opens AA-G160C to pass a $p8n$ ($t10n$) to set AA-FF700 (see FIGURE 10a). The assumption is made, therefore, that every digit is alphabetic until proven otherwise. All decimal digits contain pulses in the $p(9-11)n$ positions, which pulses are gated by AA-G704 to restore AA-FF700. Since the decimal digits carry zero in both zone indicator positions, the $p(12,13)n$ at AA-G706 passes no pulses to set AA-FF700 again. All other combinations are

considered as alphabetic and in all but two cases, carries zone pulses which are gated by AA-G706. The two exceptions are the code combinations for space and ignore. (See FIGURE 2.) These characters possess zero zone indicators making them appear numerical. However, they carry no pulses in the three positions $p(9-11)n$. Therefore, no pulses are gated by either G704 or G706 for either character and FF700 remains set indicating an alphabetic digit.

Neither a check pulse nor the least significant digit in the seven group can effect AA-FF700 since neither AA-G704 nor AA-G706 is open during these two pulse times, and therefore, $p8n$ is the best pulse with which to set AA-FF700 for each digit.

AA-G704 is inhibited during $p(87,88)$ in order to delete the third and fourth pulses of the sign digit while AA-G706 is open during $p(87,88)$ in order to detect any character in the sign position that is greater than zero. Since the plus (zero) and minus signals have pulses in the two least significant positions only, any digit with pulses in the third and fourth positions must be considered as alphabetic and is, therefore, by-passed.

The set output of AA-FF700 is applied to the two clock gates AA-CG708A and AA-CG709A (see FIGURE 10a). These gates transfer the state of AA-FF700 at the end of the seven pulse group to AA-FF702 in order to free AA-FF700 to examine the next digit while AA-FF702 remembers what to do with the present digit. If AA-FF700 is set, indicating an alphabetic digit, AA-CG709A passes a $p7n$ (in the present example a $p14$) to AA-FF702 thus setting it. If AA-FF700 is restored indicating a numerical digit, AA-CG709A passes a $p14$ to restore AA-FF702. One pulse later, another $p8n$ (specifically a $p15$) passes through AA-G160C to set AA-FF700 for the next digit.

The sum output of AA-FF702 indicates an alphabetic digit, while the restored output indicates a non-alphabetic or numerical digit. If the digit is alphabetic, the set output of AA-FF702 opens AA-G714 to allow the digit to by-pass the binary adders.

In an exactly identical manner AA-FF701 and AA-FF703, in conjunction with corresponding gates, examine the digit on the other input. (See FIGURE 10b.) If an alphabetic digit (including space and ignore) is discovered, AA-G715 by-passes the digit into the algebraic adder output line.

Whenever either AA-FF702 or AA-703 is set, the outputs are buffed together in order to inhibit AA-G736 shown in the lower right corner of FIGURE 10d.

The numerical digit accompanying an alphabetic digit is permitted to enter the binary adder with the alphabetic digit and is thereby combined. However, the result, being meaningless, is suppressed by AA-G726. (See FIGURE 10d.)

Any alphabetic digit entering the algebraic adder during an addition or subtraction operation is by-passed through a seven pulse delay, a pulse former and either AA-G714 or AA-G715 (see FIGURES 10a and 10b) to the algebraic adder output delay and pulse former. The total delay is, therefore, eight pulses which is identical to the route through the adder. Moreover, each digit is examined while it is being added to the other digit. The seven pulse delay between the input gates and the by-pass route stores the digit until the examination is complete. Then the digit is either by-passed through AA-G714 or AA-G715 when it emerges from the seven pulse delay and AA-G736 is inhibited in order to suppress the sum, or the sum is allowable and leaves through AA-G736.

One special problem associated with alphabetic digits is the generation of a new tens complement correction pulse if the digits of the two words are being subtracted. For this reason, the buffed outputs of the set sides of AA-FF702 (see FIGURE 10a) and AA-FF703 (see FIGURE 10b) are applied to AA-G727B (see FIGURE

10c). In conjunction with the S1CP signal from the complementer, and a $p8n$, AA-G727B inserts a new complement correction pulse whenever the previous digit in either word was an alphabetic character. Whenever either input has an alphabetic character, the signal from AA-FF702 or AA-FF703 indicating this (see FIGURES 10a and 10b), inhibits gate AA-G721 which suppresses any carry pulse which may appear in the long carry loop from binary adder A. Such a carry pulse would have been generated from the addition of a numerical and an alphabetic digit and would, therefore, have no meaning as to the next addition.

The one situation not permitted by the algebraic adder is the addition and subtraction of two alphabetic digits at the same time. Whenever AA-FF702 and AA-FF703 are both set, the two set outputs meet in AA-G720 which then connects with AA-FF704. (See FIGURE 10a.) AA-FF704 is applied to the check buffers. The operation in the algebraic adder finishes out the minor cycle but the results have no meaning since AA-G714 (see FIGURE 10a) and AA-G715 (see FIGURE 10b) have superimposed the two characters on each other.

The sign digit attached to the result of any addition or subtraction is the sign digit of the minuend. Whenever the two alphabetic indicating flip-flops, AA-FF702 and AA-703 indicate that the twelfth digit is numerical (which is true for both sign digits) the restored outputs of these flip-flops operate AA-G718 in conjunction with the sign gating signal. AA-G718, when open, by-passes the minuend sign digit into the same by-pass group used by an alphabetic digit and the sign digit is attached to the sum as it leaves the algebraic adder. The sign of the subtrahend and the minuend actually reach the binary adders but the result of this addition is suppressed at AA-G736. AA-G755, shown slightly left of the center of FIGURE 10a generates a signal which inhibits AA-G736.

If an alphabetic digit occurs in either word in the sign position, it is by-passed by the same route used for other digit positions. If an alphabetic character appears in the sign position of both words, AA-FF704 is set indicating an error.

If two numerical quantities whose total exceeds the eleven digit capacity are added together, a condition known as overflow is said to exist. The overflow condition is detected by an overflow circuit which operates when a carry pulse is produced by the addition of the two digits in the eleventh place.

AA-G726 (see FIGURE 10d) detects the overflow pulse. First AA-G726 examines only the carry pulses which follow the long carry path indicating thereby a carry from one decimal computer digit to the next. Secondly, the cycling unit pulse $p81$, specifically tests that pulse position which would indicate that the adder has obtained a carry pulse from the twelfth position. Thirdly, such a carry pulse has no significance if either eleventh digit is alphabetic. Therefore, AA-G726 is inhibited by AA-FF702 (see FIGURE 10a) or AA-FF703 (see FIGURE 10b) whenever the previous digit is alphabetic. Fourthly, a carry pulse normally does occur from the eleventh position on subtraction but has no significance; AA-G726 is inhibited by the S1CP signal indicating that a subtraction is in process. Therefore, during an addition, an eleventh digit carry pulse is considered an overflow providing the eleventh digit was non-alphabetic. FT714 can also inhibit AA-G726 but its purpose will appear later.

If an overflow occurs AA-G726 passes the $p81$ ($t87$) to AA-FF705, the overflow flip-flop. (see FIGURE 10d.) The output of the overflow flip-flop prevents the control counter reading from being increased by unity and causes the control register and static register to search the zero memory location during the next β cycle. Once set, the flip-flop remains set until the next β cycle because FT737 does not occur until then. Moreover, it is not until the time selector signal of the β cycle occurs that a $t1$

is finally gated by AA-G737 to clear this flip-flop. (It should be remembered that this material, which deals with circuits not included in the arithmetic circuit, is described in detail in co-pending application S.N. 279,710.

Twelve place addition, as distinguished from eleven place addition which takes place during subtraction and addition, is used during the multiplication and division instructions as well as instructions $3n$, $4n$, $5n$, $7n$, PMC and MC and the β cycle. The division instruction is the only one in this group in which complementing occurs; all others perform additions only. In all of this group except the multiplication and division operations, one of the input words is manufacture in the cycling unit. For the periodic memory check and memory clear the word is composed of all zeros except the next to least significant digit which is a one. After each tank of ten memory locations has been checked or cleared, the quantity ten is added to the word in the control register. (In other words, the instruction has both an alphabetical and a numeric component and the quantity ten is to be added to the numeric component of this instruction.) During the execution of the $3n$, $4n$, $5n$ and $7n$ instructions, either of two manufactured words are added five times dependent on whether they are performed during the γ or δ cycle of operation. If the instruction occurs during the δ cycle, the word added is identical to the word during the periodic memory check and memory clear. If the instruction occurs during the γ cycle, a second word having zeros in all positions except the eighth, which contains a one, is added. Either word increases the memory location associated with the instruction by ten.

During the β cycle, the control counter reading is increased by unity by passing the control counter reading through the adder and adding it to a word from the cycling unit containing all zeros except the least significant digit which is a one.

For all twelve place addition operations, the alphabetic detection circuits in the algebraic adder are disabled. Moreover, the input switching system controlled by the S'2 and S''2 signals from the comparator is not used. The only input gates are the AA-G700A for the minuend and the AA-G701C for the subtrahend. (See FIGURES 10a and 10b.) Both gates are controlled by FT714 which also inhibits the normally opened AA-G700B and AA-G701B.

The input switching system is disabled for twelve place addition because none of the operations requires algebraic operation. In fact, all operations except division are always additions, and for division the determination of the subtrahend and minuend is not dependent upon a comparison of magnitudes or of signs.

The operation of the long and short carry loops around binary adder A has already been described. The excess three corrector and binary adder B also operate as described previously. The overflow gate AA-G726 is inhibited by FT714 during any twelve place operation.

However, one important point of difference between eleven and twelve place operation is the inhibition of AA-G755 by AA-FF707. (See FIGURE 10a.) During eleven place addition, and at all other times except when FT714 is present, this flip-flop is restored by a $p3$ ($t12$). During twelve place operation, however, FT714 opens AA-G738 to permit a $p5$ ($t14$) to set this flip-flop. The purpose of this flip-flop is to extend the effect of FT714 beyond the end of a minor cycle in order to inhibit AA-G755 during the sign gating interval $t(3-9)$. The flip-flop is then restored at $t12$. The inhibition on AA-G755 prevents a sign gating signal from inhibiting AA-G736 during the most significant digit interval.

During multiplication, the A-register is connected to the minuend input of the algebraic adder and the word containing the round off correction and the multiplicand always enter through the subtrahend input. As the successive transfers of the absolute value of the multiplicand or the quantity equal to three times the absolute value of

the multiplicand occur, the partial product is built up in the A-register. If there should be an alphabetic character in the multiplicand, its zone indicator and check pulse is deleted at AA-G724 (see FIGURE 10a) and the four binary digit portion of the combination enters into the addition as if it were a numerical digit. The result of this operation will have no meaning but neither will such an operation stop the computer. For the 3n, 4n, 5n, 7n, periodic memory check, memory clear and β cycle operations, the manufactured word is always applied to the subtrahend input. For all of these operations except the β cycle operation, the minuend input comes from the control register. During the β cycle the minuend comes from the control counter. These operations are always additions. The input-output instructions 3n, 4n, 5n and 7n may have alphabetic characters associated with them. Such a character is the alphabetic symbol for the other instruction which may be associated with the input-output instruction in the same word. Since the instruction word enters the minuend input, the zone pulses are not deleted. Furthermore, the alphabetic digit is added to zero. Since the carry pulse loops cannot effect the zone pulses, the digit passes on to the excess three corrector where the zero is subtracted out. Therefore, the alphabetic character passes through the adder without change. Similarly, all numeric digits are unchanged except as they are effected by the non-zero part of the manufactured word or by carry over. Since the non-zero digits of the manufactured word are in either the first or second digit positions of the memory locations only, and since the instruction digits are separated from the memory location digits by an unused digit normally filled with a zero (see FIGURE 1a) no carry over pulse can ever affect the instruction symbol digit.

During division, the divisor is often to be subtracted from and added to the remainder; the remainder, at the beginning of the first step of division being the original dividend. The dividend is stored in the A-register and appears, therefore, in the minuend input of the algebraic adder. The divisor appears at the subtrahend input. During the first step, the complement is excited by the S1X signal (this signal is supplied from the comparator). This S1X signal also excites AA-G727A (see FIGURE 10c) in the short carry loop around binary adder A in order to insert the complement correction pulse therein. The divisor is subtracted from the dividend until the quantity in the A-register becomes the negative, i.e., the complement. During this first step in the division process, the S1X signal is applied to AA-G725 and AA-G145C. Since this is a subtractive step, a carry pulse originates from the twelfth digit for every minor cycle except when the output of binary adder A has become a complement. Therefore, AA-G725 examines for a p88 (r0) in the carry loop of the binary adder A. If a carry pulse is present, the gate AA-G725 is inhibited by the carry pulse when the p88 is produced. If the carry pulse is missing, the p88 pulse is gated by AA-G725 to the multiplier-quotient counter wherein the OR stage is initiated. During this OR stage the remainder in the A-register is shifted, and the binary counter which generates the S1X signal is pulsed to its opposite position, which removes the S1X signal from the next step in division. During this next step, the divisor is added to the shifted remainder. Each addition brings the remainder closer to zero. When the remainder finally changes to a positive quantity, a carry pulse occurs in the loop around binary adder A. The carry pulse is gated through AA-G145C by the combined effect of FT145, the p88 (r0) pulse and the absence of S1X. The pulse gated by AA-G145C performs the same function as a pulse from AA-G725. AA-G145C requires an FT145 since the gate would normally gate a p88 pulse during every other twelve place addition operation as S1X is not present to inhibit this gate.

The Multiplier-Quotient Counter

The Multiplier-Quotient Counter, otherwise known as the MQC, comprises a four-stage binary counter and circuits for controlling the counter and registers during a multiplication or division. It is illustrated in FIGS. 8a, b, c, d and e, where FIGS. 8a-d together form a single detailed block diagram and FIG. 8e is a simplified block diagram of the circuit.

Referring to FIG. 8e first, the four counter stages are designated MQC1, MQC2, MQC3 and MQC4. It should be noted that identical reference characters are used for the same elements in both the detailed and the simplified diagrams. A numerical digit is applied to the four-stage counter from a distributor; the digit being applied to the input of the distributor in serial form. Since the MQC is supplied with individual multiplier digits during multiplication and supplies quotient digits during division, the distributor has two sets of outputs. The distributor itself is a calibrated delay line, and the first set of outputs, which are shown in FIG. 8e extending from its lower portion, supply a properly timed pulse to the individual output gates G116A-E to open these gates in the proper sequence. In this manner a statically stored quotient digit is transmitted to the X register in serial form. Gates G116A-E are shown at the top of FIG. 8e.

The second set of outputs from the distributor applies the digit input signals to the timing ages G119A-D, and when a properly timed impulse is applied to the line 257, the input digit is transferred to the four stages of the counter itself. The counter can count in one direction only and the pulse which steps the counter along is applied through gate G127A and line 267, or from the output of flip-flop FF120, through gate G130 to line 267. Each time the counter is pulsed, it counts upward one digit, and the output is applied through the appropriate "0" and "1" lines and through a set of either forward gates or backward gates to the matrix. The selection of whether the forward gates or backward gates will supply the count to the matrix is determined by the condition of binary counter BC120. During multiplication, the MQC contains a single multiplier digit, and each time the multiplicand is added to itself in the algebraic adder, the quantity in the MQC is reduced by one until it reaches zero, signifying that the number of additions required by a particular multiplier digit has been completed, and the next succeeding digit determines the succeeding operations. However, since the MQC can count upwardly only, the backward gates are used to transfer the complement of the count in the counter to the matrix.

This is readily accomplished by merely controlling which output lines of the counter stages are applied to the matrix. Since, in the XS-3 system of notation, a nines complement of a number is obtained merely by substituting zeros for ones and ones for zeroes, the complement of the count in MQC1-4 is represented by the energization of the corresponding zero lines. Thus, the backward gates transmit the zero line information to the matrix and, the forward gates transmit the appropriate one line information to the matrix. The binary counter BC120 energizes the forward gates through line 262 and the backward gates through line 250 upon receiving the appropriate r1 and OR signals. Only during division is the binary counter BC120 continually stepped so that the forward and backward gates are alternately used. This is necessary because of the method of division used by this system, which method of division will be explained in greater detail hereinafter.

The matrix is a standard diode matrix with two sets of outputs. The outputs which are used during multiplications are those which appear on the right side of the matrix in FIG. 8e. In multiplication, either the multiplicand itself or three times the multiplicand may be added to the contents of the A register during the derivation of the partial product of any individual multiplier digit. Whether it is the multiplicand or three times the multi-

plicand which is to be transferred to the AA is determined by the size of the multiplier digit remaining in the MQC counters after each addition. This is represented by the energization of the individual output lines from the matrix. Thus, if the quantity 4 were still remaining in the MQC, the matrix would signal the fact that the contents of the MQC was greater than 3 and a 713 signal would be applied to the F register to transfer three times the multiplicand to the algebraic adder. At the same time, a signal would be applied through gate G130 to step the MQC three times. If however, the amount remaining in the MQC during a multiplication operation is less than three, this is signalled at the output of the matrix, and flip-flop FF120 is set to indicate to the L register that the multiplicand itself should be transferred to the algebraic adder. When the amount contained by the MQC during a multiplication operation has been reduced to decimal zero, this information is also signalled, and appropriate output circuits (not shown in FIG. 8e) generate the IER and the OR signals, which control the operation for either multiplication or division, so that the end of one step can initiate the subsequent step.

The method of division used in this system repeatedly subtracts the divisor from the dividend until the remainder has passed through zero; then the divisor is shifted to the next lower order and it is repeatedly added to the remainder until the remainder has then again passed through zero. This process is repeated until the capacity of the A register is reached. The function of the MQC during division is to accumulate each quotient digit as the appropriate step is in process. This is accomplished by stepping the MQC each time the divisor is subtracted from or added to the dividend. During the subtraction operation, the actual count in the MQC is desired, and this is transferred to the matrix through the forward gates. The vertical outputs from the matrix are fed to gates G116A-E and are subsequently applied to the X register. The output from the distributor reaches the individual G116 gates in proper sequence to open them and transfer the static digit from the matrix to the X register in serial form. When the divisor is being added to the remainder, it is desirable to transfer the complement of the contents of the MQC to the matrix, and for this purpose, the gate G142 is opened by the OR signal generated at the end of each division operation to allow a 71 signal to step the binary counter BC120. Thus, when the divisor is being subtracted from the dividend, the forward gates are energized through line 262, and when, in the succeeding steps, the divisor or a submultiple thereof is being added to the remainder, the backward gates are energized by line 250.

At the beginning of each operation, the MQC is cleared to binary zero by the application of the appropriate signals from the cycling unit. The MQC can be cleared to absolute zero also by the application of signals to line 256.

The subsequent detailed description of the functioning of the MQC in the multiplication and division operation of this system will serve to give a detailed understanding of the operation of each element in the multiplier quotient counter and its controlled circuits.

The multiplier-quotient counter and associated circuits, is a four stage binary counter which count the number of additions per step in the multiplication process, the number of additions or subtractions per step in the division process and the number of words checked or cleared per memory tank in the periodic memory check or memory clear operation. (The periodic memory check and periodic memory clear operations are described in detail in copending application S.N. 279,710.) The multiplier-quotient counter block diagram is shown in FIGURES 8a, 8b, 8c and 8d. The multiplier-quotient counter is duplicated.

The arithmetic circuits perform a multiplication by repeated additions and shifts. The multiplicand is first stored in the L-register from which it can be transferred the required number of times to the accumulator where

it is added to the partial product in the A-register. The multiplier digits are first stored in the X-register from which each digit is sequentially transferred to the multiplier-quotient counter beginning with the least significant digit. Since each multiplier digit determines the number of additions to be made in each step, the multiplier-quotient counter counts the number of additions according to the value of each multiplier digit, and at the appropriate time, sends an IER signal, which causes both the remaining multiplier digits in the X-register and the partial product in the A-register to shift right one place and begins a similar adding operation under the control of the next multiplier digit.

In order to reduce the length of the steps involved in the multiplication process the quantity equal to three times the absolute value of the multiplicand is built up and stored in the F-register. The multiplier digits beginning with the least significant digit are taken sequentially from the X register, coming from a tap on a seven pulse delay, shown on the left hand side of FIG. 14, and are fed into Q-G112C of the MQC, shown at the bottom of FIG. 8b. Each digit is fed by Q-G112C through a pulse-former and appropriate amplifiers and delays to a distributor line in the multiplier-quotient counter, which distributor line actually comprises a delay line. Taps are taken from the delay line at delays of one pulse time, and some of the taps are fed to a group of gates Q-G116A-E, which are used during the division operation, and other taps feed through appropriate gates Q-G119A-D to the four counters which comprise the multiplier quotient counter. By means of the distributor line a serially arranged digit is applied to the counter in parallel distribution. When this quantity is added to the partial product in the A-register, three additions are performed during one minor cycle. In order to use this quantity, two additional signals are required for the multiplier-quotient counter: the ≥ 3 signal indicating that at least three more additions are necessary, which transfers this quantity from the F-register into the A-register and advances the multiplier-quotient counter three steps; and the < 3 signal which transfers the absolute value of the multiplicand from the L-register into the A-register and advances the multiplier-quotient counter one step. The multiplier-quotient counter is a four stage binary counter which advances positively each time it is pulsed. This counter is indicated as MQC1, MQC2, MQC3 and MQC4 on FIGURES 8b and 8d.

In order to understand how this binary counter operates, it is necessary to refer back in the specification to the discussion of the basic binary counter. A group of binary counters may be connected together as a multistage counter as shown in FIGURES 8b and 8d. The result of this connection is that each time that any one counter of the group is pulsed and it passes from binary one to binary zero, the binary one output delivers a pulse to the input of the next higher stage in the counter. When all the stages have reached one (which in the case of four counters is equivalent to decimal 15), all stages produce carry pulses which turn every stage back to zero. At any time after a string of pulses has been supplied to the least significant digit counter input, the four stage counter illustrated will indicate how many pulses up to fifteen have been applied. The sixteenth pulse clears the counter to zero. Hence, every time a multiple of 16 pulses occurs, the counter clears to zero and starts counting again.

Since each multiplier digit is considered as a positive quantity, the multiplier-quotient counter must effectively count backwards to zero. Rather than make this counter count backwards, the multiplier digit, in passing from the X-register to the multiplier-quotient counter, is complemented by passing through an odd number of signal inverting stages. Each binary pulse in the multiplier pulse combination is inverted, the zeros becoming ones and the ones becoming zeros. When a number in the excess

three code is thus inverted, the resultant combination is the nines complement of the original number. Since the nines complement is set up in the multiplier-quotient counter, the multiplier-quotient counter can then count forward until it reaches nine, since the difference between the nines complement of a number and nine is the number itself. The multiplier-quotient counter, when it has reached nine, has counted the number indicated by the multiplier digit and generates the IER signal.

The value standing in the multiplier-quotient counter at any time can be read out through the multiplier-quotient counter output function table. (See FIGURES 8a and 8c.) This function table has two sets of input gates from the multiplier-quotient counter. One of these sets is a group of gates, called the backward read gates, which again invert the pulse combination. The backward read gates are used during multiplication. The output of the multiplier-quotient counter function table during multiplication is, therefore, the nines complement of the nines complement or the number itself. As the multiplier-quotient counter is advanced during each step of multiplication, the nines complement of the function table decreases until, when the multiplier-quotient counter reads nine (1100), the function table reads zero (0011). The zero (Z) line of the function table generates the IER signal that signals the end of that step of multiplication.

In order to operate the backward read gates FT139 opens Q-G139 (see FIGURE 8b) during the first step of multiplication, which gates a t_1 pulse to clear binary counter Q-BC120 to zero. The multiplier-quotient counter backward signal from the zero output of Q-BC120 is amplified and opens the backward read gates (Q-G179A-Q-G179H). (See FIGURES 8a and 8c.) These gates remain open for the duration of the multiplication operation.

The signals from the zero and one outputs of the four stage binary counter pass through the complementing backward read gates and through amplifiers into the four paired input lines to the multiplier-quotient counter function table. This function table decodes each binary pulse combination on its input into a single corresponding output line. The function table input lines are paired (binary zero and binary one) and one or the other line of each pair is always selected. The effect of the selected input line is to prevent the selection of any output line to which it is connected. That output line is selected, therefore, that is not connected to any selected input line.

The circuits which generate the ≥ 3 and the < 3 signals are controlled by the function table output lines Z, 1 and 2. (See FIGURES 8a and 8c.) These three lines are buffed together to control Q-G140 (see FIGURE 8d) and through an additional amplifier to inhibit Q-G147c. FT147 alerts Q-G147c (see FIGURE 8d) during the steps of multiplication. When a multiplier-quotient counter function table line other than Z, 1 or 2 is selected, Q-G147c gates a t_1 pulse to set a flip-flop Q-FF120 (see FIGURE 8d). The set output for the Q-FF120 is the ≥ 3 signal and the reset output is the < 3 signal. The ≥ 3 signal is amplified and sent to the F-register where it causes the transfer of the quantity which is equal to three times the absolute value of the multiplicand into the A-register. When one of the lines Z, 1 or 2 is selected, Q-G140 gates a t_1 pulse to reset Q-FF120. The < 3 signal is amplified and sent to the L-register where it causes the transfer of the absolute value of the multiplicand into the A-register.

The advancing pulse from the multiplier-quotient counter is obtained from Q-G147D (see FIGURE 8d) for any < 3 step. FT147 opens Q-G147D which is inhibited during the time out and IER cycles. The pulse gated by Q-G147D is a t_8 pulse. If ≥ 3 signal is present Q-G130 (see FIGURE 8d) gates two pulses (t_{28} and t_{60}) which are buffed with the t_8 pulse from Q-G147D. These three pulses advance the multiplier-quotient counter three times in one minor cycle.

For example, if the multiplier digit is 4 (0111), the nines complement, 5 (1000), is set up in the multiplier-quotient counter. The backward read gates again invert the combination and set up in the multiplier-quotient counter function table the number 4 (0111) which indicates that four additions are required. The ≥ 3 signal is generated and the multiplier-quotient counter is advanced three times. The multiplier-quotient counter now reads 8 (1011) and the nines complement in the multiplier-quotient counter function table is one (0100). The < 3 signal is generated and the multiplier-quotient counter is advanced once to read 9 (1100) and the multiplier-quotient counter function table reads (0011). The zero (Z) line generates the IER signal and starts the process anew with the next multiplier digit.

The transfer of the multiplier digits from the X-register begins during the fourth step of multiplication. The first operation is to clear the multiplier-quotient counter to binary zero. FT112 opens Q-G112B (see FIGURE 8b) which after time out ends, gates a t_8 pulse to set Q-FF125 (see FIGURE 8b). This set output applies a clear signal to the four binary counters MQC1, MQC2, MQC3 and MQC4. Q-FF125 is reset seven pulse times later by a t_{15} . FT112 also opens Q-G112C (see FIGURE 8b) which connects the X-register to the multiplier-quotient counter distributor line. On FIG. 14 the output of the X register which connects to gate Q-G112C of the multiplier-quotient counter is shown at the left coming out of the upper portion of the recirculation path of the X register as a tap on a seven pulse delay. Simultaneously, FT112 also opens Q-G112D which gates a delayed t_{19} pulse (delayed by half a pulse time). This delayed pulse is applied to Q-CG150 (a clock gate). The output of this Q-CG150 triggers a blocking oscillator (see FIGURE 8b) which generates a sharp transfer pulse. This transfer pulse is then applied to the four transfer gates (Q-G119A-Q-G119D) which connect the multiplier-quotient counter distributor line to the multiplier-quotient counter binary counters. (See FIGURES 8b and 8d.) During subsequent steps, FT112 is absent but is replaced by the IER signal on gates Q-G112B, Q-G112C and Q-G112D.

The circuits which generate the IER signals are controlled by the Z line from the multiplier-quotient counter function table. Whenever the Z line is excited, Q-G147E (see FIGURE 8d) gates a t_2 pulse to set Q-FF121A (see FIGURE 8c). When this flip-flop is set, its outputs are amplified as the IER signals. The t_2 signal from Q-G147E also sets Q-FF121C whose outputs are amplified as the IER or OR signals.

Q-FF121A and Q-FF121C (see FIGURE 8c) which respectively generate the IER and the IER or OR signals, are maintained in reset state by a t_2 pulse which passes through a normally open Q-G148. (See FIGURE 8d.) The signal from the Z line passes through Q-G147A to inhibit Q-G148 thereby preventing the t_2 pulse from resetting both of these flip-flops during the IER minor cycle.

The multiplication process reaches an end after the IER minor cycle of the last step of multiplication. Nothing prevents this IER signal from setting up the next multiplier digit, which is the sign digit, in the multiplier-quotient counter although its presence there is not significant. If a minus sign is set up, it does not select any function table line. But if a decimal zero (which indicates a positive number) is set up, it selects the Z line. During the aforesaid step of multiplication, FT149 is applied to Q-G149. (See FIGURE 8d.) When the IER signal occurs, Q-G149 gates a t_{86} - t_8 signal lasting from t_{86} to t_8 of the following minor cycle. This signal is applied to Q-G147A where it prevents the Z line from inhibiting Q-G148. Thus, Q-FF121A and Q-FF121C are both reset by the next t_2 pulse. The signal from Q-G149 also passes through a two pulse delay to inhibit Q-G147E which thereby prevents Q-FF121A and Q-FF121C from being set. This delay is required because Q-FF121A is

sufficiently fast that it might remove the IER signal from Q-G149 and consequently, remove the inhibition from Q-G147E in time to pass the last part of the *t*₂ pulse through Q-G147E and reset Q-FF121A. (See FIGURES 8c and 8d.)

The signal which advances the program counter during a multiplication process is generated in Q-G143. (See FIGURE 8b.) The IER signal is applied to Q-G143 which, in the absence of time out, gates a *t*₁ pulse to gates G222B and G244 in the control circuits. During various steps of multiplication, the pulse passes through Q-G222B to step the program counter without setting the time out flip-flop. The pulse also passes through Q-G244 to step the program counter and set the time out flip-flop during the next to last step of multiplication, thus providing time for the function table signals for the last step of multiplication to stabilize.

The succession of digits which form the quotient in a division operation are generated from the multiplier-quotient counter and then transferred into the X-register, one by one, until the entire quotient has been obtained. Division is performed by repeated subtractions and additions of the divisor and the dividend or remainder. Each step is continued until the remainder passes through zero. The remainder is then shifted to the left and the opposite operation is initiated, until the remainder again passes through zero. Each time the remainder is shifted, the quotient in the X-register is also shifted in order that the X-register can accept the new digit from the multiplier-quotient counter at the same input point. The multiplier-quotient counter counts the number of additions or subtractions in each step excluding the last operation which causes the remainder to pass through zero. In order to obtain quotients which are always less than one, the dividend must always be less than the divisor.

Subtraction is performed by complementing the subtrahend and adding, ignoring the carry in the most significant digit. When a larger number is subtracted from a smaller number, the result is the complement of the difference, and there is no carry from the most significant digit.

When this condition occurs, the lack of a carry pulse from the most significant digit causes an overflow signal (abbreviated as OF) to be sent from the algebraic adder to the multiplier-quotient counter, where the divisor signal (OR) is generated. (The OR signal is the counterpart of the IER signal.) The OR signal terminates the step, shifts the contents of the A-register and X-register one place to the left and transfers the digit set up in the multiplier-quotient counter to the X-register where the quotient is built up.

During the next step the divisor is added to the complement of the remainder in the A-register until an overflow signal occurs, this time, caused by the presence of a carry in the most significant digit position. The multiplier-quotient counter counts the number of additions, but the backward read gates are used, and when the OR signal transfers the quotient digit from the multiplier quotient counter to the X-register, the nine's complement of the number of additions is sent.

During the first step of the division operation (D₁), FT138 opens Q-G138A and a *t*₁ pulse passes through to set Q-FF124. (See FIGURE 8b.) The set output of Q-FF124 passes through an amplifier and clears the four stage binary counter to decimal zero, in preparation of the first subtraction routine. Q-FF124 is then reset by a *t*₈ pulse.

FT138 also alerts Q-G138B and, after a time out inhibition is removed, gates a *t*₁ pulse to clear Q-BC120 to "one." Q-BC120 (see FIGURE 8b) remembers whether an addition or subtraction routine is taking place. The one output of this counter passes through an amplifier and opens the forward read gates (Q-G180A-Q-G180H), (see FIGURES 8a and 8c), which transfer the pulse combination in the multiplier-quotient counter directly into

the multiplier-quotient function table without complementing it. The "one" output of this counter is also supplied through three amplifiers to Q-G145B (see FIGURE 8a). This gate is opened by FT145 during the third through fourteenth steps of division, except when the time out or OR inhibitions are present. The "one" output of this counter passes through Q-G145B, to become the S1X signal. (See FIGURE 8a). This S1X signal is sent to the adder where it causes the incoming divisor to be complemented and, therefore, subtracted from the remainder. When the S1X signal is not present, the complementer is inoperative and, therefore, an addition is performed.

At the end of each addition or subtraction routine, the OR signal is supplied to a gate Q-G142 (see FIGURE 8b) which, in the absence of time out gates a *t*₁ pulse. The pulse from Q-G142 sets Q-FF124 in order to clear the multiplier-quotient counter to zero in preparation for the following steps; it then advances Q-BC120 to its opposite state; and finally this pulse from Q-G142 is buffered together with the output of Q-G143 in order to step the program counter through Q-G222B or Q-G244 in the control circuits.

The overflow signal from the adder (produced during division) passes through a pulse spreader network (see FIGURE 8d) constituted by Q-FF122 and Q-CG117A and Q-CG117B and a two pulse delay line to set Q-FF121B and Q-FF121C. Q-FF121B generates the OR signals and Q-FF121C generates the IER, OR signals. The overflow signal is also tapped from the two pulse delay line and is applied to Q-G148, where it inhibits the *t*₂ pulse which normally would have reset Q-FF121B and Q-121C. (See FIGURE 8c.)

The signal which advances the multiplier-quotient counter in order to count the number of additions or subtractions is generated in Q-G145D (see FIGURE 8d), which is opened through the third through fourteenth steps of division by FT145. Q-G145D is inhibited by the time out signal, the OR signal and the overflow signal, which passes from the output of the delay line driver through two amplifiers to Q-G145D. The OR signal, which is removed by a *t*₂ pulse and the time out signal which is removed by a *t*₁ pulse, prevent the *t*₁ sampling pulse from passing through Q-G145D during the first minor cycle of a step in division. This gate, therefore, counts each addition or subtraction after it occurs, but it is prevented by the overflow signal from counting the addition or subtraction which causes overflow. The overflow signal is a TO pulse but because it passes through a pulse spreader network (and, therefore, is a broader pulse) it can still inhibit Q-G145D at *t*₁.

The pulse combination in the multiplier-quotient counter is converted into a serial dynamic pulse train by successively sampling the five gates Q-G116A-Q-G116E. (See FIGURE 8a.) It is then transferred to the X-register during the OR minor cycle. Each of these gates is sampled at the time shown in Table 2.

TABLE 2

Gate	Digit	Sampling Pulse
Q-G116E.....	2 ⁰ Least Significant.....	<i>p</i> ₈
Q-G116D.....	2 ¹ Next Least Significant.....	<i>p</i> ₉
Q-G116C.....	2 ² Next Least Significant.....	<i>p</i> ₁₀
Q-G116B.....	2 ³ Next Least Significant.....	<i>p</i> ₁₁
	Zone.....	
	Zone.....	
Q-G116A.....	Check Pulse.....	<i>p</i> ₁₄

When a "zero" line of one of the four input pairs to the multiplier-quotient counter function table is selected, it applies an inhibition to one of these gates (excluding Q-G116A) and prevents the passage of a pulse in that position. When a "one" line is selected, the inhibition is absent and the corresponding pulse passes through. In the multiplier-quotient function table, all pulse combinations which require a check pulse are decoded and their

output lines are buffed together to open Q-G116A which generates the check pulse.

The sampling pulses for the gates listed above are generated in the multiplier-quotient counter distributor line. A t5 (p7) pulse is fed into the distributor line which is tapped at intervals to provide appropriately timed sampling pulses.

The outputs of these gates are buffed together and passed through a PFR and a cathode follower to the X-register. Every successive combination of the multiplier-quotient counter, or the complement of this combination, is composed into a pulse train in these gates, but only that pulse train is admitted to the X-register which occurs during the OR cycle. The input gate to the X-register, X-G137, is controlled by the OR signal.

The method of division that is used requires that the divisor be larger than the dividend; if it is not, the third step of the subtraction routine requires ten or more subtractions before a carry occurs to generate the OR signal. If the OR signal occurred in such a case, it would transfer an incorrect quotient digit into the X-register. Such an improper division is prevented by Q-G118 (see FIGURE 8a) which is alerted by an amplified signal from the "one" output of the binary counter Q-BC120, and opened by an amplified signal from the "nine" line of the multiplier-quotient counter function table. Q-G118 is sampled by every pulse that advances the multiplier-quotient counter, and if there is a pulse to advance the multiplier-quotient counter the tenth time during a subtraction routine, the pulse passes through Q-G118 as the multiplier-quotient counter carry output. During the third through fourteenth steps of division, the FT145 opens Q-G145A (see FIGURE 8a) to send the carry output pulse through an amplifier and a cathode follower as the improper division signal to the control circuits where it terminates the instruction by restoring the flip-flop Q-FF204 and generating an ending pulse (EP). The signal from Q-G145A also passes through a cathode follower as the improper division signal to the algebraic adder, where it sets the overflow flip-flop AA-FF705 and initiates a special overflow routine by transferring control temporarily to memory location 000.

During the periodic memory check or a memory clear operation, the multiplier-quotient counter counts the number of words checked or cleared in each memory tank, then generates an MQCm signal which sets up the address of the next tank. To insure that each ten word tank is completely checked or cleared, including the space between words, the multiplier-quotient counter counts thirteen words before generating this signal.

During the first step of the periodic memory check, FT138 opens Q-G138B (see FIGURE 8b) in order to clear Q-BC120 to "one"; Q-BC120 then opens the forward read gates and alerts Q-G118. The generation of the SIX signal is trivial in this case. FT194 inhibits Q-G138A in order to prevent Q-FF124 from clearing the multiplier-quotient counter to decimal zero. Instead, FT194 is buffed together with FT112 and the IER signal to open Q-G112B and Q-G112D. The signal from Q-G112B sets Q-FF125 and clears the multiplier-quotient counter to binary zero. The signal from Q-G112D is trivial in this case.

During the second step of periodic memory check, FT127 opens Q-G127A (see FIGURE 8d) which is inhibited by a time out signal. Each minor cycle a t1 pulse passes through Q-G127A to advance the multiplier-quotient counter and to sample Q-G118 (see FIGURE 8a). Since the multiplier-quotient counter is cleared to binary zero initially, twelve advancing pulses are required before the "nine" line in the multiplier-quotient counter is selected and opens Q-G118. The thirteenth advancing pulse passes through Q-G118 as the carry output. FT127 opens Q-G127B and the carry output pulse passes through Q-G127B to set Q-FF125, (see FIGURE 8b) clearing the multiplier-quotient counter to binary zero once more.

The output of Q-G127B also passes through a cathode follower to the control circuits as the MQCm signal, which clears the static register, sets up the static register the new memory address, and sets the time out flip-flop. The MQCm signal also becomes the MQ-13 signal which generates the address of the next memory tank by adding ten to the number in the control register. (A more complete discussion of the periodic memory check and memory clear operations is described in copending application S.N. 279,710.)

The A-Register

The A-register is a one word mercury delay line type register which is duplicated in the arithmetic circuit. It is the principal arithmetic register used in the arithmetic circuit. The A-register is used during addition, subtraction, multiplication, division and shifting. The A-register and the algebraic adder are closely associated functionally. A word can enter the A-register from the high speed bus amplifier either directly or through the algebraic adder. The A-register recirculation loop can be altered so that an A register word circulates through the algebraic adder. (The adder is treated more fully in a following section.)

Because the transit time for propagation of an electric effect through, for example, a wire, is too short to realize any practical or realizable storage capacity, other devices for delaying the passage of an electrical effect have been sought. There are several known methods by which the propagation of an electrical effect may be retarded. One of these is to convert the electrical effects into acoustical patterns and thus make use of the much slower rate of propagation to this end. A mercury tank, having transducing crystals at each end is typical of this type of storage. The acoustic propagation through the mercury between the transmitting and receiving crystals is exactly analogous to the acoustic transmission described above. All of the delay lines used in the arithmetic registers are of this type and utilize the mercury delay line. The mercury delay line for the A-register is indicated on FIGURES 12a and 12c by the Main Delay Group, FIGURES 12a to 12d being the block diagram of the A-register. The signal circulating around the closed loop enters the Main Delay Group through an electrical delay (D) and then goes to a pulse former and reshaper (abbreviated as PFR). The pulse former is a device which supplies the energy of circulation to the system. Passage of pulses through any of the elements such as gates or delays causes deterioration of the pulses. The proper shape and timing of pulses is dependent upon the PFR's which are introduced at many points throughout the computer. The signal leaving the pulse former enters first a small mercury line delay and after emerging therefrom, enters the main mercury line wherein the pulse is converted into an acoustic signal by an appropriate transducer. The acoustic signal then travels to a second transducer which converts it into an electrical signal and applies the electrical signal to the intermediate frequency amplifier detector (IFAD). This pulse is then supplied to another pulse former and supplied through various delays back to the entrance gate in the recirculation loop.

The A-register is shown in FIGURES 12a-12d. The main recirculation loop is shown in a heavy line. Words enter the A-register from the high speed bus amplifier through A-G105 (FIGURE 12c). As mentioned above, the high speed bus amplifier, which is more clearly illustrated and described in the copending application S.N. 279,710, is a switching central through which information is passed from the memory, and to and from the various registers. This path is shown at the lower right side of the main recirculation loop. A-G105 is opened either by FT105 or by an extraction signal (E1-) unless this gate is inhibited by a time out signal. At this same junction where this input line meets the recirculation loop, the A-register receives sign digits from the comparator and it receives the number 000 000 000 005 during initial clear.

The latter number is inserted into the A-register recirculation loop, through gate A-G115, during initial clear to prevent spurious signals from being generated in the recirculation loop after the A-register has been cleared.

Words from the algebraic adder enter the A-register recirculation loop through A-G109E (FIGURE 12c). The least significant digit of the word in the A-register can be transferred to the X-register during the IER stage in multiplication through a connection shown just prior to A-G124 in the main path of circulation. (This IER stage is described in more detail in the multiplier-quotient counter description.) A-G124 (FIGURE 12c) is the delete gate which deletes any digits which have been shifted during the shifting operation into the space between words. The contents of the A-register and the duplicated A-register are compared continuously in the checking circuits. The connection to the checking circuits (CKA) is shown in the upper left corner of the main recirculation path (see FIGURE 12a).

A-G100 is output gate to the high speed bus amplifier and is connected to the second 7-pulse delay. (See FIGURE 12a.) There is a connection from the A-register to the comparator just before the third 7-pulse delay.

Any signal on A-G101B, (FIGURE 12a) shown at the left of the main loop, inhibits this gate and interrupts circulation therethrough. FT101 inhibits A-G101B either to clear the A-register or to close the normal path for shift operations. FT102 inhibits A-G101B to clear the A-register during the C instruction. The extract signals from the F-register (E2) inhibit A-G101B at the same time that the extract signal opens the A-register input gate A-G105 during the extraction operation. A-G101B is also inhibited by the FT170 through A-G170 (FIGURE 12a) during shift instructions (0n and -n) for the period p7-p83. However, A-G170 closes during the sign digit position (p84-p90) so that A-G101B is opened to pass the sign digit without shifting. The IER and OR signals also inhibit A-G101B through A-G101A during multiplication and division.

Any word circulating in the A-register may be shifted one computer digit per circulation time by altering the total delay around the loop by one computer digit time. If the word is to be shifted to the right (equal to dividing by ten) then a seven pulse delay section is removed from one minor cycle. If the word is to be shifted to the left (multiplying by ten) then a seven pulse delay must be added to the normal path. The A-register contains, therefore, three different paths: (1) normal, (2) seven pulse times shorter than normal and (3) seven pulse times longer than normal.

For either shift operation, FT101 or the IER or OR signal from the multiplier-quotient counter inhibits A-G101B (FIGURE 12a) in the normal circulation path. For a right shift, the word passes through A-G106A; for a left shift, the word is passed through A-G103 (FIGURE 12a).

Certain operations shift all digits but the sign digit of the word. Such a shift is called an incomplete word shift. In incomplete word shifts, the shifted portion of the word passes through A-G104 (FIGURE 12a) (left shift, 0nm instruction), and the sign digit passes through A-G101B. During this type of shift operation A-G101B is inhibited and the shift path remains open until the sign digit appears at A-G101B, which then opens, closing the shift path.

The junction between the main recirculation loop and three of the shift paths appears (see FIGURE 12a) along the lower left section of the main loop. From this junction the word passes through a normally conducting amplifier and a buffer to another junction point. Decimal zeros (indicated as Z's) are inserted in the A-register at this junction during certain computer instructions. (The Z signal is supplied from the cycling unit and appears in the A-register as shown in FIGURE 12b.) From this junction point the word passes through an amplifier to another junction point located in the center of the lower

section of the main circulation loop. (See FIGURE 12c.) At this junction point a word may leave the main recirculation loop if the word is to circulate through the adder. The word that continues circulating in the A-register passes through A-G109C and joins with the input from the comparator, with the initial clear digit input, and with the input from the high speed bus amplifier (FIG. 12c).

We have said that decimal zeros are inserted in the A-register during certain computer operations. Such decimal insertions are required to fill the digit spaces left vacant by word shifting. The gating system for these Z's is shown on the A-register block diagram in the left center section. (See FIGURE 12b.) A-G171 supplies Z's during the left shift instruction; A-G106B and A-G107B supply Z's during the right shift instruction. A-G102A and A-G108 supply Z's during the respective C instruction, and the K and multiplication instructions. A-G171 is alerted by either FT171 or by the OR signal. When a least significant digit signal is also present, A-G171 gates a Z into the A-register. This least significant digit signal appears at A-G171 during the time $t(9-15)$. A Z entering the A-register from A-G171 at that time fills the vacant least significant digit space in the A-register word after the word has been shifted left. A-G171 is inhibited during time out by the time out signal.

A-G106B (FIGURE 12b) is alerted either by FT106 or by the IER signal. When either signal is present, A-G106B gates a Z when a sign gating signal is also present. The sign gate signal appears at A-G106B during the time $t(86-1)$. A Z entering the A-register through A-G106B fills the vacant sign position space after the word has been shifted right. The vacant sign position can also be filled by a sign gated from the comparator during which operation FT161 inhibits A-G106B. A-G106B is inhibited by the TO+ signal.

A-G107B gates a Z into the most significant digit position left vacant when the word in the A-register has been shifted to the right; this gate is controlled by FT107 and is inhibited during time out.

Sign digits gated to the A-register by the comparator arrive at the A-register through an amplifier and a buffer. The same entrance point in the A register loop is used during initial clear. During initial clear, A-G115 passes the word (000 000 000 005) into the A-register. The A-register input from the comparator is shown at the same point as the direct input from the high speed bus amplifier near the right center of the block diagram. (See FIGURE 12c.) Sign digits gated to the A-register by the comparator arrive at this same point.

In order to perform addition, subtraction, multiplication or division, the algebraic adder is switched in the recirculation path of the A-register. When so connected, the A-register becomes an accumulator since any words transferred to it are added to the word already in the A-register. As is shown on FIG. 12d the algebraic adder has two inputs, a minuend input and a subtrahend input. The minuend input is switched into the circulation path of the A-register by gate A-G109B. Other signals to be applied to the minuend input of the algebraic adder are shown in FIG. 12b and originate in the control counter, applied through gate A-G212A; from the control register, applied through gate A-G230A; and from the cycling unit, the number 000, 000, 000, 005, which is the round-off number. To the subtrahend input of the algebraic adder signals from the high speed bus amplifier may be applied through gate A-G109A and from the L register through gate A-G110A. In addition, numbers originating in the cycling unit, which may be used in the extract instruction and similar operations, are applied through appropriate gates shown on FIG. 12d. Also applied to the subtrahend input of the algebraic adder through gates shown on FIG. 12d are control signals such as time-out and time selection. As shown in FIG. 12d there is a

single output from the algebraic adder, and that output may be applied through gates A-109E (FIG. 12c) or to the control register and the control counter counter (FIG. 12d). The appropriate inputs to the algebraic adder from the control counter and control register and the appropriate inputs to the control register and control counter from the algebraic adder are illustrated more clearly and described in the copending application S.N. 279,710.

The delay encountered in the algebraic adder is eight pulse times. Therefore, the points in the A-register circulation path which connect the algebraic adder are separated timewise by an eight pulse delay. The substitution of the algebraic adder for the eight pulse delay is controlled by a group of gates labelled A-G109B, A-G109C and A-G109E. A-G109B (FIGURE 12c) opens the A-register loop to the minuend input; A-G109C (FIGURE 12c) closes the normal path to clear the old word from the register, and A-G109E (FIGURE 12c) passes the total back into the A-register loop.

A-G109F passes a p4 (t14) to set A-FF101 (FIG. 12c). This flip-flop holds A-G109E open until p2 (t12) of the next minor cycle, since the function table signals are synchronized with beginning and ending of the minor cycles. Since there is a delay in the algebraic adder, the sum is still passing from the algebraic adder into the A-register when the minor cycle ends.

The signal which operates the three switching gates A-G109B, A-G109C and A-G109E, as well as operating A-G109 is generated by either A-G109D or A-G113. A-G109D opens in the presence of FT109 except during time out, the space between words, and the IER or OR signal. A-G113 opens in the presence of FT113 except during time out and the space between words. The delete signal on A-G109D and A-G113 is required when shifting occurs with addition, since the normal delete gate A-G124 is located after the adder connection on the A-register loop. (See FIGURE 12c.)

Concurrently, with FT109, A-G109A opens except during time out to admit a word from the high speed bus amplifier. Thus the 109 gate system, when operated by FT109, switches the A-register and the high speed bus amplifier to the adder while FT113 switches only the A-register to the adder.

Output paths lead from the A-register to the X-register, to the high speed bus amplifier and to the duplicated A-register (for comparison purposes), and to the comparator. These output paths are shown along the top of the A-register block diagram. (See FIGURES 12a and 12c.) The output path to the X-register passes through a cathode follower (FIGURE 12c). This path is controlled by X-G114 in the X-register. X-G114 is alerted by the IER and most significant digit signals and is inhibited by a time out signal. During various steps of multiplication, X-G114 opens to transfer the least significant digit in the A-register to the most significant digit position in the X-register.

The output path to the high speed bus amplifier starts at a tap on the seven pulse delay line network (FIGURE 12a). The output connection is made so that a pulse appears at the tap six pulse times after the pulse enters the delay network. Therefore, the seven pulse delay includes the usual compensating delay Dc. A-G100 controls the A-register output to the high speed bus amplifier for transferring contents of the A-register to the main memory, or to the L-register or to the F-register or the output synchronizer register and is opened by FT100.

The A-register output path to the comparator starts at a tap near the beginning of the first seven pulse time delay network in the left shift path. (See FIGURE 12a.) Since the output connection comes before the left shift gates, A-G103 and A-G104, the path to the comparator is always supplied with the contents of the A-register. This gate leads to CP-G151A in the comparator.

Associated with the A-register and used by both the

A-register and the algebraic adder (see FIGURE 12c) are a number of input and output paths.

The inputs from the control counter and the control register are controlled by respective gates, A-G212A and A-G230A (FIGURE 12c). A-G212A is alerted by FT212 and the time selector signal and is inhibited by the overflow signal. (The overflow signal is discussed in the description of the algebraic adder.) A-G212A modifies the control counter recirculation loop, so that, during the β cycle, the contents of this recirculation loop can be circulated once through the algebraic adder. A-G230A is alerted by FT230 and is inhibited by the time out signal. (This gate is used during the tape instructions and during periodic memory check.) The outputs of A-G212A or A-G230A are buffed together with the line by which the A-register contents from A-G109B can enter the minuend input of the adder. A-G109B is alerted by either A-G109D or A-G113.

Another input to the minuend input gate of the algebraic adder is controlled by A-G111 which passes the round-off number 000 000 000 005 into the algebraic adder during the last step in division. This gate is opened by FT111 and is inhibited during the time out (FIGURE 12c).

From the minuend input of the algebraic adder, a cathode follower (see FIGURE 12d) leads to the odd-even checking circuits.

The subtrahend input of the adder is supplied by a gating system composed of A-G109A, A-G110A, A-G110B, A-G112A, A-G212D, A-G232A, A-G233A and A-G242B (FIGURES 12b and 12d).

A-G109A is alerted by FT109 and is inhibited by the time out signal. This gate admits signals from the high speed bus amplifier into the subtrahend input of the algebraic adder (FIGURE 12b).

A-G112A is used during multiplication. It is opened by FT112 and is inhibited by the time out signal. When opened, A-G112A passes the round-off correction 050 000 000 000 into the algebraic adder (FIGURE 12b).

A-G110A and A-G110B pass the absolute value of the L-register contents into the algebraic adder during each of the first three steps of multiplication. A-G110A is alerted by FT110 and is inhibited by the time out and sign gate signals. A-G110A passes the entire L-register word except the sign digit which is deleted by the sign gating signal into the A-register. A-G110B supplies Z for the sign position. This gate is alerted by the FT110 signal and the sign gating signal and is inhibited by the time out signal (FIGURE 12d).

A-G212D is alerted by the same signal as A-G212A. When the contents of the control counter enter the algebraic adder minuend input by way of A-G212A, A-G212D passes the number 000 000 000 001 to the algebraic adder input. By this arrangement, the number in the control counter is increased by unity in preparation for the next instruction sequence. (The operation of the control counter is described in more detail in copending application S.N. 279,710.)

A-G232A, A-G233A and A-G242B are used in conjunction with A-G230A when the control register contents are circulated through the algebraic adder (FIGURE 12d). This occurs during transfer between the main memory and the input-output system, during periodic memory check and during memory clear. The control register contents entering the algebraic adder are unchanged if A-G242B passes decimal zeros into the algebraic adder subtrahend input. When the control register number is to be increased by ten, A-G232A is opened by its corresponding function table signal, thus either passing the number 000 000 000 010 into the algebraic adder subtrahend input in order to add ten to the right hand instruction, or passing the number 000 010 000 000 to add ten to the left hand instruction.

The subtrahend input to the adder like the minuend input arrives at the algebraic adder by way of a com-

compensating delay network and is connected by a cathode follower to the odd-even checking circuits.

The X-Register

The X-register is a one word mercury delay line type register, the block diagram of which is shown in FIGURE 14. The X-register is duplicated. The X-register is used to store the multiplier during multiplication; it stores the quotient during division; it stores the least significant digit portion of the product after twenty-two place multiplication; it receives and stores words transferred from the memory by the various computer instructions as explained in more detail in copending application S.N. 279,710.

The recirculation loop (see FIGURE 14) is shown with a heavy line. Several input gates to the X-register from the high speed bus amplifier, from the A-register and from the comparator, are shown in the right section of this drawing. The several output gates to the high speed bus amplifier and to the input checking circuit are shown along the top of the drawing and the output to the comparator is shown at the right side of FIGURE 14 within the recirculation loop. Interconnections between the X-register and the multiplier-quotient counter are shown at the left. X-G128 inserts at (79-85) during initial clear to insure that spurious signals are not developed in the recirculation loop of the X-register when this register is cleared.

The input and output connections to the X-register are connected with the appropriate inputs and outputs of the other circuits. For example, in the lower left hand corner of FIG. 14, the X-G137 is shown connecting to the input of the X-register the digit from the multiplier quotient counter. The input to X-G137 is connected to the output of the multiplier quotient counter shown in the upper left hand portion of FIG. 8a. Also, the output of the X-register to the multiplier quotient counter is shown as a tap on a seven pulse delay at the lower right hand portion of FIG. 14. This output from the tap of the seven pulse delay is connected to the input to Q-G12C shown in the lower left hand portion of FIG. 8b of the multiplier-quotient counter. Also, the least significant digit from the A-register is shown in FIG. 14 at the upper left hand portion connected into X-G114. The output from the A-register, which is connected to X-G114, is shown in FIG. 12c, at the upper portion thereof, connected through a cathode follower from the main recirculation path of the register. An input to the X-register, connecting in the sign from the comparator, is shown in FIG. 14 in the left hand portion thereof near the quarter-adder 152. The sign, which is applied to this input, originates in the comparator and is illustrated in the lower right hand portion of FIG. 6d. The output from the X-register to the comparator is taken from a tap of a compensating delay in the recirculation path, shown on the left hand side of FIG. 14. This signal is applied to C-G152D of the comparator and is shown in FIG. 6b. Thus, by referring from the FIG. 14 of the X-register to the appropriate figures of the other elements of the system, the direct connections among the elements of the system may be readily followed.

One output from the high speed bus amplifier passes through gate X-G126. This gate is opened by FT126 and is inhibited by the time out signal. This input path is open during the A1, B, L, M1 and P1 instructions.

The other input from the high speed bus amplifier passes through X-G153B and a quarter adder, X-Q152. This input is used during the S1 and N1 instructions. X-G153A and X-G153B are controlled by FT153 and the time selector signal. When these gates are open, the sign of the word entering the X-register is changed by the quarter adder.

A plus sign is represented by a 1 00 0011 and a minus sign by 0 00 0010. If either sign representation is applied to a quarter adder which, in turn, is supplied at its other input with a pulse in the two extreme positions, each sign will be replaced by the other. Since a quarter adder

possesses no carry over, the two "additions" are as follows:

$$\begin{array}{r} 1\ 00\ 0011 \\ 1\ 00\ 0001 \\ \hline 0\ 00\ 0010 \end{array} \text{ and } \begin{array}{r} 0\ 00\ 0010 \\ 1\ 00\ 0001 \\ \hline 1\ 00\ 0011 \end{array}$$

X-G153A is supplied with $p(85,91)=t(86,1)$ which are the pulses in the two extreme positions and which effect the change in the sign of the word entering the X-register through X-G153B.

The sign of the product or quotient is received from CP-G161A and CP-G161B in the comparator (see FIGURE 14) during the appropriate stages of multiplication and division. The sign digit enters just after the sign changing quarter adder X-Q152.

Digits may be transferred from the A-register to the X-register without entering the high speed bus. The digit from the A-register is admitted to the X-register through gate X-G114. This gate is controlled by the IER signal and by the most significant digit signal from the cycling unit. X-G114 is inhibited by the time-out signal.

This path is used during multiplication to transfer the least significant digit of each partial product formed in the A-register into the X-register. This digit is shifted into the space between words in the A-register, but before it is deleted in the A-register, it is transferred through X-G114 to the X-register. The point of entry to the X-register is two decimal digits earlier time-wise than the point of departure from the A-register so that the digit is shifted time-wise through the sign digit position in the X-register to the most significant digit position in the X-register. Thus the least significant digit of each partial product in the A-register is transferred to the X-register to become the most significant digit therein. Since the X-register and the A-register both shift digits during multiplication, the digits transferred through X-G114 will move to successively less significant positions.

The left shift path consists of an amplifier, an electric delay line driver, a seven pulse time delay network, a pulse former and reshaper, an amplifier and a gate X-G122 (see FIGURE 14). The right shift path consists of an amplifier and X-G123. The main recirculation path is through X-G121 which is normally open. Whenever the word in the X-register is to be shifted, X-G121 is inhibited and either X-G122 or X-G123 is opened. A left shift is executed during various steps of division when the OR signal opens X-GG122 and adds a seven pulse delay to the loop. The right shift is executed during the multiplication instructions when the IER signal is present and during both multiplication and division when FT123 is present. The IER signal and FT123 are buffed together to open X-G123 to provide the shorter path.

The IER signal, the OR signal and FT120 (which is present in conjunction with FT123 during any right shift operation) are buffed together to inhibit X-G121 and to close the normal path. Before inhibiting X-G121, these signals pass through a gate X-G120 which is inhibited by a time out signal. The normal path through X-G121, therefore, is not closed during time out. The shift gate X-G122 and X-G123 are inhibited by the time out signal so that no shift can occur during time out.

FT120 is present (but not FT123 during the A1, B, L and S1 instructions and the first step of multiplication) and inhibits X-G121 in order to clear the X-register before accepting a new word from the memory during each of these transfers.

Whenever a word in the X-register is shifted, one or more of the extreme digits, depending upon the direction of shift, moves into the space between words. To insure that the space between words is kept clear of signals, a delete signal is applied to X-G121, X-G122 and X-G123 which inhibits each of these gates during $t(0-6)$.

The path leading to the multiplier-quotient counter is connected to the X-register left shift path. The path to the multiplier-quotient counter starts at a tap on the seven

pulse time delay network and continues through an amplifier to the multiplier-quotient counter. All signals in the X-register pass into the seven pulse delay even though they may not pass through X-G122.

The path from the multiplier-quotient counter starts at Q-G116A, Q-G116B, Q-G116C, Q-G116D and Q-G116E in the multiplier-quotient counter. The path enters the X-register through an amplifier, gate X-G137, and a buffer into the main path. X-G137 is controlled by the OR signal and is inhibited by the time-out signal.

The X-register output paths appear along the top of the block diagram of FIGURE 14. The path through cathode follower to the checking circuits is always open to permit continuous comparison of the contents of the duplicated X-registers. The output paths of the high speed bus amplifier includes a cathode follower, an amplifier and a gate X-G125, which is controlled by FT125. This output is used during A2, S2, X, D15 and J instructions.

The L-Register

The L-register is a one word mercury delay line type register. It holds the multiplicand during multiplication and holds the divisor during division. When the comparator is testing two words for equality, the L-register holds the standard against which a word in the A-register is compared. The L-register is duplicated.

FIGURE 16 is the block diagram of the L-register. The recirculation loop is shown with a heavy line. The word enters from the high speed bus amplifier to input gate L-G185A.

The L-register may be initially cleared by the initial clear signal (IC) which is supplied from another portion of the computer. One initial clear signal (IC1) closes the clear gate L-G186, stopping the recirculation of all of the register contents until this signal is removed. At this point, another initial clear signal (IC2) opens the initial clear input gate G189 to permit the entrance of a set of pulses $t(79-85)$. The reason that such a set of pulses are inserted into the L-register is to allow the recirculation loop to continue circulating some pulses through the circulation line after the register has been cleared in order to prevent the generation of spurious signals within the register.

There are three L-register output paths. One output is through a parallel gating system composed of gate L-G187, L-G188A and L-G188B. All three gates enter the contents of the L-register into the high speed bus amplifier. L-G187 is opened by an FT187 during the comparison operation when words are tested for equality or inequality. When L-G187 is open, the word in the L-register travels to the comparator where the contents from registers A and L are subjected to a comparison of either magnitudes or algebraic signs. Since the input to the L-register and the outputs from the L-register all take place through the high speed bus amplifier, reference is made to the copending application S.N. 279,710 for a more detailed discussion of these input and output connections. The inputs and outputs of the L-register will not be further discussed herein.

L-G188A and L-G188B are used during division and multiplication operations. During the minor cycle when these gates operate, the multiplier-quotient counter must supply a <3 signal and must not transmit an IER or an OR+ signal to the gates. (These <3, IER and OR+ signals are described in the multiplier-quotient counter discussion.) A sign gate signal (abbreviated as SG) on L-G188A deletes the entire sign digit by inhibiting that gate during the sign digit time interval. Simultaneously, another SG opens L-G188B to insert a decimal zero (zero in the excess three binary system) into the sign digit position. FT188 is present on both L-G188A and L-G188B during these operations.

Another output from the L-register is to the checking circuits. The checking circuits continuously compare

the contents of the duplicated L-registers to determine whether or not the contents are identical.

Still another output from the L-register is through a tap on the compensating delay network (Dc) shown in FIGURE 16. A word leaving the L-register via this path passes to the algebraic adder or to the comparator during the multiplication or division operations. When a word is read into the L-register FT185 opens L-G185B and the input gate L-G185A. L-G185B inhibits the clear gate L-G186 thereby clearing the L-register.

The F-Register

The F-register is a one word mercury delay line type register. The F-register is used both in the extraction and multiplication operations. The F-register is duplicated.

The extraction instruction places one or more digits in one word with the correspondingly located digits in another word according to the digits of an extractor word. The F-register holds the extractor word that controls the extraction process.

During multiplication, the F-register holds an operand which is three times the absolute value of the multiplicand. If any digit of the multiplier is three or greater, the quantity in the F-register is added to the partial product in the A-register.

FIGURE 18 is the block diagram of the F-register. The recirculation loop is shown with a heavy line. The F-register has two input paths and three output paths. The output through F-G194 admits $t(9-15)$ pulses during the initial clear operation. These pulses are inserted into the F-register recirculation loop during initial clear to prevent spurious signals from being generated within the loop after the F-register has been cleared. The input through F-G190A admits words from the high speed bus amplifier.

The contents of the F-register may be read out on any one of three paths. One output leads to the high speed bus amplifier, another output controls the extraction (replacement) of digits during the extraction operation and still another output feeds the checking circuits to compare the contents of the duplicated F-registers.

The output path to the high speed bus amplifier starts at the second PFR shown at the upper left corner of the block diagram. The word traveling along this path arrives at two gates F-G188C and F-G192 simultaneously. The output gate F-G188C of the F-register and the input gate A-G109A of the A-register are open whenever the F-register's contents is transferred over the high speed bus amplifier to the A-register. The other output gate F-G192 in the F-register output path also reads the F-register contents into the high speed bus amplifier. Unlike F-G188C, F-G192 is not under the control of the IER signal or of the ≥ 3 signal from the multiplier-quotient counter.

The extraction operation uses three words simultaneously; a word in the A-register, a word in the high speed bus amplifier and a word in the F-register. The word in the F-register is examined one digit at a time. For each digit in the F-register which is odd, the corresponding digit of the word in the A-register is cleared out and the corresponding digit of the word in the high speed bus amplifier is inserted into the word in the A-register as a replacement. For any even digits in the F-register nothing happens.

The extract control signal is developed in the F-register at a tap on the second compensating delay (Dc) in the F-register recirculation loop. (See FIGURE 18.) This tap is shown near the center of the lower part of the recirculation loop on the block diagram FIGURE 18. The tap is connected to F-G193. At F-G193, the least significant digit of each computer digit ($p8n$) is examined by the $p8n$ signal. During the extraction operation, FT193 is present and, when the word whose digits are to be extracted into the A-register has been located in the

memory, the TS signal is present. Therefore, the results of the $p8n$ examination are communicated to the clock gate F-G195A. For each odd digit in the F-register F-G193 opens F-G195A to gate a timing pulse to the FFR. For each even digit, no signal is developed by F-G193 and, therefore, a TP- is passed by to FFR.

The extraction signals (E1+ and E2-) control the A-register input gate A-G105 and the A-register clear gate A-G101B respectively. Both signals are present when the flip-flop register (abbreviated FFR) receives the positive timing pulse; both are absent when the flip-flop register receives the negative timing pulse. The extraction signals are, therefore, the control signals developed in the F-register by the extractor word during the time selection minor cycle when the word from the memory is available.

The output path for comparing the contents of the F-register with the duplicate F-register goes through cathode follower F-CF2 to the checking circuits.

FIGS. 20, 21 and 22 illustrate the cooperation among the components described above in detail. The connections and elements utilized during addition and subtraction are shown in FIG. 20. In these figures, emphasis is placed upon clearly setting forth the arrangement of parts and their operation, and all hardware not necessary to the description has been omitted. Only those components and the portions of those components actually used in the operation described are shown on the drawings, since the detailed structure of each unit has already been described. FIG. 20 is considered first.

The addition operation of this system adds the contents of the A register and the contents of a specific memory location which has been transferred to the X register. The comparator examines the sign position (the 12th digit) of both quantities and the relative magnitude of the two quantities. The signals developed by the CP control the process of addition in the AA. Preparatory to the actual addition, the X and A registers are cleared and the two quantities to be added are inserted therein. Gate G120 in the X register is opened and the output of this gate inhibits gate G121 to clear the old contents of the X register. At the same time, gate G126 in the X register is opened to admit the word to be added to the contents of the A register. The contents of the X register and the A register are transferred to the comparator by way of special paths shown in FIG. 20, and the CP performs its function by examining the algebraic sign positions and the magnitudes of the inputs. The S2 and the S1CP signals are developed by the CP as they are required and control the actual addition process in the algebraic adder. The contents of the A register are read out of the A register and into the algebraic adder through gate G109B and the contents of the X register are transferred to the algebraic adder through gate G125 and gate G109A. When the contents of the A and the X registers are presented to the comparator, the relative absolute magnitudes of the two words are compared by the binary subtracter, and flip-flop FF155 generates the S2CP signal, when appropriate, to control the input switching gates of the algebraic adder. In this manner, the smaller quantity is always applied through the complementor to the subtrahend input of the binary adder A and the larger quantity is always applied to the minuend input of that adder. The comparison of the signs of the two quantities contained in the X and A registers is made by the half adder HA150 and half adder HA151, and their determinations set or restore flip-flop FF152 to generate the S1CP signal when it is required. Since the addition performed by the algebraic adder is an algebraic addition, an actual subtraction must be made if one of the signs is different from the other, and the S1CP signal generated by the comparator, when it has determined that the two signs are different, conditions the complementor to complement the smaller quantity and thus achieve an algebraic addition. When the addition has been completed

by the algebraic adder in the manner described in detail above, the result is sent to the A register by means of gate G109E. A difference in position along the recirculation path of the A register at which the information is read out and the results are read in, is provided to compensate for the delay produced during passage through the algebraic adder. Thus, since there is a delay of 8 pulse times in the adder, the sum from the adder approaches G109E at a later time from that at which it left through gate G109B. As a result the sum enters the recirculation loop of the A register at a point such that the timing is the same as during a normal recirculation.

The A-instruction requires an average time of 525 mc. or 13 minor cycles. The B-instruction is the same as the A-instruction except that it provides for the simultaneous transfer of information words to both the A and the X register prior to the addition of those two words in the algebraic adder. In a like manner, the X-instruction is also similar to the A-instruction, but utilizes the information already contained in the A and the X registers, adding that information to produce a sum which is transferred to the A register while the X register retains the quantity it originally had. The S-instruction algebraically subtracts the contents of a specified memory location from the contents of the A register. This is accomplished in a manner similar to that of the A instruction except that the complementor is energized to provide a subtraction operation by the algebraic adder rather than the addition in the A-instruction. Each of these addition and subtraction instructions utilizes the portion of the system illustrated in FIG. 20.

Multiplication

FIG. 21 is a block diagram illustrating the components which are used during multiplication and the cooperation among these components. The components are illustrated in simplified form eliminating all buffers, amplifiers, gate circuits and other hardware not necessary to the particular operation being illustrated. In this manner a comparatively simplified block diagram is achieved which illustrates the manner in which the various components of the system cooperate to produce a particular operation without unduly cluttering the drawings and rendering them highly complex.

The M, N, and P-instructions all multiply the contents of the L register with the contents of a specified memory position and transfer the product of this multiplication to the A and the X registers. At the end of the multiplication operation, the A register contains the 11 most significant digits of a product preceded by a sign, and the X register contains the 11 least significant digits preceded by the same sign. In the following discussion, the M-instruction is taken as the standard and differs from the M-instruction only in that the opposite algebraic sign of the product is obtained; the P-instruction differs only in that the round-off correction is not applied to the product. These differences will be described with the particular steps in which they occur.

The multiplication process requires 15 separate steps. In step 1, the multiplier word is transferred from its memory location into the X register. At the same time, the A register is cleared to decimal zeros, and the zeros are sent to the algebraic adder along with the absolute value of the multiplicand, which has previously been placed in the I register. The sum is sent to the A register. In both step 2 and step 3, the absolute value of the multiplicand (ICAND) is again added to the contents of the A register, so that three times the multiplicand is built up in the A register. On the fourth step the contents of A are sent to the F register. In the M and N instruction a round-off correction is placed in the A register during step 4, and thereafter the A register contains the partial product as it is developed on steps 5-15. The X register initially contains the multiplier (IER). On each of steps 5 through 15, the X register supplies a new multiplier

digit to the multiplier quotient counter (MQC) and receives the LSD of the previous partial product from the A register. By this repetitive process, the product is built up in the A and the X registers. On step 3, the comparator determines the correct sign of the product and stores it. (The N instruction stores the opposite sign in the CP.) On step 14 the sign is supplied to the A and the X registers.

The separate steps are as follows:

Step 1: After the appropriate instruction has been set up, the operations of the first step begin. Gate G139 in the MQC passes a pulse which places binary counter BC120 in a state to open the backward gates. These gates are used during steps 5 to 15. During step 1, the IER is transferred from its memory location to the X register and is checked for accuracy during its transfer. In the X register, the clear gate G121 is closed to clear the contents of the register, and the input gate is opened to allow the admission of the IER during this transfer. The M and P instructions use gate G126 for applying the initial information to the X register. The N instruction uses gates G153A and B which also accomplish a reversal of sign. In the A register, the clear gate G101B is closed to clear the contents of the register and a special input gate G198 is opened to admit decimal zeros to the register. At the same time, the algebraic adder is switched into the recirculation loop of the A register so that the adder output, which, in this case, is the sum of the contents of rL and rA , enters the A register. The algebraic adder is inserted in the recirculation path of the A register by opening gates G109B and G109E, allowing information to pass from gate G109B into the adder and from the adder through gate G109E back into the A register. The input to the adder from the L register is through a special path which utilizes gate G110A. Also during the first step, decimal zeros are inserted into the sign positions of the contents of both the A and the L registers so that in multiplication the adder always receives two inputs which have zeros in their sign positions. During step number 2, the contents of rA is added to the contents of rL , and the sum is sent to the A register. The AA is inserted in a recirculation path of the A register as it is done in the first step and the A register is cleared to receive the sum from the AA. Gate G110A is opened to admit the contents of RL to the AA subtrahend input. In the AA, a twelve place addition is now formed. The result is sent to the A register. Since the A register contained the multiplicand and the L register contained the multiplier, at the end of the second step the A register contained two times the multiplicand. During step number 3 the same operation is accomplished as was performed during step number 2 and in addition, the contents of the L register and of the X register are sent to the comparator to determine the algebraic sign of the product. At the end of the third step, the A register contains three times the multiplicand. In the comparator, the sign is compared and determined in the sign comparison and storage circuits and the resultant sign is stored in flip-flop FF152.

Step 4: the fourth step concludes the preparatory stages of the multiplication operation. The subsequent stages generate the final product. At the conclusion of the fourth step, the F register contains three times the multiplicand; the round-off correction has been transferred to the X register (M and N instruction only); the sign of the final product is stored in the comptator; the L register contains the multiplicand; the multiplier is stored in the X register (shifted one place to the right); and the complement of the least significant digit of the multiplier is set up in the MQC.

The contents of the A register (3XICAND) is read out of the register through gate G100 to the input of the F register G190A, and the A register is cleared by inhibiting gate G101B. When the A register is cleared, decimal zeros are admitted through gate G198, filling the recirculation loop of the register with decimal zeros.

After the quantity is read out of the A register it enters the high-speed-bus. From the high-speed-bus the word, which is three times the multiplicand, is transferred through the input gate G190A to the F register and enters the circulation path of that register. At the same time, gate G190B inhibits the clear gate G191 of the F register to clear its former contents. Thus, the result of the first three multiplication steps is transferred into the F register. While the contents of the A register is being transferred to the F register and the A register is being cleared and filled with decimal zeros, the gate G109B and gate G109E are opened to place the algebraic adder in the circulation loop of the A register.

During the M and N instructions, the round-off correction is applied to the subtrahend input of the adder through gate G112A at the same time that the decimal zeros contained in the A register are applied to the minuend input of the adder. The result, which is the round-off correction, is then transferred to the A register.

At the same time, the complement of the least significant digit of the multiplier is transferred from the X register through gate G112C and the complementing amplifier into the MQC. In addition, all of the multiplier digits are shifted one digit position to the right in the X register, thus clearing the least significant digit position. Gate G123 in the X register is opened and the clear gate G121 is closed, eliminating a seven pulse delay and causing the multiplier to circulate through the right shift path in the X register. The distributor in the MQC serves to transfer a serially arranged digit into the MQC counters 1, 2, 3, and 4 in parallel fashion. At the end of the fourth step, the clear gates of registers A, F, and X are opened, and the input gate G109A of the F register is closed.

In steps 5 to 15 the multiplicand is multiplied by the separate digits of the multiplier and the results are added in the properly shifted positions in the X and the A registers. The individual steps are identical in method as far as the multiplication process is concerned. Steps 14 and 15, which conclude the multiplication operation, perform additional operations incidental to attaching the algebraic sign to the final product.

At the end of the fifth step, the A register contains the product of the multiplicand and the least significant digit of the multiplier. This product is the result of the consecutive additions of the contents of the A register to the contents of either the F or the L register. (The F register contains three times the multiplicand and the L register contains the multiplicand.) The decision as to the selection and the number of the additions is made by the MQC which tests the IER digit for magnitude and, if the digit is not zero, develops either the greater than or equal to three signal (≥ 3) or the less than three signal (< 3). After the first test is made and the corresponding addition is made to the contents of the A register, the IER is effectively decreased by either three or one, as required, and tested again. This process is repeated until the number of additions of the ICAND made to the contents of rA is the same as the IER digit. Since the contents of rA was zero in the beginning, at the end of the opening multiplication step the A register contains the product of the ICAND and the least significant digit of the IER. When the IER is the same as the number of ICAND additions made to the contents of the A register, the contents of the A register are shifted to the right so that its least significant digit goes to the X register. The vacant digit space in the most significant digit (MSD) position of the A register is filled with a zero. The contents of the X register is also shifted to the right and the least significant digit (LSD) is thus brought into position in the MQC to control the following steps. If the IER digit is zero to begin with, the shifts in the A and X register occur immediately after the zero is set up in the MQC.

In each of the steps which follows, additions of three

times the ICAND and/or one times the ICAND are made to the shifted contents of the A register as required, and the partial product is built up in the A and the X registers. After the last digit of the IER has been multiplied, the algebraic sign, which was stored, is sent into the sign position of both the rA and the rX, and the process is complete. The A register then contains an algebraic sign and the 11 most significant digits of a 22 digit product; the X register contains the 11 least significant digits and the same algebraic sign.

Throughout the steps 5 to 13, the A register and the high speed bus are open to the algebraic adder minuend and subtrahend input respectively, except when the IER signals appear at the end of each individual multiplication step. The A register accumulates the partial product and repeatedly supplies the adder minuend input. The adder subtrahend input arrives from the high speed bus. The F and L registers supply the high speed bus with the ICAND and three times the ICAND respectively as required by the MQC.

The A register output, clear and input gating system consists of gates G109C, G109D, G109E, and G109B, and flip-flop FF101. During the IER minor cycle at the end of each step the IER signal on gate G109B prevents the operation of this gating system.

The F register contents are read out to the algebraic adder through gate G188C when the ≥ 3 signal is present when generated by the ≥ 3 gates in the MQC. The contents of the L register are read out to gate G188A when that gate is opened by the < 3 signal generated by the < 3 gates in the MQC, and when that gate is not inhibited by the IER signal which occurs at the end of each step. Since only the backward gates are used during multiplication, binary counter BC120 of the MQC is not stepped and remains in the condition it was originally placed early in the multiplication process.

When a particular combination of binary ones and zeros (a coded decimal digit) is admitted to the binary counters of the MQC, one line of a function table in the MQC is excited. When the line for zero, one or two is excited, the appropriate gates pass a signal known as the less than three signal. If some other line is excited, then the gate develops a signal known as the equal to or greater than three signal. As these signals are developed, they are also used to step the MQC counters appropriately, once when the < 3 is developed and three times when the ≥ 3 signal is present. If the binary counters excite the zero line, the IER signals are developed by the IER, OR gates denoting the end of the multiplication step.

The IER signals are responsible for the procedures which end the particular step. In the F register the output gate G188C is closed by the IER signal. Similarly, the other output gates G188A and G188B are closed by the IER signal. In the A and X registers, special paths with a digit less delay than the normal recirculation movement loop (right shift), are opened to shift the contents of the A and X registers to the right. At the same time, the paths through the normal loop are cleared. In the X register gate G123 deletes the least significant digit of the IER and the remainder of the word is passed under the influence of the IER signal. G114 is opened by the IER signal to allow the LSD from the A register to pass into the MSD of the X register. The IER and MSD signal position in the A register is filled by a decimal zero.

In addition to the final multiplication, the fifteenth step also transfers the algebraic sign of the product from the CP to the A and the X registers. Depending upon whether flip-flop FF152 in the CP is restored or set, either gate G161A or gate G161B will be opened to allow the plus or the minus sign to be read out through special paths to both the A and the X registers. The occurrence of the IER signal at the end of the last multiplication shifts the contents of both the A and the X registers. In the X register, the former space-between-words (SBW)

goes to the MSD position and leaves a vacant space available to receive the sign from the comparator. In the A register no decimal zero is gated in as occurs on the previous steps; thus, the former SBW in the A register is also available as a most significant position to receive the sign from the comparator.

It should be noted that the M, N, and P instructions each require an average time of 2150 mc. or 53 minor cycles.

The D instruction, which is illustrated in simplified block form in FIG. 22, divides the contents of a specified memory location by the contents of the L register and rounds off the quotient to eleven digits. At the end of the instruction, the A register contains the rounded quotient and the X register contains the unrounded quotient. The D instruction requires 16 separate division stages or steps. During step 1 the dividend is placed in the A register and the contents of the A register and those of the L register are compared in the comparator to determine the algebraic sign of the quotient. In addition, the MQC is prepared for the first division step. During the second division step, the sign is stored in the comparator for use during the 16th step and the dividend is shifted left one decimal digit. During the 12 steps from step 3 through step 14, the actual division process takes place. During step 15, the round-off correction is applied to the unrounded quotient in the X register and the result is sent to the A register. During the 16th step, the algebraic sign stored in the comparator is transferred to the rounded quotient in the A register and also to the unrounded quotient in the X register.

This information handling system employs a non-restoring method of division. In this method the divisor is first subtracted from the shifted dividend until an overdraft occurs. The number of subtractions, not counting the last one (the one which produced the overdraft) becomes the most significant digit of the quotient. The dividend is again shifted left and the divisor is added back until an overdraft again occurs. In this case, the nine's complement of the number of additions, again not counting the last (which one produced the overdraft), becomes the second quotient digit. This sequence of alternate subtractions and additions is continued, the dividend being shifted before each step, until 12 quotient digits have been determined. At the end a round-off correction is added and the quotient is shifted right to become a rounded 11 digit quotient. The 12th digit position receives the algebraic sign.

The MQC counts the number of additions or subtractions necessary to cause an overflow signal to be developed by the algebraic adder which actually performs the additions and subtractions. The MQC counts in only one direction (from zero to 9); however, either forward or backward readout gates may be used. By clearing the binary counters to decimal zero and counting forward when the complement readout gates are used (backward), the effect is the same as clearing the counters to 9 and counting backwardly.

Initially, the forward read-out gates are used. Thereafter, the MQC reverses the read-out gates at the end of a step, when the OR signals appear, and at the same time, reverses the operation (addition or subtraction) in the AA. When the forward read-out gates are used, subtraction is called for by the SIX signal. When the complement read-out gates are used, addition is permitted because the SIX signal is not developed. At the end of a step, the OR signal shifts the contents of the A register one place to the left and inserts the decimal zero in the vacant least significant digit position. The OR signal also shifts the contents of the X register one place to the left to make room in the least significant digit position for the quotient digit developed by the MQC.

In the first step of the D instruction gate G138 in the MQC passes a pulse to the binary counter BC120 to place the counter in condition to energize the forward gates,

which are used first. Thereafter, BC10 is stepped at the end of each operation by the OR signal, allowing a t_1 pulse to pass through gate G142 so that the counter alternately opens the backward and the forward gates. Also during the time of the first step, the dividend is read out of the memory location and into the A register. In the A register the former contents are cleared by the closing of the clear gate G101. The dividend enters the A register from the memory at gate G105. At the time the transfer to the A register occurs, the contents of the L register are transferred to the comparator and the dividend is also transferred to the comparator for the determination of the sign.

During the second step of the division operation the algebraic sign determined in the comparator is stored in the sign storage flip-flop FF152. In the A register, during this step, gate G103 is opened and gate G101 is closed to provide for the left shift of the dividend. At the same time, gate G171 is opened and a decimal zero is fed therethrough into the vacant least significant digit position. During the division steps 3 through 14, the routine of actual division by the nonrestoring method is carried out. The output of the A register is opened to the minuend input of the algebraic adder and the output of the L register is opened to the subtrahend input of the adder except when the OR signals are developed at the end of any particular division step. The input, output, and clear gating systems in the A register used during the D instruction consist of gates G101, G109B, G109E, and G109C. This system is operated as in other cases when the algebraic adder is switched into the A register recirculation group.

The algebraic adder, the MQC, the X register operate together to accumulate the quotient digits. In the initial division step, binary counter BC120 in the MQC is in the condition necessary to open the forward read-out gates, having been placed in that condition during the first step. Gate G145B then passes the S1X signal to the algebraic adder to condition the complementor for subtraction. During a subtraction routine in the algebraic adder, gate G725 is opened by the S1X signal but is inhibited by carry pulses from the binary adder. This continues until an overflow occurs, at which time no carry pulses inhibit gate G725 and a pulse is permitted to pass therethrough to gate CG117A in the MQC to become the overflow signal and pass on to the IER—OR gates to become the OR signal. In addition, the overflow signal inhibits gate G145D in the MQC to prevent it from passing a t_2 signal which steps the counters each minor cycle. At this time the particular combination of lines excited in the matrix of the MQC is excited by the number set up in the binary counters. During the first division step, the forward read-out gates are opened and the number finally set-up is the first quotient digit. The vertical matrix lines carry permissive signals to the output gates which transfer, in serial form, the pulses of the quotient digit to the X register. This is accomplished by the output pulses along the distributor which open the output gates of the MQC serially to allow the quotient digit to transfer to input gate G137 of the X register in serial form. The transfer occurs only when an OR signal opens G122 and inhibits gate G121 in the X register to provide a left shift of the information contained therein. Thus, the digits set up in the binary counter of the MQC enters the X register in the now vacant least significant digit position.

The OR signal applied to gate G103 in the A register shifts the contents of the A register left by closing gate G101. Thereby the former space-between-words which, in the shift position becomes the least significant digit, is filled by a decimal zero gated in at G171 by the OR signal. At the same time, the OR signal opens gate G142 to allow a t_1 pulse to pass to set binary counter BC120 to its other state and to clear the MQC counters to decimal zero.

During the fourth division step, operations similar to those which took place during the third division step are performed. However, in this case the algebraic adder uses gate G145C to detect overflow because there is no S1X signal available to open gate G725 and inhibit gate G145C. A carry is delivered only at the time that overflow occurs and at that time passes gate G145C to become the overflow signal for the MQC. In the MQC, the number set up in the binary counters is read out through the backward read gates, and the X register receives the complement of the number in the MQC. This digit is the second quotient digit. By repeated steps such as step number 3 and step number 4, a 12 digit quotient is assembled in the X register during division steps 3-14.

During the division step 15, the contents of the X register are sent to the high speed bus, and the A register is cleared. The X register is not cleared but the round-off correction is added to the X register and the result is sent to the A register. At the end of the 15th step the A register contains the 12 digit rounded quotient and the X register contains the 12 digit unrounded quotient. In the A register, gate G101 is closed to clear the register and at the same time gate G125 is opened in the X register so that the contents of the X register may be read-out through gate G109A to the subtrahend input of the algebraic adder. The round-off correction is admitted at the algebraic adder minuend input through gate G111. The output of the added is admitted to the A register through gate G109E.

During the 16th division step, the rounded 12 digit quotient is shifted to the right one digit and the algebraic sign is applied from the comparator. The word in the X register is also shifted only digit to the right and also receives the algebraic sign from the comparator. The shifts are accomplished in the A register by the opening of gate G106A and the closing of gate G101. In the X register, gate G123 is opened and gate G121 is closed to accomplish the right shift. The appropriate signal is read from flip-flop FF152 through gates G161A or G161B dependent upon whether the signal is plus or minus.

MAJOR COMPONENTS, SCHEMATIC CIRCUIT DIAGRAMS

The Comparator (Schematic)

The schematic drawing of the comparator is shown in FIGURES 7a through 7k. The negative going signals of 30 volt amplitude appearing on the high speed bus are communicated to the input gate CP-G152A via diode CP-D500 (FIG. 7f). CP-G152A is controlled by FT152 and the check pulse eliminator signal (CPE). FT152 is normally at +90 but under excitation for a comparison operation it falls to +60. Check pulse eliminator is normally at 60 volts except during the check pulse interval of each computer digit when it rises momentarily to +90, thus eliminating any check pulses which may appear on the high speed bus word. The output of CP-G152A is via diode CP-D501 through a common line leading to CP-V502. The input from the X-register in the form of positive going pulses are capacitively coupled into CP-V503. The output of CP-V503 is connected to CP-G152B by way of diode CP-D504. The negative going pulse from CP-V503 pass through CP-G152B provided that the output from CP-G152F is at +60 volts. In addition, a check pulse eliminator (CPE) is applied by way of diode CP-D505 to CP-G152B. The output of this gate is communicated via diode CP-D506 into a common line leading to CP-V502, which is a clock gate driver. The output of the clock gate drives a pulse forming flip-flop (FIG. 7d) composed of CP-V507 and CP-V508. This forms one input to the comparator.

A second input from the high speed bus is shown at point 509 (FIG. 7f). This input drives gate CP-G152C. This gate is controlled by function table signal 152 which is normally at +90 but during excitation for a comparison drops to +60 volts. Also applied by way of CP-D510

a check pulse eliminator (CPE) signal deletes the check pulses in the computer digits entering from the high speed but. A third signal applied to CP-G152C is FT156. This signal is applied by way of diode CP-D511 and CP-D512 to the junction point of CP-G152C. The output of this gate is buffed into a common line leading to the comparator circuits via diode CP-D513.

Another input to the comparator from the X-register is by way of CP-V514. This valve receives the positive going pulses from the X-register and applies them to gate CP-G152D. This gate is influenced by function table signal 156 and the sign gate signal SG. Either FT156 or the sign gate signal is capable of opening CP-G152D. In the absence of FT156, only the sign of the word from X is allowed to enter the comparator. One additional restriction imposed upon CP-G152D is the output of gate CP-G152E. This gate permits FT152 to drive CP-G152E and, in turn, inhibit CP-G152D except during time out. Time out signal is applied to CP-G152E by way of diodes CP-D514 and CP-D515. FT152 is supplied to CP-G152E by way of the normally conducting tube CP-V516. The output of CP-V516 is communicated by way of diode CP-D517 to CP-G512E. Also applied to CP-G152D is the check pulse eliminator signal which eliminates the check pulses from each computer digit entering from the X-register. FT152 is also applied to CP-G152F by way of normally conducting amplifier CP-V518. The output of CP-V518 is connected by way of CP-D519. The inhibition of time out is applied to CP-G152F by way of diodes CP-D520 and CP-D521. The combined signals of CP-G152F are then applied to CP-G152B by way of diode CP-D522.

Still another input to the comparator is the minus sign signal generated in the cycling unit. This signal appears at diode CP-D523. The minus sign consists simply of a p86 pulse. The minus sign normally enters via CP-G156A except in the presence of FT156 which is applied from the function table output circuits via normally conducting amplifier CP-V524. CP-V524 is for the purpose of inverting the function table signal, converting it from a permissive polarity to an inhibiting polarity. It is applied to CP-G156A by way of diode CP-D525. The outputs of CP-G152D, CP-G152C and CP-G156A are buffed together by diodes CP-D526, CP-D513 and CP-D527. The output of these three diodes is capacitively coupled into a clock gate driver CP-V528 (FIG. 7d).

A third source of input signals to the comparator is CP-G151A (FIG. 7a), which receives the signals from the A-register by way of a capacitor and is applied to CP-V530 (FIG. 7a). The negative going output signals from this tube are applied to CP-G151A through diode CP-D531. The conditions at CP-G151A are controlled by the output of CP-G151C. CP-G151C is controlled by FT151 whose polarity is reversed from a permissive signal into an inhibiting signal by action of tube CP-V532. The output of this tube is connected to the input gate CP-G151A through CP-G151C by way of diode CP-D533. CP-G151C also receives the check pulse eliminator (CPE) signal via diode CP-D534 and is inhibited during time out via CP-D535 and CP-D536. If the combined output of CP-G151C is at 60 volts, this signal is communicated to CP-G151A. If the conditions in CP-G151C are favorable, that is, FT151 is present and time out is absent, then CP-G151A is inhibited. Under this condition, the signal applied is a 90 volt signal masking any signals appearing from the A-register at the junction point of CP-G151A.

Still another input to the comparator is via CP-G151B. The signals from the L-register are applied capacitively to the input amplifier CP-V537 where the signal from the L-register is inverted. This inverted signal is applied to CP-G151B by way of diode CP-D538. To the gate CP-G151B are applied FT151 through diode CP-D539, the time out signal by way of CP-D540 and the check pulse eliminator signal (CPE) by way of CP-D541. The

combination of these three signals is applied to CP-G151B by way of CP-D542. Under favorable conditions, i.e., the presence of FT151 and the absence of time out the signal applied by way of CP-D542 is a 60 volt potential permitting the signals coming from CP-V537 to enter the comparator. During the check pulse eliminator signal, the potential on CP-D542 rises to +90 and thus masks the pulses arriving from CP-V537, thereby eliminating them. The outputs from CP-G151B are combined with the output of CP-G151A by CP-D543' and CP-D543 respectively. The combined output signal is then capacitively coupled into normally conducting amplifier CP-V544; which is a clock gate driver. The output of the clock gate driver CP-V544 is applied to a pulse forming flip-flop composed of CP-V545 and CP-V546. The output from CP-V546 is applied to half adder CP-HA150 (FIG. 7c). It is also applied through a six section delay line with taps to a binary subtractor (FIG. 7b). Into the other side of the binary subtractor, noted as minuend input, are supplied the signals generated in the input gate system CP-G152B or CP-G152A (FIG. 7f) through a pulse former consisting of CP-V508 and CP-V507 (FIG. 7d). The output of CP-V507 is applied via a delay line to the minuend input of the binary subtractor. The output from CP-V546 becomes the subtrahend input of the binary subtractor.

The effect of the binary subtractor is to obtain a signal from a flip-flop which indicates the identity of any pair of quantities applied to the two input systems of the comparator. The pulses applied to the subtrahend input are positive going pulses while those applied to the minuend input are negative going. The output from the two input amplifier valves CP-V547 and CP-V548 are each clamped between the limits -71 and -89 volts. These output signals are applied each to two gates. These gates are supplied with clock pulses, indicated by TP+ and TP-. The configuration of diodes associated with these two clock gates is such that if a signal is applied to both inputs, neither clock gate will produce an output pulse but if only one of the inputs is excited, there will be an output pulse from the clock gate to the flip-flop whose polarity will indicate which input was excited and consequently, which one was not. A typical operation might be illustrated by applying a pulse to CP-V547 and no pulse to CP-V548. Under these conditions CP-V547 will assume an anode potential of -89 volts. Similarly CP-V548 will maintain an anode potential of -89 volts. Consideration must now be given to the potentials permitted at two points 549 and 550. Point 549 will not be clamped from the upper level by -89 volts applied from both CP-V547 and CP-V548. Point 550 will be clamped from a lower limit by the minus 89 volts from CP-V547 and CP-V548. Due to the D.C. average level of the timing pulses it is now possible to say that a tp- will be gated through point 550. The tp+ normally rises from -91 to -53 volts. Due to the clamping at -89 on point 549, only approximately three volts of the positive tp could effect point 549. However, the negative timing pulse ranges from -71 to -109 volts due to the 18 volt differential, so that an 18 volt negative going pulse will be applied to CP-V555 and CP-V556 of a pulse forming flip-flop.

This may be referred to as a set pulse to flip-flop CP-FF156. A set pulse, therefore, may be considered to indicate inequality in the two inputs to the binary subtractor. Furthermore, the inequality is in favor of the subtrahend input which carried a binary one or a pulse. In converse manner, it can be shown that if a pulse is applied to the minuend input but not to the subtrahend, a positive timing pulse will be gated to CP-FF156 and will cause CP-V555 to conduct and thereby indicate inequality but this time in favor of the minuend input. If both inputs receive a pulse simultaneously, then neither tp is gated to CP-FF156 and the flip-flop is left in whatever state it was placed by the previous input combination. A reset pulse is applied to CP-FF156 by way of valve

CP-V557, a normally conducting valve which receives negative pulses from the cycling unit designated as *t5*. The output of this tube is connected to the reset side of the clock gate by way of CP-D558. In order to avoid the restrictions placed upon the *tp* inputs to the two clock gates by CP-V547 and CP-V548, an additional *tp* input is applied to the output of CP-V557 in order to sharpen the signal produced at CP-V557. This timing pulse input is by way of CP-D559. The combined action of CP-V557 and the *tp* input 559 is such as to produce a negative going signal which is buffed into the clock gate circuit by way of CP-D560 and thence to CP-FF156. The combined effect of these two inputs, the *t5* in the cycling unit and the *tp* from the timing pulse generator produce a positive going pulse which causes CP-V555 to conduct in CP-FF156. This restoring action or resetting takes place prior to any inputs to the subtrahend or minuend input of the binary subtracter. In the restored condition, CP-FF156 indicates that the subtrahend is greater than the minuend input and this assumption is made prior to any comparison. If both inputs should be identical, it will appear as if the minuend was greater. The output of CP-FF156 is obtained from CP-V555 through CP-V561. CP-V561 is normally conducting but when CP-FF156 is in restored condition, the lower anode potential on CP-V555 cuts off CP-V561 and gives a 90 volt signal out as the signal indicating that the minuend is greater than the subtrahend.

For purposes of comparing the signs of quantities entering the comparator, two half adders are used in corresponding circuits. These half adders are CP-HA151 and CP-HA150. The operation of these two circuits is identical, although the significance of each is different from that of the other, and the description of that operation will be restricted to half adder 150 (FIG. 7c). The signals appearing via CP-G152C, CP-G152D and CP-G156A (FIG. 7f) are buffed together and applied to the pulse former consisting of CP-V557 and CP-V558 (FIG. 7d). This pulse forming flip-flop is driven from a clock gate. The output from the pulse forming flip-flop is obtained from CP-V558. Turning now to the other input to CP-HA150 namely through gates CP-G151A and CP-G151B, any input pulses occurring at these two gates appear at the anode of a pulse forming flip-flop composed of CP-V545 and CP-V546 (FIG. 7a). The output pulses are obtained from the anode circuit of CP-V546, which drives a short delay line section.

As shown in FIG. 7c the two input amplifiers from CP-V557 and CP-V558 (a flip-flop) are CP-V564 and CP-V565. The input amplifiers from CP-V545 and CP-V546 (a flip-flop) is through CP-V562 and CP-V563. The operation of a half adder has been described elsewhere (see copending application S.N. 279,710) but in quick review it is as follows. The signals applied to CP-V563 and CP-V565 are undelayed from the corresponding flip-flop inputs. Connected between the anodes of CP-V563 and CP-V565 is a gating arrangement composed of diodes CP-D567 and CP-D568. When and only when both anodes of CP-V563 and CP-V565 drop to +60, the junction point between the two diodes also drops to +60 volts. This voltage change is connected via diode CP-D569 to CP-V566. This signal is referred to as the carry signal and indicates when two binary ones have been applied to both inputs of the half adder. The delayed inputs to the half adder are via CP-V562 and CP-V564. Connected between the anodes of these two valves are two diodes CP-D569' and CP-D570. These diodes serve as buffering diodes which pass a pulse appearing at either input valve into the sum line. The sum pulse appears at diode CP-D571 where a gate is formed which depresses the sum pulse if there is a carry pulse. This depression occurs via diode CP-D572. In the case when there is only one input, no signal is applied to CP-D572 to inhibit the carry gate and, therefore, the pulse appearing on either one of the two delayed input valves passes

through CP-D571 and out the sum output line via diode CP-D573. If, however, two pulses do occur, the signal appearing on diode CP-D572 suppresses the sum pulse coming from CP-V562 and CP-V564. The behavior then of the half adder is such as to produce a pulse if one and only one input is excited but produce no pulse if both inputs are excited. The output of CP-HA150 is connected to a gate CP-G156B via two valves CP-V574 and CP-V575. The output of CP-HA150 is also connected via CP-V576 to a clock gate and pulse former CP-FF150, which stores the comparison of the sign digit position of the two words applied to the comparator. By the fact that CP-FF150 is put into normal or restored condition by a *t86* pulse from the cycling unit it is of no importance that the previous pulses of the word being prepared have been effecting CP-FF150. The only essential period for CP-FF150 is that interval between *t86* and *t2* which corresponds to *p84-p91*.

Associated with the half adder CP-HA151 in the flip-flop CP-FF151, the corresponding flip-flop is CP-FF151. The outputs from these two flip-flops control CP-G172B and CP-G172D (FIG. 7j).

CP-G172B is controlled by the signal developed in CP-G172A (FIG. 7h) and appears at point 530. In addition, it is controlled by the output of flip-flop CP-FF153 (FIG. 7h) which appears on lead 581. The other control signals are the set outputs from CP-FF150 and CP-FF151, FT172 and a *p91* pulse from the cycling unit. The output applied by CP-FF151 is inhibitory while that from CP-FF150 is permissive as are FT172 and the output of CP-FF153. The signal from CP-G172A is inhibitory. The combined effect of these signals is communicated to CP-FF155. This output is in the form of a *p91* pulse which sets CP-FF155.

CP-G172D is controlled by FT172, a permissive signal via CP-V582. In addition, this gate is controlled by the restored or reset outputs of CP-FF150 and CP-FF151. Both of these signals are permissive. The output of CP-G172D is applied as an inhibitory signal to CP-G167. The input to CP-G167 is via diode CP-D583. The other control signals associated with CP-G167 are a *p91* applied from the cycling unit via diode CP-D584, a permissive signal, either by FT156 by way of valve CP-V585 or FT159 by way of CP-V586. Either signal if present, inhibits CP-G167. In addition, the output of CP-G172A is applied by way of valve CP-V587 and is permissive in nature. An additional signal is also applied to CP-G167 which is the output of CP-FF154 (FIG. 7h). This signal appears by way of CP-V588. The signals appearing on CP-V587 and CP-V588 are buffed together by diodes CP-D589 and CP-D590. Either signal is sufficient to apply the necessary permissive signal on CP-G172D provided the other signals are also favorable. The output of CP-G167 is a *p91* pulse which is applied to CP-FF155.

The third source of signals to CP-FF155 are via CP-G156C. CP-G156C is controlled by FT156 supplied by way of CP-D591 and a *p91* from the cycling unit applied via CP-D592 and finally, the output from the restored or reset side of CP-FF153 by way of CP-D593. The output of CP-G156C is buffed into the common line to CP-FF155 by way of CP-D594. The common input line to CP-FF155 is by way of valve CP-V595. This valve drives an eight section delay line for the purpose of delaying the output pulses from the three gates supplying signals to CP-FF155 for approximately two pulse times. The purpose of this delay is to prevent the generation of the signals at CP-FF155 until the proper time. The output of the delay line drives CP-V596 which, in turn, is connected to the set input of CP-V155. CP-FF155 is composed of valves CP-V597 and CP-V598. The output of CP-FF155 is the CT or additional transfer signal which is used during the Q and T instructions in order to transfer control to a new memory location. These output signals are passed via CP-V599 and CP-V600 on the one side of CP-FF155 to the control counter

and checking circuits. The other output from CP-V593 is by way of valves CP-V601 and CP-V602 (FIG. 7i). CP-V601 supplies the signal to CP-G438 and CP-G439 in the checking circuits while CP-V602 supplies the signal to CP-G160B. This signal is eventually connected to the algebraic adder as signals S2A and S2B which cause the complementer to complement the incoming signal to the subtrahend input of the algebraic adder in order to perform a subtraction. CP-G160B is controlled by FT160 applied by way of CP-D603 and a time out inhibition applied by way of CP-D604. FT160 is permissive while the time out signal is inhibitory. The output of CP-G160B is applied by way of a diode to valves CP-V605 and CP-V606 which, in turn, generate S2A and S2B respectively. CP-FF155 is restored by signals from CP-G159 which are applied to CP-V598.

One additional feature of CP-FF155 is the initial transfer control switch which permits the operator to observe whether or not a transfer of control is going to take place and if so, force the computer to ignore the transfer instruction and proceed along the original sequence of instructions. This transfer switch is shown just below CP-FF155 and applies a forcing signal to CP-FF155 which places it in whatever position the operator chooses without regard to the input signals which may have been generated by the comparator. CP-G157 and CP-G158 (FIG. 7i) compare the conditions of CP-FF150 and CP-FF151 in order to determine their likeness or unlikeness of setting and thus give an indication of the comparison of the signs of the words entering the comparator. Both gates are controlled by both outputs from these flip-flops. However, the control is such that the set output of CP-FF151 is permissive on CP-G158 while the restored output of CP-FF151 is inhibitory on CP-G157. A similar system is on CP-G158.

The signal from CP-FF150 is applied to CP-G157 and CP-G158 by way of CP-V611 and CP-V612 respectively. Adjacent to CP-V611 is CP-V610 which provides the signal from CP-FF150 to CP-G172B, discussed above. CP-V612 is the input valve from CP-FF150 to CP-G157 and CP-G158. Adjacent to CP-V612 is CP-V613 which provides the signal for CP-G172D already discussed above.

The signals from the two outputs of CP-FF151 are applied to CP-G157 and CP-G158 by way of CP-D614 and CP-D615 respectively. These signals are developed through amplifier and signal level changing stages between CP-FF151 and the input diodes. In addition to the signals from CP-FF150 and CP-FF151 a cycling unit pulse p91 is applied to the two gates by way of CP-D616 and CP-D617. Still another control signal on these two gates is FT159 which, by way of CP-V618 can inhibit the operation of both gates. Normally CP-V618 is conducting and its anode is, therefore, +60 volts. This voltage level is communicated to the two gates by way of CP-D619 and CP-D620. With the anode potential at each of these diodes at +60, no inhibition is applied to either gate. When FT159 is present, the anode potential of CP-V618 rises to +90 volts and by way of CP-D619 and CP-D620, inhibits any activity in gates CP-G157 and CP-G158. The signals from the two flip-flops CP-FF150 and CP-FF151 are all +60 to +90 volt signals but the oppositely phased signals from each side of each flip-flop is combined in CP-G157 and CP-G158. Initially with both flip-flops restored, the following conditions exist: CP-D621 and CP-D615 each are at +90 volts, and CP-D622 and CP-D614 are at +60 volts. The presence of the two 90 volt signals is sufficient to inhibit both gates. If either flip-flop reverses its state, the two diodes corresponding to it will exchange their voltages, that is, if CP-FF150 is set then the potential on CP-D621 is +60 volts and that on CP-D622 is +90 volts. In this condition CP-G158 has 60 volts applied to it by CP-D621, CP-D614 and CP-D620. It is then possible for the negative going p91 from the cycling unit to pass through CP-D617 to the output of

the gate. In the meanwhile the 90 volts applied to CP-D622 and CP-D615 are sufficient to inhibit CP-G157. If the opposite condition obtains, i.e., CP-FF151 is set and CP-FF150 is restored, the same condition exists in CP-G157 as previously existed in CP-G158. In this case, CP-G157 passes the p91 to the output. If both flip-flops are set, then CP-D621 and CP-D615 each have 60 volts impressed on them and CP-D622 and CP-D614 have 90 volts impressed on them. This condition is the same as the initial one in which both flip-flops were initially restored. Thus, CP-G157 and CP-G158 only pass a p91 to the output if the two flip-flops are in opposite states. In identical states, neither gate passes a pulse. The output from the two gates are buffed together by CP-D623 and CP-D624 into a common output line which passes to CP-FF152.

The input to FF152 from CP-G157 and CP-G158 is via CP-V625 (FIG. 7g). The output of CP-V625 passes through a delay line and into an amplifier CP-V626. The output of CP-V626 then is passed to the set input of CP-FF152. When CP-FF152 is in set condition, it indicates that the quantity generated in the A-register as the result of an arithmetic operation is negative. Conversely, CP-FF152 indicates a positive quantity when restored. If a pulse arrives from CP-G157A, this indicates that a negative sign is required and, therefore, CP-FF152 is set. CP-FF152 is restored by a p91 pulse gated through CP-G159. CP-G159 is controlled by FT159 applied via CP-V627 into a gate CP-G159. If CP-V627 is cut off, its anode rises to 60 volts and permits the p91 pulse from the cycling unit to pass through to CP-V628 which in turn is connected to the restore input of CP-FF152. CP-FF152 is composed of CP-V628 and CP-V629. The output of CP-FF152 is obtained from the anodes of both valves. That from CP-V628 is connected via CP-V630 to CP-G161B. That from CP-V629 is connected via CP-V631 to CP-G160A and CP-G161A. The same pulse which restores CP-FF152 is also connected to restore CP-FF155, discussed above.

The set output from CP-FF152 is connected to CP-G161A by way of diode CP-D640 (FIG. 7k). Correspondingly, the restore output of CP-FF152 is connected into CP-G161B by way of diode CP-D641. In each case FT161 is also applied to the gates diodes CP-D642 and CP-D643. Each gate is furthermore inhibited by the time out signal via diodes CP-D743 and CP-D644. These two gates are mutually exclusive in that only one of them can be opened since the signals applied from CP-FF152 are permissive in each case and since only one such permissive signal is possible at one time. CP-G161A generates the minus sign if such is called for. In this case, CP-FF152 is set and FT161 is present. The minus sign is substantially at t87 equal to t86. It is sufficient to gate this one pulse through CP-G161A from the cycling unit. This pulse is applied via CP-D645. In the case of CP-G161B it is necessary to gate a decimal zero (indicated by the symbol Z which also represents a plus sign) if the quantity is positive. The Z or + signal is applied via CP-D646 to gate CP-G161B. Two additional signals are applied to these two gates, either of which is sufficient to control the gates. One is the IER signal during multiplication and the other is FT106. These are applied to the two gates via CP-D647 and CP-D648, respectively. The output of the two gates are buffed together via CP-D649 and CP-D650 into a short compensating delay and there into CP-V651. CP-V651 amplifies the output signal and applies it to cathode follower CP-V652. The output of the cathode follower drives the input point in the A and X-registers for the sign signal.

In addition to the Z signal from the cycling unit, one other signal (SG) the sign gate signal, is applied through CP-D653 to CP-G161B. This signal inhibits this until the one computer digit time corresponding to the Z which is required for the sign position occurs. Normally, the

Z signal continues to supply decimal zeros through every computer digit time within the word time.

One other gate driven by CP-FF152 is CP-G160A. This gate generates the control signal S1CP which causes the complementer to operate in the algebraic adder. CP-G160A is controlled by FT160 as well as the set output of CP-FF152. CP-G160A is also inhibited during time out. If CP-FF152 is set and FT160 is present and time out is absent, a signal is applied to CP-V654 which is connected to the complementer in the algebraic adder.

CP-FF156 controls CP-G172A and CP-G172C (FIG. 7h). The set output of FF156 is applied to these two gates by way of CP-D660 and CP-D661. CP-G172A is further controlled by FT172 applied via CP-D662, the output of CP-FF153 by way of valve CP-V663 and a p91 pulse from the cycling unit applied via CP-D664. All signals are permissive except the output from the restore side of CP-FF153. If all conditions are favorable, CP-G172A gates a p91 pulse to an output amplifier CP-V665 by way of CP-D666. CP-V665, a normally conducting amplifier, then applies the signal to CP-G172B at point 580 (FIG. 7j).

The output of CP-FF156 applied through CP-D661 to CP-G172C controls this gate along with FT172 via valve CP-V667 and a p84 pulse from the cycling unit applied via CP-D663. The output of CP-G172C via CP-D669 is applied to the set input of CP-FF154. CP-FF154 consisting of valves CP-V670 and CP-V671 develops a signal for CP-G167 (FIG. 7j). The output for CP-G167 is obtained from the anode of CP-V670. The reset or restore circuit for CP-FF154 is simply a p7 pulse from the cycling unit which every minor cycle restores CP-FF154 so that CP-V671 is non-conducting.

The output from CP-HA150 is applied via CP-D672 to CP-G156B. In addition, the sign gate (SG) signal is applied via CP-D673 and FT156 is applied through CP-D674. Each of these signals is permissive except the sign gate signal which is inhibitory during the sign gate or twelfth digit position. Otherwise, this signal is also permissive. The output of CP-G156B via CP-D675 is applied to CP-V676 which, in turn, is applied to the set input to CP-FF153. The set input is composed of a clock gate CP-CG144C which in addition to the output of CP-V676 is controlled also by timing pulses (tp) from the time pulse generator. CP-FF153 is composed of CP-V677 and CP-V678. The restoring circuit for CP-FF153 is designated CP-G141C. CP-G141C is a gate controlled by the p5 pulse from the cycling unit which, in turn, gates a tp from the timing pulse generator. This indicates that CP-FF153 is restored every minor cycle at time p5. The output of CP-FF153 is obtained from the anodes of both valves. The signal from CP-V678 is applied to CP-V663 already described in connection with CP-G172A and CP-V679 which develops the signal for CP-G156C already described above. The output from the anode of CP-V667 is applied via valve CP-V680 to CP-G172B also described above.

The Algebraic Adder (Schematic)

The algebraic adder (AA) is shown schematically in FIGS. 11a through 11t.

The minuend input from the A-register is applied to the "addend" input of binary adder A via amplifier AA-V14 and gate AA-G700A, a compensating delay line and cathode follower AA-V10 (FIG. 11a). The termination network for the compensating delay line consists of diode AA-DK38, resistor AA-RJ38, diode AA-DN36 and resistor AA-RM36. Both resistors AA-RJ38 and AA-RM36 are returned to a +80 volt source. Whenever the junction point of AA-G700A is at +60 volts diode AA-DN36 connects drawing current from the +80 volt source and resistor AA-RM36 terminates the delay line.

When the junction point of AA-G700A is at +90 volts, diode AA-DK38 connects drawing current from

the +80 volt source and resistor AA-RJ38 terminates the delay line.

The subtrahend input from the A-register is applied to the complementer via AA-V14', AA-G701C, a compensating delay line network consisting of two inductors and a capacitor, and cathode follower tube AA-V10' (FIG. 11b). The network of the compensating delay functions similarly to the termination network for the delay line between AA-G700A and cathode follower AA-V10. The minuend input is also applied to gates AA-G700B (FIG. 11a) and AA-G701A (FIG. 11b) while the subtrahend input is applied to gates AA-G701B (FIG. 11b) and AA-G700C (FIG. 11a).

FT174 inhibits AA-G700B via the normally conducting inverter tube AA-V13. Signal S'2 from the comparator (FIG. 11c) opens AA-G700C via a coupling capacitor and amplifier AA-V9.

The output signals from AA-G700B and AA-G700C are buffed together by buffing diodes. The buffed signal is applied to the addend input of the binary adder A via the normally conducting delay line driver tube AA-V8, a resistor, a coupling capacitor, an amplifier AA-V12, a buffing diode and a cathode follower AA-V10.

The buffed signal also reaches AA-G714 and AA-G718 via delay line driver AA-V8, a seven pulse time delay line, a typical clock gate and PFR network and amplifier AA-V10". The signals which pass through AA-G714 and AA-G718 are buffed together by buffing diodes. The buffed output signal reaches AA output line via the normally conducting inverter tube AA-V9 (FIG. 11c), amplifier AA-V5 (FIG. 11s), a buffing diode, a compensating delay line, a normally conducting clock gate driver tube AA-V7, a typical clock gate and PFR circuit, and cathode follower tube AA-V10IV.

The output signals of AA-G701A and AA-G701B are buffed together by diodes. The buffed signal reaches the AA output line via a normally conducting delay line driver tube, AA-V8'', a seven pulse time delay line, a normally cut off clock gate driver tube AA-V2, a typical clock gate and PFR circuit, amplifier AA-V5', AA-G715, a buffing diode and the same circuitry as the buffed output signal from AA-G714 and AA-G718.

The output signal from cathode follower AA-V10' (FIG. 11b) is not applied to the control grid of the normally conducting complementer input tube (FIG. 11h), which inverts the input signal. The complementer is a typical half adder circuit, which consists of tubes AA-V41, AA-V51, AA-V61, AA-V71, and AA-V81 and associated circuitry. The output signal from the complementer is applied to the augend input of binary adder A via the check pulse delete gate AA-G724.

The binary adder A (FIGS. 11g, 11i, and 11j) is a typical full binary adder circuit where the addend input is inhibited by the check pulse eliminator signal (CPE) from the CU via the normally cut off inverter tube AA-V1 and a buffing diode. When a CPE is present the junction point of the positive clock gate is held at -88 volts thus preventing the PFR flip-flop from being set.

The carry output signal from binary adder A is applied to AA-G722 and AA-G723 (FIG. 11k) via cathode follower AA-V112 (FIG. 11j) and amplifier AA-V92 (FIG. 11k).

The signal which passes through AA-G723 reaches the binary adder A carry input line via compensating delay line, a normally conducting clock gate driver tube AA-V122, a typical clock gate and PFR circuit, a normally conducting delay line driver tube AA-V113, a two pulse time delay line, amplifier AA-V72, AA-G721, two buffing diodes, and another compensating delay line and lead AA-121.

The signal from AA-G723 also opens AA-G731 and AA-G732 (FIG. 11o) via cathode follower tube AA-V114, a normally conducting clock gate driver tube VV-V102, a clock gate, AA-FF706 and amplifiers AA-V211 and AA-V221 respectively. AA-FF706 is

restored by a TP— pulse whenever the $t7n$ pulse passes through inverter AA-V73 and lowers the potential of the negative clock gate junction point from -71 volts to -89 volts. The pulses which pass through AA-G731 and AA-G732 are buffed together. The buffed output signal is applied to the augend input line of binary adder B (FIG. 11n).

The signal which passes through AA-G722 is buffed into the carry input line of binary adder A via a buffing diode and a compensating delay line and lead AA-121. The signal which passes through AA-G727A (FIG. 11j) is also buffed into the binary adder A carry line input AA-121 via a buffing diode. The signal which passes through AA-G727B is buffed into the binary adder A carry input line via a buffing diode. The carry output signal from binary adder A is also sent to the AA-G145C (FIG. 11m) via cathode follower AA-V112, a coupling capacitor, and an amplifier AA-V53. The signals from the anode of AA-V53 are also applied to AA-G725 via the normally conducting inverter tube AA-V43. The signals which pass through gates AA-G145C and AA-G725 are buffed together by buffing diodes. The buffed output signal is sent to the MQC via cathode follower AA-V212.

The "sum" output from binary adder A is applied to the addend input line of binary adder B via a compensating delay line (FIG. 11i), a normally conducting clock gate driver tube AA-V123 (FIG. 11j), a typical clock gate and PFR circuit, amplifier AA-V103, a normally conducting delay line driver tube AA-V113, and a three pulse time delay line. Binary adder B (shown in FIGS. 11n, 11p, and 11r) is a typical full binary adder circuit. The "carry" output from binary adder B is reapplied to its input via AA-G713 (FIG. 11r) and a one half pulse time delay line.

The "sum" output signal from binary adder B reaches the AA output line via a compensating delay line, a buffing diode, a normally conducting clock gate driver tube AA-V124, a typical clock gate and PFR circuit, a compensating delay line, amplifier AA-V4, AA-G736, a buffing diode, a compensating delay line, a typical clock gate and PFR circuit, and cathode follower AA-V101V.

The "sum" output pulse is also applied to the control grid of the clock gate driver tube AA-V134 (FIG. 11q) via a cathode follower AA-V114 and a coupling capacitor.

When AA-V134 is cut off, a positive-going pulse from its anode is applied to the control grid of clock gate driver AA-V125 and causes it to conduct. The next TP— pulse passes through the negative clock gate and sets the high speed binary counter AA-BC700 to the "0" position when the signal from the anode of the normally conducting tube AA-V114, holds the junction point of the negative clock gate at -89 volts.

When this counter is in the "0" position, the signal from the anode of AA-V94 passes through a compensating delay line and is applied to the control grid of the normally conducting amplifier tube AA-V144. The same signal also cuts off AA-V114 which causes the junction point of the positive clock gate to be held at -71 volts allowing the next TP+ to pass through a buffing diode and to restore the counter to the "one" position. The counter can also be restored to the "one" position when a $p7n$ pulse opens a positive clock gate via a normally conducting clock gate driver AA-V84. The next TP+ signal then restores AA-BC700 via a buffing diode when the junction point of the positive clock gate driven by AA-V134 is held at -71 volts by a signal from the anode of AA-V114. Tube AA-V114 serves as a memory which remembers the previous state of AA-BC700.

The "0" output signal from the compensating delay line reaches the AA output line via the normally conducting amplifier AA-V114, AA-G735, a buffing diode, a typical CG and PFR circuit, amplifier AA-V44, AA-G736, another buffing diode, a compensating delay line, another typical CG and PFR circuit, and cathode followers AA-V101V and AA-V11.

The buffed output signal from AA-G700B and AA-G700C (FIG. 11a) is applied to AA-G704 and AA-G706 (FIG. 11c). The signal which passes through AA-G709 opens the negative clock gate AA-CG711A via a buffing diode, a normally conducting inverter AA-V5 and clock gate driver AA-V12.

The signal which passes through AA-G706 opens the positive clock gate AA-CG710A via a buffing diode, a compensating delay network and a normally conducting clock gate driver AA-V115. FT160 is buffed into the AA-CG710A input line via AA-G160C and a buffing diode. The signals which pass through these positive and negative clock gates are buffed together by buffing diodes.

The buffed output signal sets AA-FF700 when it is positive-going and restores AA-FF700 when it is negative-going. The set output signal from AA-FF700 opens clock gates AA-CG708A and AA-CG709A via clock gate driver AA-V146. The signals which pass through these clock gates are buffed together; the resultant buffed output signal sets AA-FF702 if it is negative-going and restores AA-FF702 if it is positive-going.

The restored output signal from AA-FF702 alerts AA-G718 (FIG. 11a) via amplifier AA-V76. The set output signal from AA-FF702 opens gate AA-G714 via amplifier AA-V116, inhibits AA-G736 via amplifier AA-V77 (FIG. 11f), a buffer diode, cathode follower AA-V107, and the normally conducting inverter tube AA-V37 (FIG. 11s), and alerts AA-G727B via amplifier AA-V77, a buffer diode, cathode follower AA-V97, a normally conducting inverter tube AA-V87 (FIG. 11k), and a normally cut off inverter tube AA-V47 (FIG. 11j).

The AA-FF702 set output signal also opens AA-G721 via amplifier AA-V77 a buffing diode, cathode follower AA-V97 and a normally conducting inverter tube AA-V87. The signal from the cathode of cathode follower AA-V97 inhibits AA-G726 via connection L and lead AA-130 (FIG. 11j) and the normally conducting inverter tube AA-V98 (FIG. 11m).

When the AA-FF702 set output signal is applied to the suppressor grid of the coincidence gate tube AA-V67 (AA-G720) in the presence of a positive-going signal on the AA-V67 control grid, a negative-going signal from the anode sets AA-FF704 (FIG. 11f). The AA-FF704 set output signal is applied to error gate AA-G216. The buffed output signal from AA-G701A and AA-G701B is applied to AA-G705 and AA-G707 via delay line driver tube AA-V811 (FIG. 11b) and amplifier AA-V818 (FIG. 11d).

The signal which passes through AA-G705 reaches clock gate AA-G711B via a buffing diode, a normally conducting inverter tube AA-V38 and clock gate driver AA-V58. The signal which passes through AA-G707 is applied to AA-CG710B via a buffing diode, a compensating delay line, and the normally conducting clock gate driver tube AA-V4. An FT160 is buffed into the AA-G710B input line via AA-G160D and an input diode. The signals which pass through clock gates AA-CG710B and AA-CG711B are buffed together by buffing diodes. The buffed output signal sets AA-FF701 if it is positive-going and restores AA-FF701 if it is negative-going.

The AA-FF701 set output signal is applied to clock gates AA-CG708B and AA-CG709B via the normally cut off clock gate driver tube AA-V919 (FIG. 11f). The signals which pass through these clock gates are buffed together by buffing diodes. When the buffed output signal is negative-going, it sets AA-FF703 and when it is positive-going, it restores AA-FF703. The AA-FF703 set output signal opens AA-G715 via amplifier AA-V49 (FIG. 11d) and is also applied to the control grid of coincidence gate tube AA-V67 thereby opening AA-G720. The AA-FF703 set output signal is also buffed together with AA-FF702 set output signal via amplifier AA-V58 and a buffing diode.

Flip-flop AA-FF707 is set by a $t14$ pulse which passes

through AA-G738 (FIG. 11f). The AA-FF707 set output is buffed together with the AA-FF702 and AA-FF703 set output signals via the normally conducting inverter tube AA-V128, connection X (FIG. 11f), AA-G755, and a buffing diode.

AA-FF705 is set by a negative-going pulse from the X-register via a coupling capacitor and a buffing diode or by the pulse which passes through AA-G726 (FIG. 11m) and a buffing diode.

The Multiplier-Quotient Counter (Schematic)

The schematic diagram of the multiplier-quotient counter is shown on FIGS. 9a through 9m.

An input pulse from the X-register is applied to the MQC distributor line via inverter tube Q-V141 (FIG. 9d), Q-G112C, a buffing diode, a typical clock gate and PFR circuit, amplifier Q-V101 (FIG. 9g), and the normally conducting distributor driver tube Q-V91.

The distributor line output pulses t_6 , t_7 , t_8 , t_9 and t_{12} are sent to the X-register via gates Q-G116A through Q-G116E, corresponding buffing diodes, a typical clock gate and PFR circuit, and cathode follower tube Q-V1 (FIG. 9a).

The distributor line output pulses which occur at time t_9 , t_{10} , t_{11} and t_{12} are applied to the normally conducting tube of binary counters MQC1, MQC2, MQC3 and MQC4 and set the four binary counters to the "one" position via gates Q-G119A through Q-G119D.

Cathode follower tube Q-V44 (FIG. 9i), connects the anode of the normally conducting tube of MQC4 to the normally cut off tube of MQC3 and similarly cathode follower tubes Q-V71 and Q-V102 connect MQC3 to MQC2 and MQC2 to MQC1 respectively. The binary counter MQC1 is triggered by a pulse from a cathode follower tube.

The output signals from the four stage binary counters are applied to a decoding function table via gates Q-G179A through Q-G179H and Q-G180A through Q-G180H. The "0" output signal from the MQC function table is generated by line Z Q-24 and is applied to Q-G147A and Q-G147E via amplifier tubes Q-V111 respectively. The signal which passes through Q-G147A inhibits Q-G148 via a normally conducting inverter tube. The signal which passes through Q-G147E sets the (IER) flip-flop Q-FF121A and also sets the (IER, OR) flip-flop Q-FF121C via buffing diodes.

The (OR) flip-flop Q-FF121B is set by overflow (OF) signal via a pulse spreader network consisting of a resistor, two diodes, an impedance matching network formed by a resistor and a capacitor and an open-circuited section delay line, a normally conducting delay line driver tube, a two pulse time delay line, an amplifier tube, a coupling capacitor and two coupling diodes. The OF signal from the delay line driver also sets the (IER, OR) flip-flop Q-FF121C via a coupling capacitor, a buffing diode and a coupling diode.

The "0" MQC signal also restores Q-FF120 via an amplifier, a coupling capacitor and two coupling diodes. The signal from the amplifier also inhibits Q-G147C via a normally conducting inverter tube.

The ≥ 3 signal is obtained from the set output state of Q-FF120 and is applied to the F-register via an amplifier. The ≥ 3 signal is also applied to Q-G130, permitting a t_{28} and a t_{60} pulse to pass through gate Q-G147D via a normally conducting inverter tube and an amplifier. The signal which passes through Q-G147D is then applied to the control grid of a cathode follower, the output signal from whose cathode advances the four binary counters MQC1, MQC2, MQC3 and MQC4 via lead Q-60 (FIG. 9m). The signal from the anode of this cathode follower is applied to Q-G113 via lead Q-61 amplifier Q-V122 and a buffing diode.

The pulse which passes through Q-G113 is applied to the control grid of the normally conducting amplifier

tube Q-V132. The negative-going "carry" output is thus secured from the anode of Q-V132.

This carry signal passes through Q-G145A and is applied to the control grid of a cathode follower tube and to the control grid of a normally conducting inverter tube. The "improper division" output signal from Q-G145A is sent to the algebraic adder (AA).

The carry signal is also applied to the control grid of a normally conducting inverter tube via Q-G127B. The signal from the anode of the inverter tube is sent to the control circuits as the MQC-m signal via a cathode follower.

The signal from the inverter tube is also applied to the control grid of another inverter tube, the anode signal from which sets Q-FF125 and a differentiating network (FIG. 9c) via a buffing diode, consisting of a capacitor and resistor and two coupling diodes. The Q-FF125 output signal then clears the four binary counters to decimal zero via amplifier Q-V52, and a differentiating network consisting of a resistor and a capacitor. Diode DM-24 is an upper clamp which prevents the clearing signal from rising above -191 volts.

At t_1 pulse is applied to the control grid of a normally conducting inverter tube via Q-G142. The signal from the anode of this inverter tube is applied to the control grid of two amplified tubes. The signal from the anode of one amplifier tube sets Q-FF124 via a cathode follower, a differentiating network consisting of a capacitor and resistor RM17 and two coupling diodes (FIG. 9c). Diode DM16 is an upper clamp for the grid potential of the normally conducting tube of Q-FF124, preventing it from rising above -95 volts. The Q-FF124 output signal clears the four binary counters to decimal zero via amplifier tube Q-V62 and a differentiating network consisting of a capacitor and resistor. Diode DM17 (FIG. 9f) is an upper clamp which prevents the signal from rising above -190 volts.

The signal from the anode of the above-mentioned inverter tube is applied to the control grid of amplifier Q-V102 (FIG. 9j) via a coupling capacitor. Diodes DJ36 and DK36 which are connected across the grid resistor provide D.C. restoration for the incoming signal.

The signal from the anode to Q-V102 is applied to a typical binary counter, Q-BC120.

During the division process a t_1 pulse passes through Q-G139 and sets this counter to the "one" position. When the counter is in the "one" position, the Q-V102 output signal is applied to all backward gates Q-G179A through Q-G179H via the normally conducting inverter tube Q-V62.

During the multiplication process a t_7 pulse passes through Q-G138B and sets Q-BC120 to the "zero" position. When Q-BC120 is in the "zero" position, the output signal from the anode of Q-V102 is applied to all forward gates, Q-G180A through Q-G180H via inverter tube Q-V72. The MQF signal is also applied to Q-G118 via inverter tubes Q-V52 and Q-V42, and amplifier Q-V212.

The signal from the anode of the normally conducting inverter tube Q-V42 is sent to the complementer via amplifier Q-V32, Q-G145B and the normally conducting amplifier tube Q-V43.

When a t_{19} pulse passes through Q-G112D (FIG. 9c) it is applied to the normally conducting amplifier Q-V133 via a coupling capacitor. The positive-going pulse from the anode of Q-V133 alerts Q-CG150 and allows a TP+ to fire the blocking oscillator trigger tube Q-V123 via a coupling capacitor.

When Q-V123 conducts it applies a negative-going pulse to the tertiary winding of the blocking oscillator. Both halves of the blocking oscillator tube are normally cut off since their control grids are returned to a -30 volt source via the secondary winding of the blocking oscillator and a resistor. The negative-going trigger pulses in the tertiary winding induces a positive-going

pulse in the primary and the secondary winding of the blocking oscillator.

The positive-going pulse induced in the secondary winding raises the control grid potential of both halves of Q-V113 sufficiently high to cause them to conduct. As the control grid potentials increase, the anode potentials of Q-V113 decrease causing regenerative feedback in the tertiary and secondary windings. The primary winding of the blocking oscillator applies a sharp pulse to the control grid of the four transfer gate tubes Q-V73, Q-V83, Q-V93 and Q-V103.

When the potential across the grid capacitor becomes sufficiently large to exceed the regenerative voltage across the secondary winding, the control grid potentials of Q-V113 decrease, the anode potentials increase and degenerative feedback causes both halves of Q-V113 to cut off.

The L-Register (Schematic)

The schematic diagram of the L-register is shown in FIGURES 17a through 17e. Since the block diagram of the L-register has already been described in detail, and since the electronic circuitry of the A-register has been described in considerable detail (much A-register circuitry being duplicated in the L-register), it is believed that the following discussion on the L-register will be self-explanatory.

The main recirculation loop of the L-register is shown on FIGS. 17a, 17b, 17c and 17d. Incoming signals to the recirculation loop enter either through L-D100 or through diode L-D101. (See FIGURE 17c.) The signal thus entering the main loop travels through a compensating delay line, a driver tube L-V1, and enters a typical one word mercury delay line chassis, then travels through a normally conducting tube L-V13 into the clock gate. This clock gate is shown in FIGURE 17b. The signal then leaving the clock gate enters the pulse former flip-flop formed by L-V11 and L-V12. The output signal from L-V12 travels through a normally conducting driver tube L-V10, through a second compensating delay line (both of which are shown in FIG. 17a), and then travels through amplifier L-V3, through clear gate L-G186, and back to the point of entry. This pulse, of course continues to recirculate in the loop until the clear gate is closed.

The output signals yielded by the L-register travel from the anode of L-V11 of the pulse former flip-flop, through a cathode follower L-V5, into the A-register and the comparator. The signal also travels from the anode of L-V11, through cathode follower L-V14, to the checking circuits. Finally the output signal yielded by L-V11 travels through cathode follower L-V12 (see FIGURE 17a) and through gates L-G183a and L-G183b into the high speed bus amplifier. (These gates are shown in FIGURE 17e.)

The X Register (Schematic)

The X-register is shown schematically in FIGS. 15a-15g. The main recirculation loop is indicated by a heavy line.

An incoming pulse enters the main recirculation loop via X-DJ31 or buffing diode X-DN3. The pulse in the main recirculation is applied to a typical one word mercury delay line chassis via a normally conducting driver tube, X-V5. The pulse which leaves the mercury delay line reaches its point of entry via a typical clockgate and PFR circuit, inverter tube X-V14, amplifier X-V6, clear gate X-G121, two buffing diodes, a normally conducting compensating delay line driver tube X-V10, a compensating delay line and amplifier X-V7. The pulse continues to recirculate in the loop until the clear gate X-G121 is closed.

When a pulse circulating in the main recirculation loop enters the left shift circuits it re-enters the main recirculation loop via amplifier X-V9, a normally conducting delay line driver tube X-V8, a 7 pulse time electric delay line, a typical clockgate and PFR circuit, amplifier X-V5,

gate X-G122 and buffing diodes X-DM13 and X-DN18.

When a pulse enters the right shift circuits from the main recirculation loop it re-enters the main recirculation loop via amplifier X-V8 and X-G123 thus by-passing a portion of the main recirculation loop.

The X-register output to the high speed bus is obtained from the control grid of inverter tube X-V14 via cathode follower X-V5. The digit output from the X-register is sent to the MQC distributor line from the delay line in the left shift circuits via amplifier X-V14.

The A-Register (Schematic)

The schematic diagrams of the A-register are shown in FIGURES 13a-13s. The direct input to the A register from the high speed bus is by way of diode A-D300 and A-G105 (FIG. 13a). The negative going pulses which appear on the high speed bus can pass through A-G105 provided FT105 is present and time-out signal is absent. The FT105 signal is normally at 90 volts but during a direct input operation, that is, direct to the A register and not by way of the algebraic adder, the signal 105 drops to plus 60 volts. In opposite manner, the time-out signal is normally at plus 60 volts except during the time-out period when it rises to plus 90 volts. The time-out signal, therefore, inhibits A-G105 during time-out but otherwise permits pulses to pass from the high speed bus to the input circuit of the A register provided FT105 is also present.

A second source of signals directly entering the A register is via gate A-G115. This gate inserts a decimal five in the least significant digit position and decimal zeros elsewhere as part of the initial clear operation of the A register. The signal for the decimal five is generated in the cycling unit and is applied to gate A-G115 via diode A-D302. Also applied to gate A-G115 is the initial clear signal from the supervisory control. This signal is applied through diode A-D303 (FIG. 13a). The IC signal is normally at plus 90 volts but during initial clear, the IC signal drops to plus 60 volts permitting the similar potential change of the pulses of the decimal five signal to enter through A-G115 into the A register. Diode A-D304 is a buffing diode which prevents a back circuit with the signals arriving from valve A-V305.

The input from the comparator for the sign indication for a word in the A register following a multiplication or a division operation is applied through A-V305 to the direct input of the A register. The sign digit from the comparator appears in the form of positive going pulses which are capacitively connected to A-V305, a normally non-conducting amplifier. The output of A-V305 is clamped between 60 and 90 volts. The pulses appearing at the anode of A-V305 are negative going pulses between the limits of the clamping diodes. The combination of the initial clear signal from A-G115 and the sign pulses from A-V305 are buffed into the input amplifier of the A register A-V306 by way of diode A-D307. A-D307 and A-D308 serve as buffers to prevent back circuits between the sign and initial clear signals and the main input from the high speed bus and the recirculating signals from gate A-G109C.

The input amplifier A-V306 (FIG. 13b) is a clock gate driver whose anode is clamped between minus 71 and minus 89 volts. Any signals applied to the grid of A-V306 appear as positive going pulses at the anode and in turn are applied to the clock gate following A-V306. The clock gate is a standard array of diodes and timing pulse input signals from the cycling unit. (See compending application S.N. 279,710.) Following the clock gate is a pulse forming flip-flop composed of A-V309 and A-V310. The output positive-going pulses from this pulse forming flip-flop is applied to A-V311, a normally conducting valve whose lower anode potential is clamped at +60 volts and whose upper limit is approximately +80 volts. The output signal from A-V311 is capacitively coupled to A-V312, a delay line driver circuit. The anode

of A-V312 is clamped between plus 80 volts and plus 106 volts. The signals appearing on the anode of A-V312 are positive going pulses and these in turn are applied to a compensating delay. The delay normally encountered in passing through one or two amplifiers is not sufficient to equal a half-pulse of delay. Because these additional pulses are going to be applied within the block marked "mercury delay line," the compensating delay is inserted and adjusted such that the timing of pulses arriving at the clock gate have proper timing. A-V313 (FIG. 13c) is an amplifier which produces 30 volt negative-going pulses at its anode. These signals are applied through diode A-D314 to a junction point 315. Into this junction point 315 also come pulses either from the output of the algebraic adder via diode A-D316 or from the right shift path via diode A-D317. The nature of the signals applied via these diodes are identical, namely, they are negative going signals of 30 volt amplitude clamped between the limits of plus 90 and plus 60 volts. The pulses arriving through A-D316 will be described as the output pulses from the algebraic adder. The pulses arriving on A-D317 will be described during the right shift operation.

Pulses arriving at junction point 315 pass into a compensating delay whose purpose is to bring the pulses into proper timing for the operation of a clock gate which appears in the beginning of the one word delay line assembly. Between the delay line and the clock gate driver, however, is an additional amplifier A-V318, a normally conducting amplifier whose output pulses are of approximately 20 volt amplitude positive going and whose lower level is clamped at plus 60 volts.

The output of the one word mercury delay line chassis (see copending application S.N. 279,710) is in the form of negative going pulses which are capacitively coupled to A-V319. A-V319 is a standard clock gate driver whose output is coupled to a typical clock gate composed of an array of diodes and timing input pulse signals from the cycling unit. The output of the clock gate is applied to a pulse forming flip-flop composed of valves A-V320 and A-V321 (FIG. 13d). The positive-going output pulses of A-V321 are applied to A-V322 (FIG. 13e) and A-V328 simultaneously at junction point 327. The purpose of the connection via A-V328 is for transferring the least significant digit of the partial product to the X register just before being cleared from the A register by the MSD signal at A-G124 (FIG. 13e). The timing requirement at the input point to the X register is such that point 327 in the A register must be used for transfer from A to X. The output signals from point 327 are applied through valve A-V328, a cathode follower circuit which passes the positive going pulses from A-V321 to a gating circuit A-C114 (FIG. 13d).

A-G114 is controlled by three signals, MSD, IER and time-out. As mentioned in connection with A-G124 the least significant digit of the partial product is at this point in the A register in time with the most significant digit (MSD) time at the C.U. Therefore, the MSD signal from the cycling unit is used to operate A-G114. However, in addition to this signal, the IER signal which marks that minor cycle introduced between each stage of the multiplier operation during which the new multiplier digit is transferred to the MQC, is here used to control the passage of the least significant digit of the partial product from the A register to the X register. In order to introduce sufficient time for the new control signals for the IER stage to establish themselves, the time-out signal is applied for one minor cycle. The signals appearing at the anode of A-V329 (FIG. 13d) are negative going signals of 30 volt amplitude clamped between the limits of plus 90 and plus 60 volts. The MSD and IER signals are both normally at 90 volts except during the significant portion of their cycle during which time they fall to plus 60 thus permitting signals from A-V329 to pass through A-G114. In addition, however, the time-out signal which

is normally at plus 60 volts rises to plus 90 during the time-out interval. The 90 volt signal on the time-out input therefore inhibits any signals through A-G114 until time-out is released.

The output pulses of A-V322 (FIG. 13e) are negative going pulses of 30 volt amplitude and these are applied to gate A-G124. The purpose of gate A-G124 is to delete any digits shifted into the space between words. Due to the timing at this point in the register, the C.U. signal equivalent to the space between words corresponds to the most significant digit (MSD) which signal is represented by the cycling unit signal $t(79-85)$. This signal is applied to the main circulation path by way of diode A-D323 (FIG. 13e). Normally, the MSD signal is at plus 60 volts but during the interval $t(79-85)$ this signal rises to plus 90 volts and effectively masks any signals arriving from A-V322 by way of diode A-D314. The purpose then of the MSD input signal at this point is to clear the space between words during each circulation of the contents of the A register.

The pulses which pass through A-G124 (FIG. 13e) are communicated by way of diode A-D325 to the input of A-V326. A-V326 drives a compensating delay line equal to seven pulses of delay. A tap on the seven pulse delay line is connected through a capacitor to A-V330, a clock gate driver. The output of A-V330 drives a standard clock gate array of diodes and input timing pulses from the cycling unit. The output of the clock gate drives a pulse forming flip-flop composed of A-V331 and A-V332 (FIG. 13e). The positive-going output from the pulse former is obtained from the anode circuits of A-V331 and drives a normally non-conducting amplifier A-V333 (FIG. 13f). The output of A-V333 is clamped on its lower limit at plus 60 volts. These pulses are coupled capacitively to A-V334 (FIG. 13g), a normally conducting amplifier whose output is clamped between plus 80 and plus 106 volts. The output of A-V334 is applied to a seven pulse delay line section. The purpose of the seven section delay line is to introduce seven pulses of delay (equal to one computer digit) in order to permit right shifting to occur. The right shift connection is from junction point 335 (FIG. 13f). The path through the right shift circuit will be discussed separately below.

A tap at the very beginning of the seven pulse delay line, connected to the anode of A-V334 (FIG. 13g) is also connected to an output clock gate pulse former circuit which eventually leaves the A register by way of gate A-G100 (FIG. 13h) and passes those signals in the A register to the high speed bus system. The clock gate driver of this output circuit is A-V336 (FIG. 13g) which, in turn, is followed by standard clock gate array. The output of the clock gate drives a pulse forming flip-flop composed of A-V337 and A-V338 (FIG. 13h). The output of the clock gate is obtained from the anode of A-V337 and is applied to a cathode follower A-V 339. The outputs of A-V337 are in the form of positive going pulses clamped between the limits of minus 35 volts and minus 5 volts. The output of A-V339 is connected by a capacitor to A-V340 a phase inverter and amplifier for the output gate A-G100. A-G100 is controlled by FT100. The pulses appearing at the anode of A-V340 are negative going pulses of 30 volt amplitude clamped between the limit of plus 90 volts and plus 60 volts. These signals are permitted to pass through A-G100 when FT100 is at plus 60 volts. A-G100 is closed whenever FT100 rises to 90 volts. FT signal 100 is normally at plus 90 volts except during an output instruction from the A register to the high speed bus.

The other tap from the end of delay line section (FIG. 13g) associated with the anode of A-V334 is connected to a clock gate driver A-V341 (FIG. 13g). The output of A-V341 is connected to a standard clock gate array which in turn is connected to a pulse forming flip-

flop composed of A-V342 and A-V343. The normal recirculation path of the A register is obtained from the anode of A-V342. These pulses are positive going between the limits of minus 35 and minus 5 volts. They are applied to the input grid of A-V344 (FIG. 13i), a normally nonconducting amplifier. The output of A-V344 is clamped between plus 60 and plus 90 volts and is applied by way of diode A-D345 (FIG. 13j) to A-G101B. AG101B is the gate which is normally closed during any shift operations and for any clearing operations.

Altogether, there are five possible sources of inhibition which can be applied to A-G101B. Associated with this gate are three other gates which combine the conditions required by various operations to close A-G101B.

A-G101A (FIG. 13k) is the gate which inhibits A-G101B during that stage in multiplication and division during which the partial product or the remainder is shifted one digit either right or left depending on the particular instruction or which clears the A register. The conditions necessary for the shift operation are:

- (1) The IER, OR signal is present indicating the between steps cycle occurring in division and multiplication.
- (2) Time is *not* out.

The conditions for a clearing operation are:

- (1) FT signal 101 is present.
- (2) Time is *not* out.

A-G101A is composed of valve A-V346 and various diodes which combine the signals mentioned above. The IER, OR signal arrives by way of diode A-D347. This signal is generated by a flip-flop in the MQC. Its level is at plus 90 volts but during the IER, OR stage, it drops to plus 60 volts. The 101 signal from the function table is connected into A-G101A by way of diode A-D348. This signal also is normally at plus 90 volts but during the clear operation drops to plus 60 volts. Diodes A-D348 and A-D347, therefore, buff either signal into the input grid of A-V346. The connection of these two signals into the grid of A-V346 is through a divider circuit consisting of a 10K resistor, a 50K resistor and a 182K resistor placed in series between a plus 166 volt potential source and a minus 301 volts potential source (FIG. 13k). The proportion of these resistors is such that the potential applied as bias to the grid of A-V346 is such that A-V346 normally conducts. When the signals 101 or IER, OR draw their respective diodes from 90 v. down to 60 v. a signal is impressed upon A-V346 which cuts this tube off. The anode of A-V346 is clamped between 90 and 60 volts. When neither signal 101 nor IER, OR is present, the anode potential of A-V346 is plus 90 volts. During the presence of either signal the anode drops to plus 60 volts. A-V346, therefore, serves purely as an inverting element to produce the right polarity of signal for A-G101A. The output of A-V346 is communicated to A-G101A by way of diode A-D349 (FIG. 13k). The junction point of A-G101A is returned to plus 380 volts. Whenever A-V346 is at plus 90 volts, diode A-D349 effectively clamps the junction point of A-G101 to a potential of plus 90 volts. Also connected to this junction point is the time-out signal input by way of diodes A-D350 and A-D351. The time-out signal normally exists at plus 90 volts except during time-out when it falls to plus 60 volts. The junction point between these diodes, therefore, follows the time-out signal alternating between plus 90 when time is not out and plus 60 during time-out. Since the anode of A-V346 is normally at 60 volts, the junction point at A-G101A is held at plus 60 volts by the action of time-out as well as those signals applied to A-V346. When this tube stops conducting and its anode rises to plus 90, indicating the presence of one of the two signals appearing on its grid, its diode

A-D349 will only permit the junction of A-G101A to rise to 90 if the time-out signal also rises to plus. The polarization of the two diodes A-D349 and A-D351 is such that both signals must rise to 90 volts before the gate itself can rise to plus 90. Effectively then the time-out prevents the signals 101 or IER, OR from passing through A-G101 to diode A-D351.

A second source of signals which inhibit A-G101B is from the F register where the extract signal (E) is generated in a flip-flop (FIG. 13k). This signal, designated the E signal, is capacitively coupled into A-V353, a normally conducting amplifier, whose anode is connected by way of diode A-D354 to the gate A-G101B. The signal appearing at anode of A-V353 is identical to that appearing at diode A-D352 in gate A-G101A. This signal is normally at plus 60 volts until the E signal occurs when it rises to plus 90 volts.

A third source of signals to gate A-G101B is from A-G170 and A-G102B (FIG. 13k). A-G170 is for the purpose of by-passing the sign digit through the normal recirculation path when the normal recirculation path is otherwise closed due to a shifting operation. In this gate, FT170 is normally at plus 90 volts except during the shift operation when the 170 signal is excited. The DG signal from the cycling unit (9-85) also is normally at plus 90 volts except during the period (9-85). In addition, the time-out signal, which is normally at plus 60 except during time-out when it rises to plus 90 volts is applied to A-G170. A combination of these three signals produces at diode A-D355 a signal which passes from plus 90 to plus 60 during the interval (9-85). Diode A-D355 is a buffering diode which combines the signals from gate 170 into a junction point.

A-G102B is a clear gate used only during a transfer from the A register to the memory. For such a transfer, FT102 which is normally at plus 90 volts, drops to plus 60 volts. At the same time, the TS signal which is normally at plus 90 volts also drops to plus 60 volts and for the length of one word when the word from A may enter the memory location specified. Thus the output of A-G102 passes to diode A-D356 and there meets at a junction point with the output from gate A-G170.

A voltage variation from either A-G170 or A-G102B is capacitively connected to A-V357. A-V357 (FIG. 13k) is a normally conducting amplifier which, when it receives a signal from either A-G170 or A-G102B is cut off. Its anode potential, which is normally at plus 60, rises to plus 90 being limited in each case by clamping diodes. The signal, therefore, impressed by A-V357 on diode A-D358 is identical to that impressed upon diodes A-D354 and A-D352 by the other gates. These three diodes, therefore, buff together all the signals of the several gates whose outputs can inhibit A-G101B. In each case, these signals pass from 60 volts to 90 and in so doing impress on A-G101B by way of diode A-D359 (FIG. 13j) masking signals which prevent any signals appearing at diode A-D345 from passing through to the normal recirculation path.

One additional signal which also joins the recirculation path at this point is the initial clear signal (IC) by way of diode A-D360 (FIG. 13j). During initial clear the signal IC from the supervisory control rises from plus 60 to plus 90 and masks any signals appearing at diode A-D345. The output of A-G101B passes to diode A-D361 and then in the normal recirculation path to diode A-D362. To the junction point between these two diodes comes a signal via diode A-D363 (FIG. 13j) from the shift path one computer digit time shorter (right shift) than the normal path. This path will be discussed later. Following diode A-D362 is an output point going to A-G103 and A-G104 (FIG. 13j) whose purpose will be discussed later. The normal recirculation path continues to valve A-V364 (FIG. 13a). A-V364 is a normally conducting amplifier which receives the negative going signals from A-G101B. The

output of A-V364 is clamped between 60 and 90 volts. The output pulses from A-V364 are connected to a junction point 365 (FIG. 13a) by way of diode A-D366. Junction point 365 receives the signals not only from A-V364 which are completing a recirculation of the register but also certain special signals which are injected into the A register for various purposes. In general, these signals are 0's and the various conditions under which they are inserted into the A register will be discussed later. Signals reaching point 365 are capacitively coupled into A-V367 a normally non-conducting amplifier whose anode is clamped between plus 90 and plus 60 volts. The anode potentials are negative going pulses which in turn are connected to junction point 368 (FIG. 13a). Junction point 368 is that point at which signals may leave the A register to enter the algebraic adder through a special gate A-G109B (FIG. 13m). Signals passing point 368 are communicated through diode A-D369 to gate A-G109C (FIG. 13a). Control signals are impressed on A-G109C by way of diode A-D370. These signals are generated in a special gating circuit not shown in this figure but which will also be discussed later. The effect of the signals on diode A-D370 is to clamp the junction point of the gate at plus 90 thus preventing the negative going signals from A-V367 from passing through to the output diode A-D371. If no inhibition is applied through diode A-D370, the signals pass through diode A-D371 to diode A-D308. Diode A-D308 marks the point at which the signals first appeared from the high speed bus and thus the normal recirculation path of the A register is completed.

Associated with the normal recirculation path within the A-register are numerous auxiliary paths and special input circuits. Three of the special paths are called the shift paths. There is one left shift path and two right shift paths in the A-register. In each case a seven pulse delay is either added or removed from the normal path of circulation in order to bring about a shift in time of seven binary digits which is equal to one computer digit of the contents of the A-register. Also, in each case, certain control signals are developed to inhibit the normal path through A-G101B (FIG. 13j) while other control signals operate to open one of the three alternate routes. The left shift path picks up from junction point 372 (FIG. 13i) which is between A-V342 (FIG. 13g) and A-V344 (FIG. 13i) in the normal recirculation path. Signals passing this junction point are also communicated to A-V373 (FIG. 13i). A-V373 is a normally non-conducting amplifier whose anode is clamped at a lower limit of plus 60 volts. The signals appearing on the anode of A-V373 are capacitively coupled to A-V374 a normally conducting amplifier whose output is clamped between +80 volts and +106 volts. A-V374 drives a seven pulse delay line. This delay line introduces the additional seven pulses of delay which, upon each recirculation of the contents of the A-register increases the timing of the contents by one computer digit, i.e., seven binary pulses. There are two taps from the seven pulse delay line. The earlier tap drives A-V375 (FIG. 13i), a cathode follower which in turn communicates to the comparator the contents of the A-register. It will be noted that even though the left shift path controlled by a gate appearing later in the circuit may not be open, A-V375 is still able to communicate the signals in the A-register to the comparator from this branch circuit. The connection between the A-register and the comparator is used during various comparison operations such as that preceding the multiplication and division operations as well as addition and subtraction and further for the Q and T instructions. The later tap on the seven, pulse delay line appearing in the anode circuit of A-V374 is connected to A-V376 (FIG. 13i) a normally non-conducting amplifier. A-V376 is a clock gate driver. Following the clock gate is a pulse forming flip-flop

composed of valves A-V377 and A-V378. The positive going output pulses from the pulse forming flip-flop appear in the anode of A-V377. These pulses connect to A-V379 (FIG. 13j) a normally non-conducting amplifier whose anode is clamped between +60 and +90 volts. The purpose of A-V379 is to shift the level of the pulses appearing at the anode of A-V377 from -5 to -35 up to the +60 +90 volt range. Obviously an inversion also occurs in A-V379. A-V379 drives A-G104 and A-G103 (FIG. 13j) A-G104 is the gate normally used to pass the contents of the A-register through a longer delay path than normal thus shifting it in significance one decimal digit in the more significant direction, with the exception of the sign digit. Three control signals are applied to A-G104, FT104, the digit gate (DG) signals and the time out signal. When an instruction calls for the left shift without shifting the sign, FT104 develops by dropping from +90 to +60 volts. This signal is communicated to A-G104 by way of diode A-D380. The DG signal also drops from +90 to +60 during each minor cycle in the interval from $t(9-85)$. Otherwise this signal is at +90 volts. The DG signal is communicated to A-G104 by way of diode A-D381. Finally, the time out signal is communicated to A-G104 by way of diode A-D382. Time out signal normally is at +60 except during time out when it rises to +90 and thereby inhibits the other signals applied to A-104 from being effective in permitting the pulses from A-V379 (FIG. 13j) to pass through the gate. As soon as time out is released, if the other signals are present, the junction point at A-G104 may follow the voltage variations appearing on the anode of A-V379. These variations are communicated by diode A-D383 to the junction point of the gate.

A-G103, which is a parallel path from A-V379 into the normal recirculation path of the A-register, is operated whenever the entire word in A is to be shifted to the left. The conditions under which this action occurs is during a division or during a full shift instruction. There are, therefore, two principal control signals, FT103 for the full word shift instruction and the OR signal from the multiplier-quotient counter used during division. These two signals are buffed together by diodes A-D384 and A-385. Both these signals normally are at +90 volts. Therefore, A-D386 effectively clamps the junction point of A-G103 also at +90 volts. When either signal drops to +60 volts or both, the diode A-D386 removes the 90 volt clamp from the junction point of A-G103. In order for the negative going pulses appearing on the anode of V379 to pass through A-G103, however, it is necessary that the time out signal also be at +60 volts. This condition occurs whenever time is not out. Time out signal is communicated to the gate by way of diode A-D387 (FIG. 13j).

A-D388 and A-D389 buff the outputs of A-G104 and A-G103 together and A-D390 applies the combined output into the main recirculation path.

There are two right shift paths each of which removes effectively seven pulses of delay from the normal recirculation paths, and therefore, decreases the significance of the contents of the A-register by one computer digit for each circulation of the contents with the shift gates in the shifting position. The right shift path by way of A-G106A (FIG. 13i) is used for any complete word shift. This operation occurs during multiplication, as the entire partial product is shifted to the right and also in response to the specific right shift instruction for the entire word. The other right shift path by way of A-G107A is used for a partial shift in which the eleven digits of a numerical quantity may be shifted to the right one place per circulation but in which the sign digit or twelfth digit is maintained in its normal position and zeros are inserted between the sign digit and the first significant digit. The forward shift path by way of

A-G106A leaves the normal recirculation path at junction 391 (FIG. 13i). The signals are applied by way of A-D392 (FIG. 13e) to A-G106A. A-G106A is controlled either by the IER signal or the FT106. Both of these signals are normally at +90 volts during the corresponding right shift operation drop to +60 volts. The negative going signals appearing at the anode of A-V344 (FIG. 13i) are therefore permitted to pass through A-G106A whenever either signal drops to +60 volts and time out signal is at +60 volts also. The output of A-G106A is communicated to a normally conducting amplifier A-V393 (FIG. 13). The output of this valve is applied to a compensating delay line section equal to about two pulses of delay.

The reason that the two pulses of delay are introduced at this point is that this right shift path is in parallel with 9 pulses of delay in the normal recirculation path. It will be observed that the normal recirculation path carries a delay of 8 pulses between the point of departure and the point of return of the right shift path in the normal path for the algebraic adder and an additional one pulse of delay in a compensating delay at a pulse former circuit. Since the shifting path must only be shortened by seven pulses, an additional two must be put into this right shift path in order to bring about the proper timing at the point where the right shift path returns to the normal path. The output of the delay line is capacitively coupled to an amplifier A-V394 (FIG. 13e). This valve produces 30 volt signals clamped between +90 and +60 volts. The signals are communicated from A-V394 to the normal recirculation path by way of A-D317 (FIG. 13c) which in turn connects to the regular path at junction point 315.

Another connection leading out of the A-register is from the anode of A-V343 (FIG. 13g). Signals appearing at A-V343 are communicated to a cathode follower A-V395. The output of A-V395 drives checking circuits for the A-register duplication.

The 109 gating system is for the purpose of stopping the normal path of recirculation in the A-register and opening a parallel path through the algebraic adder. In this system are gates A-G109E and A-G109B which, when open permits the contents of A-register to pass into the minuend input of the algebraic adder. A-G109C (FIG. 13a) is in the main path of recirculation just following the tap to A-G109B. When inhibited A-G109C prevents the contents of the A-register from passing through the normal recirculation path. A-G109F (FIG. 13m) permits a pulse to set a flip-flop A-FF101 (A-V465 and A-V466—FIG. 13m) for the purpose of maintaining a signal on A-G109E (13n) which permits the output of the AA to re-enter the normal recirculation path of the A-register. The purpose of A-FF101 is to apply a signal to A-G109E at a different interval of time from that normally defined by the function table signals. The timing of the A-register at this point is such that a minor cycle does not fall in the range of the normal function table signal minor cycle. In addition, A-G109D and A-G113 (FIG. 13m) are used to develop the various control signals to control A-G109B (FIG. 13m), A-G109C (FIG. 13a) and A-G109F (FIG. 13m). A-G109D and A-G113 (FIG. 13m) are parallel gates which process function table signals and other signals in order to develop the signal finally applied to these three gates A-G109B, A-G109C and A-G109F. A-G113 is controlled by FT113, time out, and the delete signal ($t(2-8)$). These three signals are applied to A-G113 via A-D400 through A-D402 (FIG. 13m) respectively. All three signals are normally at +90 volts. When FT113 is present, it falls to +60 volts. Time out is normally at +60 volts but during time out it goes to +90. This, therefore, inhibits A-G113 during time out. The delete signal (DEL) is normally at +60 except during the interval $t(2-8)$ therefore, the signal impressed upon A-D403 is a dropping potential from 90 to 60 volts, ex-

cept during time out and during the interval $t(2-8)$. The signal developed in gate A-G109D is identical to that developed in A-G113. The conditions in A-G109D are obtained by a combination of FT109, time out, delete (DEL) and IER, OR. The combined signals from A-G109D are communicated to junction point 404 by way of A-D405. The negative going signals appearing at junction point 404 are capacitively coupled into A-V406 (FIG. 13m). This signal is of approximately 20 volts amplitude. The output of A-V406 is a 30 volt signal which is normally at +60 but during excitation rises to +90 volts. This signal is applied directly to A-G109C which exists in the normal path of circulation in the A-register. As this signal rises to +90 volts, it prevents any of the negative going signals appearing in the circulation path from passing through A-G109C. The signal appearing on A-V406 is also communicated through a capacitor to A-V407. A-V407 is essentially an inverter which changes the signal from A-V406 to a signal of opposite polarity. This signal from A-V407 is communicated by way of A-D408 to A-G109B and A-D409 to A-G109F. These gates in opposite fashion from A-G109C require a signal going from +90 to +60. The signals in the A-register recirculation path appear at A-D410 in A-G109B. When the voltage applied to the cathode of A-D408 is +60 volts, the normally more positive potential applied to A-D408 from A-V407 is sufficient to mask the negative going pulses which appear in the normal recirculation path of the A-register also appearing at A-D410. When the A-D408 conducts indicating a permissive signal applied to A-G109B, the drop in anode potential is sufficient to allow the negative going pulses from the A-register to pass through A-G109B to A-D411 (FIG. 13m) and from there to A-V412 (FIG. 13o).

Also combined at A-V412 are three other sources of input signals to the minuend input of the algebraic adder. These signals arrive from gates A-G212A, A-G230A and A-G111 (FIG. 13o). A-G212A is the gate by which the contents of the control counter (CC) can be applied to the minuend input of the algebraic adder. The signals from the control counter are applied to A-V413 a normally non-conducting amplifier whose output is communicated by A-D414 to the junction point of A-G212A. The conditions necessary for A-G212A to pass signals from A-V414 into A-V412 are that FT212 be present, that TS be present and that there be no overflow (OF). The negative going signals appearing at the anode of A-V413 are permitted to pass this gate provided these conditions are met and are buffed into the common line to A-V412 by way of A-D415. The second source of signals is the control register whose circulation path is connected to A-V416 (FIG. 13o) a normally non-conducting amplifier. The negative pulses appearing on its anode are connected to A-G320A by A-D417. The conditions necessary for A-G230A to pass the signals from A-V416 to A-V412 are that FT230 be present and that time out be absent. When these conditions are met, signals from A-V416 pass by way of A-D418 into the common line to A-V412. A-G230A is used whenever the word in the control register must be augmented by ten in order to accommodate multi-word transfers within the computer. Finally the signals appearing at A-G111 are also buffed into the common line to A-V412 by way of A-D419 (FIG. 13o). The signal which is gated through A-G111 is a 000 000 000 005 which represents the quotient round off quantity added in during the last stage of the division. The conditions necessary for A-G111 to pass this quantity into the minuend input of the algebraic adder are the presence of FT111 and the absence of time out. A-V412 is a clock gate driver. All signals appearing at it are then applied to a clock gate and a pulse former flip-flop following it composed of A-V420 and A-V421 (FIG. 13o). The output of the pulse forming flip-flop is the anode of A-V421. These signals are

communicated both to the minuend input of the algebraic adder and to the odd-even checker for the algebraic adder #1. This latter connection is by way of A-V422 (FIG. 13n). Concurrent with the operation of A-G212A described above is the operation of A-G212D. This gate shown in FIG. 13p, consists of diodes A-D423 through A-D426. To A-D423 is applied the quantity 000 000 000 001 from the cycling unit. In addition to this signal, FT212 and the time selector signal (TS) are applied to A-D425 and A-D424 respectively. In the presence of FT212 and the TS signal, the quantity 000 000 000 001 is admitted through A-D423 and communicated by way of A-D426 to the common line leading to the subtrahend input of the algebraic adder. This quantity is the quantity which is added to the control counter reading during each β cycle in order to increase that reading by unity. Also buffed into this line is the output of A-G242B (FIG. 13p). A-G242B supplies decimal zeros to the A-register during multi-word transfers involved in the input-output instructions. During such instructions, the instruction word stored in CR is continuously read through the algebraic adder. At the end of each series of ten word times, the quantity in CR must be increased either by 000 000 000 010 or 000 010 000 000. These two quantities are chosen depending upon whether the input-output instruction occurs in the δ or γ cycle of operation. During nine minor cycles the decimal zeros supplies to A-G242B are applied to the subtrahend input of the algebraic adder while the word in CR passes to the minuend input via A-G230. During the tenth minor cycle (also in the case of periodic memory check and memory clear at the end of 13 cycles) A-FF202 applies a permissive signal to A-G232A and A-G233A (FIG. 13p). Depending upon whether FT232 or FT233 is present, one or the other gate will admit the word which will augment the memory location either by ten in the γ position or in the δ position. The combination of A-FF203 (FIG. 13q) and A-FF202 (FIG. 13p) operate on A-G233A and A-G232A. The initiating pulse is applied to A-FF203 from the multiplier-quotient counter in the control circuits. When set, A-FF203 delivers a negative going pulse to A-V427 (FIG. 13q). After passing through a short delay, the output of A-V427 is applied to A-V428 (FIG. 13q). A-V428 drives A-G242A (FIG. 13q). This gate is operated by FT242 and is inhibited by time out. If these two signals are present plus that from A-V428 a p2 pulse passes through A-G242A to set a A-FF202 to restore A-FF203.

When set, A-FF202 applies a permissive signal to A-G233A and A-G232A (FIG. 13q). A separate amplifying valve A-V429 (FIG. 13p) inverts the output signal from A-FF202 and shifts its level to the +60 +90 volt range. This signal is applied to the two gates by way of A-D430 and A-D431 (FIG. 13p). A-G233A is also supplied by FT233 via A-D432 (FIG. 13p) and with the quantity from the cycling unit 000 010 000 000, by way of A-D433. A-G232A is supplied with FT232 by way of A-D434 and with the quantity from the cycling unit 000 000 000 010 by way of A-D435. In each case, the signals applied to these input diodes are all normally at +90 volts except during excitation when they drop to +60 volts. The output signals are buffed together to a common line by way of A-D436 and A-D437. This buffed output in turn is buffed into the outputs from A-G212D and A-G242B by way of A-D438 and A-D439. The common output is then applied by way of a capacitor to valve A-V440 (FIG. 13r). It is a normally conducting tube which drives a buffing diode A-D441.

Also arriving at junction point 442 are the signals generated in A-G110A, A-G110B, A-G109A and A-G112A (FIG. 13r). A-G109A consists of A-D443 through which is applied the FT109, A-D444 through which is applied a time out inhibition and A-D445 through which comes signals appearing on the high speed bus. A-G109A is that gate through which signals pass into the

A-register from the high speed bus by way of the algebraic adder. The output of A-G109A is buffed into a common line to the adder by way of A-D446 (FIG. 13r).

A-G112A is used during multiplication and is specifically for inserting the round off quantity 050 000 000 000. The position of the five in this case is in the second significant digit position since the quantity as it is developed in the A-register which will become the product is gradually shifted to the right. Since this round off quantity is inserted before multiplication begins the five will, by the time the product is fully determined, have been shifted into least significant position. The round off quantity is generated in the cycling unit in the form of negative going pulses between the limits of +90 and +60 volts. Also controlling gate A-G112A are FT112 and a time out inhibition signal applied through A-D447 and A-D448 respectively. The output of A-G112A is buffed into a common line with the output of A-G109A by way of diode A-D449.

The combined outputs of A-G109A and A-G112A are buffed into the outputs of A-G110A and A-G110B by way of A-D450 (FIG. 13r). The 110 gating is used during the initial three stages of multiplication during which three times the multiplicand is manufactured in the A-register. Through A-G110A comes the signal from the L-register representing the multiplicand. This signal exists as positive going pulses which are applied through a capacitor to A-V451. A-V451 generates negative going pulses between 90 volts and 60 volts. The output of A-V451 is applied to A-G110A via A-D452. A-G110A is also controlled by the buffed effect of FT110 and time out. The presence of FT110 and the absence of time out is required in order to have A-G110A open. One additional control signal applied to A-G110A is the sign gate (SG) signal from the cycling unit. This signal exists effectively from t1 to t86. Due to its polarity, its effect on this gate is to hold it open for the 11 digits plus the space between words during which the 11 digits of the multiplicand from the L-register may enter the A-register. A-G110B applies a zero to the sign position left vacant in the multiplicand by the SG signal applied to A-G110A. Purely for convenience the 050 000 000 000 from the cycling unit is used to obtain this one zero in the sign position. The CU signal is applied by way of A-D453 to gate A-G110B. In addition, FT110 is applied by way of A-D454, a time out inhibition is applied by way of A-D455, and finally the sign gate signal (SG) is applied by way of A-D456. The polarity of the sign gate signal is such that A-G110B is only open during the interval t86 to t1. This interval defines the 12th digit position and, therefore, selects only that most significant zero in the quantity from the cycling unit. The outputs of A-G110A and A-G110B are combined together through two diodes and through A-D457 are buffed into the input of A-V458. The output of A-V458 representing any signals appearing at A-G109A, A-G112A, A-G110A and A-G110B are buffed by way of A-D459 into junction point 442. Any signal appearing at junction point 442 passes through a short delay (FIG. 13n) bringing the timing of any of these signals into proper synchronism at a clock gate driver A-V460. The output of the clock gate driver gates tp's into a pulse forming flip-flop composed of A-V461 and A-V462. The output signals from A-V461 are connected directly into the subtrahend input of the algebraic adder and by way of A-V463 to the odd-even checker in the case of algebraic adder 2 (FIG. 13r).

The third gate in the 109 system which is directly effected by the outputs of A-G109D or A-G113 is A-G109F which gates a t14 pulse into A-FF101 (FIG. 13m). Due to the timing of the word appearing at the output of the algebraic adder, it is necessary to develop a separate signal which begins after the normal function table signal would arise and must extend into the next minor cycle beyond the point when the normal function table signal would disappear. In order to accomplish this

effect, a separate flip-flop A-FF101 is used to develop this one minor cycle signal but is placed in time with respect to the normal computer minor cycle. This signal exists from t_{14} of one minor cycle to t_{12} of the following minor cycle. Any signal to be applied to the gate system consisting of A-G109B (FIG. 13m) A-G109C (FIG. 13a) and A-G109F (FIG. 13m) is developed as soon as time out disappears which is approximately corresponding to t_1 . This signal then lasts for an entire minor cycle. However, the output of the algebraic adder is approximately t_9 which requires then that A-FF101 be set in order to open A-G109E (FIG. 13m) somewhere between t_1 to t_{14} . Since the algebraic adder may have been used in the previous minor cycle for other purposes it is not desirable to open A-G109E until at least t_9 when the last binary pulse of the previous addition has left the output of the algebraic adder. Therefore, the pulse used to set A-FF101 is t_{14} which is approximately five pulses into the space between words. Therefore, A-G109F receives the normal 109 signal via A-D409 (FIG. 13m). Also applied to A-G109F by way of A-D464 is the t_{14} pulse from the cycling unit. The signal applied to A-D409 is normally at +90 volts. When A-G109F is to pass a t_{14} the signal on A-D409 drops to +60 volts thus permitting the negative going pulse t_{14} to enter the gate. The output of the gate is capacitively coupled into a A-FF101 consisting of A-V465 and A-V466. The output of A-FF101 is obtained from the anode of A-V465. This signal is a positive going signal of sufficient amplitude to cause A-V467 to conduct. The output of A-V467 is a negative going signal between 90 and 60 volts and is applied by A-D468 to A-G109E (FIG. 13n). The restoring pulse to A-FF101 is a t_{12} occurring two pulses short of a four minor cycle after the t_{14} which originally set A-FF101. This pulse from the cycling unit is a negative going pulse capacitively coupled into the control grid of A-V466. Thus the signal applied to A-D467 and in consequence to gate A-G109E, is a minor cycle signal which is similar to those generated normally in the function table but displaced from the normal minor cycle time by approximately 12 pulses. The output of the algebraic adder is applied to A-V469 (FIG. 13n) in the form of positive going pulses through a capacitor. The output of A-V469 is clamped between plus 90 and plus 60 volts. The negative going pulses appearing at the anode of A-V469 representing the sum from the algebraic adder is applied to gate A-G109E by way of A-D470 (FIG. 13n). Provided a permissive signal is applied to A-D468, the algebraic adder output pulses pass through A-G109E into the A-register through A-D315, and into the normal recirculation path at junction point 315 (FIG. 13c).

F Register Schematic Write-Up

The F register is a one word mercury delay line type circulating register. During the M, N or P instructions, the F register stores three times the multiplicand and during the E instruction, it stores the extractor word.

The input to the F register is at F-100 from the high speed bus (see FIG. 19e). The negative going signal from the high speed bus is impressed upon diode F-D101 moving the potential of its anode from 90 to 60 volts in the presence of pulses. The diode forms one of the three inputs to gate F-G190A. The second signal which controls input gate F-G190A is FT190. Function table signal 190 is normally at plus 90 volts. Whenever signals on the high speed bus are intended to enter the F register, FT190 drops from plus 90 volts to plus 60 volts. In addition to FT190, a third signal, time-out (TO), also effects the operation of F-G190A. During the time-out period, the time-out signal is at plus 90 volts and is applied to input gate F-G190A via diode F-D102. If either signal, i.e., time-out or FT190 is at 90 volts, its potential appearing on the anode of its respective diode is sufficient to hold the junction point of this gate at plus 90 volts drawing current from a minus 106 volt sup-

ply through 12K ohm resistor. Therefore, in order for signals from the high speed bus to pass through this gate into the F register, it is necessary to have FT190 at 60 volts and time-out at 60 volts. Under these conditions, the signals on the high speed bus are impressed on diode F-D103.

The anode of diode F-D103 is connected to the anodes of two other diodes F-D104 and F-D105, respectively, which in turn are all connected into a six section delay line stick. Diode F-D104 connects the initial clear signal, $t(9-15)$ into the F register under the influence of the initial clear (IC) signal. Together the initial clear signal and the $t(9-15)$ signal join in F-G194 to pass into the F register. More details of this circuit will be given later. The signals appearing on diode F-D105 are those which have made a complete circulation of the F register and are returning to the starting point. This also will be discussed later.

The output of the six section delay line is a capacitor connected to the F-V107, a normally conducting amplifier tube. The output of this tube is obtained from the anode circuit and is connected into a one word mercury delay line chassis. The operation of the circuit of the mercury delay line chassis is described elsewhere. (See co-pending application S.N. 279,710.) The lower limit on the signal from F-V107 is clamped to plus 60 volts. The upper level of this signal is somewhere just below plus 80 volts. The pulses appearing on the anode of F-V107 are positive going pulses between plus 60 and just less than plus 80 volts.

The output of the one word mercury delay line chassis is applied to the grid of the F-V108, a normally conducting amplifier. The pulses obtained from the delay line circuit are negative going pulses. The output of F-V108 appearing on the anode are clamped between -71 volts and -88 volts. They are positive going signals which are then applied (see FIGURE 19c) to a typical clock gate array of diodes and resistors connected to the timing pulse generator. The operation of a typical clock gate circuit is described in co-pending application S.N. 279,710. The output of the clock gate is applied to a pulse forming flip-flop composed of F-V109 and F-V110. The recirculating pulses are obtained from the anode circuit of F-V109 and are 30 volts in amplitude and negative going between minus 4 volts and minus 34 volts. These pulses are applied to the grid of F-V111 (see FIG. 19a), a normally conducting amplifier whose principal purpose is to invert the polarity of the pulses from F-V109. The signals appearing on the anode of F-V111 are clamped between plus 70 and plus 95 volts. The output of F-V111 is applied to an eight section delay line normally referred to as a compensating delay. Such a compensating delay in this case is intended to equal that delay experienced by pulses leaving the normal output gate (to be described later) of the F register and passing over the high speed bus system to re-enter the input gate of either the F register or some other similarly timed register. The tap which leads off the compensating delay to F-V112 (see FIG. 19c) is adjustable, such that the timing at F-V112 is correctly timed with relation to any incoming signals.

F-V112 is a normally non-conducting amplifier the anode of which is clamped between plus 60 and plus 90 volts. The signals appearing on the anode of F-V112 are negative going signals of 30 volt amplitude. The output of F-V112 is applied to the clear gate F-G190B, F-G190V and F-G190A (see FIG. 19e), the input gate, must be considered simultaneously. In general, any occasion for opening an input of a register must also be accompanied by a closing of the clear gate so as to clear out any previously stored pulses circulating within the register in order not to superimpose the old set of pulses on top of the new. Both gates F-G190A and F-G190B are under the influence of FT190 and the time-out (TO) signal. As is normal elsewhere in this computer, the

function table signal 190 rises somewhat slowly and not sufficiently accurately in time to open and close these gates. The time-out signal is, therefore, used to control accurately the operation of these two gates. The time-out signal is a sharply determined signal generated by a fast acting flip-flop. In the case of F-G190A as previously described it is sufficient that all inputs fall from plus 90 to plus 60 volts for a signal to pass into the F register. In gate F-G190B, it is necessary that all signals combine to hold the normal recirculation pass at plus 90 volts thus masking any pulses delivered from F-V112. Since FT190 is normally at 90 volts when not present and at plus 60 when present, F-V113 (see FIG. 19c) is introduced in order to invert function table signal 190. The output of F-V113 is clamped between plus 60 and plus 90 volts. The 60 volt clamp normally conducts in the absence of function table signal 190. The effect of time-out (TO) on gate F-G190B is to add an additional gating signal to FT190 before it is applied to the clearing gate of the F register. During time-out, the time-out signal is at plus 60 volts and, therefore, permits diode F-D115 to impress on diode F-D116 the 60 volt potential. The potential on diode F-D116, therefore, overrides the 90 volt potential that may be on diode F-D114. However, when time-out releases diode F-D115 and holds diode F-D116 up to plus 90 the inhibition on the function table signal 190 is removed and it is allowed to pass through diode F-D117 to the main recirculation path of the F register. In summary, therefore, in the presence of function table signal 190 and in the absence of time-out signal diode F-D117 holds the recirculation path at plus 90 volts thus masking the signals from F-V112. A similar but distinct action occurs in gate F-G191 (see FIG. 19c) by virtue of the initial clear (IC) signal from the supervisory control. This signal is applied through diode F-D118 to the recirculation path of the F register. The IC signal is normally at plus 60 volts and, therefore, does not influence pulses occurring at the anode of F-V112. However, during the initial clear operation diode F-D118 is connected to a plus 90 volt source and therefore, masks or clears those pulses from the F register which appear at the anode of F-V112.

Except during initial clear or action by FT190 and the time-out signal, the pulses appearing at the anode of F-V112 normally reach diode F-D105 (see FIG. 19e) where they appear as normal recirculating pulses which then enter the six section compensating delay line. The purpose of this second compensating delay line is to adjust the timing of incoming pulses or recirculating pulses such that they reach the pulse former at the beginning of the mercury delay line chassis in time to gate clock pulses.

Concurrent to the clearing action applied to the F register through F-G191 from the initial clear signal from the supervisory control, initial clearing pulses, $t(9-15)$, are applied through F-G194 (see FIG. 19e) to the input of the F register. The entrance of these pulses is controlled by the initial clear (IC) signal from the supervisory control applied through diode F-D119, these pulses are put into the F register during the initial clear in order that the gain control circuit which appears in the mercury delay line circuit be limited by the presence of some pulses although not pulses that are significant and have any meaning.

The output of the F register is obtained from the anode circuit of the F-V110 of the pulse forming flip-flop (see FIGURE 19c). The pulses appearing at the anode of F-V110 are positive going pulses moving between the limits of minus 4 volts and minus 34 volts. The output pulses are applied to F-V119 (see FIG. 19a, upper right), a cathode follower which drives the checking circuits which compare the contents at all times of the two F registers which appear in duplicate.

The output pulses from V-110 are also applied to F-V120, a cathode follower (see FIG. 19a, middle), 75

which in turn drives F-V121. F-V121 drives two output gates, F-G188C and F-G192. There is also connected from the anode of F-V121 an output network for observing the contents of the F register with an oscilloscope. The outputs of F-G192 and F-G188C are buffed together to enter the high speed bus system. F-G188C is controlled by the combined action of FT188, the IER signal and the greater than or equal to three signal. FT188 appears during each of the three multiplication instructions, M, N, and P. The greater than or equal to three signal appears whenever a multiplier digit of three or more is set up in MQC. The IER signal occurs whenever the computer has finished with one multiplier digit and exists during the time in which the next multiplier digit is transferred into the multiplier quotient counter. FT188 is normally at 90 volts but when activated by one of the three multiplication instructions drops to plus 60 volts. The greater than or equal to three signal similarly is at plus 90 volts except during that period when a quantity in the multiplier quotient counter is greater than or equal to three during which time the signal falls from plus 90 volts to plus 60 volts. The IER signal is normally at 60 volts except during the IER stage when it rises to plus 90 volts. Thus FT188 and the greater than or equal to three signal are permissive in nature, while the IER signal is inhibitory. The IER signal is present on this gate in order to prevent the quantity in the F register from reaching the high speed bus when the new digit is set up in the MQC and which may be greater than or equal to three. As soon as the computer is ready to begin the actual transfer from the F register during multiplication, the IER signal disappears thus releasing gate F-G188C. The signals which pass from F-V121 to the high speed bus are negative going signals between plus 60 and plus 90 volts.

The purpose of gate F-G192 is to transmit the pulses stored in the F register to the high speed bus during the G instruction which calls for the transfer of the contents of the F register to the memory. F-G192, therefore, has only FT192 to control it. The normal level of FT192 is plus 90 volts. During the G instruction, this signal falls to plus 60 and, therefore, permits the negative going signals appearing at the anode of F-V121 to pass through to the high speed bus.

During the extract instruction a word is stored in the F register which indicates by the oddness and evenness of each of the computer digits within that word whether or not the corresponding digits of a second word are to be transferred into the A register to replace corresponding digits in a third word previously stored in the A register. The second word is obtained from the memory and is available on the high speed bus in synchronism with the words in the A and the F registers. In order for a computer digit to be considered odd, it is sufficient that a pulse appear in the least significant binary pulse position of the seven for that computer digit. The examination of this position occurs in the extract signal generator. A tap on the compensating delay line following F-V111 (see FIG. 19a) is connected to F-V122 (see FIG. 19b, top left). F-V122 amplifies all pulses which appear at the tap on the compensating delay and applies those pulses to the grid of F-V123. F-V123, a normally conducting amplifier with a D.C. restoration diode connected in its grid circuit, produces negative going pulses of 30 volt amplitude between the limits of plus 60 volts and plus 90 volts. The anode of F-V123 is connected to F-G193. The purpose of gate F-G193 is to select the least significant digit of each computer digit for examination. Three additional conditions are imposed on F-G193: FT193, the time selector signal (TS) and $p8n$. Each of these signals is normally at plus 90 volts. Whenever an extract instruction is called for, FT193 falls to plus 60 volts. When the word to be obtained from the memory finally becomes available, the

time selector signal (TS) also falls from plus 90 volts to plus 60 volts. The junction point of the gate, however, is still held at plus 90 by the combined influence of the $p8n$ signal and the signal from the anode of F-V123. The $p8n$ signal occurs every computer digit time and specifically occurs during least significant binary digit position of each computer digit. As $p8n$ appears the junction point of the three input diodes falls to plus 60. If there happens simultaneously to be a pulse on the anode of F-V123 then the junction point of F-G193 falls to plus 60 volts. This signal is communicated via diode F-D124 to clock gate driver F-V124. If $p8n$ occurs and there is no pulse at F-V123, the potential on the anode of F-V123 is plus 90 and this voltage supersedes all other controls on F-G193. Similarly, if F-V123 produces a pulse in the absence or at other times than a $p8n$ then the 90 volt potential applied through the $p8n$ input supersedes any signals on F-V123 thus holding the junction point at F-G193 at plus 90 volts. Thus the output of gate F-G193 is a result of the combined action of the pulses applied to F-V123 and the $p8n$ signal form the cycling unit. Whenever there is coincidence and a pulse is applied to F-V124, this indicates that the computer digit then passing from F-V111 (see FIG. 19a) in the main circulation path to F-V112 (see FIG. 19c) is considered an odd digit. F-V124 impresses this information on the clock gate F-CG195 which is a standard array of diodes and input signals and is discussed in copending application S.N. 279,710. In addition to the standard circuit, a separate input marked $t1n$ is applied to the TP minus side of the clock gate. The $t1n$ signal is for the purpose of setting the extract flip-flop composed of F-V125 and F-V126 (see FIG. 19d) to known or standard position before each examination made by the $p8n$ at gate F-G193 (see FIG. 19b). The output of the extract flip-flop composed of F-V125 and F-V126 is obtained from the anode circuits of the two valves. F-V125 is connected to F-V127 and F-V126 is connected to F-V128. F-V127 and F-V128 are cathode followers which produce the E1 and E2 signals. The E1 and E2 signals are the extract signals which are applied to the input gates in the A register in order to control the clearing out of the digit in A and replacing it with a digit from the high speed bus in the case of an odd digit in the extractor word in the F register. In the case of even digits in the F register, no action occurs. The extract flip-flop remains restored and no E1 or E2 signal appears to effect either the clearing or input of the A register. The magnitude of the voltage appearing at the outputs of F-V128 and F-V127 is approximately 30 volts.

While various tube designations and equivalent identification of components have been made throughout the accompanying description of schematic circuits of the various units comprising this system, it should be borne in mind, that any form of component suitable for the circuits can be utilized. Specifically, the various vacuum tubes utilized for this circuitry have been chosen from the group commercially designated as follows: 25L6, 6BE6, 25D7, 7AK7, 6AK5, 6AL5, 6AN5, 6AV6, 6SV7, 4032, 807, 2050, 5651, 5545, 6AL6 and 5687.

The many diodes which have been referred to throughout the description are of the germanium type and are of any form desired such as those numbered by Sylvania Corporation 1N34A or WE400A or B.

The type of resistors or capacitors utilized throughout in the circuits have been selected for the specific duties which they have to perform within these circuits and all the components can be selected by anyone skilled in the art to serve the purposes specified.

Many other modifications and variations of the invention, adapted to meet specific environmental circumstances, but not departing essentially from the essence thereof, will be apparent to those skilled in the art.

What we claim as new, and desire to secure by Letters Patent, is:

1. The combination comprising a full binary adder for operating on trains of electrical signals representative of alphabetical and numerical information; each of said trains comprising a first group of pulse positions representing by the combinations of pulses present and absent in individual positions of said group information of different relative values and a second group of pulse positions identifying by the absence of pulses therefrom information represented by said first group as numerical and identifying by the presence of pulses therein the information represented by said first group as alphabetical; said adder having a first input, a second input, and an output; means for applying a first train of electrical signals to said first input; means for applying a second train of electrical signals to said second input; a bypass network connecting said inputs and said output; a first means interposed between said first input of the adder and said bypass network for detecting the presence of pulses in the second group of pulse positions in first trains of electrical signals applied to said first input to cause said first trains of signals to be bypassed around said adder; and a second means interposed between said second input of the adder and said bypass network for detecting the presence of pulses in the second group of pulse positions in second trains of electrical signals applied to said second input to cause said second trains of signals to be bypassed around said adder.

2. The combination as defined in claim 1 further including a first signal source generating a first preselected sequence of signals, a second signal source generating a first preselected sequence of signals, a second full binary adder having first and second inputs and an output, the first input of said second binary adder being connected to the output of said first binary adder, means responsive to a first stimulus to connect said first signal source to the second input of said second binary adder and means responsive to a second stimulus to connect said second signal source to the second input of said second binary adder.

3. The combination as defined in claim 2 further including first and second storage devices for storing trains of electrical signals representative of information, each device having a means for allowing the entry of trains of electrical signals representative of information, a first conditionally responsive transfer network including gating means coupling the output of the first device to one of the inputs of the first adder and coupling the output of the second device to the other input of the first adder and a second conditionally responsive transfer network including gating means coupling the output of said second adder to the entry means of one of the said storage devices.

4. The combination as defined in claim 3 wherein said first network includes a conditionally responsive switching means actuated by a predetermined set of stimuli wherein in a first condition said switching means respectively couples the output of said first and second devices to said first and second inputs of said first adder and in a second condition said switching means respectively couples the outputs of said first and second devices to said second and first inputs of said first adder.

5. The combination as defined in claim 2 further including means selectively connected to one input of said first adder for modifying a train of electrical signals applied thereto, said means applying to said input the complement of the information represented by said train of signals.

6. The combination as defined in claim 1 further comprising means connected to both said first and second detecting means for inhibiting the output of said binary adder when any detecting means detects pulses in any second group of pulse positions in trains of electrical signals.

7. The combination as defined in claim 1 further including first and second storage devices for storing trains of electrical signals representative of information, each device containing a train of electrical signals representative of information constituting an entry, a first conditionally responsive transfer network including gating means respectively coupling the outputs of said first and second storage device to the first and second inputs of the said adder and a second conditionally responsive transfer network including gating means for coupling the output of said adder to the input of one of the said storage devices.

8. The combination as defined in claim 7 wherein said first network includes a conditionally responsive switching means actuated by a predetermined set of stimuli wherein in a first condition said switching means respectively couples the output of said first and second devices to said first and second inputs of said first adder and in a second condition said switching means respectively couples the outputs of said first and second devices to said second and first inputs of said first adder.

9. In combination a first register for storing a first train of electrical signals representative of numerical information; a second register for storing a second train of electrical signals representative of numerical information having a value which is a predetermined multiple of the value of the information of said first train; a third register having a recirculation storage path with a finite recirculation period, adding means having first and second inputs and an output; means for selectively connecting the output from said third register to said first input of said adding means and the input to said third register to said output of said adding means to effectively place said adding means in the recirculation path of said third register; a counter; means for applying electrical signals to said counter to represent the complement of a numerical value; signal generating means responsive to the complement of information in said counter to generate a first control signal when the complement of the value in said counter is less than said predetermined multiple and a second control signal when the complement of the information in said counter is equal to or greater than said predetermined multiple; means responsive to said first control signal for connecting said first register for the period of one recirculation of said third register to said second input whereby the contents of said first register is added to the contents of said third register; means responsive to said second control signal for connecting said second register to said second input for the period of one recirculation of said third register whereby the contents of said second register are added to the contents of said third register; said third register accumulating the results of such successive additions; means operative when the connection of said first register to said second input is effective to step said counter forward one count; means operative when the connection of said second register to said second input is effective for stepping said counter forward a number of counts equal to said predetermined multiple; and means for generating an ending signal when said counter reaches the limit of its count to clear said counter, to initiate the introduction of a new value into said counter, and to cause the contents of said third register to shift one digit to the right.

10. The combination defined in claim 9 wherein said third register comprises first, second and third recirculation paths; said first recirculation path providing a time of recirculation equivalent to the length of time required for the contents of the register to pass a given point, said second recirculation path providing a time of recirculation which is shorter than the recirculation time of said first path by an amount of time required for a single decimal digit to pass a given point, said third recirculation path providing a time of recirculation which is longer than the recirculation time of said first path by an amount of time required by a single decimal digit to pass a given

point; a first normally open gate in said first recirculation path; a second normally closed gate in said second recirculation path; and a third normally closed gate in said third recirculation path; means responsive to said ending signal to generate a control signal for closing said first gate and opening said second gate for a period equivalent to the recirculation time of said first path.

11. The combination defined in claim 9 wherein said multiple is three.

12. The combination defined in claim 10 further including a fourth register, second means for selectively connecting the output from said third register to the input of said fourth register, and a fourth normally closed gate in said selective connecting means, said control signal opening said fourth gate for the period of time that the least significant decimal digit of the information in said third register is present at said fourth gate whereby the least significant digit of the information accumulating in said third register is transferred to said fourth register upon each generation of said control signal.

13. An algebraic adder comprising a first binary adder circuit having a first input, a second input, a first output and a carry output; a first input terminal to said algebraic adder and a second input terminal to said algebraic adder; first, second, third, and fourth input gating means; said first gating means being connected between said first input terminal and said first input to said binary adder, said second input gating means being connected between said second input terminal and said first input to said binary adder, said third input gating means being connected between said second input terminal and said second input to said binary adder, and said fourth input gating means being connected between said first input terminal and said second input to said binary adder; first means for simultaneously inhibiting said first and third gating means and for opening said second and fourth gating means; means for applying a first train of electrical pulses representative of a first numerical quantity to said first input terminal to said algebraic adder, second means for applying a second train of electrical pulses to said second input terminal to said algebraic adder; comparator means for comparing the absolute magnitudes of said first and second quantities; means responsive to a determination of said comparator that the second quantity is larger than said first quantity for generating signals for simultaneously inhibiting said first and third gating means and for opening said second and fourth gating means whereby the train of electrical pulses applied to said first input terminal is transmitted to said second input to said binary adder and the train of pulses applied to the second input terminal is transmitted to the first input to said binary adder.

14. The apparatus defined in claim 13 further including a complementor inserted between the output of said third and fourth gating means and said second input to said binary adder for obtaining the nines complement of the quantities applied to said second input to said binary adder.

15. The algebraic adder defined in claim 14 wherein said binary adder comprises a third input, and further including gating means connected to said third input to provide additional signals for correcting the nines complement to a tens complement output.

16. An algebraic adder for producing the sums of two quantities represented by combinations of pulses in trains of seven electrical pulse positions wherein the four least significant pulse positions represent a numerical value, the two immediately more significant pulse positions identify the presence of alphabetic or symbolic information, and wherein the most significant pulse position represents a check position for checking the existence of an erroneous pulse combination; said algebraic adder comprising a first input terminal to which a first quantity is applied; a second input terminal to which a second input quantity is applied; a binary adder having first, second, and third in-

put terminals and first and carry output terminals; means for connecting said first input terminal to said first input of said binary adder; means for connecting said second input terminal to said second input of said binary adder; means connected to said first and second input terminal for checking information supplied thereto for the presence of pulses in said more significant pulse positions which identify alphabetical and symbolical information; a flip-flop responsive to said checking means for generating an output signal upon the determination of the existence of alphabetical or symbolical information applied to said first or second input terminals; a gating means connected between the output of said binary adder and an output terminal from said algebraic adder; a first by-pass path connected between said first input terminal and said output terminal; and second by-pass path connected between said second input terminal and said output terminal; normally closed gating means in each of said by-pass paths; and means for applying the output from said flip-flop to said gating means in said by-paths to open said gating means and to said gating means between the output of said binary adder and said output terminal to close said gating means whereby alphabetical or symbolical information is transmitted from said first and second input terminals to said output terminal in unmodified form.

17. A multiplication and division counter and control apparatus comprising a counter, means for stepping said counter in response to an individual multiplication and an individual division operation, first read gates connected to the output of said counter, second read gates connected to the output of said counter, a matrix connected to the outputs of said first and second read gates, control lines selectively energized by said matrix in accordance with the value in said counter when said first read gates are opened and selectively energized in accordance with the complement of the value in said counter when said second read gates are opened, and means for selectively opening said first and second read gates.

18. The apparatus defined in claim 17 wherein said means for opening said first and second read gates maintains said second read gates open during multiplication operations.

19. The apparatus defined in claim 17 further including means for causing said means for opening said read gates to alternately open said first and second read gates on successive division operations.

20. The apparatus defined in claim 17 wherein said means for selectively opening said read gates comprises a single stage binary counter.

21. The apparatus defined in claim 17 further comprising output gates connected to said matrix for emitting the value decoded by said matrix at the end of a division operation.

22. The apparatus defined in claim 21 further including means for sequentially opening said output gates to cause the value decoded by said matrix to be emitted in serial form.

23. The apparatus defined in claim 17 further including means for inserting the complement of a multiplier digit into said counter in parallel form.

24. The apparatus defined in claim 17 wherein said control lines include a first line which is energized when the counter has been stepped to the limit of its count, a second line which is energized when the value in said counter is less than a predetermined amount, and a third line which is energized when the value in said counter is equal to or greater than said predetermined amount.

25. An information comparator comprising a first information input, a second information input, a sign input, a magnitude detector, means for connecting said first information input and said second information input to said magnitude detector, said magnitude detector generating an output signal when information applied to said first information input has a greater value than information applied to said second information input, an equality de-

tector, means connecting said first and second inputs to said equality detector, said equality detector generating an output signal when information applied to said second input is not equal in value to information applied to said first input, a first sign detector, means for connecting said first input and said sign input to said first sign detector, said first sign detector generating an output signal when sign information applied to said first input is different from sign information applied to said sign input, a second sign detector, means for connecting said second and sign inputs to said second sign detector, said second sign detector generating an output signal when sign information applied to said second input is different from sign information applied to said sign input, and gating means connected to the outputs of said magnitude, equality, first sign and second sign detectors and selectively opened to pass output signals only when the algebraic value of information applied to a predetermined one of said first and second inputs is greater than the algebraic value of the information applied to the other of said first and second inputs.

26. The comparator defined in claim 25 further comprising a magnitude memory for storing the output information from said magnitude detector.

27. The comparator defined in claim 25 further comprising an equality storage for storing output information from said equality detector.

28. The comparator defined in claim 25 further including a sign comparator, means for connecting the output from said first and second sign detectors, said sign comparator generating an output signal when the outputs from said first and second sign detectors are different.

29. The comparator defined in claim 28 further including a result sign storage for storing output information from said sign comparator.

30. The comparator defined in claim 25 wherein said magnitude detector comprises a first gate, a second gate, and a flip-flop, means for connecting said first input to said first gate so that information applied to said first input opens said first gate, means for connecting said first input to said second gate so that information applied to said first input closes said second gate, means for connecting said second input to said first gate so that information applied to said second input closes said first gate, means for connecting said second input to said second gate so that information applied to said second input opens said second gate, and means for connecting said flip-flop to the outputs of said first and second gates to indicate which gate was last opened.

31. The comparator defined in claim 25 wherein said equality detector comprises a third gate and a fourth gate, means for connecting said first input to said third and fourth gates so that information applied to said first input opens said third gate and closes said fourth gate, and means for connecting said second input to said third and fourth gates so that information applied to said second input closes said third gate and opens said fourth gate.

32. In an information handling system apparatus for performing division, said apparatus comprising a first electronic register having a recirculation storage path, an input and an output and containing a first train of electrical pulses representative of a dividend; a second electronic register having an input and an output and containing a second train of electrical pulses representative of a divisor; an electronic algebraic adder having a first input, a second input, binary adder means connected to said first input, a complementor connected between said second input and said binary adder means to supply to said adder means the nine's complement of a number applied to said second input, and means connected to said binary adder means for correcting nine's complement results to ten's complement results; first gating means connected between the output of said first register and the first input to said algebraic adder, second gating means

connected between the output from said algebraic adder and the input to said first register whereby said algebraic adder may be selectively inserted into the recirculation path of said first register; the output from said second register being connected to said second input to said algebraic adder; division control means including a counter, a counter read-out means including a device for reading out the complement of the value stored in the counter, means for rendering the complement read-out effective and non-effective, complement signal generating means in said division control means for generating a signal rendering the complement in the algebraic adder effective to cause said adder to subtract the information applied to said second input from the information stored in said first register each time the information stored in said first register circulates through its recirculation path; means in said algebraic adder responsive to the generation of a carry by said binary adder means to step said counter during subtraction; means responsive to the interruption of carry generation by said binary adder means during subtraction to halt subtraction operations and to cause read-out of the value stored in the counter; third register means for receiving the values read-out from said counter; means in said division control means in response to the interruption of repeated subtraction operations for rendering said complement in said algebraic adder ineffective to complement, for rendering the read-out complement in said division control means operative to complement, for causing the contents of said first register to shift one digit to the left thereby producing an effective multiplication of that quantity by the radix, and for initiating another series of repeated transfers of the contents of said first register through said algebraic adder producing repeated additions of the contents of the quantity applied to the second input to said algebraic adder by the second register to the contents of the first register; means responsive to each circulation of the contents of the first register through said algebraic adder to step said counter, means responsive to the generation of a carry by said binary adder means as a result of said additions to interrupt said series of additions, to cause read-out of the complement of the quantity stored in said counter to said third register, to shift the contents of said first register one digit to the left, to render the complement in said algebraic adder operative, to render said read-out complement in said division control means inoperative, and to initiate a new series of repeated circulations of the contents of said first register through said algebraic adder to repeatedly subtract the contents of said second register therefrom.

33. A mathematical sign determining apparatus comprising first and second dynamic storage devices for storing trains of electrical pulses representing information including a mathematical sign, a first half-adder having first and second inputs and first and second outputs, means for connecting the output of said first storage device to said first input of said first half-adder, means for connecting to said second input of said first half-adder a source

of electrical signals representative of a first mathematical sign, said first output of said first half-adder being energized when said first mathematical sign and the sign from said first storage device are dissimilar and said second output from said first half-adder being energized when said two signs are similar, a second half-adder having third and fourth inputs and third and fourth outputs, means for connecting to said third input the output from said second storage device, means for connecting to said fourth input a source of electrical signals representative of a second mathematical sign, said third output being energized when the sign from said second storage device is similar to said second mathematical sign and said fourth output being energized when said sign from said second storage device and said second mathematical sign are dissimilar, and means for indicating when said first and third outputs are energized.

34. The combination as defined in claim 33 further including an apparatus for performing mathematical operations on trains of electrical signals representative of information, means for selectively coupling the outputs of both devices to the said apparatus, said apparatus combining the portion of the train of electrical signals not representative of a mathematical sign from said first device with the corresponding portion of the train of electrical signals from said second device.

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