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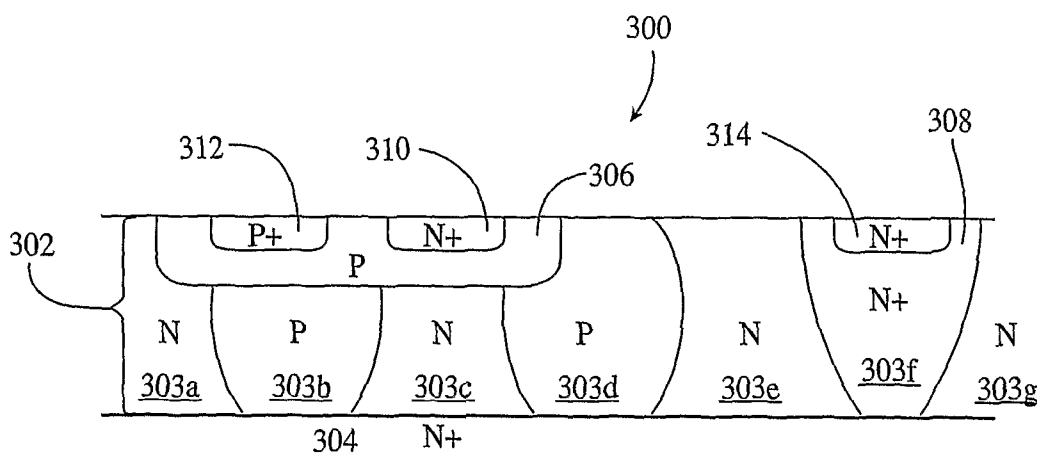
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(54) Title: BIPOLAR STRUCTURES HAVING IMPROVED BVCEO/RCS TRADE-OFF MADE WITH DEPLETED COLLECTOR COLUMNS



(57) Abstract: In accordance with the invention, there are various methods of making an integrated circuit comprising a bipolar transistor. According to an embodiment of the invention, the bipolar transistor can comprise a substrate, a collector comprising a plurality of alternating doped regions, wherein the plurality of alternating doped regions alternate in a lateral direction from a net first conductivity to a net second conductivity, and a collector contact in electrical contact with the collector. The bipolar transistor can also comprise a heavily doped buried layer below the collector, a base in electrical contact with a base contact, wherein the base is doped to a net second conductivity type and wherein the base spans a portion of the plurality of alternating doped regions, and an emitter disposed within the base, the emitter doped to a net first conductivity, wherein a portion of the alternating doped region under the emitter is doped to a concentration of less than about  $3 \times 10^{12} \text{ cm}^{-2}$ .

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UNITED STATES PATENT APPLICATION  
FOR  
BIPOLAR METHOD AND STRUCTURE HAVING IMPROVED BVCEO/RCS TRADE-  
OFF MADE WITH DEPLETABLE COLLECTOR COLUMNS  
BY  
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## DESCRIPTION OF THE INVENTION

### Field of the Invention

[0001] The subject matter of this application relates to integrated circuits having bipolar transistors. More particularly, the subject matter of this application relates to bipolar transistors comprising super junctions.

### Background of the Invention

[0002] Many bipolar transistors have their size set to meet a required collector resistance ( $R_{CS}$ ).  $R_{CS}$  is proportional to collector resistivity and to the length of the collector between the base and buried layer. Thus, to minimize  $R_{CS}$ , one typically minimizes both collector resistivity and collector length.

[0003] Fig. 1 shows a conventional NPN bipolar transistor 100 consisting of an N- collector 102 formed over an N+ buried layer 104, a P base 106 and an N+ sinker 108 formed in the N-collector 102, an N+ emitter 110 and a P+ base contact 112 formed in the P base 106, and an N+ collector contact 114 formed in the N+ sinker 108. In the conventional bipolar transistor, the collector 102 is doped to the same conductivity throughout. The breakdown voltages  $BV_{CEO}$  and  $BV_{CBO}$  of the conventional bipolar transistor 100 are both reduced when the resistivity of N- collector 102 is reduced. These breakdown voltages are also reduced when the length of the N- collector 102 is reduced to less than the collector depletion layer thickness at breakdown. Thus, there is a tradeoff between breakdown and  $R_{CS}$  for bipolar transistors of a given size. Conventional PNP bipolar transistors typically consist of a similar structure but have inverted conductivities.

[0004] One approach to increase the breakdown of a transistor with a given collector doping is to cascade the collector with a junction field effect transistor (JFET). The area required for the JFET, however, can consume more area than is saved by reducing the collector doping in some cases so other methods and structures are desired.

[0005] Thus, there is a need to overcome these and other problems of the prior art to provide a method and a device to reduce the size of a bipolar transistor while also achieving an improved  $R_{CS}$ .

### **SUMMARY OF THE INVENTION**

[0006] In accordance with the invention, there are various methods of making an integrated circuit comprising a bipolar transistor. According to an embodiment of the invention, the bipolar transistor can comprise a substrate, a collector comprising a plurality of alternating doped regions, wherein the plurality of alternating doped regions alternate in a lateral direction from a net first conductivity to a net second conductivity, and a collector contact in electrical contact with the collector. The bipolar transistor can also comprise a heavily doped buried layer below the collector, a base in electrical contact with a base contact, wherein the base is doped to a net second conductivity type and wherein the base spans a portion of the plurality of alternating doped regions, and an emitter disposed within the base, the emitter doped to a net first conductivity, wherein a portion of the alternating doped region under the emitter is doped to a concentration of less than about  $3 \times 10^{12} \text{ cm}^{-2}$ .

[0007] According to another embodiment of the invention there is another integrated circuit comprising a bipolar transistor. The bipolar transistor can comprise a

substrate, a base formed in the substrate, a collector comprising a doped first region doped to a net first conductivity disposed under the base, wherein the base is doped to a net second conductivity type, and doped second regions doped to a net second conductivity disposed on opposite sides of the doped first region, and a collector contact in electrical contact with the collector. The bipolar transistor can also comprise a more heavily doped layer buried below the doped first region and the doped second regions, and an emitter doped to a net first conductivity disposed within the base, wherein the doped region disposed beneath the emitter depletes at a reverse bias collector base voltage of magnitude less than an absolute value of  $BV_{CEO}$ .

**[0008]** According to another embodiment of the invention there is a method of forming an integrated circuit comprising a bipolar transistor. The method can comprise forming a device layer doped over a substrate, forming a buried region in the device layer, and forming a first layer doped to a net first conductivity over the device layer.

The method can also comprise forming at least one second conductivity type region using a dopant material of a second conductivity type in the first layer, wherein the at least one second conductivity type region is bounded by at least one region doped to the first conductivity type, forming a base region in the first layer, and forming an emitter in a portion of the base region.

**[0009]** According to another embodiment of the invention there is a method of making a bipolar transistor. The method can comprise forming a device layer over a substrate, forming a buried region under the device layer, and forming a patterned layer over the device layer, wherein the patterned layer comprises an opening that exposes a portion of the device layer. The method can also comprise providing dopants of a first

conductivity type to the exposed portion of the device layer to form a column of first conductivity type dopants in the device layer, providing dopants of a second conductivity type to the exposed portion of the device layer to form an intrinsic base in the device layer, forming an emitter that contacts a portion of the exposed device layer, and forming an emitter contact over the emitter.

**[0010]** According to another embodiment of the invention there is a method of making a bipolar transistor. The method can comprise forming a device layer over a substrate, forming a buried region under the device layer, forming a patterned insulator over the device layer, wherein the patterned insulator comprises a first opening that exposes a first portion of the device layer, providing dopants of a first conductivity type to the exposed first portion of the device layer to form a base in the device layer, and forming a patterned base insulator over the exposed first portion of the device layer, wherein the patterned base insulator comprises a second opening that exposes an area of the first portion of the device layer. The method can also comprise providing dopants of a second conductivity type to the exposed area of the first portion of the device layer to form a column of second conductivity type dopants in the device layer, forming an emitter that contacts a portion of the exposed area of the first portion of the device layer, and forming an emitter contact over the emitter.

**[0011]** It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

[0012] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate several embodiments of the invention and together with the description, serve to explain the principles of the invention.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0013] Fig. 1 shows a conventional NPN bipolar transistor.

[0014] Fig. 2 depicts a schematic representation of a super junction.

[0015] Fig. 3A depicts a schematic representation of an NPN bipolar transistor comprising a super junction structure according to various embodiments of the invention.

[0016] Fig. 3B depicts a schematic representation of a PNP bipolar transistor comprising a super junction structure according to various embodiments of the invention.

[0017] Figs. 4A-4E depict schematic representations of a method for forming an integrated circuit device comprising an NPN and a PNP bipolar transistor comprising a super junction structure according to various embodiments of the invention.

[0018] Figs. 5A-5I depict schematic representations of a method for forming an integrated circuit device comprising a PNP double polycrystalline silicon bipolar transistor architecture comprising a super junction structure according to various embodiments of the invention.

[0019] Figs. 6A-6I depict schematic representations of a method for forming an integrated circuit device comprising a PNP single polycrystalline silicon bipolar transistor architecture comprising a super junction structure according to various embodiments of the invention.

[0020] Fig. 7 is a plot of exemplary collector resistances achieved using the super junction structures described herein in comparison to conventional collector structures.

[0021] Fig. 8 is another plot of exemplary collector resistances achieved using the super junction structures described herein in comparison to conventional collector structures.

[0022] Fig. 9 depicts an exemplary dopant profile for a super junction structure before a diffusion step.

[0023] Figs. 10A-C depict exemplary dopant profiles for a super junction structure after a diffusion step.

### **DESCRIPTION OF THE EMBODIMENTS**

[0024] In the following description, reference is made to the accompanying drawings that form a part thereof, and in which is shown by way of illustration specific exemplary embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention and it is to be understood that other embodiments may be utilized and that changes may be made without departing from the scope of the invention. The following description is, therefore, not to be taken in a limited sense.

[0025] Notwithstanding that the numerical ranges and parameters setting forth the broad scope of the invention are approximations, the numerical values set forth in the specific examples are reported as precisely as possible. Any numerical value, however, inherently contains certain errors necessarily resulting from the standard deviation found in their respective testing measurements. Moreover, all ranges disclosed herein are to be understood to encompass any and all sub-ranges subsumed



therein. For example, a range of "less than 10" can include any and all sub-ranges between (and including) the minimum value of zero and the maximum value of 10, that is, any and all sub-ranges having a minimum value of equal to or greater than zero and a maximum value of equal to or less than 10, e.g., 1 to 5.

**[0026]** Prior to discussing the specific features of the exemplary embodiments, a discussion of a super junction structure is provided. According to various embodiments, a super junction structure can be formed at the collector-base junction in an NPN bipolar transistor 200 and a PNP bipolar transistor 250 as shown in Fig. 2A and Fig. 2B, respectively. Generally, a super junction structure is a structure that allows the doping on the lightly doped side of a PN junction to be increased and the length of the lightly doped side to be reduced as compared to the same junction in a conventional device for a given breakdown voltage. In a bipolar transistor device, the uniform collector doping, such as that shown in conventional device 100 of Fig. 1 is replaced with alternative P and N doped columns, such as those shown in Figs. 2A and 2B. Moreover, the doping of the columns can be matched. For example, the thickness of the P column times its doping can be equal to the thickness of the N column times its doping.

**[0027]** The thickness of the columns can be determined such that when the junction is reverse biased, they totally deplete before breakdown is reached. The super junction column properties can be expressed as:

$$\text{[0028]} \quad t_N \cdot N_D = t_p \cdot N_A \quad [1]$$

**[0029]** where  $t_N$  = thickness of the N column,  $N_D$  = doping of the N column,  $t_p$  = thickness of the P column, and  $N_A$  = doping of the N column; and

$$\text{[0030]} \quad t_{\max} = 2E_{\max} \cdot \epsilon / q \cdot N \quad [2]$$

[0031] where  $t_{\max}$  = maximum thickness of the column,  $E_{\max}$  = maximum electric field before breakdown occurs,  $\epsilon$  = dielectric constant of the substrate, such as silicon,  $N$  = doping level of the column.

[0032] The doping of the depletable columns is disconnected from breakdown because once it depletes, a constant electric field extends the length of the column.

Breakdown is approximated by:

$$[0033] \quad BV = E_{\text{crit}} * l \quad [3]$$

[0034] where  $BV$  = breakdown voltage,  $E_{\text{crit}}$  = critical electric field for breakdown,  $l$  = length of the column.

[0035] The depletable columns of a super junction can be used to form drain regions that have shorter and higher doped layers than in conventional DMOS structures of the same breakdown voltage. In particular, they provide reduced "on" resistance in a given area.

[0036] Super junctions can also be applied to reduce  $R_{\text{cs}}$  in bipolar transistor devices. Moreover, similar column structures can be used to improve both NPN and PNP bipolar transistor devices, such as when both devices are formed in the same wafer.

[0037] Turning to Fig. 2A, a schematic representation of an NPN bipolar transistor 200 is shown that comprises a collector, generally referred to as 202, formed over an N+ buried layer 204, a P base 206 and an optional N+ sinker 208 formed in the collector 202, an N+ emitter 210 and a P+ base contact 212 formed in the P base 206, and an N+ collector contact 214 formed in the optional N+ sinker 208. The doping of the collector 202 comprises alternating N and P doped regions or columns 203a-i.

**[0038]** In Fig. 2B, a schematic representation of PNP bipolar transistor 250 is shown that comprises a collector, generally referred to as 252, formed over a P+ buried layer 254, an N base 256 and an optional P+ sinker 258 formed in the collector 252, a P+ emitter 260 and an N+ base contact 262 formed in the N base 256, and a collector contact 264 formed in the optional P+ sinker 208. The doping of the collector 252 comprises alternating P and N doped regions or columns 253a-i.

**[0039]** As shown in Fig. 2A, at least the region under the base 206 comprises alternating N and P columns 203c-203f. Similarly in Fig. 2B, at least the region under the base 256 comprises alternating N and P columns 253c-253f.

**[0040]** The steps used to form the N and P columns can be similar for the NPN bipolar transistor device as for the PNP bipolar transistor device. For example, the NPN can be formed over an N+ buried layer, such as N+ buried layer 204, and the PNP can be formed over a P+ buried layer, such as P+ buried layer 254. Further, the collector contact 214 can be formed in an N column, such as 203h. Alternatively an optional N+ sinker, such as sinker 208, can be formed through N and/or P columns, such as columns 203g and 203h, to connect the buried layer to the surface of the device. The PNP collector contact can be formed in a similar manner to that of the NPN but with the conductivity types inverted.

**[0041]** In prior art super junctions, the integrated doping of the P and N columns may require matching. According to various embodiments of the invention, there is provided a super junction structure that relaxes the matching requirements while at the same time, retaining the  $R_{cs}$  improvement, at least for bipolars designed to meet a required  $BV_{CEO}$ .

**[0042]** According to various embodiments, a bipolar transistor device can be provided that comprises a super junction structure comprising at least one depletable column of a first conductivity type located under an emitter. The depletable column can be formed adjacent to at least one column doped to a second and opposite conductivity type. According to various embodiments, second conductivity type columns can be formed adjacent to each side of the depletable column. The adjacent columns can have doping high enough so that these columns do not totally deplete under reverse bias.

**[0043]** For example, the column under the emitter can be designed to deplete at a reverse bias voltage applied to the collector and the base with a magnitude that is less than the absolute value of  $BV_{CEO}$ . Moreover, in contrast to conventional structures, structures described herein can comprise columns (such as P-type columns) of opposite conductivity adjacent to collector columns (such as an N-type column) located below the emitter. According to various embodiments, a depletion layer can spread out from the vertical junction between P-type and N-type columns when the collector base junction is reverse biased. The thickness and doping of the N-type column can be determined using equations 1 and 2 described herein to insure that the N-type column totally depletes. This is also in contrast to conventional structures that cannot provide similar depletion across the entire length of the collector from a vertical junction.

Conventional structures can only deplete from the horizontal junction between the base and the collector. And in some embodiments, the depletable column can be designed to totally deplete before  $BV_{CEO}$  occurs in the column.

**[0044]** According to various embodiments, the depletion characteristics of the columns can be achieved by controlling the doping of the column under the emitter. As

discussed above, the depletable column under the emitter doped to the first conductivity and the columns of the second conductivity can be formed adjacent to the column under the emitter. According to various embodiments, the doping in a horizontal direction between the adjacent second conductivity type columns can be less than about  $3 \times 10^{12}$  atoms/cm<sup>2</sup>. In some cases, this doping can be less than about  $1 \times 10^{12}$  atoms/cm<sup>2</sup>. This doping can be derived using equation [2] for  $t_{\max}$  shown above using a suitable  $E_{\max}$ . It is to be noted that  $E_{\max}$  can be a slowly decreasing function of breakdown voltage. As such, there may not be a single solution for all voltages.

**[0045]** According to various embodiments of the invention, the length of the columns can be controlled to provide a given breakdown voltage. For example, the general length of the depletable column under the emitter, between the base and the buried layer, can be determined by  $BV_{CEO}$ . Thus, the length of column can be determined using equation [3] above. In an exemplary embodiment,  $E_{\text{crit}}$  may be  $2 \times 10^5$  V/cm. It is to be noted that  $E_{\text{crit}}$  can decrease slowly as the voltage increases so the results obtained from equation [3] may slightly underestimate the minimum attainable voltage for low voltage (e.g., about 30 V) devices. However, this calculation can be used as a general guide line to determine the length of the base to the buried layer.

**[0046]** Figs. 3A and 3B depict NPN and PNP bipolar transistor devices 300 and 350, respectively, having super junction structures such as those described herein. In Fig. 3A, the NPN bipolar transistor 300 comprises a collector, generally referred to as 302, formed over an N+ buried layer 304, a P base 306 and an optional N+ sinker 308 formed in the collector 302, an N+ emitter 310 and a P+ base contact 312 formed in the P base 306, and a collector contact 314 formed in the optional N+ sinker 308. NPN

bipolar transistor 300 can also comprise alternating P and N doped regions or columns (labeled 303a-e). Moreover, NPN bipolar transistor 300 can comprise alternating N and N+ regions (303 e-g), which can be considered a single N-type column.

**[0047]** In Fig. 3B, the PNP bipolar transistor 350 comprises a collector, generally referred to as 352, formed over a P+ buried layer 354, an N base 356 and an optional P+ sinker 358 formed in the collector 352, a P+ emitter 360 and an N+ base contact 362 formed in the N base 356, and a collector contact 364 formed in the optional P+ sinker 308. PNP bipolar transistor 350 can also comprise alternating N and P doped regions or columns (labeled 353a-e).

**[0048]** According to various embodiments, the NPN bipolar transistor 300 and the PNP bipolar transistor 350 comprise depleteable columns 303c and 353b, respectively, under the emitters 310 and 360, respectively. The depleteable columns 303c and 353b are bounded on two sides by opposite conductivity type columns, such as 303b and 303d, and 353a and 353c, respectively, that do not totally deplete. This is in contrast to conventional superjunction structures that can have alternating P and N columns all of which totally deplete. Moreover, the embodiments of the present invention described herein require fewer columns than conventional devices.

**[0049]** According to various embodiments, the layers that are used to make the columns shown in Fig. 3A and Fig. 3B can also be used to make collectors of conventional structure bipolar devices, such as those shown in Fig. 1, that have a lower  $BV_{CEO}$  and that are formed on other areas of the integrated circuit. Thus, it is possible to use common process steps to make two sets of bipolar devices having two different breakdown voltages.

**[0050]** An integrated circuit device having multiple bipolar transistors devices comprising a super junction structure, where one of the columns of the super junction structure is self-aligned to the emitter is contemplated. An example of forming such an integrated circuit device is shown in Figs. 4A-4E. Further, a method of forming a double polycrystalline silicon ("polysilicon" or "poly") bipolar transistor architecture is shown in Figs. 5A-5I and a method of forming a single poly transistor architecture is shown in Figs. 6A-6I. The bipolar transistors can comprise a depletable column of the super junction structure that is self-aligned to the emitter. Moreover, various methods of making bipolar transistor devices, some of which are described herein, comprise the use of multiple ion implantations at various energies to form the collector columns without the use of multiple epitaxial collector layer depositions.

**[0051]** As stated above, a depiction of a method for forming NPN and PNP bipolar transistors devices comprising super junction structures on the same integrated circuit is shown in Figs. 4A-4E. In Fig. 4A, a device layer 410, such as an N-type epitaxial layer, can be formed over a substrate 415. According to various embodiments, the device layer 410 can have a thickness in the range of about 2  $\mu\text{m}$  to about 15  $\mu\text{m}$ . The substrate 415 can comprise a semiconductor wafer 417, such as silicon, and a bond oxide 419. According to various embodiments, the device layer 410 can be bonded to the semiconductor wafer 417 with the bond oxide 419 to facilitate handling.

**[0052]** In Fig. 4B, heavily doped N<sup>+</sup> and P<sup>+</sup> buried regions 422 and 424 can be formed in the device layer 410. According to various embodiments, the heavily doped N<sup>+</sup> buried region 422 can be formed by masking and ion implanting N-type ions into a portion of the device layer 410. Similarly, the heavily doped P<sup>+</sup> buried region 424 can

be formed by masking and ion implanting P-type ions into another portion of the device layer 410. Heavily doped N+ buried region 422 can serve as the buried region for the NPN device and heavily doped P+ buried region 424 can serve as the buried region for the PNP device. According to various embodiments, the N+ buried region 422 can be made by implanting phosphorous (or another N-type dopant) with an energy of about 70 KeV to about 130 KeV and a dose of about  $8E14$  ions/cm<sup>2</sup> to about  $3E15$  ions/cm<sup>2</sup>. In still further embodiments, the N+ buried region 422 can be made by implanting phosphorous (or another N-type dopant) with an energy of about 100 KeV and a dose of about  $1E15$  ions/cm<sup>2</sup>. According to various embodiments, the P+ buried region 424 can be made by implanting BF<sub>2</sub> (or another P-type dopant) with an energy of about 20 KeV to about 40 KeV and a dose of about  $8E14$  ions/cm<sup>2</sup> to about  $3E15$  ions/cm<sup>2</sup>. In still further embodiments, the P+ buried region 424 can be made by implanting BF<sub>2</sub> (or another P-type dopant) with an energy of about 30 KeV and a dose of about  $1E15$  ions/cm<sup>2</sup>. According to some embodiments, buried regions 422 and 424 can be formed using a diffusion process.

**[0053]** As shown in Fig. 4C, a first epitaxial layer 430 is formed over the device layer 410. According to various embodiments, the first epitaxial layer 430 can be doped N-type. Subsequently, the first epitaxial layer 430 can be masked and implanted with dopants that will form the collector. For example, the first epitaxial layer 430 can be masked, shown for example with mask layer 432, to allow P-type ions 434 to be implanted into regions 435 and 436 of the first epitaxial layer 430 above the buried region 422 when the first epitaxial layer 430 is doped N-type. The mask layer 432 can also be defined to allow P-type ions 434 to be implanted into one region 437 of the first



epitaxial layer 430 above the buried region 424 when the first epitaxial layer 430 is doped N-type. According to various embodiments, the P-type ions, such as boron or the like, can be implanted with an energy from about 150 KeV to about 220 KeV and a dose from about  $1\text{E}12$  ions/cm<sup>2</sup> to about  $1\text{E}13$  ions/cm<sup>2</sup>. In still further embodiments, the P-type ions, such as boron or the like, can be implanted with an energy of about 180 KeV and a dose of about  $5\text{E}12$  ion/cm<sup>2</sup>. According to various embodiments, the dose can be chosen so as to provide the appropriate doping required for the desired breakdown voltage after the ions are diffused.

**[0054]** As shown in Fig. 4D, a second epitaxial layer 440 can be formed over the first epitaxial layer 430. According to various embodiments, the second epitaxial layer 440 can be doped N-type. Portions of the first epitaxial layer 430 and the second epitaxial layer 440 form the region that will be, generally, collector 448 and collector 449, in the NPN and PNP bipolar transistors, respectively. Subsequently, the integrated circuit 400 can be heated to allow the dopants 434 implanted into regions 435, 436, and 437 to diffuse and form the P-type columns 445, 446 in the NPN collector 448 and to form P-type column 447 in the PNP collector 449. According to various embodiments, the NPN collector 448 doping can be from about  $1\text{E}15$  ions/cm<sup>2</sup> to about  $5\text{E}16$  ions/cm<sup>2</sup>. For a BVCEO of about 70V, a doping of about  $2\text{E}15$  ions/cm<sup>2</sup> can be used. Further, the columns 445 and 446 can have a length of about 5 microns and a thickness of about 8 microns for a device having a BVCEO of about 70V. Moreover, equations 1 and 2, as set forth herein, can be used to set the length and thickness for a desired breakdown voltage. Still further, the thickness of the column under the emitter can be greater than the similar dimension of the emitter above it so that substantially the entire emitter lies

above a collector column of like conductivity type. According to various embodiments, the PNP collector 449 doping can be from about  $1\text{E}15$  ions/cm<sup>2</sup> to about  $1\text{E}17$  ions/cm<sup>2</sup> and in some embodiments, about  $4\text{E}15$  ions/cm<sup>2</sup>. Further, for a device with a BVCEO of about 70V, the column 447 can have a length of about 4 microns and a thickness of about 4 microns. Moreover, equations 1 and 2, as set forth herein, can be used to set the length and thickness for a desired breakdown voltage. Still further, the thickness of the column under the emitter can also be greater than the similar dimension of the emitter above it so that substantially the entire emitter can lie above a collector of like conductivity type.

**[0055]** According to various embodiments, the N-type columns of the transistors can be formed from the two N-type epitaxial layers 430 and 440. Further, the P-type columns can be formed from the P-type implant into the epitaxial layers 430 and 440. Moreover, the P-type implant is diffused down to the N+ and P+ buried regions 422 and 424, respectively, and up through the second N epitaxial layer 440 after it is deposited. While the figures show two columns formed in the NPN collector 448 and one column formed in the PNP collector 449, it is to be understood that more columns can be formed. Moreover, the above described procedure can be carried out multiple times.

**[0056]** As shown in Fig. 4E, a P-type base 450 is formed in the NPN collector 448 and an N-type base 460 is formed in the PNP collector 449. To form the base 450, the surface can be masked by a first mask (not shown) and P-type ions can be implanted to form the P-type base 450. Similarly, the surface can be masked, either by the first mask or by a second mask (not shown) and N-type ions can be implanted to form the N-type base 460. Subsequently, an N-type emitter 470 can be formed in the P-type base

450 and a P-type emitter 480 can be formed in the N-type base 460. An N column, which is a depletable column, thus forms directly below the emitter 470. Similarly, a P column, which is a depletable column, forms directly below the emitter 480.

**[0057]** According to various embodiments, the integrated circuit can continue being processed according to procedures known to one of ordinary skill in the art. For example, an interlevel dielectric layer can be formed, contact holes can be patterned, and the various components can be electrically connected as required. Moreover, additional NPN and PNP bipolar devices, such as conventional devices of figure 1 can be formed on the same integrated circuit. This allows bipolar transistors having different breakdown voltages to be formed on the same device.

**[0058]** According to various embodiments, a double poly transistor architecture having a super junction structure is provided. The double poly transistor architecture comprising a collector having a super junction structure as described herein can be formed. Several options exist for masking the collector implants. According to various embodiments, the columns of the super junction structure can be formed by a series of implants at different energies made through an opening in a base poly. For example, an opening can be formed that exposes the emitter regions through the base poly and the collector is implanted through the opening. Outside edges of the base poly can be patterned in a subsequent step using conventional photoresist masks. Alternatively, the base poly can be patterned with a single mask to leave a pattern such that the stack of the base poly and overlying layer of oxide is thick enough to block high energy implanted ions from reaching the island. The photoresist can also pattern oversized openings to expose the emitter such that edges of the base poly stack are exposed

around the perimeter of the emitter openings. An implant can then form the collector. Still further, the collector of the double poly transistor architecture can be formed after the base poly etch and before photoresist removal using an ion implantation. In this case, the field oxide should be thick enough to block the collector implant in unwanted areas.

**[0059]** An exemplary method of forming a double poly transistor 500 is shown for example in Figs. 5A-I. While Figs. 5A-I depict forming a PNP bipolar transistor, it is to be understood that an NPN bipolar transistor can be similarly formed by inverting the doping scheme. Turning to Fig. 5A, integrated circuit 500 includes a P+ buried layer 502 and an N-type epitaxial layer 504 (also called a device layer) formed on the P+ buried layer 502. The N-type epitaxial layer 504 forms the N-type collector columns of the resulting bipolar transistor. A P+ sinker implant 505 can also be formed by implanting P-type ions into the N-type epitaxial layer 504. According to various embodiments, the P+ sinker implant can be boron or the like, and can be implanted with an energy from about 30 KeV to about 70 KeV and a dose from about  $8E14$  ions/cm<sup>2</sup> to about  $5E15$  ions/cm<sup>2</sup>. In still further embodiments, the P+ sinker implant can be implanted with an energy of about 50 KeV and a dose of about  $2E15$  ion/cm<sup>2</sup>.

**[0060]** In Fig. 5B, a field oxide 508 is formed and the P+ sinker 505 implant is diffused into the epitaxial layer 504 so as to form P+ sinker 506 that contacts the buried layer 502. The field oxide 508 is formed so as to expose the P+ sinker 506 and a portion 510 of the epitaxial layer 504 that will form the device region. According to various embodiments, the field oxide 508 can be a local oxidation oxide, such as

LOCOS, or a shallow trench isolation oxide (STI). It will be understood, however, that other field oxide techniques are also contemplated.

**[0061]** Fig. 5C shows a patterned first poly that acts as a base contact 512 where the base contact 512 is patterned using a patterned oxide 514 and a patterned photoresist 516. The base contact 512 can be patterned to expose the epitaxial layer 504 through a hole 518 (also called an opening). P-type ions can be implanted into the epitaxial layer 504 through the hole 518. According to various embodiments, the P-type ions can be implanted with an energy of 1 MeV and dose of  $1.4 \text{ E}12 \text{ cm}^{-2}$ ; energy of 750 KeV and dose of  $1.4 \text{ E}12 \text{ cm}^{-2}$ ; energy of 500 KeV and dose of  $1.4 \text{ E}12 \text{ cm}^{-2}$ ; energy of 300 KeV and dose of  $1.0 \text{ E}12 \text{ cm}^{-2}$ ; energy of 140 KeV and dose of  $1.2 \text{ E}12 \text{ cm}^{-2}$ ; and energy of 30 KeV and dose of  $6.2 \text{ E}11 \text{ cm}^{-2}$ . The patterned photoresist 516 can be removed and the device 500 can be heated to diffuse the implanted P-type ions so as to form a column 520 in the epitaxial layer 504, as shown in Fig. 5D. Thus, the column 520 can be a region in the epitaxial layer 504 (also called the collector) that is doped to a net P-type conductivity. Moreover, the column 520 can span the thickness of the epitaxial layer 504 so as to contact the buried layer 502.

**[0062]** As shown in Fig. 5E an N-type intrinsic base 522 can be formed by implanting N-type ions using the base contact 512 and the patterned oxide 514 as a mask. Subsequently, the intrinsic base implant can be annealed so as to form the intrinsic base 522 that is contacted by the base contact 512. The intrinsic base 522 can be thus be formed in a surface portion of the epitaxial layer 504.

**[0063]** Fig. 5F shows the device 500 after spacers 524 have been formed on the sidewalls of the hole 518. Spacers 526 can also be formed on the sides of the base

contact 512 and patterned oxide 514. Spacers 524 and 526 can be formed by etching an insulating layer that has been deposited over the device 500. According to various embodiments, the spacers can comprise an oxide, a nitride, or an oxinitride, or combinations thereof. For example, the spacers can comprise silicon oxide.

Alternatively, the spacers can comprise a thin layer of silicon oxide (such as  $\leq$  about 100 Å) contacting the intrinsic base 522 with a layer of nitride disposed over the thin silicon oxide.

**[0064]** Subsequently, a layer of conducting material, such as polysilicon can be deposited over the device 500. The conducting material can then be patterned to form a second poly that acts as an emitter contact 528 and which is disposed between the sidewall spacers 524, as shown in Fig. 5G. Moreover, the conducting material can be patterned to form a collector contact 530 over the P+ sinker 506. According to various embodiments, an emitter 532 can be formed in a portion of the epitaxial layer 504 exposed by the hole 518 under the emitter contact. For example, the emitter 532 can be formed in the portion of the epitaxial layer 504 exposed between the spacers 526. Thus, the emitter 532 contacts the epitaxial layer 504. According to some embodiments, the emitter 532 can be formed by diffusing dopants into the intrinsic base 522 from the conducting material that forms the emitter contact 528. While in other embodiments, the emitter 532 can be formed by ion implanting dopants into the intrinsic base 522. Thus, the emitter 532 can be formed to be self aligned over the collector column 520.

**[0065]** In Fig. 5H an interlevel dielectric (ILD) 532 can be deposited and patterned to form windows that expose portions of the base contact 512, emitter contact

528, and collector contact 530. The ILD can be an oxide. As shown in Fig. 5I, a metal layer can be deposited over the ILD 532 and patterned so as to form base contact metal 534, emitter contact metal 536, and collector contact metal 538 through the patterned windows. According to various embodiments, the metal layer can comprise aluminum, titanium, or other contact metals as will be known to one of ordinary skill in the art.

**[0066]** In the case of the single poly transistor architecture, the opening through the base poly can be used to define the emitter area and the super junction column self aligned thereunder.

**[0067]** Figs. 6A-I depict a method of forming an integrated circuit having a super junction structure in a single poly PNP bipolar transistor 600. While Figs. 6A-6I depict forming a PNP bipolar transistor, it is to be understood that an NPN bipolar transistor can be similarly formed by inverting the doping scheme. Turning to Fig. 6A, transistor 600 includes a P+ buried layer 602 and an N-type epitaxial layer 604 (also called a device layer) formed on the P+ buried layer 602. Portions of the N-type epitaxial layer 604 form N-type collector columns of the resulting bipolar transistor. A P+ sinker implant 605 can also be formed by implanting P-type ions into the N-type epitaxial layer 604. According to various embodiments, boron (or another P-type dopant) can be implanted with an energy from about 30 KeV to about 100 KeV with a dose from about  $8E14$  ions/cm<sup>2</sup> to about  $4E15$  ion/cm<sup>2</sup>. In still further embodiments, boron (or another P-type dopant) can be implanted with an energy of about 50 KeV and a dose of about  $2E15$  ions/cm<sup>2</sup>.

**[0068]** In Fig. 6B, an insulator, such as a field oxide 608 is grown and the P+ sinker 605 implant is diffused into the epitaxial layer 604 so as to form P+ sinker 606

that contacts the buried layer 602. According to various embodiments, the field oxide 608 can be also be a local oxidation oxide, such as LOCOS, or a shallow trench isolation oxide (STI). It will be understood, however, that other field oxide techniques are also contemplated.

**[0069]** In Fig. 6C the field oxide 608 is patterned to form a hole (also called an opening) so as to expose a portion 610 of the epitaxial layer 604 that will form the device region. Fig. 6C also shows the result of an N-type base implantation 611 into the exposed portion of epitaxial layer 604. According to various embodiments, phosphorous (or another N-type dopant) can be implanted with an energy from about 30 KeV to about 100 KeV with a dose from about  $2 \times 10^{13}$  ions/cm<sup>2</sup> to about  $5 \times 10^{14}$  ion/cm<sup>2</sup>. In still further embodiments, phosphorous (or another N-type dopant) can be implanted with an energy of about 50 KeV and a dose of about  $5 \times 10^{13}$  ions/cm<sup>2</sup> to about  $2 \times 10^{14}$  ions/cm<sup>2</sup>.

**[0070]** In Fig. 6D, N-type base implantation 611 has been diffused to form an N-type base 612. A base oxide 614 can also be grown over the N-type base 612. As shown in Fig. 6E, an opening 616 through the base oxide 614 is formed using a patterned photoresist 618 so as to expose an area of the device layer. In Fig. 6F a P-type collector column 620 can be formed with the mask used to form the opening 616. P-type ions can be implanted through the opening so that the collector column 620 is self aligned to the opening 616. According to various embodiments, the P-type implants can can be made boron (or another P-type dopant) with an energy of 1 MeV and dose of  $1.4 \times 10^{12}$  cm<sup>-2</sup>; energy of 750 KeV and dose of  $1.4 \times 10^{12}$  cm<sup>-2</sup>; energy of 500 KeV and dose of  $1.4 \times 10^{12}$  cm<sup>-2</sup>; energy of 300 KeV and dose of  $1.0 \times 10^{12}$  cm<sup>-2</sup>; energy of 140 KeV



and dose of  $1.2 \text{ E}12 \text{ cm}^{-2}$ ; and energy of 30 KeV and dose of  $6.2 \text{ E}11 \text{ cm}^{-2}$ . Moreover, the collector column 620 can span the thickness of the epitaxial layer 604 so as to contact the buried layer 602.

**[0071]** A heavily doped emitter poly 622 can then be formed over the opening 616 so that the emitter area is defined by the opening 616 that defines the area where the emitter poly contacts the base 612, as shown in Fig. 6G. At this point in the process the collector column 620 can be properly diffused and activated after the photoreist 618 has been removed. According to various embodiments, the collector can be diffused before depositing the emitter poly. Fig. 6H shows a patterned hole 622 that allows dopants to be diffused into the base so as to form a base contact region 624. In Fig. 6H, dopants from the heavily doped emitter poly 622 can be diffused to form an emitter 626 positioned, and self-aligned above the collector column 620.

**[0072]** Fig. 6I shows a patterned ILD 632 having trenches that expose the base contact region 624. The ILD can be deposited over the emitter poly 622. As shown in Fig. 6I, a metal layer can be deposited over the ILD 632 and patterned so as to form base contact metal 634, emitter contact metal 636, and collector contact metal 638 through the patterned trenches. According to various embodiments, the metal layer can comprise aluminum, titanium, or other contact metals as will be known to one of ordinary skill in the art.

**[0073]** According to various embodiments, the absolute value of VCB can be less than the absolute value of  $BV_{CEO}$  when the portion of the column under the emitter totally depletes. This can be true for a PNP device where VCB and  $BV_{CEO}$  are both negative as well as the case for an NPN device where they both are positive. According

to various embodiments of an NPN device, the region that depletes can be the column in the epitaxial layer, in which the collector is formed, under the emitter. Moreover, according to various embodiments, the column under the emitter can be the column that depletes regardless of how the device is formed.

**[0074]** The collector-base capacitance of the devices made with the depletable columns will differ from that of the conventional device. For example, it may initially be higher. This can be a result of the higher doping of the columns and increased junction area. The collector-base capacitance, however, will drop abruptly when the columns totally deplete.

**[0075]** According to various embodiments, devices made with depletable columns under the emitter, such as those described herein, can have BVCEO of at least 69 V and an HFE of about 83 for an NPN device, and at least 82 V and an HFE of about 101, for a PNP device. HFE is understood to be a measure of current gain and can be described, generally, as the ratio of collector current to base current at a specified collector to emitter voltage. This is in contrast to a BVCEO of 37 V for a conventional NPN device and 40 V for a conventional PNP device made with the same doped layers but without the depletable columns under the emitters. Moreover, these new devices can have lower  $R_{CS}$ , such as 1.5k $\Omega$ , than devices made with similar emitter areas.

**[0076]** Exemplary collector resistances achieved using the super junction structures described herein (shown with a solid line) in comparison to collector resistances conventional collector structures (shown with a solid line with slashes) are shown in Figs. 7 and 8. In these figures, the NPN collector doping is about 2E15 atoms cm<sup>-3</sup>, the columns length is about 5 microns and the column thickness is about 8

microns. The PNP collector doping is about  $4 \times 10^{15}$  atoms  $\text{cm}^{-3}$ , the column length is about 4 microns and the column thickness is about 4 microns.

**[0077]** According to various embodiments, the devices of the present invention comprise a depletable collector column under the emitter and the devices can achieve a BVCEO about twice that of conventional devices. Moreover, the NPN devices of the present invention comprising a depletable collector column under the emitter can achieve an Rcs about three times lower than that of conventional devices. Still further, the PNP devices of the present invention comprising a depletable collector column under the emitter can achieve an Rcs about 30% less than conventional devices.

**[0078]** In a still further exemplary embodiment, a PNP bipolar transistor comprising a super junction structure described herein can have a breakdown of about 30 V. In this example, the column under the emitter can be about  $2.3 \mu\text{m}$  long before the base is formed. The columns of the super junction can be formed using, for example, six boron implants, with the following parameters: energy of 1 MeV and dose of  $1.4 \times 10^{12} \text{ cm}^{-2}$ ; energy of 750 KeV and dose of  $1.4 \times 10^{12} \text{ cm}^{-2}$ ; energy of 500 KeV and dose of  $1.4 \times 10^{12} \text{ cm}^{-2}$ ; energy of 300 KeV and dose of  $1.0 \times 10^{12} \text{ cm}^{-2}$ ; energy of 140 KeV and dose of  $1.2 \times 10^{12} \text{ cm}^{-2}$ ; and energy of 30 KeV and dose of  $6.2 \times 10^{11} \text{ cm}^{-2}$ . Moreover in this exemplary embodiment, the ions can be implanted into an N-type epitaxial layer about  $3 \mu\text{m}$  thick doped to a concentration of about  $5.0 \times 10^{15} \text{ cm}^{-3}$ . The epitaxial layer can be formed on a buried layer doped to a concentration of about  $2.0 \times 10^{17} \text{ cm}^{-3}$ . The dopant of the buried layer can be, for example boron. Still further, the super junction column implants can be made through a  $1.0 \mu\text{m}$  wide mask opening and the dopants can be diffused, for example at  $1200^\circ\text{C}$  for about 15 min. An exemplary dopant profile

for before the diffusion is shown in Fig. 9 and an exemplary dopant profile after the diffusion is shown in Figs. 10A-C.

**[0079]** While the invention has been illustrated with respect to one or more implementations, alterations and/or modifications can be made to the illustrated examples without departing from the spirit and scope of the appended claims. In addition, while a particular feature of the invention may have been disclosed with respect to only one of several implementations, such features may be combined with one or more other features of the other implementations as may be desired and advantageous for any given or particular function. Furthermore, to the extent that the terms "including", "includes", "having", "has", "with", or variants thereof are used in either the detailed description and the claims, such terms are intended to be inclusive in a manner similar to the term "comprising."

**[0080]** Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

**[0081]** Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

WHAT IS CLAIMED IS:

1. An integrated circuit comprising a bipolar transistor comprising:
  - a substrate;
  - a collector comprising a plurality of alternating doped regions, wherein the plurality of alternating doped regions alternate in a lateral direction from a net first conductivity to a net second conductivity;
  - a collector contact in electrical contact with the collector;
  - a heavily doped buried layer below the collector;
  - a base in electrical contact with a base contact, wherein the base is doped to a net second conductivity type and wherein the base spans a portion of the plurality of alternating doped regions; and
  - an emitter disposed within the base, the emitter doped to a net first conductivity, wherein a portion of the alternating doped region under the emitter is doped to a concentration of less than about  $3 \times 10^{12} \text{ cm}^{-2}$  in a lateral direction.
2. The integrated circuit comprising a bipolar transistor according to claim 1, wherein the portion of the alternating doped region under the emitter is doped to a concentration of less than about  $2 \times 10^{12} \text{ cm}^{-2}$  in a lateral direction.
3. The integrated circuit comprising a bipolar transistor according to claim 1, wherein a portion of the alternating doped regions disposed beneath the emitter is doped to a net first conductivity type.

4. The integrated circuit comprising a bipolar transistor according to claim 3, wherein a width of the doped region disposed beneath the emitter is substantially the same as a width of the emitter.
5. The integrated circuit comprising a bipolar transistor according to claim 3, wherein the doped region disposed beneath the emitter extends from the base to the more heavily doped buried layer.
6. The integrated circuit comprising a bipolar transistor according to claim 5, wherein the length, as defined from the base to the buried layer, of the alternating doped region under the emitter is defined by  $BV_{CEO}/E_{crit}$ .
7. The integrated circuit comprising a bipolar transistor according to claim 1 further comprising:
  - an electrical sinker in electrical contact with the collector contact and in electrical contact with the more heavily doped buried layer.
8. The integrated circuit comprising a bipolar transistor according to claim 3 further comprising:
  - at least one doped second region disposed adjacent to the doped region disposed under the emitter, wherein the at least one doped second region is doped to a net second conductivity type.

9. The integrated circuit comprising a bipolar transistor according to claim 8, wherein the doped region disposed beneath the emitter depletes at a reverse bias collector base voltage of magnitude less than an absolute value of  $BV_{CEO}$ .
10. The integrated circuit comprising a bipolar transistor according to claim 8, wherein the doped second regions disposed adjacent to the doped region disposed beneath the emitter depletes under a reverse bias collector voltage less than  $BV_{CEO}$ .
11. The integrated circuit comprising a bipolar transistor according to claim 1, further comprising a second bipolar transistor, wherein the bipolar transistor has a breakdown voltage greater than the second bipolar transistor.
12. The integrated circuit comprising a bipolar transistor according to claim 8, wherein the doped second regions disposed adjacent to the doped region disposed beneath the emitter do not totally deplete at a magnitude of collector base voltage less than the magnitude of the  $BV_{CEO}$  breakdown voltage.
13. The integrated circuit comprising a bipolar transistor according to claim 1, wherein an integral across the width of the doped region under the emitter has a value of less than about  $3E12$  ions/cm<sup>2</sup>.
14. The integrated circuit comprising a bipolar transistor according to claim 1, wherein the portion of doped region under the emitter is self aligned to the emitter.

15. An integrated circuit comprising a bipolar transistor comprising:
- a substrate;
  - a base formed in the substrate;
  - a collector comprising a doped first region doped to a net first conductivity disposed under the base, wherein the base is doped to a net second conductivity type, and doped second regions doped to a net second conductivity disposed on opposite sides of the doped first region;
  - a collector contact in electrical contact with the collector;
  - a more heavily doped layer buried below the doped first region and the doped second regions; and
  - an emitter doped to a net first conductivity disposed within the base, wherein the doped region disposed beneath the emitter depletes at a reverse bias collector base voltage of magnitude less than an absolute value of  $BV_{CEO}$ .
16. The integrated circuit comprising a bipolar transistor according to claim 15, wherein the doped second regions disposed adjacent to the doped first region do not totally deplete under reverse bias of the collector to base junction.
17. The integrated circuit comprising a bipolar transistor according to claim 15, wherein the bipolar transistor is an NPN bipolar transistor comprising a  $BV_{CEO}$  of at least 69 Volts.



18. The integrated circuit comprising a bipolar transistor according to claim 15, wherein the bipolar transistor is a PNP bipolar transistor comprising a  $BV_{CEO}$  of at least 82 Volts.

19. The integrated circuit comprising a bipolar transistor according to claim 15, wherein the bipolar transistor is an NPN bipolar transistor, and wherein the collector is doped with at least about  $2 \times 10^{15}$  atoms/cm<sup>3</sup>.

20. The integrated circuit comprising a bipolar transistor according to claim 15, wherein the bipolar transistor is an NPN bipolar transistor, and wherein first doped region has a length of about 4  $\mu\text{m}$  to about 6  $\mu\text{m}$ , and further wherein the first doped region has a width of about 7  $\mu\text{m}$  to about 9  $\mu\text{m}$ .

21. The integrated circuit comprising a bipolar transistor according to claim 15, wherein the bipolar transistor is a PNP bipolar transistor, and wherein the collector is doped with at least about  $4 \times 10^{15}$  atoms/cm<sup>3</sup>.

22. The integrated circuit comprising a bipolar transistor according to claim 15, wherein the bipolar transistor is a PNP bipolar transistor, and wherein first doped region has a length of about 3  $\mu\text{m}$  to about 5  $\mu\text{m}$ , and further wherein the first doped region has a width of about 3  $\mu\text{m}$  to about 5  $\mu\text{m}$ .

23. The integrated circuit comprising a bipolar transistor according to claim 18 further comprising:

a PNP bipolar transistor comprising a  $BV_{CEO}$  of at least 82 Volts.

24. The integrated circuit comprising a bipolar transistor according to claim 15, wherein the doped region disposed beneath the emitter is self aligned to the emitter.

25. A method of forming an integrated circuit comprising a bipolar transistor, the method comprising:
- forming a device layer over a substrate;
  - forming a buried region in the device layer;
  - forming a first layer doped to a net first conductivity over the device layer;
  - forming at least one second conductivity type region using a dopant material of a second conductivity type in the first layer, wherein the at least one second conductivity type region is bounded by at least one region doped to the first conductivity type;
  - forming a base region in the first layer; and
  - forming an emitter in a portion of the base region.
26. The method of forming an integrated circuit comprising a bipolar transistor according to claim 25, wherein the emitter is formed over one of the at least one second conductivity type regions.
27. The method of forming an integrated circuit comprising a bipolar transistor according to claim 25, wherein the emitter is formed over one of the at least one first conductivity type regions.
28. The method of forming an integrated circuit comprising a bipolar transistor according to claim 25 further comprising:
- forming a second buried region in the device layer, wherein the first buried region is doped to a net first conductivity, and wherein the second buried region is doped to a

net second conductivity, and further wherein an NPN bipolar transistor is formed using the first buried region and a PNP bipolar transistor is formed using the second buried region.

29. The method of forming an integrated circuit comprising a bipolar transistor according to claim 25, wherein the region over which the emitter is formed comprises a width substantially the same as a width of the emitter.
30. The method of forming an integrated circuit comprising a bipolar transistor according to claim 25, wherein the region adjacent the region over which the emitter is formed does not totally deplete under reverse bias of the collector base junction.
31. The method of forming an integrated circuit comprising a bipolar transistor according to claim 25, wherein the region over which the emitter is formed totally depletes when an absolute value of  $V_{CB}$  is less than an absolute value of  $BV_{CEO}$ .
32. The method of forming an integrated circuit comprising a bipolar transistor according to claim 25, wherein the bipolar transistor is an NPN bipolar transistor comprising a  $BV_{CEO}$  of at least 69 Volts.
33. The method of forming an integrated circuit comprising a bipolar transistor according to claim 25, wherein the bipolar transistor is a PNP bipolar transistor comprising a  $BV_{CEO}$  of at least 82 Volts.

34. The method of forming an integrated circuit comprising a bipolar transistor according to claim 25, wherein the bipolar transistor is an NPN bipolar transistor, and wherein the first layer is doped with at least about  $2 \times 10^{15}$  atoms/cm<sup>3</sup>.

35. The method of forming an integrated circuit comprising a bipolar transistor according to claim 25, wherein the bipolar transistor is an NPN bipolar transistor, and wherein the at least one second conductivity type regions formed by diffusing the portion of the dopant material of a second conductivity type from the first epitaxial layer into the first buried region has a length of about 4  $\mu\text{m}$  to about 6  $\mu\text{m}$ , and further wherein the region doped to the first conductivity type has a width of about 7  $\mu\text{m}$  to about 9  $\mu\text{m}$ .

36. The method of forming an integrated circuit comprising a bipolar transistor according to claim 25, wherein the bipolar transistor is a PNP bipolar transistor, and wherein the at least one second conductivity type region is doped with at least about  $4 \times 10^{15}$  atoms/cm<sup>3</sup>.

37. The method of forming an integrated circuit comprising a bipolar transistor according to claim 25, wherein the bipolar transistor is a PNP bipolar transistor, and wherein the at least one region doped to the first conductivity type has a length of about 3  $\mu\text{m}$  to about 5  $\mu\text{m}$ , and further wherein the at least one region doped to the first conductivity type has a width of about 3  $\mu\text{m}$  to about 5  $\mu\text{m}$ .

38. The method of forming an integrated circuit comprising a bipolar transistor according to claim 25 further comprising:
- forming a second bipolar transistor, wherein the bipolar transistor has a breakdown voltage greater than the breakdown voltage of the second bipolar transistor.

39. A method of making a bipolar transistor, the method comprising:
- forming a device layer over a substrate;
  - forming a buried region under the device layer;
  - forming a patterned layer over the device layer, wherein the patterned layer comprises an opening that exposes a portion of the device layer;
  - providing dopants of a first conductivity type to the exposed portion of the device layer to form a column of first conductivity type dopants in the device layer;
  - providing dopants of a second conductivity type to the exposed portion of the device layer to form an intrinsic base in the device layer;
  - forming an emitter that contacts a portion of the exposed device layer; and
  - forming an emitter contact over the emitter.

40. A method of making a bipolar transistor, the method comprising:
- forming a device layer over a substrate;
  - forming a buried region under the device layer;
  - forming a patterned insulator over the device layer, wherein the patterned insulator comprises a first opening that exposes a first portion of the device layer;
  - providing dopants of a first conductivity type to the exposed first portion of the device layer to form a base in the device layer;
  - forming a patterned base insulator over the exposed first portion of the device layer, wherein the patterned base insulator comprises a second opening that exposes an area of the first portion of the device layer;
  - providing dopants of a second conductivity type to the exposed area of the first portion of the device layer to form a column of second conductivity type dopants in the device layer;
  - forming an emitter that contacts a portion of the exposed area of the first portion of the device layer; and
  - forming an emitter contact over the emitter.



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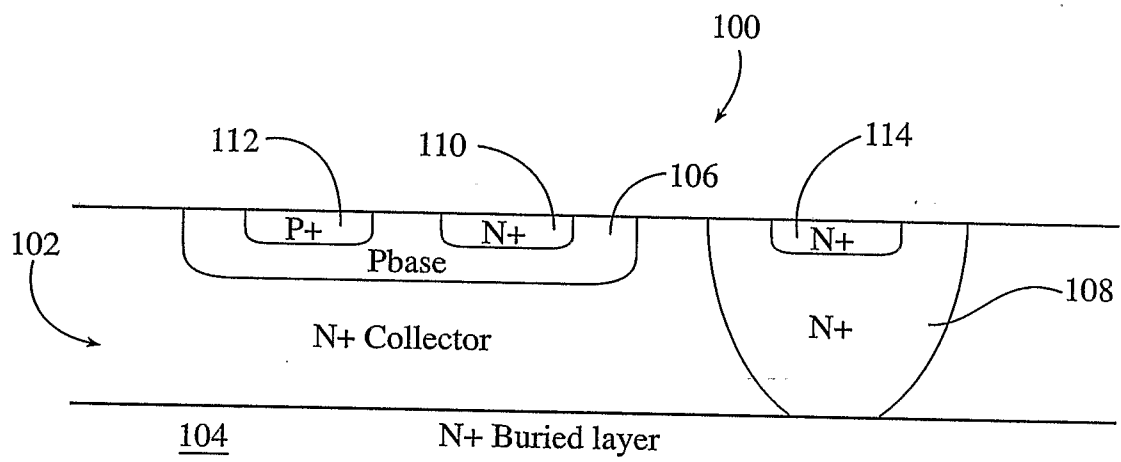


Fig 1

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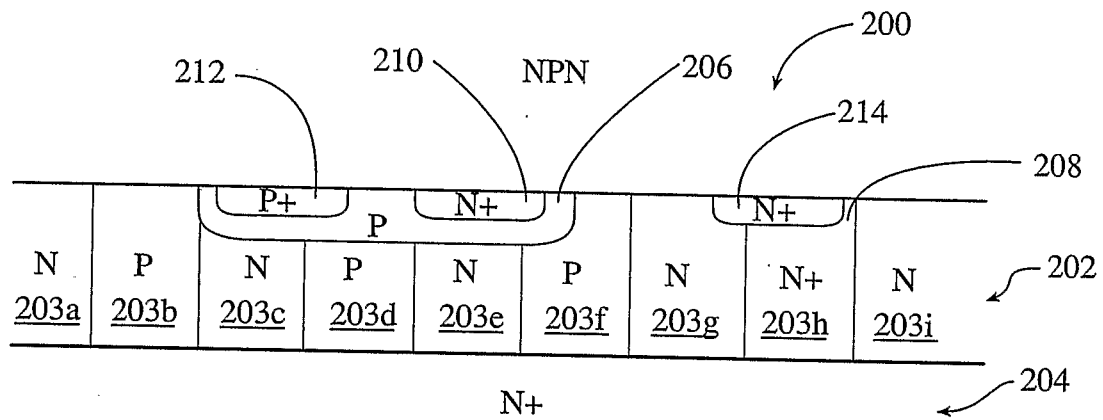


Fig 2A

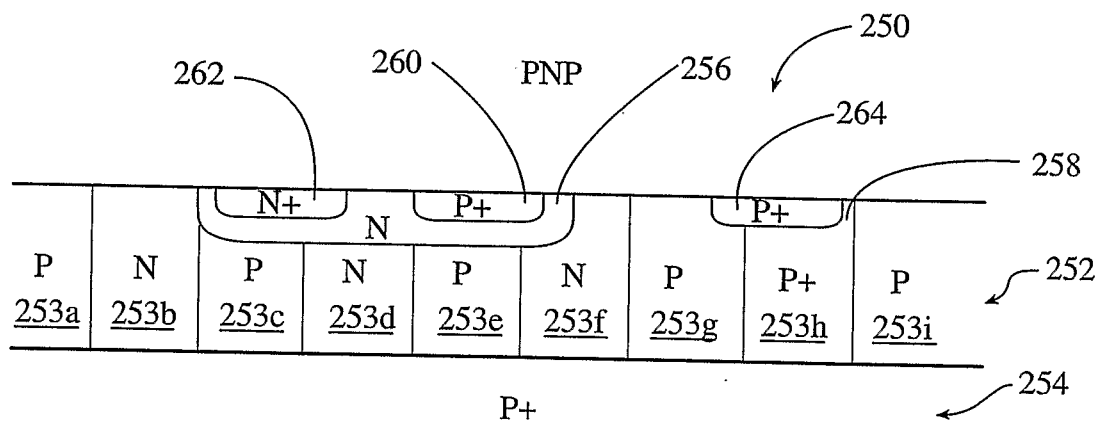


Fig 2B

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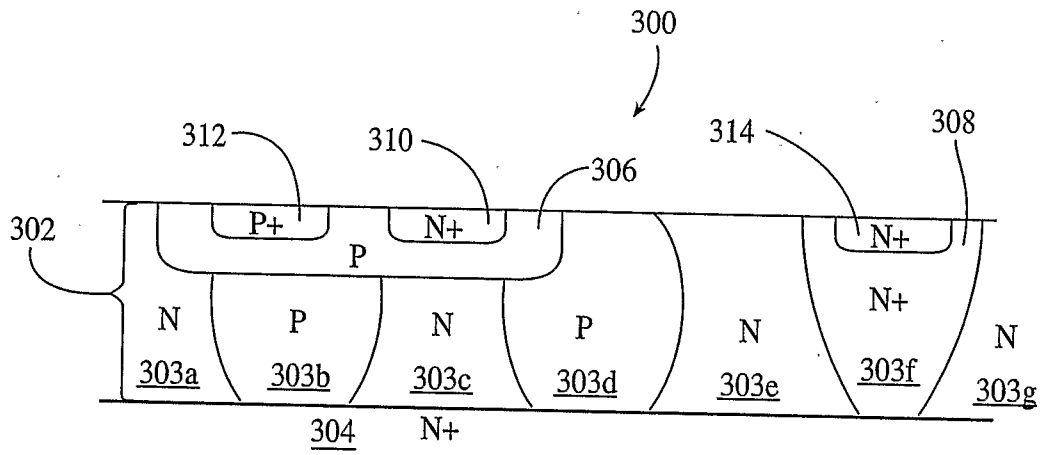


Fig 3A

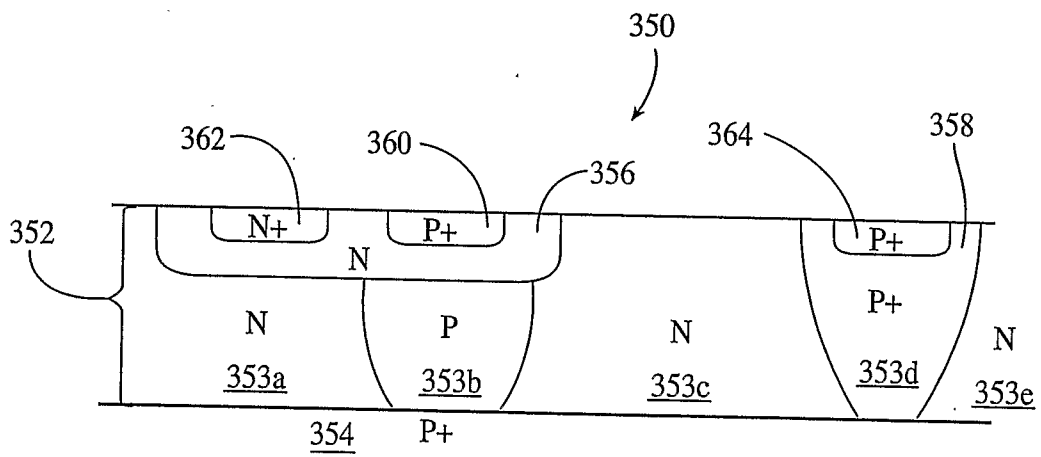
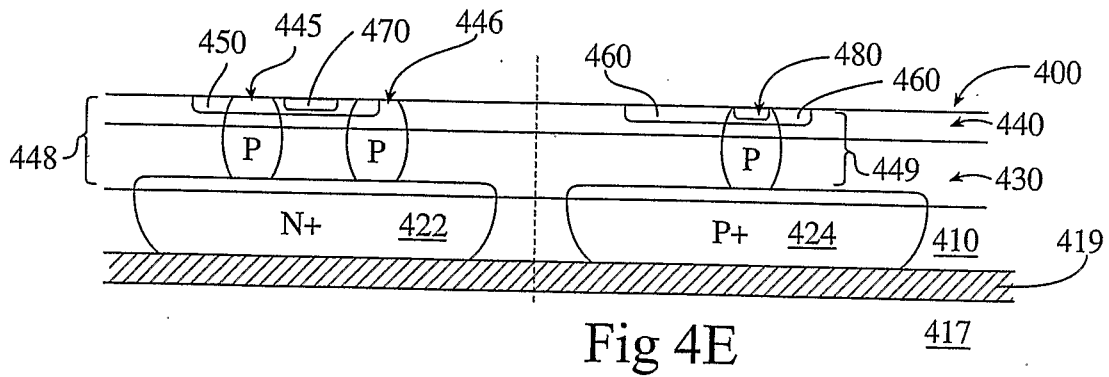
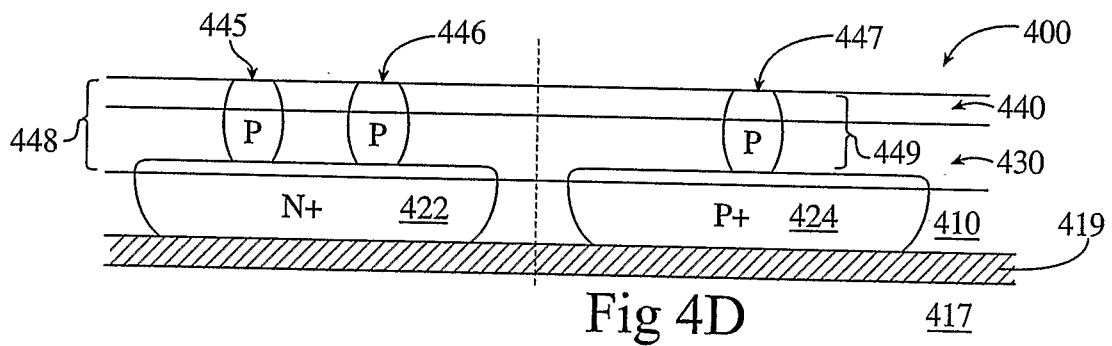
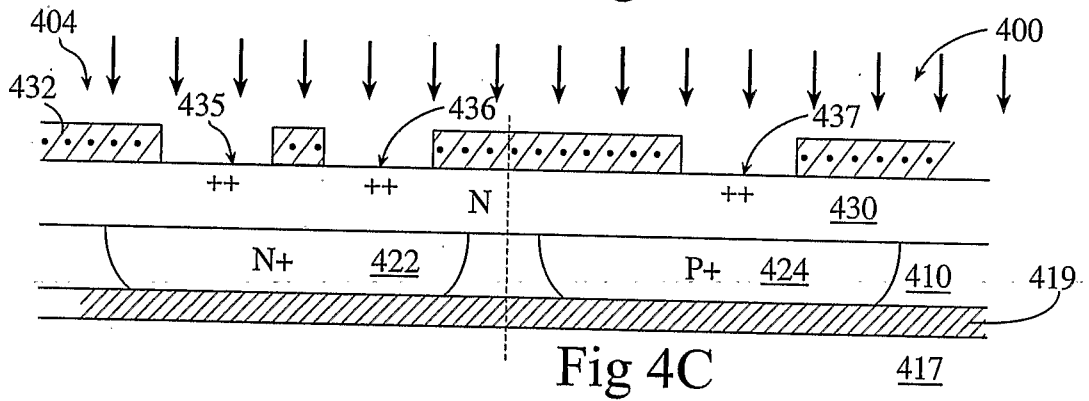
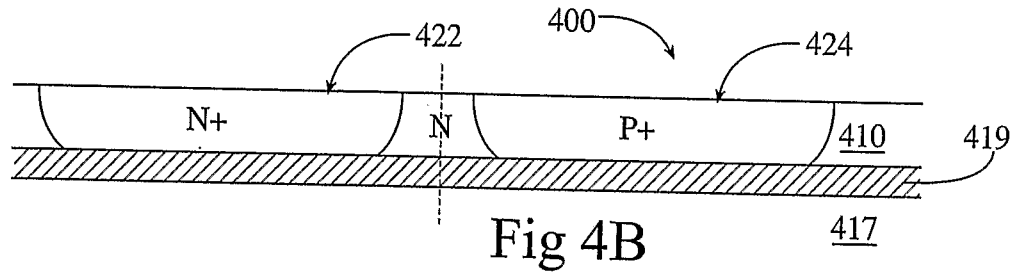
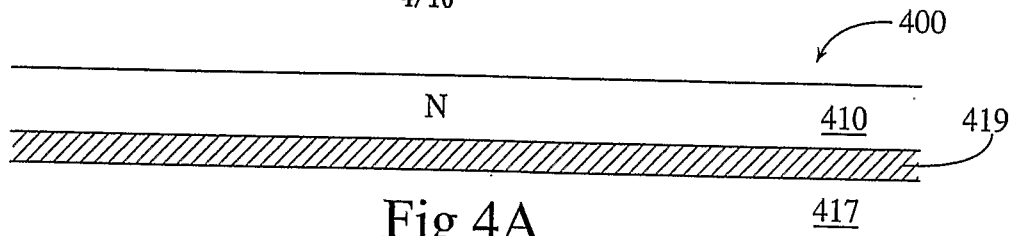
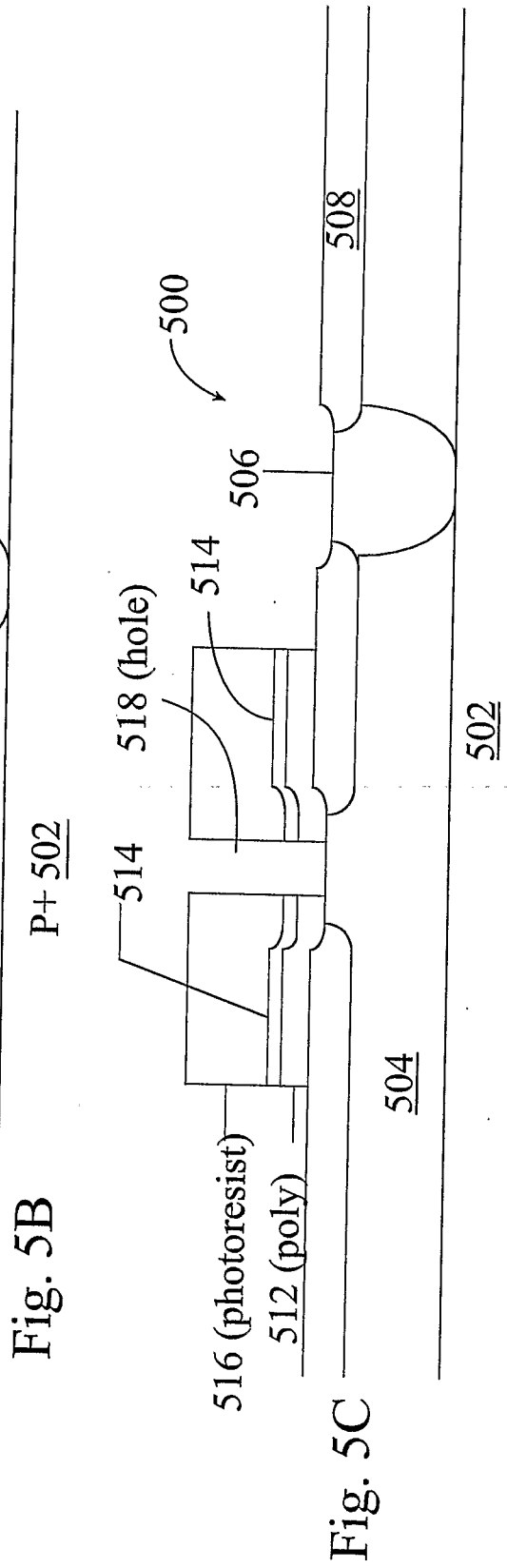
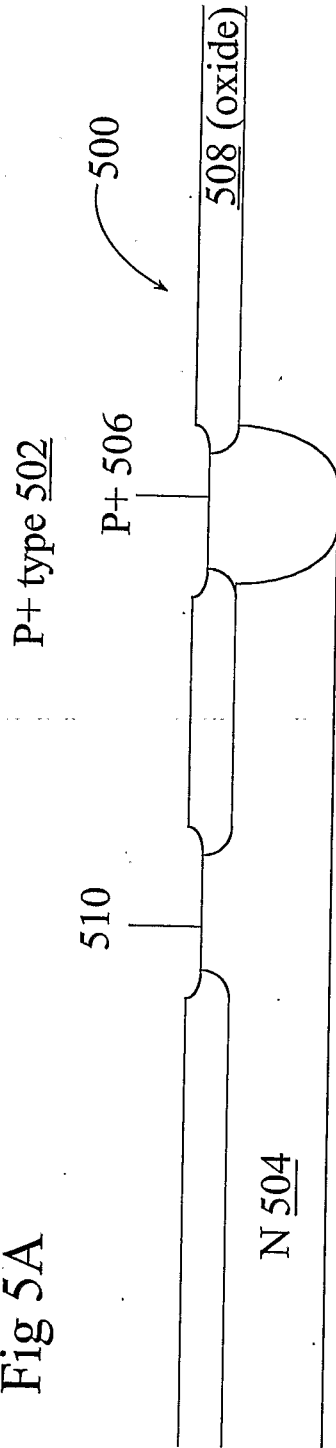
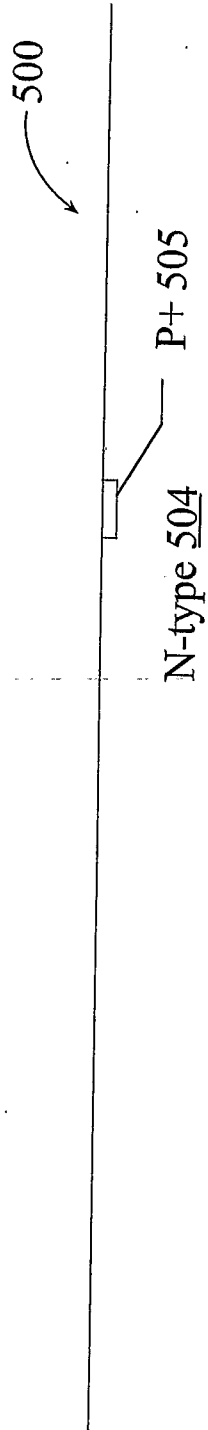


Fig 3B

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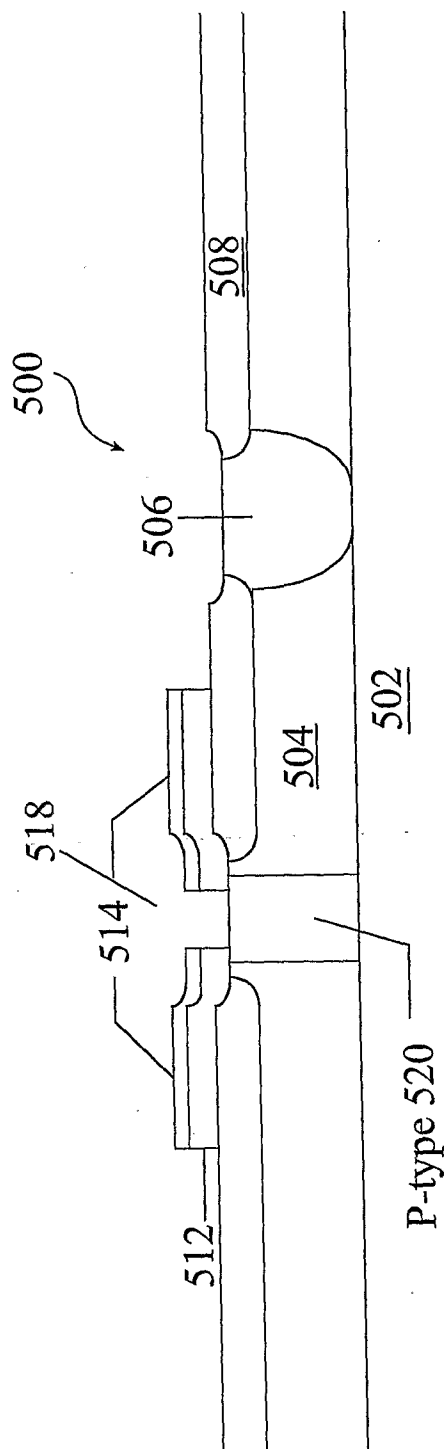


Fig. 5D

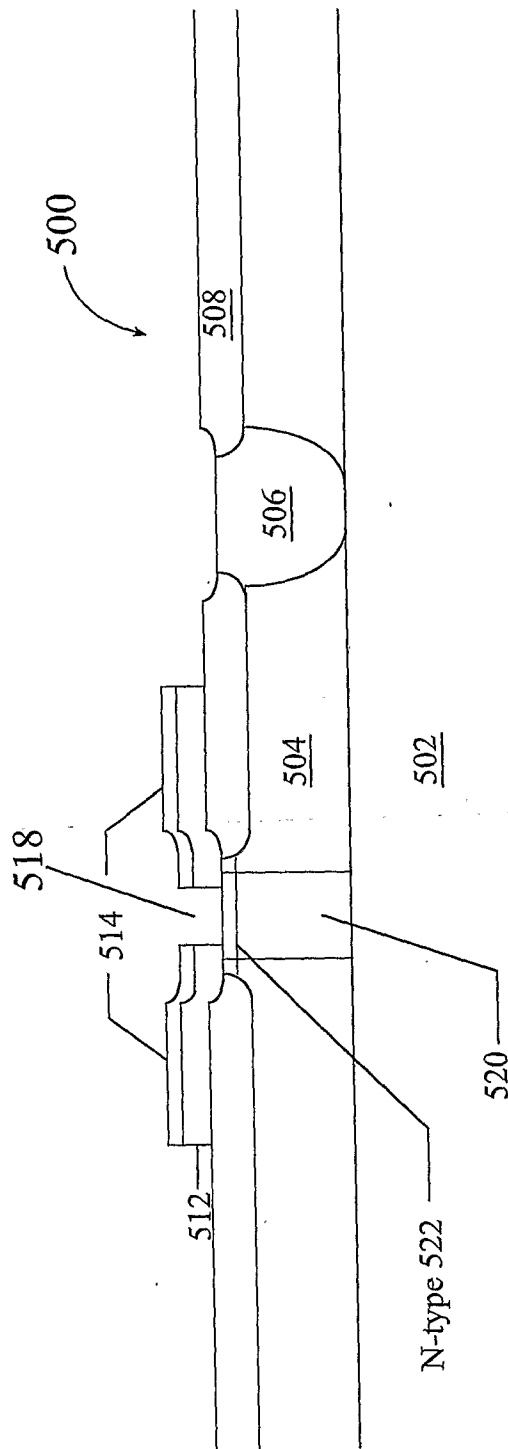
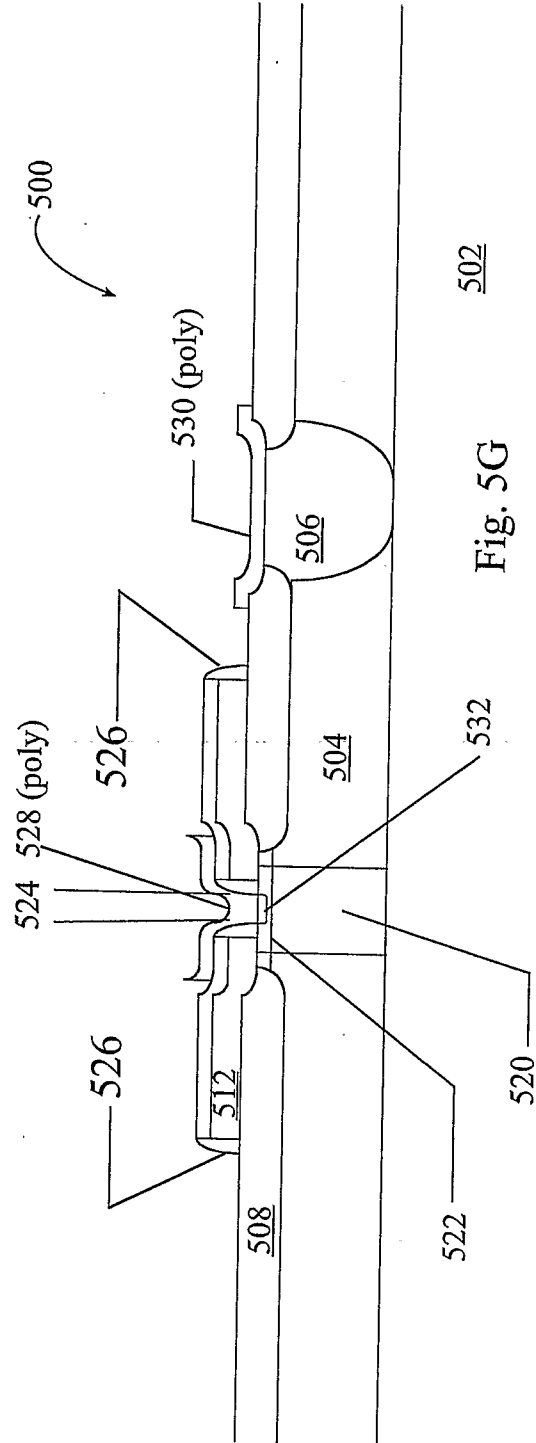
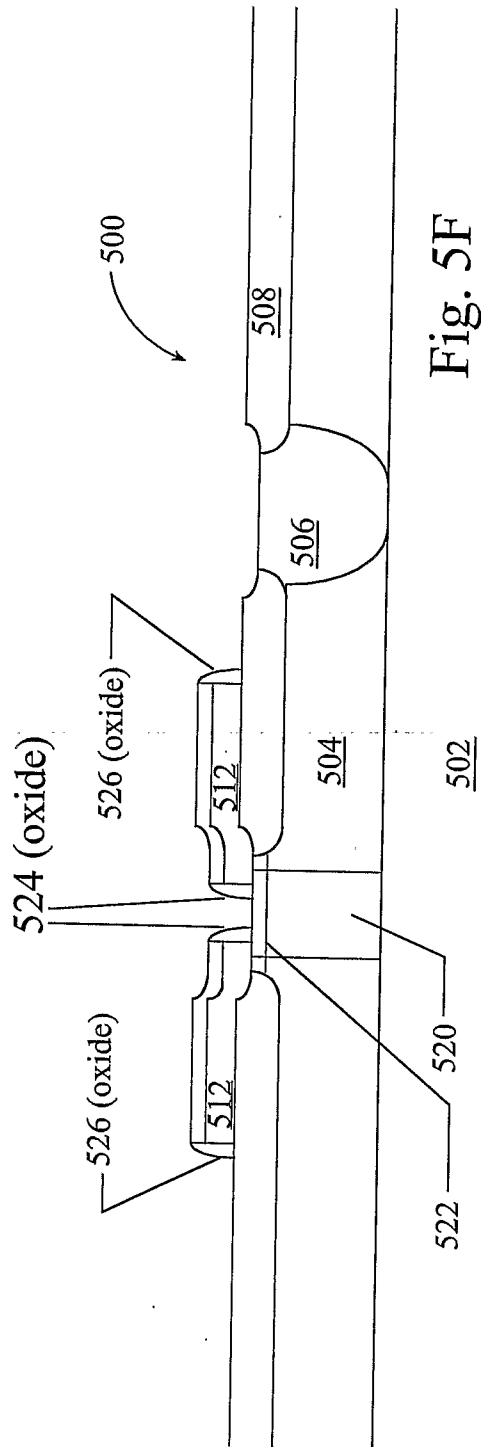
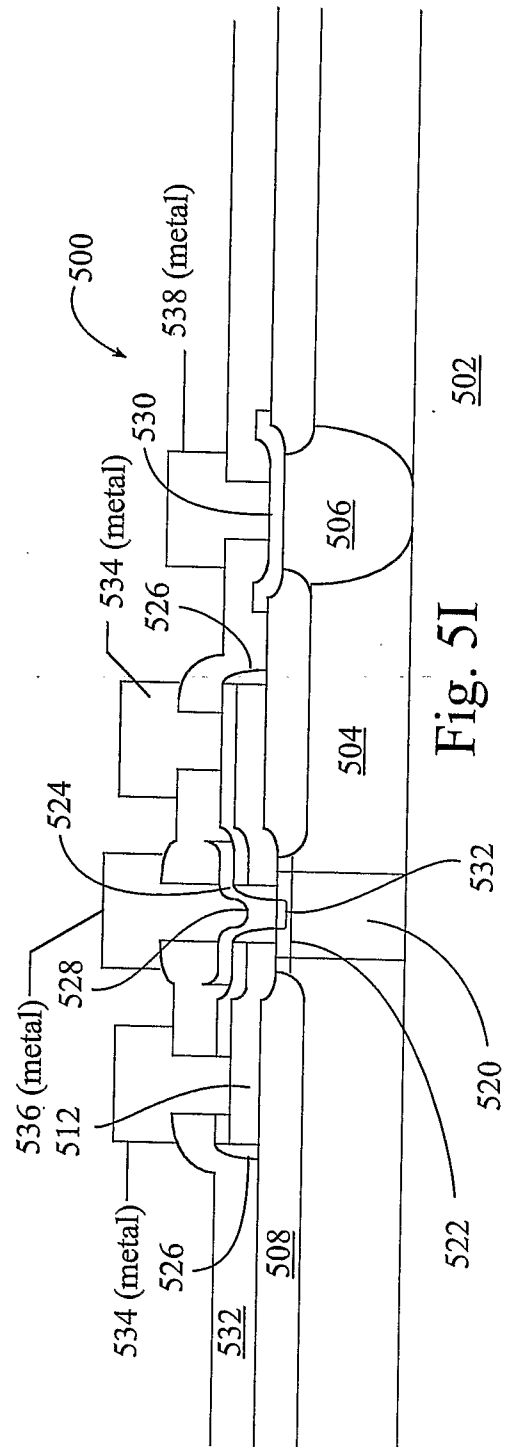
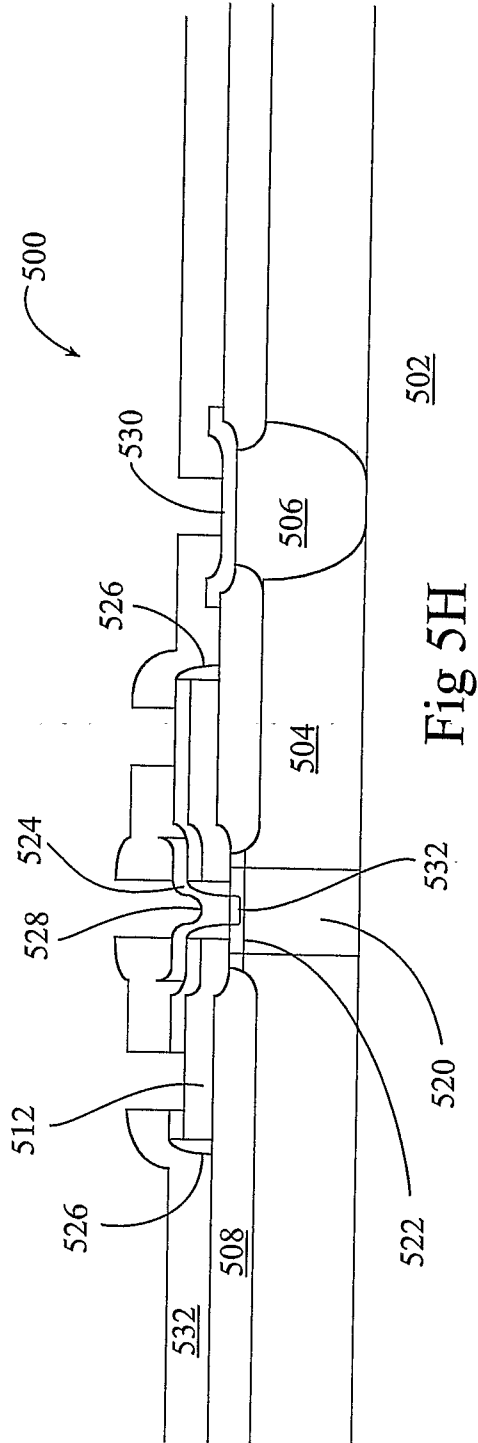


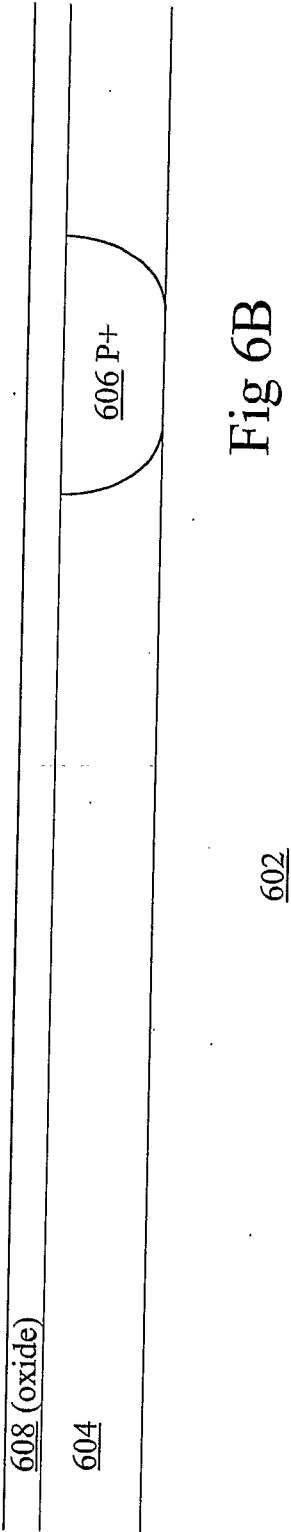
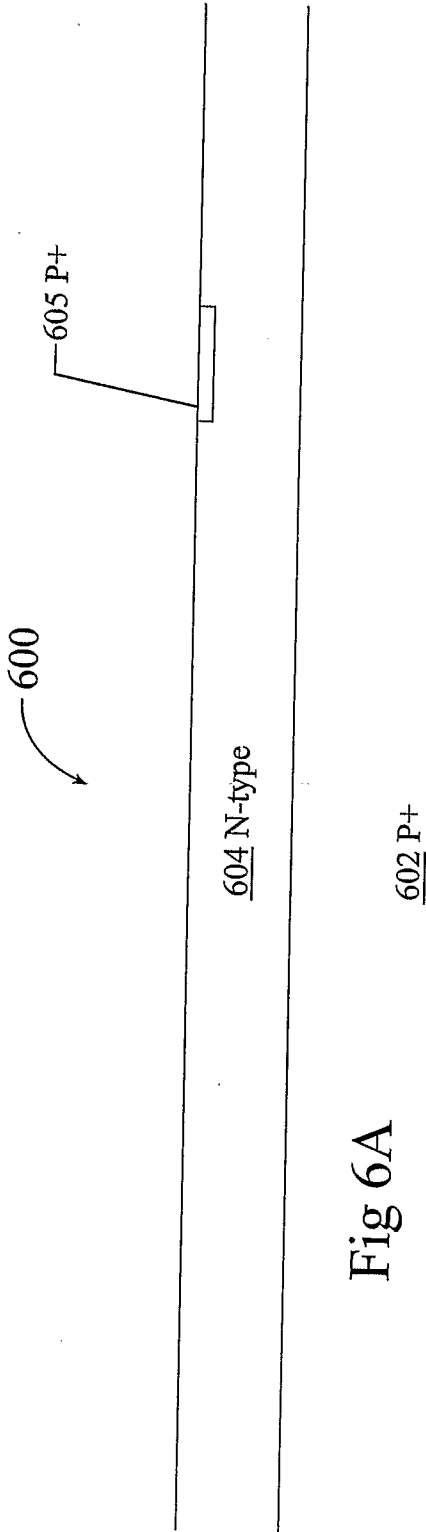
Fig. 5E

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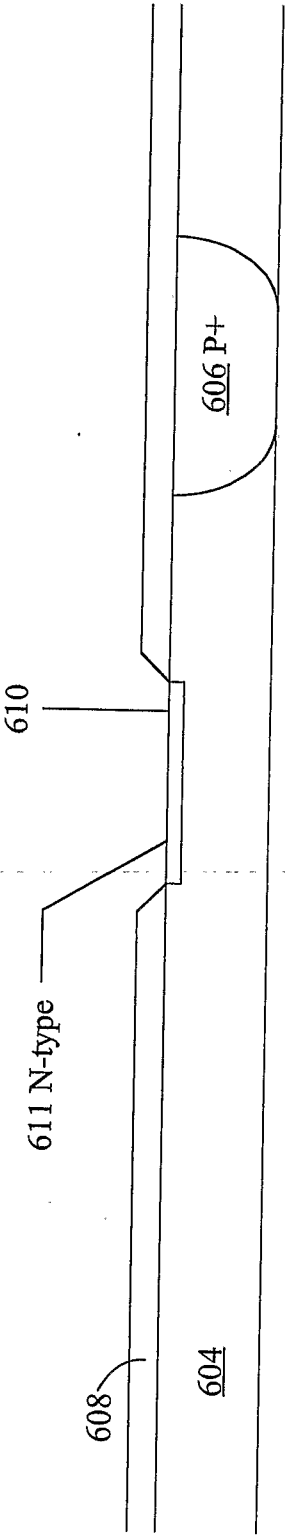


Fig 6C

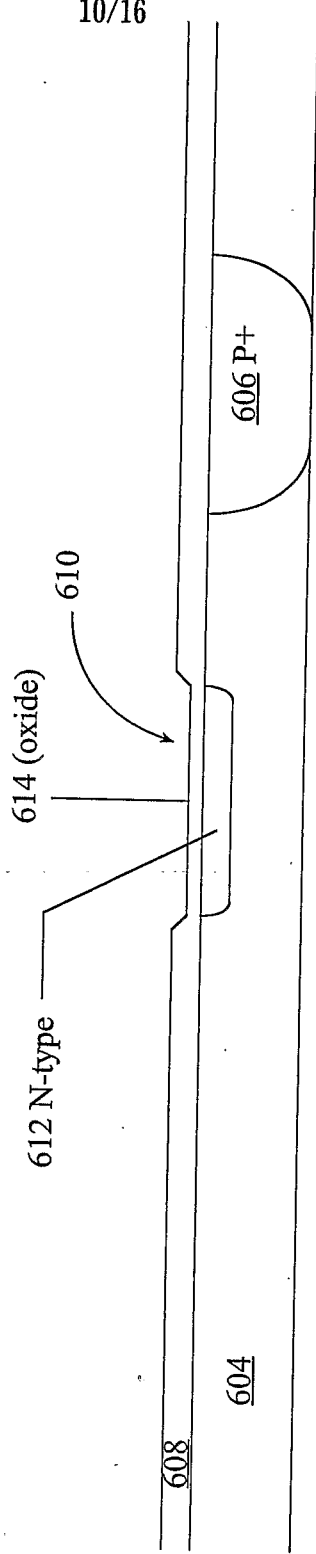


Fig 6D

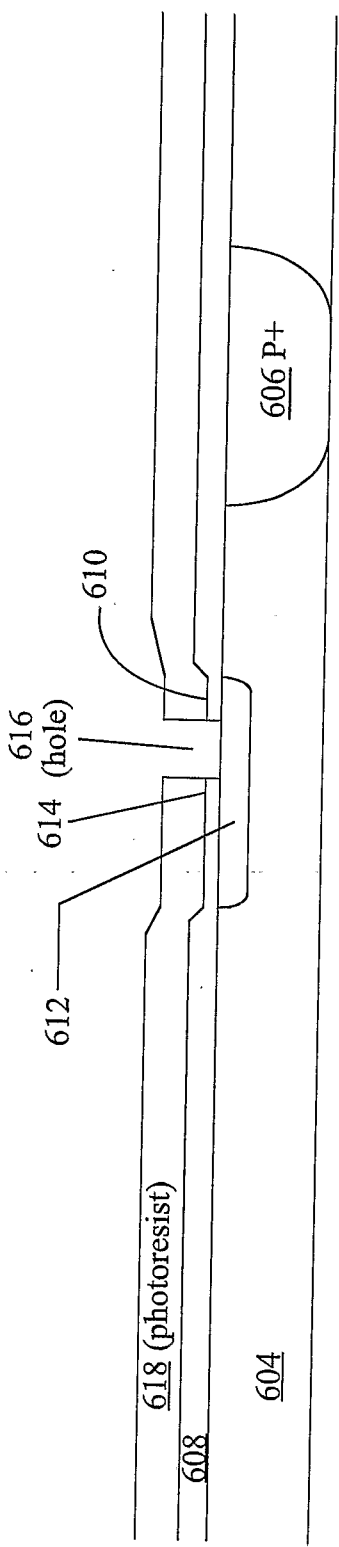


Fig 6E

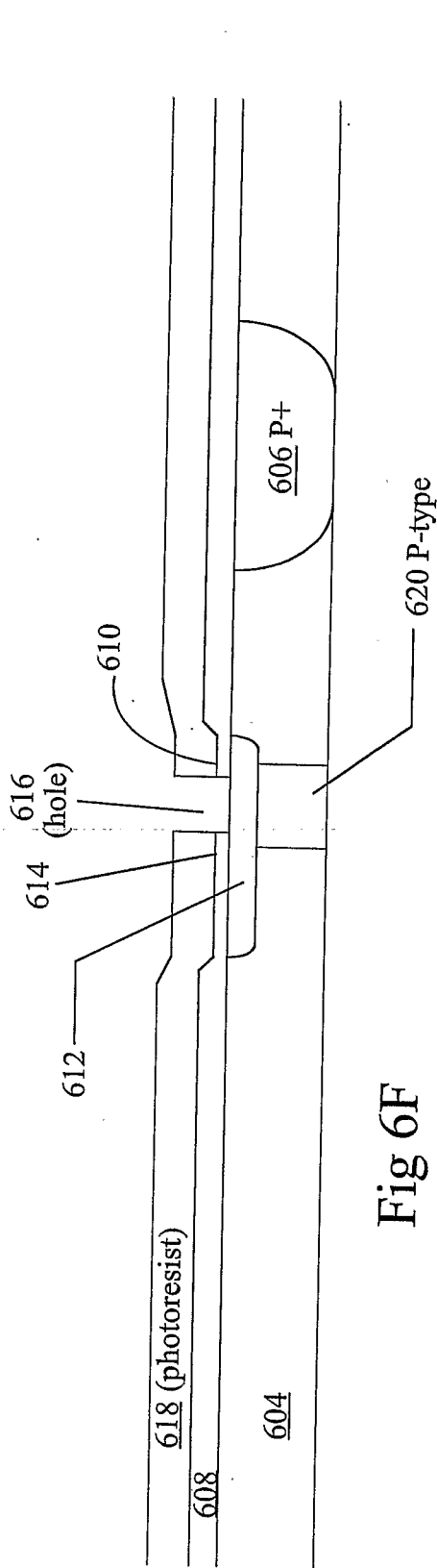


Fig 6F

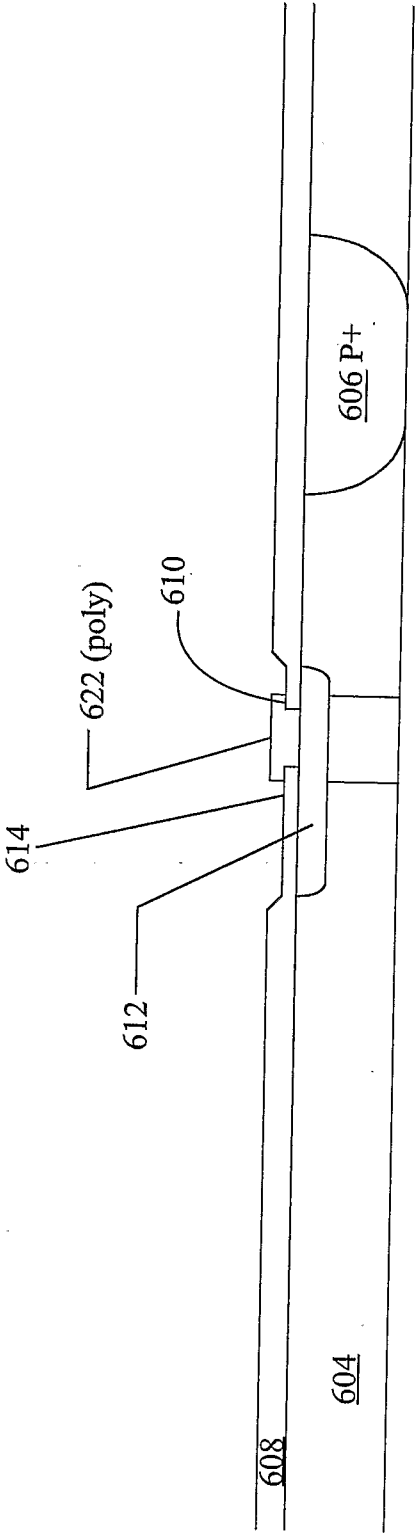


Fig 6G

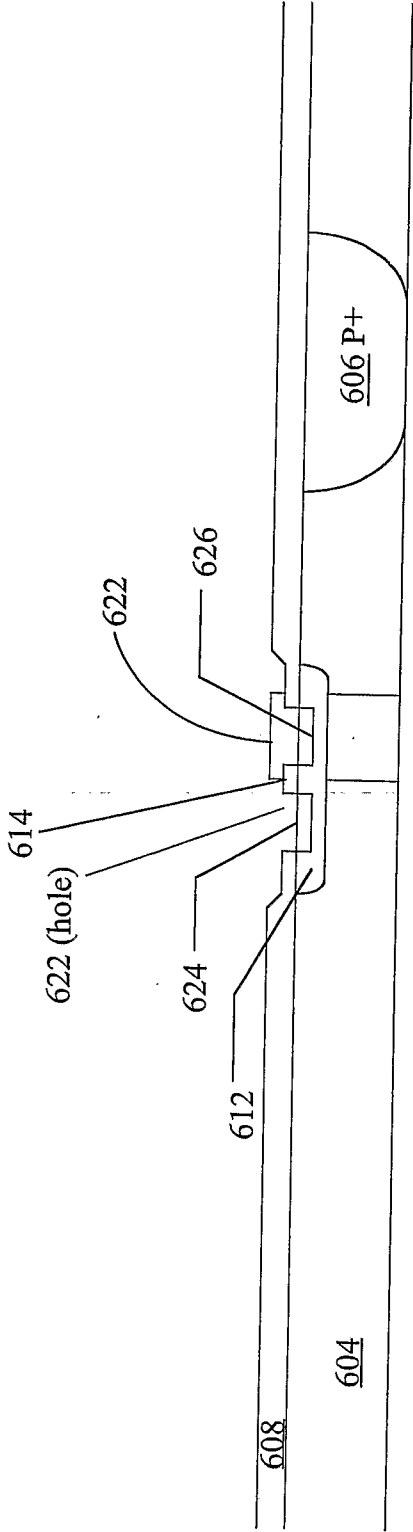


Fig 6H

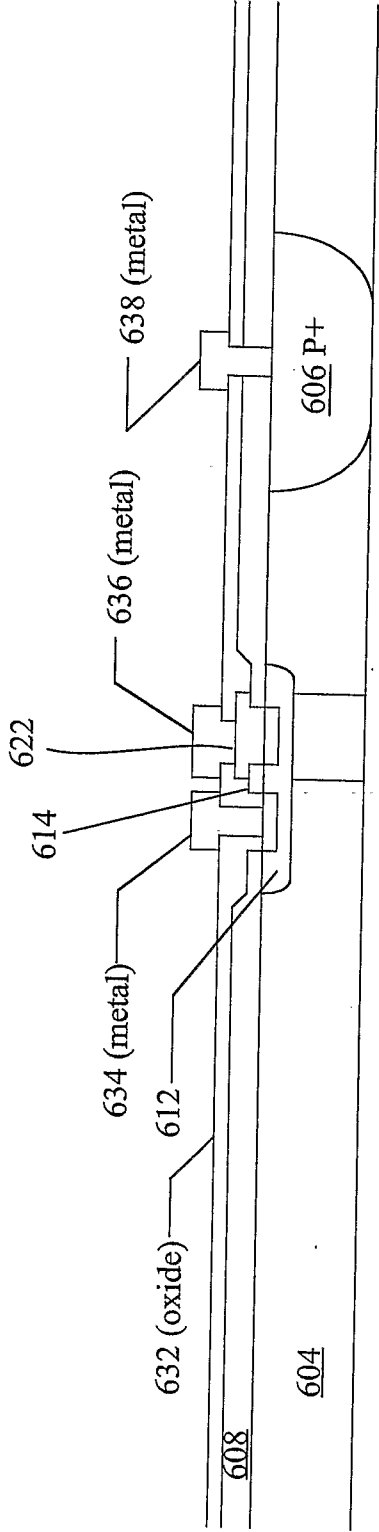


Fig 6I

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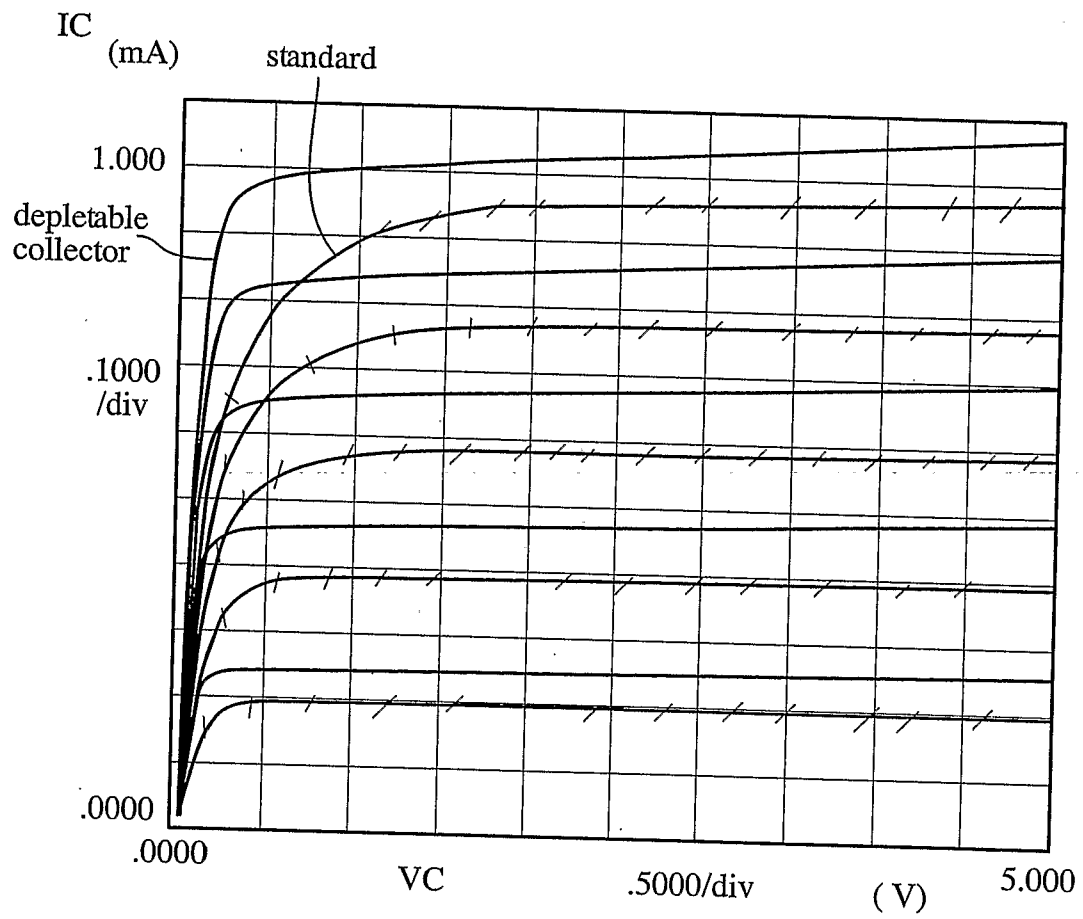


Fig 7

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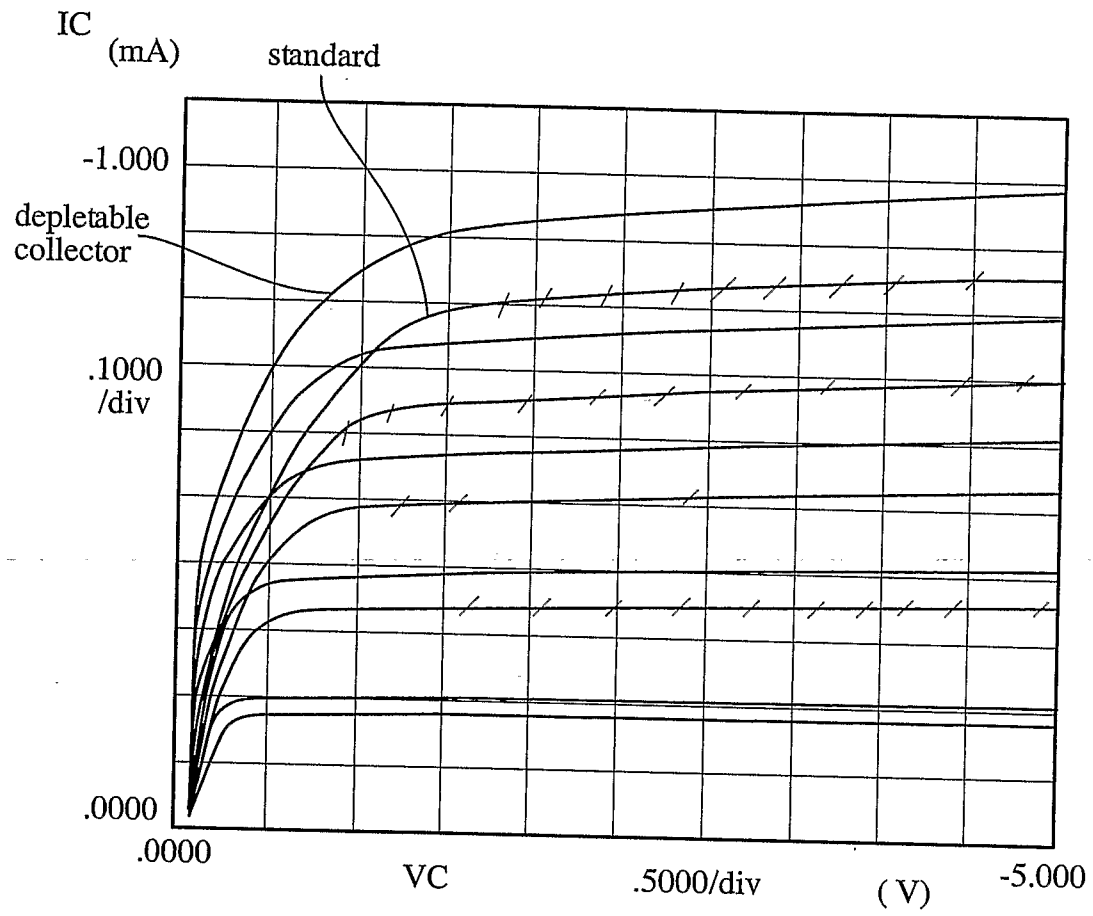


Fig 8

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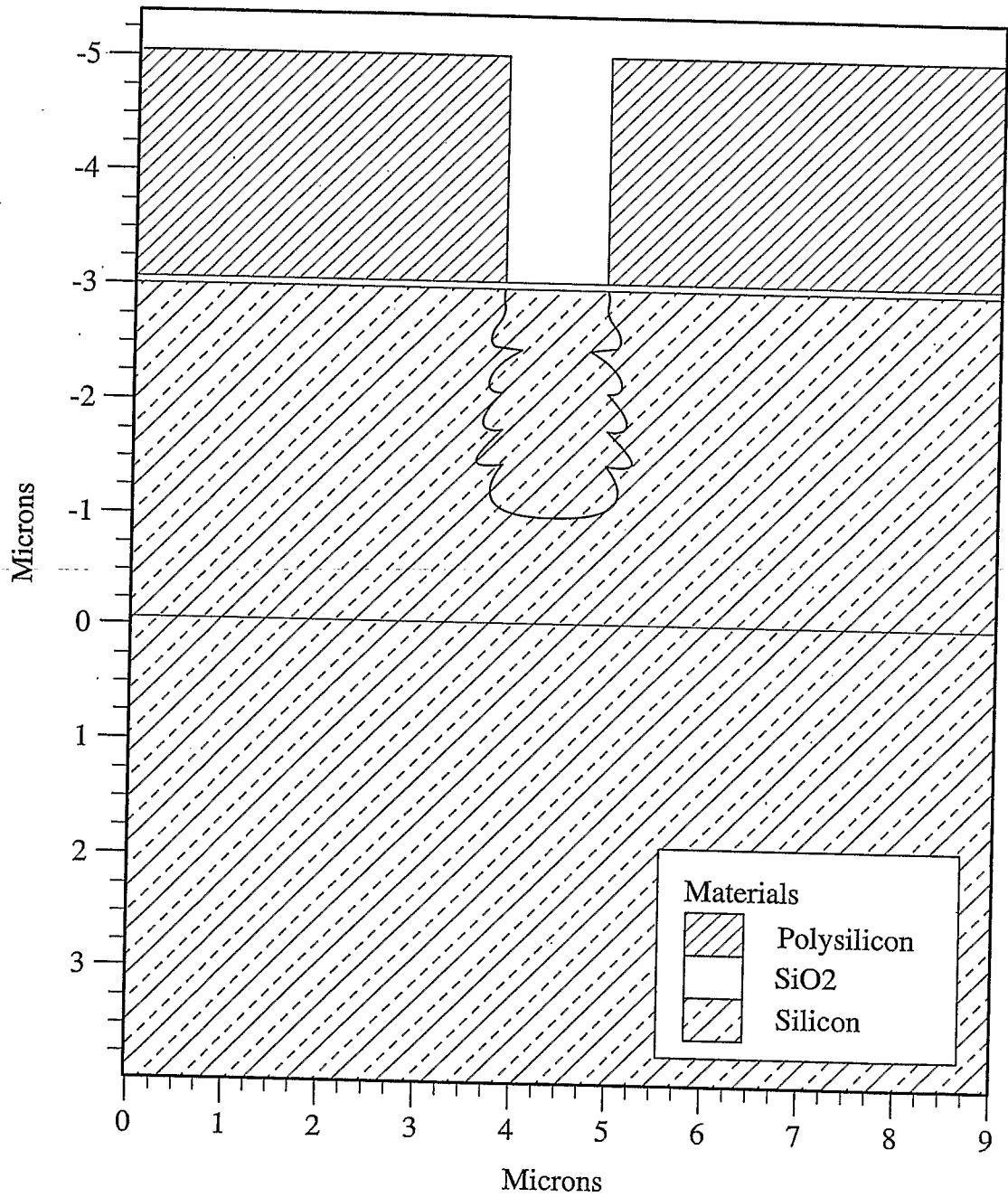


Fig 9

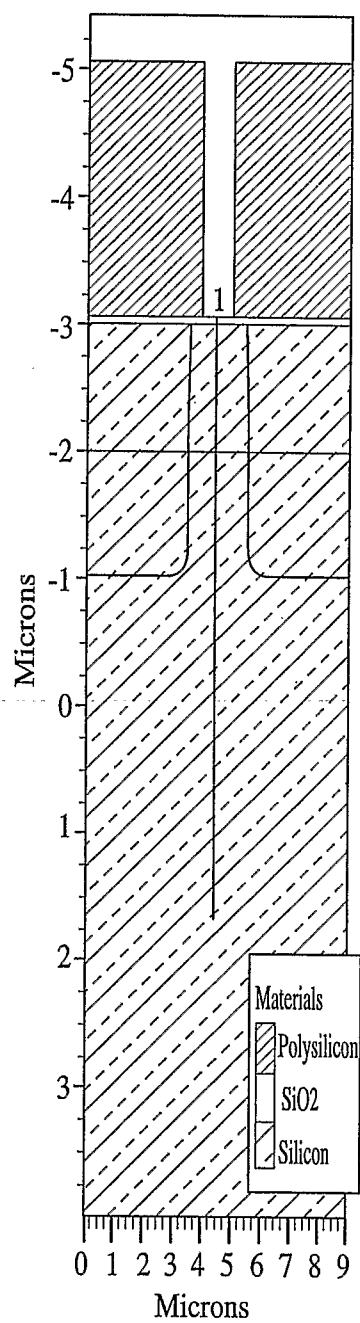


Fig 10A

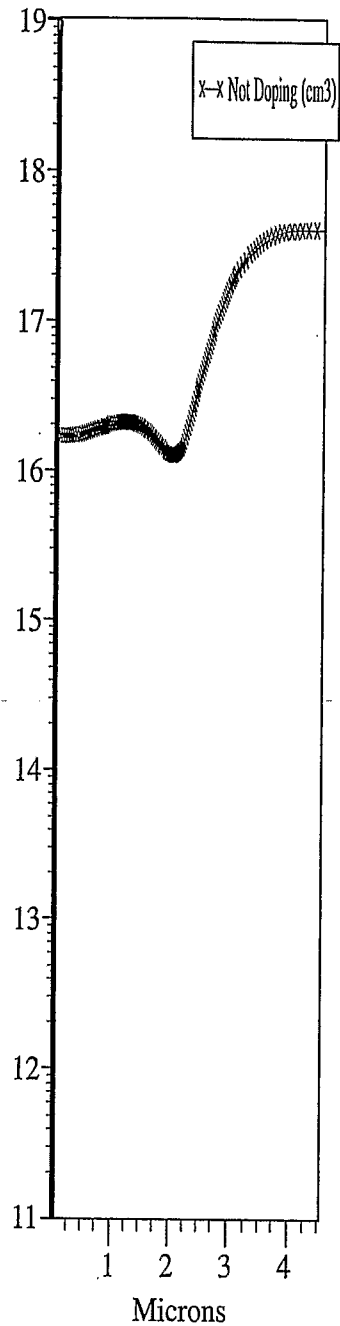


Fig 10B

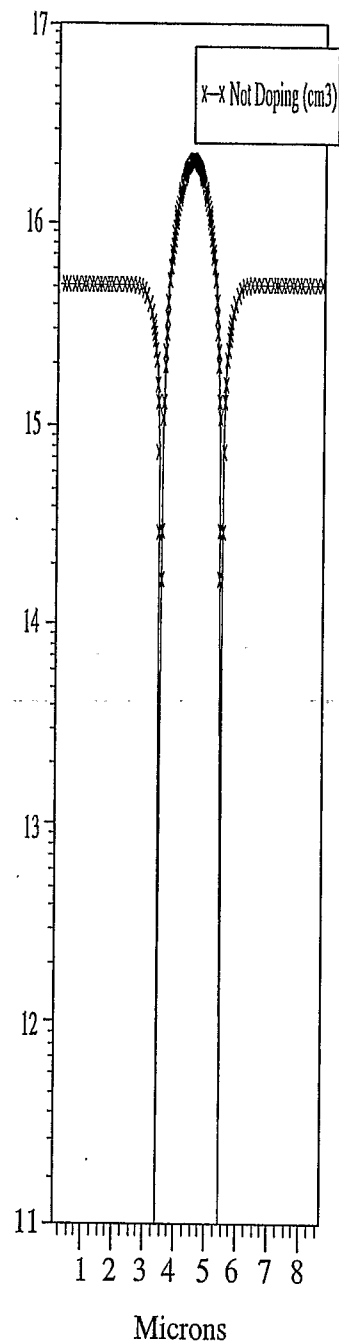


Fig 10C