

LOWER IC PACKAGE STRUCTURE FOR COUPLING WITH AN UPPER IC PACKAGE TO FORM A PACKAGE-ON-PACKAGE (POP) ASSEMBLY AND POP ASSEMBLY INCLUDING SUCH A LOWER IC PACKAGE STRUCTURE

FIELD OF THE INVENTION

5 The disclosed embodiments relate generally to integrated circuit devices, and more particularly to stacking of integrated circuit packages.

BACKGROUND OF THE INVENTION

Integrated circuit (IC) devices having a small form factor may be useful in many types of computing systems, such as cell phones, smart phones, tablet computers,
10 electronic reading devices, netbook computers, and laptop computers, as well as other hand-held or mobile computing systems. One solution to achieve a small form factor IC device is to use a package-on-package (PoP) architecture, which generally includes an upper IC package stacked over and electrically coupled with a lower IC package. The lower IC package may include one or more IC die – and perhaps one or more additional
15 components – disposed on a first substrate or other die carrier. Similarly, the upper IC package may include one or more IC die (and perhaps one or more other components) disposed on a second substrate. In some circumstances, the lower IC package may be fabricated at one manufacturing facility and the upper IC package fabricated at another manufacturing facility, and then these two IC packages will need to be mechanically and
20 electrically joined together. The lower IC package is electrically coupled to the upper IC package by one or more interconnects, and these interconnects may also provide a mechanical coupling between these two IC packages.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a schematic diagram illustrating a top view of an embodiment of a
25 lower IC package structure.

FIG. 1B is a schematic diagram illustrating a cross-sectional elevation view of the lower IC package of FIG. 1A, as taken along line B-B of FIG. 1A.

FIG. 1C is a schematic diagram illustrating a top view of another embodiment of a lower IC package structure.

30 FIG. 1D is a schematic diagram illustrating a cross-sectional elevation view of a further embodiment a lower IC package structure.

FIG. 1E is a schematic diagram illustrating a cross-sectional elevation view of another embodiment a lower IC package structure.

FIG. 1F is a schematic diagram illustrating a cross-sectional elevation view of another embodiment a lower IC package structure.

FIG. 1G is a schematic diagram illustrating a cross-sectional elevation view of another embodiment a lower IC package structure.

5 FIG. 1H is a schematic diagram illustrating a cross-sectional elevation view of another embodiment a lower IC package structure.

FIG. 1I is a schematic diagram illustrating a cross-sectional elevation view of another embodiment a lower IC package structure.

10 FIG. 1J is a schematic diagram illustrating a cross-sectional elevation view of another embodiment a lower IC package structure.

FIG. 1K is a schematic diagram illustrating a cross-sectional elevation view of another embodiment a lower IC package structure.

FIG. 1L is a schematic diagram illustrating a cross-sectional elevation view of another embodiment a lower IC package structure.

15 FIG. 2A is a schematic diagram illustrating a partial cross-sectional elevation view of an embodiment a lower IC package including a flow barrier.

FIG. 2B is a schematic diagram illustrating a partial cross-sectional elevation view of another embodiment a lower IC package including a flow barrier.

20 FIG. 2C is a schematic diagram illustrating a partial cross-sectional elevation view of a further embodiment a lower IC package including a flow barrier.

FIG. 2D is a schematic diagram illustrating a top view of yet another embodiment a lower IC package including a flow barrier.

FIG. 2E is a schematic diagram illustrating a top view of yet a further embodiment a lower IC package including a flow barrier.

25 FIG. 3 is a schematic diagram illustrating a cross-sectional elevation view of an embodiment of a package-on-package (PoP) assembly.

FIG. 4 is a schematic diagram illustrating a cross-sectional elevation view of an embodiment of a computing system including a PoP assembly.

30 FIG. 5 is a block diagram illustrating embodiments of a method of making a lower IC package structure, as well as a package-on-package assembly.

DETAILED DESCRIPTION OF THE INVENTION

Disclosed are embodiments of a lower integrated circuit (IC) package structure for a package-on-package (PoP) assembly. According to some embodiments, the lower IC package structure includes an interposer having pads to couple with mating terminals of an

upper IC package. In further embodiments, an encapsulant material is disposed in the lower IC package, and this encapsulant may be disposed proximate one or more IC die. In some embodiments, an upper IC package can be coupled with the lower IC package to form a PoP assembly. In other embodiments, such a PoP assembly is disposed on a
5 mainboard or other circuit board, and may form part of a computing system. Embodiments of a method of making the aforementioned lower IC package, as well as a PoP assembly, are also disclosed.

Turning now to FIGS. 1A and 1B, illustrated is an embodiment of a lower IC package 100. A top view of the lower IC package 100 is shown in FIG. 1A, whereas a
10 cross-sectional elevation view, as taken along line B-B of FIG. 1A, is shown in FIG. 1B. The lower IC package 100 may be coupled with an upper IC package to form a PoP assembly, and an embodiment of such a PoP assembly will be described in greater detail below (see, e.g., FIG. 3, and the accompanying text).

With continued reference to FIGS. 1A and 1B, the lower IC package 100 includes
15 a substrate 110 having a first side 112 and an opposing second side 114. An IC die 120 is disposed on the first side 112 of substrate 110 and is electrically coupled with the substrate by a number of interconnects 125. An interposer 130 is also disposed on the substrate's first side 112, and a number of interconnects 140 electrically couple (and perhaps mechanically attach) the interposer 130 to the underlying substrate 110. According to
20 one embodiment, an encapsulant material 150 is disposed in the IC package 100, and the encapsulant 150 is positioned proximate the IC die 120. In one embodiment, a layer of an underfill material 160 may be disposed between the IC die 120 and substrate 110. Further, a plurality of electrically conductive terminals 170 (e.g., lands, solder bumps, metal columns or pillars, etc.) may be disposed on the second side 114 of substrate 110, and
25 these terminals can be used to form electrical connections with a next-level component, such as a mainboard or other circuit board.

Substrate 110 – sometimes referred to as a “package substrate” – may comprise any suitable type of substrate capable of providing electrical communications between the IC die 120 and a next-level component to which the IC package 100 is coupled (e.g., a
30 circuit board). In another embodiment, the substrate 110 may comprise any suitable type of substrate capable of providing electrical communication between the IC die 120 and an upper IC package coupled with the lower IC package, and in a further embodiment the substrate 110 may comprise any suitable type of substrate capable of providing electrical communication between the upper IC package and a next-level component to which the IC

package 100 is coupled. The substrate 110 may also provide structural support for the die 120. By way of example, in one embodiment, substrate 110 comprises a multi-layer substrate – including alternating layers of a dielectric material and metal – built-up around a core layer (either a dielectric or metal core). In another embodiment, the substrate 110
5 comprises a coreless multi-layer substrate. Other types of substrates and substrate materials may also find use with the disclosed embodiments (e.g., ceramics, sapphire, glass, etc.). Further, according to one embodiment, the substrate 110 may comprise alternating layers of dielectric material and metal that are built-up over the die 120 itself, this process sometimes referred to as a “bumpless build-up process.” Where such an
10 approach is utilized, the interconnects 125 may not be needed (as the build-up layers may be disposed directly over the die 120).

The IC die 120 may comprise any type of integrated circuit device. In one embodiment, the IC die 120 includes a processing system (either single core or multi-core). For example, the IC die may comprise a microprocessor, a graphics processor, a
15 signal processor, a network processor, a chipset, etc. In one embodiment, the IC die 120 comprises a system-on-chip (SoC) having multiple functional units (e.g., one or more processing units, one or more graphics units, one or more communications units, one or more signal processing units, one or more security units, etc.). However, it should be understood that the disclosed embodiments are not limited to any particular type or class
20 of IC devices.

The IC die 120 includes a front-side 122 and an opposing back-side 124. In some embodiments, the front-side 122 may be referred to as the “active surface” of the die. A number of interconnects 125 extend from the die’s front-side 122 to the underlying substrate 110, and these interconnects 125 electrically coupled the die and substrate.
25 Interconnects 125 may comprise any type of structure and materials capable of providing electrical communication between the die 120 and substrate 110. According to one embodiment, the interconnects 125 comprise an array of solder bumps extending between the die 120 and substrate 110 (perhaps in combination with an array of copper columns and/or copper pads disposed on the die 120 and/or substrate 110), and a solder reflow
30 process may be utilized to form the interconnects 125. Of course, it should be understood that many other types of interconnects and materials are possible (e.g., wirebonds extending between the die 120 and substrate 110). In one embodiment, the interconnects 125 electrically coupled the die 120 to substrate 110, and the interconnects 125 also aid in mechanically securing the die to the substrate. In a further embodiment, a layer of

underfill material 160 is disposed around interconnects 125 and between the IC die 120 and substrate 110, and this underfill layer 160 may also aid in mechanically securing the die 120 to substrate 110, as will be described below. Underfill material 160 may comprise any suitable material, such as a liquid or a pre-applied epoxy compound.

5 Interposer 130 has a first side 132 and an opposing second side 134, with the second side 134 facing the first side 112 of substrate 110. In one embodiment, as illustrated in FIGS. 1A-1B, the interposer 130 comprises a frame shape having an opening or window 136. Opening 136 may encompass a periphery 126 of IC die 120; however, in other embodiments the opening 136 and die periphery 126 may not be aligned and/or may
10 not be concentric, and a portion of the die's periphery 126 may extend outside of the window 136.

It should be understood that the disclosed embodiments are not limited to a frame-shaped interposer and, further, that interposer 130 may have any suitable shape and configuration. For example, in another embodiment, as shown in FIG. 1C, the interposer
15 130 comprises a solid rectangular plate without an opening. According to one embodiment, the solid rectangular plate interposer 130 of FIG. 1C includes a small aperture 138 for insertion of the encapsulant 150.

Returning to FIGS. 1A and 1B, disposed on the first side 132 of interposer 130 is a plurality of electrically conductive terminals 180. Each of the electrically conductive
20 terminals 180 may comprise any suitable structure and material capable of forming an electrical connection with a mating terminal of an upper IC package to be joined with the lower IC package 100. In one embodiment, each of the terminals 180 comprises a pad or land adapted to mate with a corresponding conductive bump extending from the upper IC package, and these mating structures may be joined by a solder reflow process. However,
25 it should be understood that a terminal 180 may comprise any other type of structure (e.g., a column, bump, etc.). Further, in one embodiment, some of the terminals 180 may have a different size and/or structure compared to other terminals (e.g., terminals used for power delivery may be different than terminals used for signaling, etc.).

As noted above, a number of interconnects 140 extend between the interposer's
30 second side 134 and the first side 112 of substrate 110, and these interconnects electrically couple the interposer 130 – and, hence, an upper IC package coupled to the interposer – with substrate 110. Interconnects 140 may comprise any type of structure and materials capable of providing electrical communication between the interposer 130 and substrate 110. According to one embodiment, the interconnects 140 comprise an array of solder

bumps extending between the interposer 130 and substrate 110 (perhaps in combination with an array of copper columns and/or copper pads disposed on the interposer 130 and/or substrate 110), and a solder reflow process may be utilized to form the interconnects 140.

Of course, it should be understood that many other types of interconnects and materials are

5 possible. In one embodiment, the interconnects 140 also aid in mechanically securing the interposer 130 to the substrate 110. In a further embodiment, as will be described in greater detail below, the encapsulant material 150 may extend into the gap 190 between the interposer 130 and substrate 110, and the encapsulant may extend around at least a portion of one or more of the interconnects 140. Thus, the encapsulant 150 may also aid
10 in mechanically securing the interposer 130 to substrate 110.

As previously noted, an encapsulant 150 is disposed in the IC package 100. The encapsulant 150 may comprise any suitable material or combination of materials. In one embodiment, the encapsulant material comprises a liquid epoxy, and in a further embodiment the epoxy includes one or more filler materials to alter one or more

15 characteristics of the epoxy (e.g., curing temperature, hardness, yield strength, modulus of elasticity, coefficient of thermal expansion, etc.). According to one embodiment, the encapsulant layer increases the stiffness of the lower IC package 100 and decreases the package's susceptibility to warpage. For example, during the assembly of lower IC package 100, as well as during joining with an upper IC package, the IC package 100 may
20 be subjected to multiple high temperature cycles (e.g., during reflow, during epoxy cure, etc.), and this temperature cycling may cause warpage (e.g., due to differential thermal expansion between the die 120 and underlying substrate 110), and such warpage may lead to reduced reliability and/or structural failure. The increased stiffness provided by encapsulant 150 may alleviate the aforementioned warpage-induced failures.

25 Although referred to herein as an encapsulant, it should be understood that this element may be referred to by alternative terminology. For example, an encapsulant may be referred to as a mold, molding, overmold, or glob top.

The encapsulant 150 may be placed in the lower IC package 100 at any location or locations, as needed, to provide the desired mechanical characteristics for the package
30 assembly. According to one embodiment, as shown in FIGS. 1A and 1B, the encapsulant 150 is disposed over at least a portion of the back-side 124 of IC die 120, and in some embodiments the encapsulant overlies substantially all of the die's back-side 124 (see FIG. 1B). In a further embodiment, as also shown in FIGS. 1A and 1B, the encapsulant 150 is disposed over at least a portion of the first side 112 of substrate 110. If an underfill

material 160 is disposed between the IC die 120 and substrate 110, the encapsulant 150 may also contact portions of the underfill material (see FIG. 1B). In one embodiment, as shown in FIG. 1B, the encapsulant extends beyond the periphery 126 of die 120, but does not extend to regions on substrate 110 occupied by interconnects 140. According to one
5 embodiment, as shown in FIG. 1B, the shape of encapsulant 150 is substantially flat above the back-side of die 124 but is rounded near the die's periphery. Also, in one embodiment, as shown in FIG. 1B, the encapsulant 150 does not extend above the front side 132 of interposer 130, although in the embodiment of FIG. 1B the encapsulant extends above the interposer's second side 134 and into the window 136.

10 It should be understood that FIGS. 1A and 1B illustrate a single exemplary embodiment of lower IC package 100 and encapsulant 150. However, many other configurations of encapsulant 150 and lower IC package 100 are possible. For example, in other embodiments, the encapsulant may not extend into the window 136 and may lie below the second side 134 of interposer 130. In a further embodiment, the encapsulant
15 150 may extend above the interposer's first side 132. Also, the encapsulant may have any other suitable shape and, further, in some embodiments the encapsulant may extend to regions of substrate 110 occupied by interconnects 140. Additional embodiments of the lower IC package 150 having alternative configurations of encapsulant 150, as well as additional features, are illustrated in FIGS. 1D through 1L.

20 Referring first to FIG. 1D, in one embodiment, the encapsulant 150 extends above the first side 132 of interposer 130. Also, in the embodiment of FIG. 1D, the encapsulant has a rectangular cross-sectional profile with rounded corners. Referring to FIG. 1E, in one embodiment, encapsulant 150 has a shape in which the upper portion is substantially rounded. In a further embodiment, as shown in FIG. 1F, the encapsulant 150 has a shape
25 that, when viewed in cross-section as shown, approximates a sine wave profile. In the embodiments of FIGS. 1D, 1E, and 1F, the encapsulant is disposed over substantially all of the die's back-side surface 124 and also contacts underfill material 160. Also, in the embodiments of FIGS. 1D through 1F, the encapsulant 150 does not extend to locations where interconnects 140 are disposed.

30 Turning now to FIG. 1G, in one embodiment, the encapsulant extends into the gap 190 between the interposer 130 and underlying substrate 110. Further, the encapsulant 150 extends into regions occupied by interconnects 140. In the embodiment of FIG. 1G, the encapsulant substantially surrounds one or more of the interconnects 140. In another embodiment, as also shown in FIG. 1G, the encapsulant fully fills the gap 190 and extends

from the substrate's first surface 112 to the interposer's second surface 134. However, in other embodiments, the encapsulant may be disposed proximate the interconnects 140 and contact one or more of these interconnects, but may not fully fill the gap 190. Placing encapsulant 150 in the gap 190 between substrate 110 and interposer 130 and around one or more of the interconnects 140 may strengthen the mechanical attachment between the interposer 130 and substrate 110, as well as increasing the strength and reliability of the electrical interconnects 140. In the embodiment of FIG. 1G, an upper portion of the encapsulant 150 has a shape approximating a truncated pyramid (such a shape may be achieved by, for example, a molding process).

In the embodiments shown in FIGS. 1B through 1G, the encapsulant 150 was disposed over the back-side 124 of die 120. However, in other embodiments, the die's back-side 124 may be exposed. For example, as shown in FIG. 1H, the encapsulant 150 contacts the edges of the die's periphery 126, but the back-side 124 of the die 120 is substantially free of the encapsulant. By way of further example, as shown in FIG. 1I, the encapsulant 150 may extend into gap 190 and around one or more interconnects 140, but at least a portion of the die's back-side 124 remains substantially free of encapsulant. In the embodiment of FIG. 1I, the encapsulant may extend above the die back-side 124 and onto portions of this surface proximate the die periphery 126, while other portions of the die back-side 124 proximate the center of die 120 remain free of encapsulant. In one embodiment, exposing at least a portion of the back-side 124 of die 120 may facilitate coupling of cooling solution – e.g., a layer of thermal interface material, a heat slug, heat spreader, etc. (not shown in figures) – with the die's back-side 124. In another embodiment, an exposed portion of die back-side 124 may facilitate stacking of one or more additional die on top of die 120, such as die 121 shown in dashed line in each of FIGS. 1H and 1I. Die 121 may be coupled with die 120 by any suitable interconnect structure (e.g., thru-silicon vias, or TSVs, wirebonds, etc.).

In the embodiments described thus far, die 120 was coupled with substrate 110 by a number of interconnects 125. However, in other embodiments, alternative structures and/or methods may be utilized to couple die 120 with substrate 110. For example, as shown in FIG. 1J, the dielectric and metal build-up layers that form substrate 110 may be built up directly over the die 120, in which case a dielectric and subsequent metal layer may be formed directly on the front-side 122 of die 120, with the metal layer forming electrical contact with one or more bond pads on the die. In such an embodiment, discrete interconnects 125 may not be necessary, as metallization in the substrate may directly

contact a die bond pad. Examples of processes that may utilize the aforementioned technique include bumpless build-up layer (BBUL), die-embedding, and wafer-level packaging.

In yet another embodiment, wire bonding may be utilized to electrically couple the die 120 with substrate 110. With reference to FIG. 1K, the die 120 may be electrically coupled with substrate 110 by one or more bond wires 127, each bond wire extending between a bond pad on die front side 122 and a bond pad on substrate 110. Note that in the embodiment of FIG. 1K, the die 120 has been flipped over with the die back-side 124 located adjacent the first side 112 of substrate 110 and perhaps attached to substrate 110 by an adhesive (not shown in figures). In the embodiment of FIG. 1K, the encapsulant 150 extends over the front-side of die 122, as well as the die's periphery 126, and also over wirebonds 127. Also, in this embodiment, the encapsulant 150 has a shape that is substantially flat above die 120, but the encapsulant is rounded at the die's periphery 126 and over wirebonds 127.

Turning to FIG. 1L, in another embodiment, two or more die may be disposed on substrate 110 in a stacked relationship, and wirebonds may be used to form electrical connections between each of these die and/or with substrate 110. By way of example, as shown in FIG. 1L, three die 120a, 120b, 120c may be arranged in a stack and disposed on the first side 112 of substrate 110. One or more wirebonds 127 may electrically couple each of the die 120a, 120b, 120c to any one or more of the other die and/or with substrate 110. In the embodiment of FIG. 1L, the encapsulant 150 extends through window 136 of interposer 130 and above the interposer's first surface 132. Further, the encapsulant extends into the gap 190 between the interposer 130 and substrate 110, as well as around one or more of the interconnects 140.

As described above, in some embodiments, the encapsulant 150 may not extend into regions of the lower IC package 100 where interconnects 140 are disposed. According to one embodiment, where it is desired to prevent flow of encapsulant into regions where interconnects 140 are located (or to any other region of the lower IC package 100), one or more flow barriers or other flow control devices or structures may be utilized to control the flow of encapsulant 150 within IC package 100. Any suitable flow barrier, or combination of barriers, may be utilized to control flow of encapsulant 150, such as dams, non-wetting coatings, and trenches, as well as any suitable combination of these and/or other features. Various exemplary embodiments of flow barriers are illustrated in FIGS. 2A through 2E.

Referring to FIG. 2A, in one embodiment, a dam 205a is disposed on the first surface 112 of substrate 110. The dam 205a may be disposed at any suitable location (or locations) in lower IC package 100, as desired, to inhibit the flow of encapsulant 150. In the embodiment of FIG. 2A, for example, the dam 205a is positioned between the
5 periphery 126 of IC die 120 and the set of interconnects 140. Thus, the dam 205a inhibits the flow of encapsulant 150 into regions of IC package 100 occupied by interconnects 140. The dam 205 may be constructed from any suitable materials (e.g., metals, polymers, composites, etc.), and may be bonded to the substrate 110 by any suitable technique (e.g., by an adhesive, by reflowed solder, by diffusion bonding, etc.). In another embodiment,
10 the dam 205a is coupled with the interposer 130 rather than substrate 110, and in a further embodiment the dam 205a is coupled with both the substrate 110 and interposer 130. According to another embodiment, the dam 205a is formed integral with the substrate 110 (or, alternatively, is formed integral with interposer 130).

Referring next to FIG. 2B, in another embodiment, a non-wetting coating or layer
15 205b is disposed on the substrate's first surface 112, wherein the non-wetting layer comprises a material that is non-wetting with respect to the encapsulant material 150. The non-wetting layer 205b may be disposed at any suitable location (or locations) in lower IC package 100, as desired to inhibit the flow of encapsulant 150. In one embodiment, the non-wetting layer 205b is positioned between the periphery 126 of IC die 120 and the
20 array of interconnects 140 and, therefore, the non-wetting layer 205b inhibits the flow of encapsulant 150 into regions of IC package 100 occupied by interconnects 140. The non-wetting layer 205b may comprise any suitable material or combination of materials that is non-wetting with respect to the encapsulant material 150 (e.g., fluoropolymers, etc.), and may be disposed on the substrate 110 by any suitable technique (e.g., by spray-coating
25 using a mask, by photolithography, by dispensing using a needle or syringe, etc.). In another embodiment, the non-wetting layer 205b is disposed on the interposer 130 rather than substrate 110, and in a further embodiment a non-wetting layer 205b is disposed on each of the substrate 110 and interposer 130.

Turning to FIG. 2C, in a further embodiment, a trench 205c is disposed on the first
30 surface 112 of substrate 110. The trench 205c may be disposed at any suitable location (or locations) in lower IC package 100, as desired to inhibit the flow of encapsulant 150. In the embodiment of FIG. 2C, for example, the trench 205c is positioned between the periphery 126 of IC die 120 and the set of interconnects 140 and, accordingly, the trench 205c inhibits the flow of encapsulant 150 into regions of IC package 100 occupied by the

interconnects 140. The trench 205c may be formed using any suitable technique (e.g., by etching, by machining, by laser ablation, etc.). In another embodiment, a trench 205c is disposed on the interposer 130 rather than substrate 110, and in a further embodiment a trench 205c is formed on each of substrate 110 and interposer 130.

5 In one embodiment, a flow barrier or structure may extend around a periphery of the die 120 and through the region between the die 120 and interconnects 140. For example, in one embodiment, as shown in FIG. 2D, a barrier (e.g., 205a, or 205b, or 205c) is disposed on the first surface 112 of substrate 110, and is positioned on the substrate first surface 112 between the die 120 and a region 145 occupied by interconnects 140.

10 According to one embodiment, the flow barrier (205a, or 205b, or 205c) extends entirely around the die's periphery 126; however, in other embodiments, a flow barrier may be discontinuous and one or more breaks or voids may exist in this structure. By way of example, in one embodiment, as shown in FIG. 2E, a flow barrier (e.g., 205a, or 205b, or 205c) may comprises a plurality of separate discrete elements that, together, inhibit the
15 flow of encapsulant 150. In yet a further embodiment, a flow barrier may comprise a plurality of discrete elements disposed on the substrate 110 (or interposer 130), and these discrete elements may comprise passive electrical devices (e.g., a capacitor, resistor, inductor, or any combination of these and/or other devices).

Referring now to FIG. 3, illustrated is an embodiment of a package-on-package
20 (PoP) assembly 302. The PoP assembly 302 includes a lower IC package 100 and an upper IC package 300. Lower IC package 100 may comprise any one of the embodiments of a lower IC package described herein. According to one embodiment, lower IC package 100 includes one or more processing systems and upper IC package 300 includes one or more memory devices. In another embodiment, lower IC package 100 includes one or
25 more processing systems and upper IC package 300 comprises a wireless communications system (or, alternatively, includes one or more components of a communications system). In a further embodiment, lower IC package 100 includes one or more processing systems and upper IC package 300 includes a graphics processing system. The PoP assembly 302 may comprise part of any type of computing system, such as a hand-held computing
30 system (e.g., a cell phone, smart phone, music player, etc.), mobile computing system (e.g., a laptop, nettop, tablet, etc.), a desktop computing system, or a server. In one embodiment, the PoP assembly comprises a solid state drive (SSD).

Upper IC package 300 may comprise any suitable package structure. In one embodiment, as shown in FIG. 3, the upper IC package 300 comprises a number of IC die

320a, 320b, 320c disposed on a package substrate 310. A number of wirebonds 327 electrically connect each of the die 320a, 320b, 320c with one or more of the other die and/or with substrate 310. A molding material 355 may be disposed over the die 320a-c and substrate 310. According to one embodiment, a plurality of interconnects 340 couple
5 the upper IC package 300 to lower IC package 100. In one embodiment, the set of interconnects 340 are coupled with the set of terminals 180 on the interposer 130.

Each of the interconnects 340 may comprise any type of structure and materials capable of providing electrical communication between the upper and lower IC packages 100, 300. According to one embodiment, the set of interconnects 340 comprises an array
10 of solder bumps extending between bond pads 180 on the interposer 130 of lower IC package 100 and the substrate 310 of upper IC package 300 (perhaps in combination with an array of columns and/or pads disposed on the substrate 310). A solder reflow process may be utilized to form the plurality interconnects 340. Of course, it should be understood that many other types of interconnects and materials are possible. In one embodiment, the
15 array of interconnects 340 also aid in mechanically securing the upper IC package 300 to the lower IC package 100.

In one embodiment, as illustrated in FIG. 3, a gap 395 may exist between an upper surface of encapsulant 150 and a lower surface of substrate 310. In another embodiment, the substrate 310 may rest upon the encapsulant 150. Where the substrate 310 contacts the
20 encapsulant 150, the encapsulant may be utilized to control the stand-off height between the interposer 130 and substrate 310 and, hence, to maintain a desired height of interconnects 340.

Turning now to FIG. 4, illustrated is an embodiment of a computing system 400. The system 400 includes a number of components disposed on a mainboard 410 or other
25 circuit board. Mainboard 410 includes a first side 412 and an opposing second side 414, and various components may be disposed on either one or both of the first and second sides 412, 414. In the illustrated embodiment, the computing system 400 includes a PoP assembly 302 disposed on the mainboard's first side 412, and PoP assembly 302 may comprise any of the embodiments described herein. System 400 may comprise any type
30 of computing system, such as a hand-held computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, etc.) or a mobile computing device (e.g., a laptop computer, a nettop computer, tablet computer, etc.). However, the disclosed embodiments are not limited to hand-held and other mobile computing devices and these

embodiments may find application in other types of computing systems, such as desk-top computers and servers.

Mainboard 410 may comprise any suitable type of circuit board or other substrate capable of providing electrical communication between one or more of the various components disposed on the board. In one embodiment, for example, the mainboard 410 comprises a printed circuit board (PCB) comprising multiple metal layers separated from one another by a layer of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route – perhaps in conjunction with other metal layers – electrical signals between the components coupled with the board 410. However, it should be understood that the disclosed embodiments are not limited to the above-described PCB and, further, that mainboard 410 may comprise any other suitable substrate.

As noted above, disposed on the first side 412 of mainboard 410 is a PoP assembly 302. The PoP assembly 302 may comprise an upper IC package 300 coupled with a lower IC package 100, as previously described. The PoP assembly 302 may include any desired combination of integrated circuit devices. In one embodiment, the PoP assembly 302 includes any one or more of a processing system, a graphics processing system, a signal processing system, a wireless communications system, a network processing system, a chipset, a memory, as well as combinations of these and/or other systems. In one embodiment, an IC die disposed in PoP assembly 302 comprises a system-on-chip (SoC). However, it should be understood that the disclosed embodiments are not limited to any particular type or class of IC devices. Also, it should be noted that, in some embodiments, other components may be disposed on the PoP assembly 302. Other components that may be disposed in PoP assembly 302 include, for example, a voltage regulator and passive electrical devices, such as capacitors, resistors, filters, inductors, etc.

The PoP assembly 302 is electrically connected with mainboard 410 by a plurality of terminals 170 (e.g., lands, solder bumps, metal columns or pillars, etc.) extending from the PoP assembly, which are coupled with corresponding terminals (e.g., bond pads, bumps, columns, pillars, etc.) on the substrate 410. Any suitable process may be utilized to form electrical connections between the set of terminals 170 of PoP assembly 302 and the corresponding set of terminals on substrate 410. For example, these mating terminals may be electrically coupled (and perhaps mechanically joined) by a solder reflow process.

In addition to PoP assembly 302, one or more additional components may be disposed on either one or both sides 412, 414 of the mainboard 410. By way of example,

as shown in the figures, components 401a may be disposed on the first side 412 of the mainboard 110, and components 401b may be disposed on the mainboard's opposing side 414. Additional components that may be disposed on the mainboard 410 include other IC devices (e.g., processing devices, memory devices, signal processing devices, wireless communication devices, etc.), power delivery components (e.g., a voltage regulator, a power supply such as a battery, and/or passive devices such as a capacitor), and one or more user interface devices (e.g., an audio input device, an audio output device, a keypad or other data entry device such as a touch screen display, and/or a graphics display, etc.), as well as any combination of these and/or other devices. In another embodiment, the computing system 400 includes a radiation shield. In a further embodiment, the computing system 400 includes a cooling solution. In yet another embodiment, the computing system 400 includes an antenna. In yet a further embodiment, the assembly 400 may be disposed within a housing.

Referring to FIG. 5, illustrated are embodiments of a method of making a lower IC package, as well as attaching the lower IC package to an upper IC package to form a PoP assembly. As set forth in block 510, one or more IC die are attached to a substrate, and in some embodiments an underfill material may be disposed between an IC die and the substrate (see, e.g., die 120 – or 120a-c – and underfill 160 in any of the embodiments illustrated in FIGS. 1A through 1L, as well as the accompanying text above). As set forth in block 520, an interposer is coupled with the substrate (see, e.g., interposer 130 in any of the embodiments of FIGS. 1A through 1L). As set forth in block 530, an encapsulant is disposed in the lower IC package (see, e.g., encapsulant 150 in any of the embodiments of FIGS. 1A through 1L). The encapsulant 150 may be disposed in the IC package using any suitable technique, such as by a syringe or needle dispenser, by molding, by stencil printing, etc. In one embodiment, as set forth in block 515, one or more flow barriers are disposed in the lower IC package to control flow of encapsulant 150 (see, e.g., flow barriers 205a-c in any of the embodiments illustrated in FIGS. 2A through 2E, as well as the accompanying text above). According to one embodiment, the substrate and interposer are constructed as part of a panel or strip, and one or more of the aforementioned assembly processes may be performed at the panel level, in which case the discrete package assemblies are separated from one another by a singulation process, as set forth in block 535. In yet another embodiment, as set forth in block 540, an upper IC package is attached to the lower IC package to form a PoP assembly (see, e.g., FIG. 3 and the accompanying text above).

Numerous embodiments have been described with respect to FIGS. 1A through 1L, FIGS. 2A through 2E, FIG. 3, FIG. 4, and FIG. 5, and it should be understood that these embodiments, or certain features of an embodiment, may be used in any combination. For example, any of the flow barriers illustrated in FIGS. 2A through 2E may be utilized with
5 any of the other embodiments described herein. By way of further example, any of the embodiments of a lower IC package illustrated in FIGS. 1A through 1L may form part of a PoP assembly (e.g., see FIG. 3) or a computing system (e.g., see FIG. 4). Also, terms such as “first side”, “second side”, “first surface”, “second surface”, and so on, are used herein to describe various features of the disclosed embodiments. However, it should be
10 understood that any suitable nomenclature or terminology may be ascribed to the various features and embodiments disclosed herein (e.g., “upper side”, “lower side”, “upper surface”, “lower surface”, etc.).

The above-described embodiments may exhibit several noteworthy features. The combination of the interposer and encapsulant can reduce package warpage during
15 temperature cycling (e.g., at reflow temperatures), and can also reduce package warpage of the final assembly (e.g., at room temperature). Simulation studies have suggested that the combination of the interposer and encapsulant can, in some embodiments, potentially reduce by over half the warpage that occurs during temperature cycling and, further, reduce by over half the warpage of the final assembly. In addition, the interposer may
20 provide pads to mate with bumps (or other terminals) extending from the upper IC package, which eliminates a bump tip-to-bump tip interface that can occur where interconnects between the upper and lower IC packages comprise a bump-on-bump structure. Eliminating such bump tip-to-bump tip engagements during assembly can minimize misalignment between the upper and lower IC packages and, further, may
25 reduce non-wet solder joint failures. Also, a solder bumping step is not needed on the interposer prior to attachment to the upper IC package (however, application of a solder paste layer to pads on the interposer is within the scope of the disclosed embodiments). Furthermore, in addition to providing increased package stiffness, the encapsulant can protect any IC die disposed in the lower IC package and reduce die cracking. In some
30 embodiments, a thin die (e.g., a die having a thickness of 250 micrometers, or less) may be disposed in the lower IC package, and the encapsulant can protect such a thin die.

The foregoing detailed description and accompanying drawings are only illustrative and not restrictive. The figures may not show the actual size and/or scale of features that are represented. The figures have been provided primarily for a clear and

comprehensive understanding of the disclosed embodiments and no unnecessary limitations are to be understood therefrom. Numerous additions, deletions, and modifications to the embodiments described herein, as well as alternative arrangements, may be devised by those skilled in the art without departing from the spirit of the disclosed

5 embodiments and the scope of the appended claims.

CLAIMS

What is claimed is:

1. A lower integrated circuit (IC) package, the lower IC package for coupling with an upper IC package to form a package-on-package assembly, the lower IC package comprising:

a substrate having a first side and an opposing second side;

an IC die coupled with the first side of the substrate;

an encapsulant, the encapsulant disposed over at least a portion of a surface of the die and over at least a portion of the first side of the substrate;

- 10 an interposer having a first side and an opposing second side, the second side of the interposer facing the first side of the substrate;

a number of interconnects electrically coupling the interposer with the substrate;

and

- 15 a plurality of terminals disposed on the first side of the interposer, the plurality of terminals for forming electrical connections with the upper IC package.

2. The lower IC package of claim 1, further comprising a barrier to control flow of the encapsulant.

3. The lower IC package of claim 2, wherein the barrier inhibits flow of the encapsulant toward the number of interconnects.

- 20 4. The lower IC package of claim 2, wherein the barrier comprises a structure selected from a group consisting of a dam, a coating that is non-wetting with respect to the encapsulant, and a trench.

5. The lower IC package of claim 1, wherein a portion of the surface of the IC die is substantially free of encapsulant.

- 25 6. The lower IC package of claim 1, wherein the encapsulant extends over at least a portion of a surface of one or more of the number of interconnects.

7. The lower IC package of claim 1, wherein the interposer comprises a frame having an opening.

8. The lower IC package of claim 1, further comprising an underfill material disposed between the IC die and the first side of the substrate, wherein the encapsulant contacts at least a portion of the underfill material.

9. The lower IC package of claim 1, further comprising a number of
5 wirebonds electrically coupling the IC die with the substrate, wherein the encapsulant is disposed over at least one of the wirebonds.

10. The lower IC package of claim 1, wherein the substrate is built up directly over the IC die.

11. The lower IC package of claim 1, wherein at least one of the plurality of
10 terminals comprises an electrically conductive pad, the pad capable of forming an electrical connection with an electrically conductive bump extending from the upper IC package.

12. The lower IC package of claim 1, further comprising a second plurality of terminals disposed on the second side of the substrate, the second plurality of terminal for
15 electrically coupling the lower IC package with a circuit board.

13. A package-on-package (PoP) assembly comprising:

a lower integrated circuit (IC) package, the lower IC package including a substrate having a first side and an opposing second side, an IC die coupled with the first side of the substrate, an interposer having a first side and an opposing second side that faces the first
20 side of the substrate, a number of interconnects electrically coupling the interposer with the substrate, and an encapsulant, the encapsulant disposed over at least a portion of a surface of the die and over at least a portion of the first side of the substrate;

an upper IC package; and

a plurality of interconnects electrically coupling the upper IC package with the first
25 side of the interposer.

14. The PoP assembly of claim 13, wherein the upper IC package comprises at least one IC die disposed on a second substrate.

15. The PoP assembly of claim 14, further comprising:

an electrically conductive pad disposed on the first side of the interposer;

wherein at least one of the plurality of interconnects includes a solder bump extending from the second substrate and coupled with the conductive pad.

16. The PoP assembly of claim 13, further comprising a barrier disposed in the lower IC package to control flow of the encapsulant.

5 17. The PoP assembly of claim 13, wherein the encapsulant extends over at least a portion of a surface of one or more of the number of interconnects.

18. The PoP assembly of claim 13, wherein the interposer comprises a frame having an opening.

10 19. The PoP assembly of claim 13, wherein the substrate of the lower IC package is built up directly over the IC die.

20. The PoP assembly of claim 13, further comprising a plurality of terminals on the second side of the substrate of the lower IC package, the plurality of terminals for electrically coupling the PoP assembly with a circuit board.

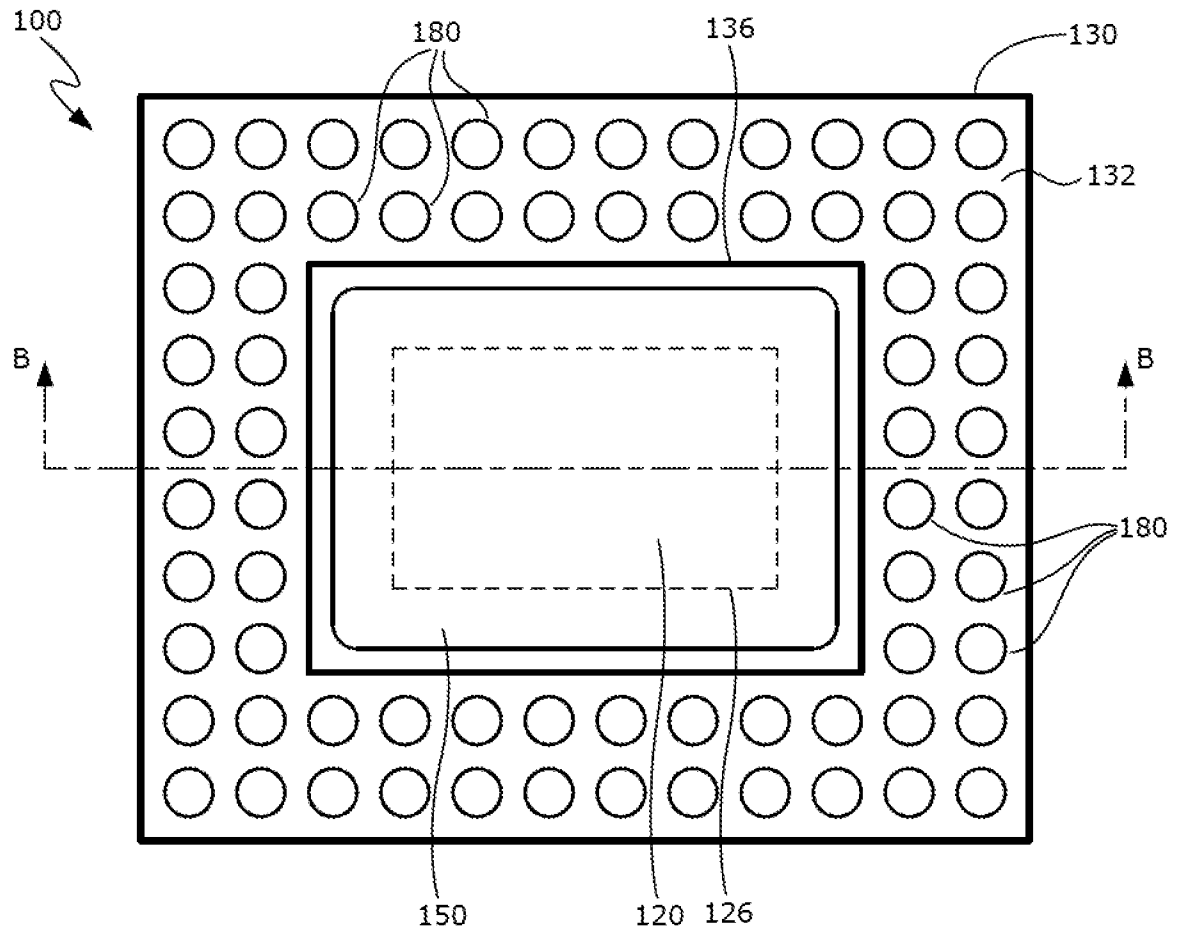


FIG. 1A

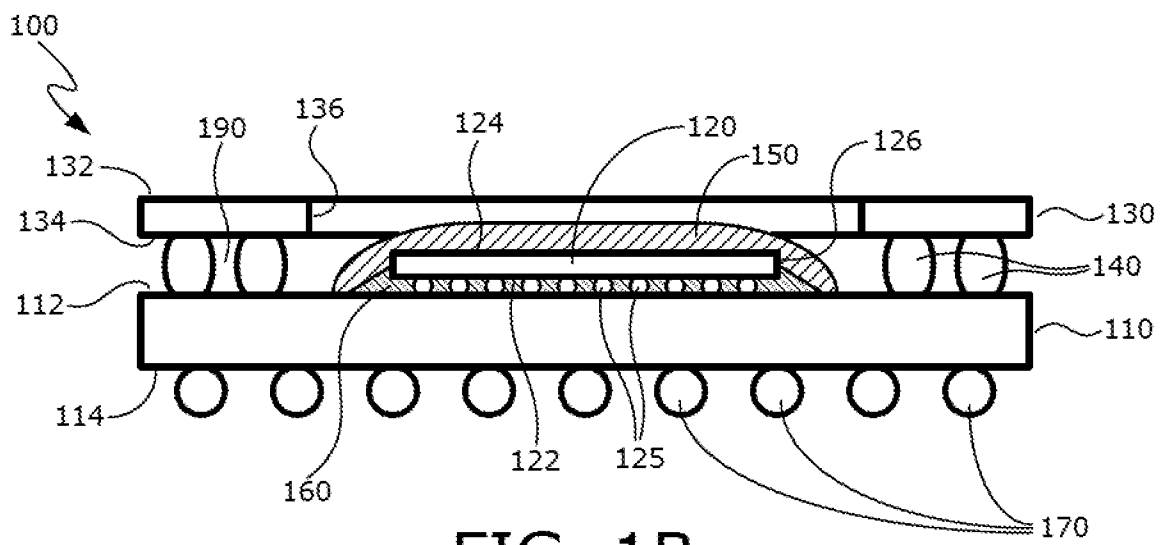


FIG. 1B

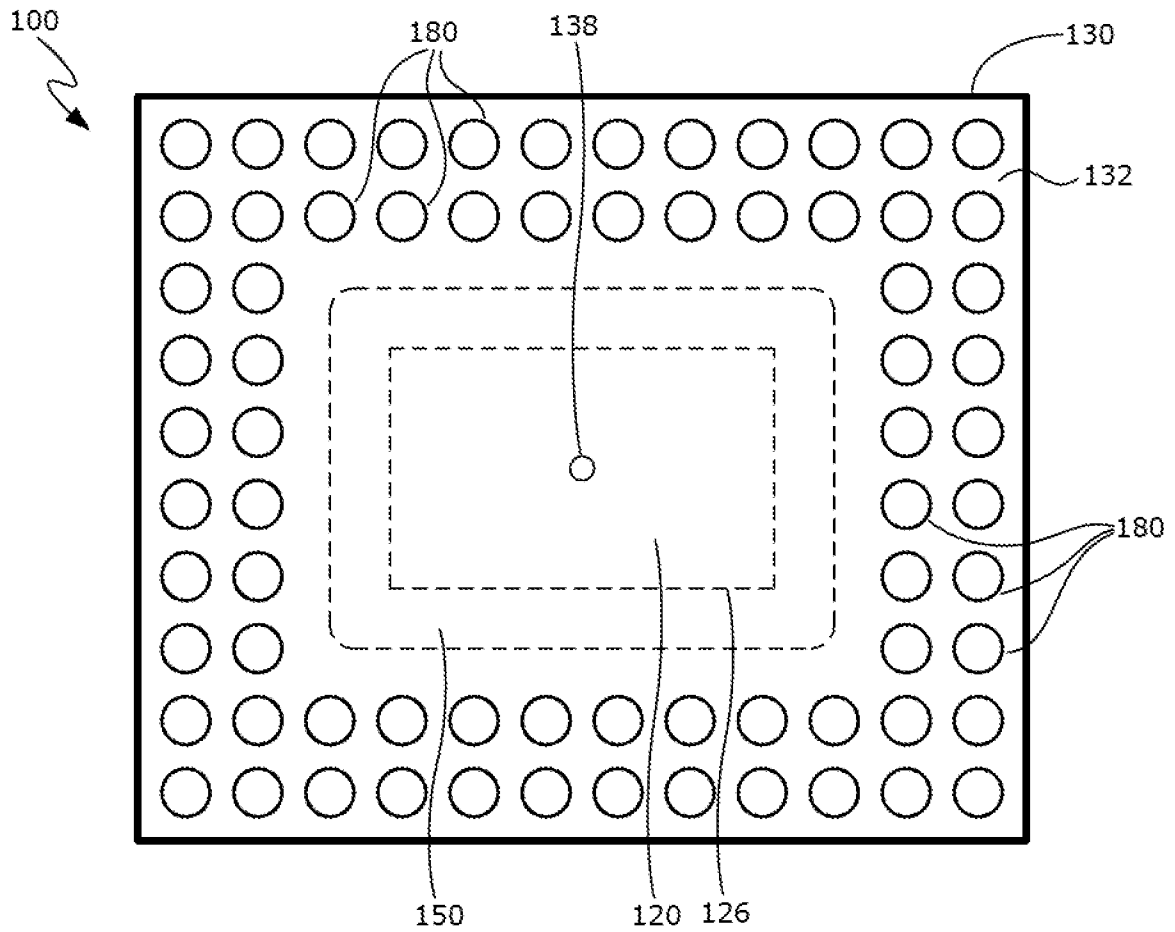


FIG. 1C

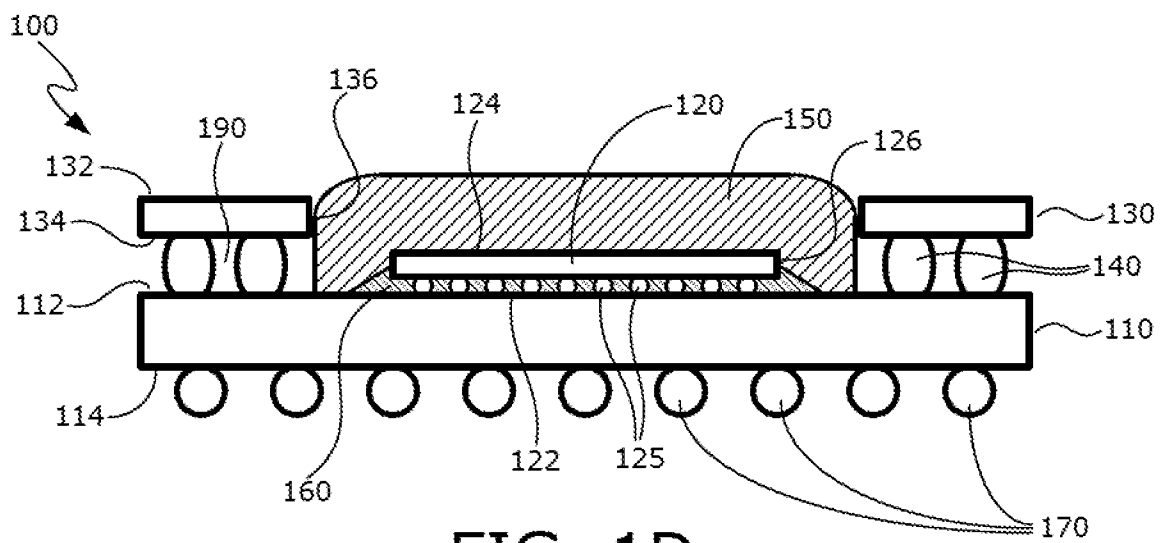


FIG. 1D

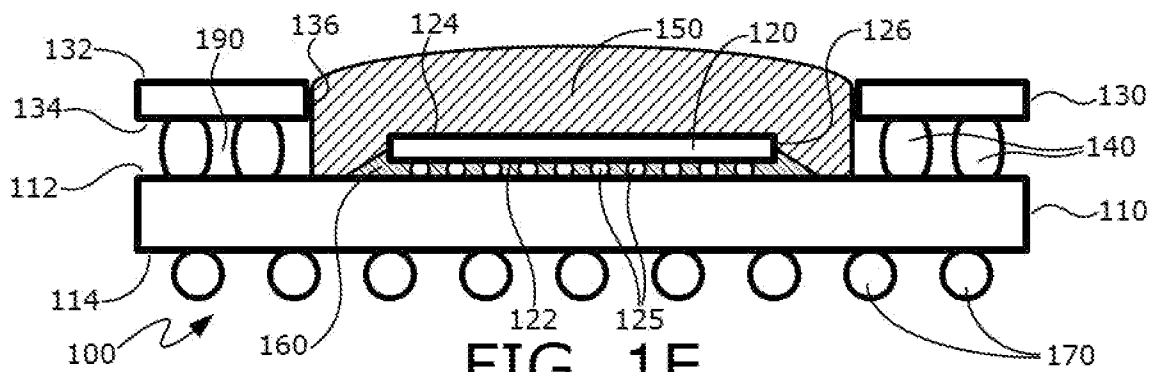


FIG. 1E

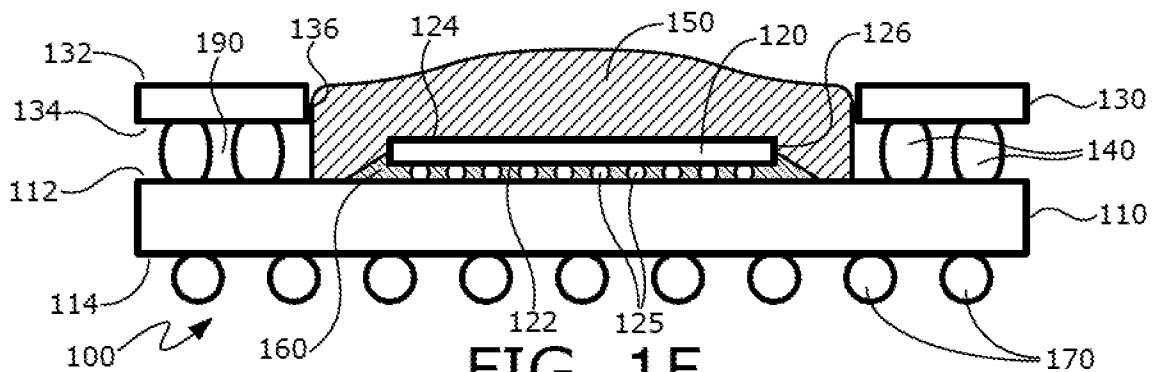


FIG. 1F

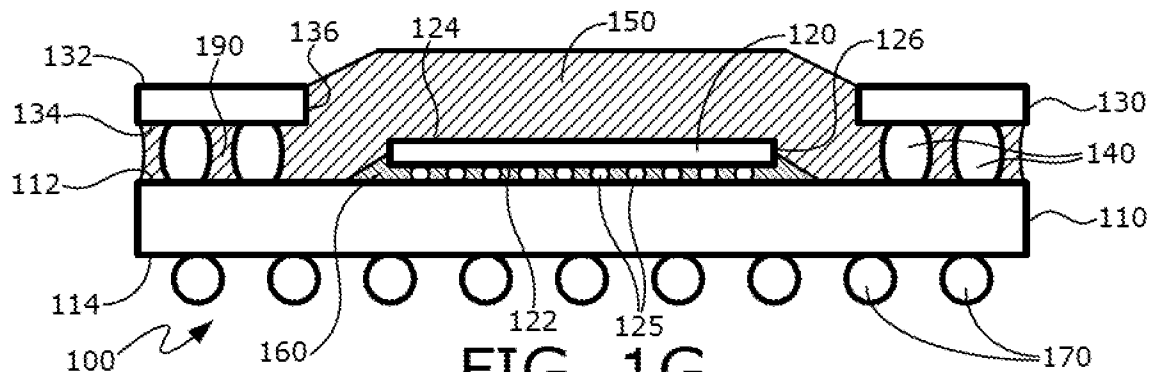


FIG. 1G

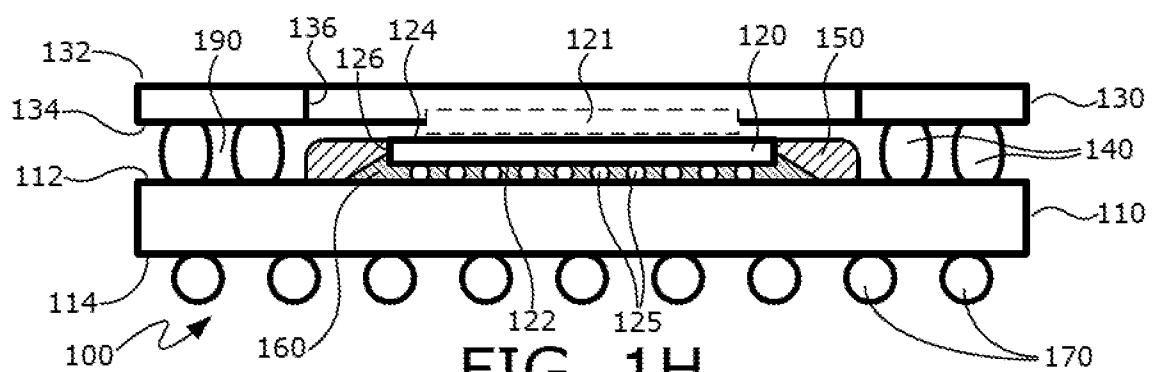


FIG. 1H

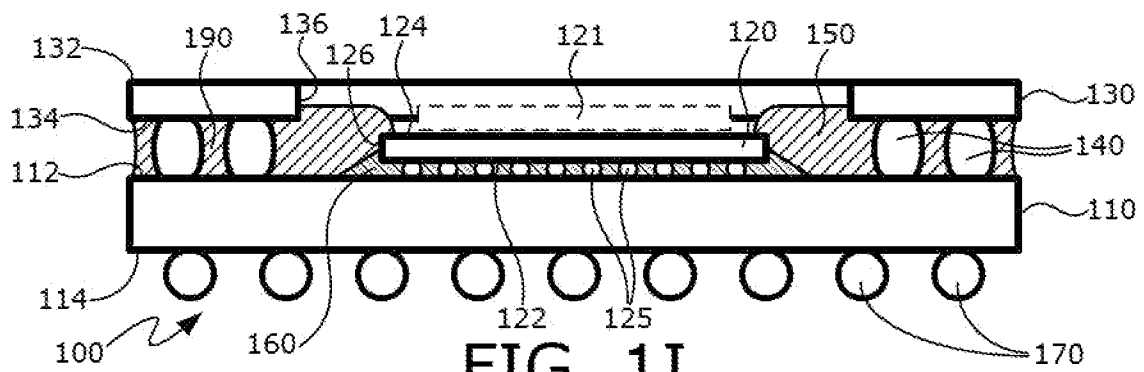


FIG. 1I

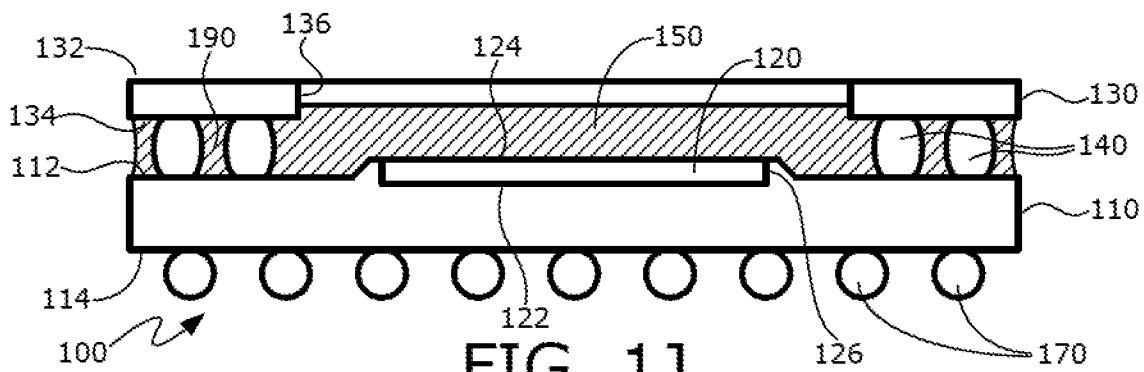


FIG. 1J

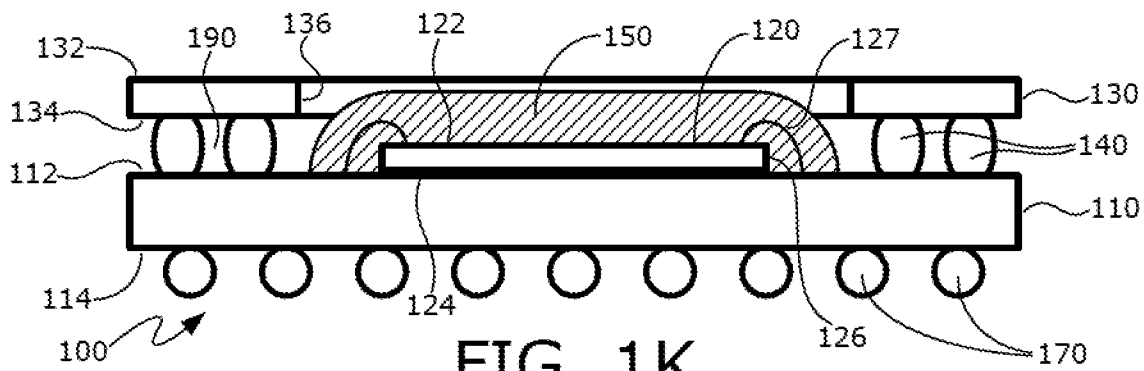


FIG. 1K

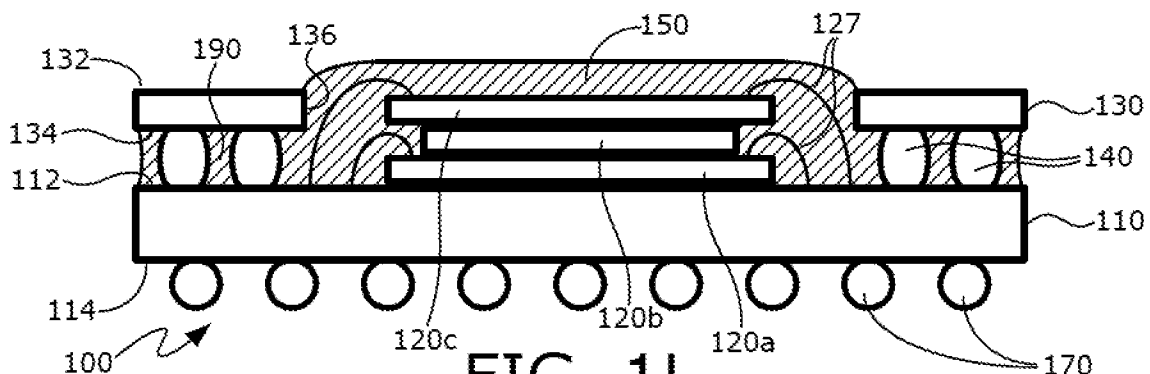
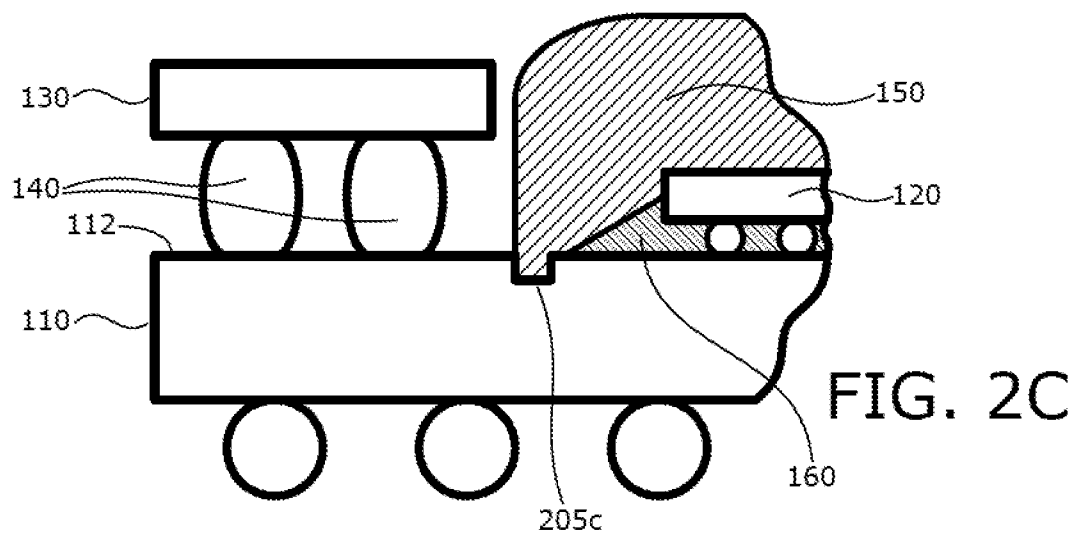
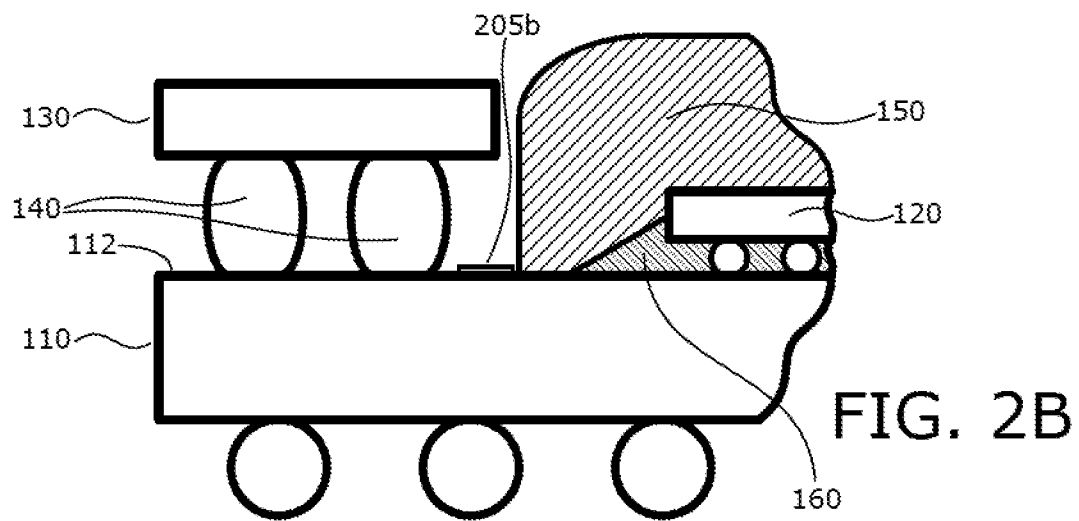
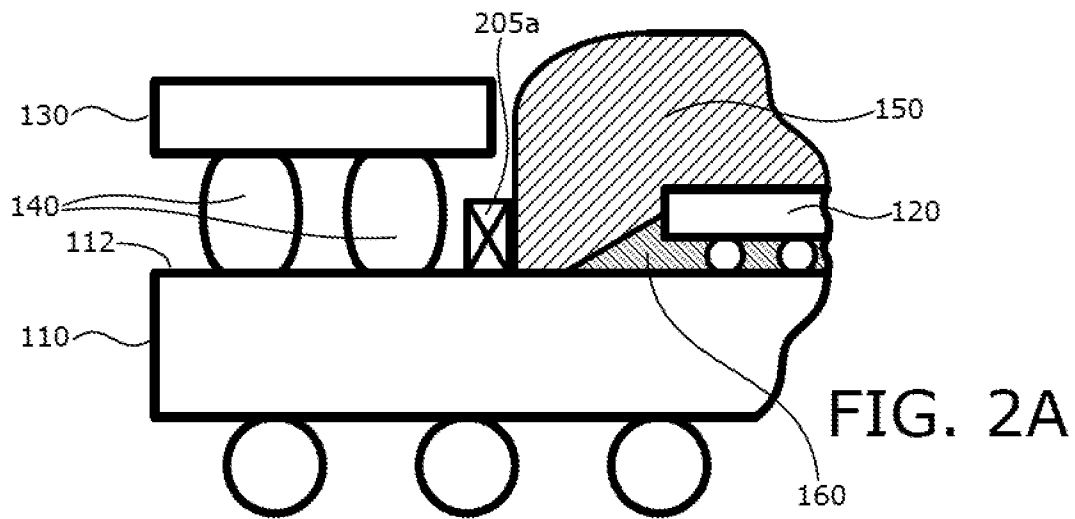
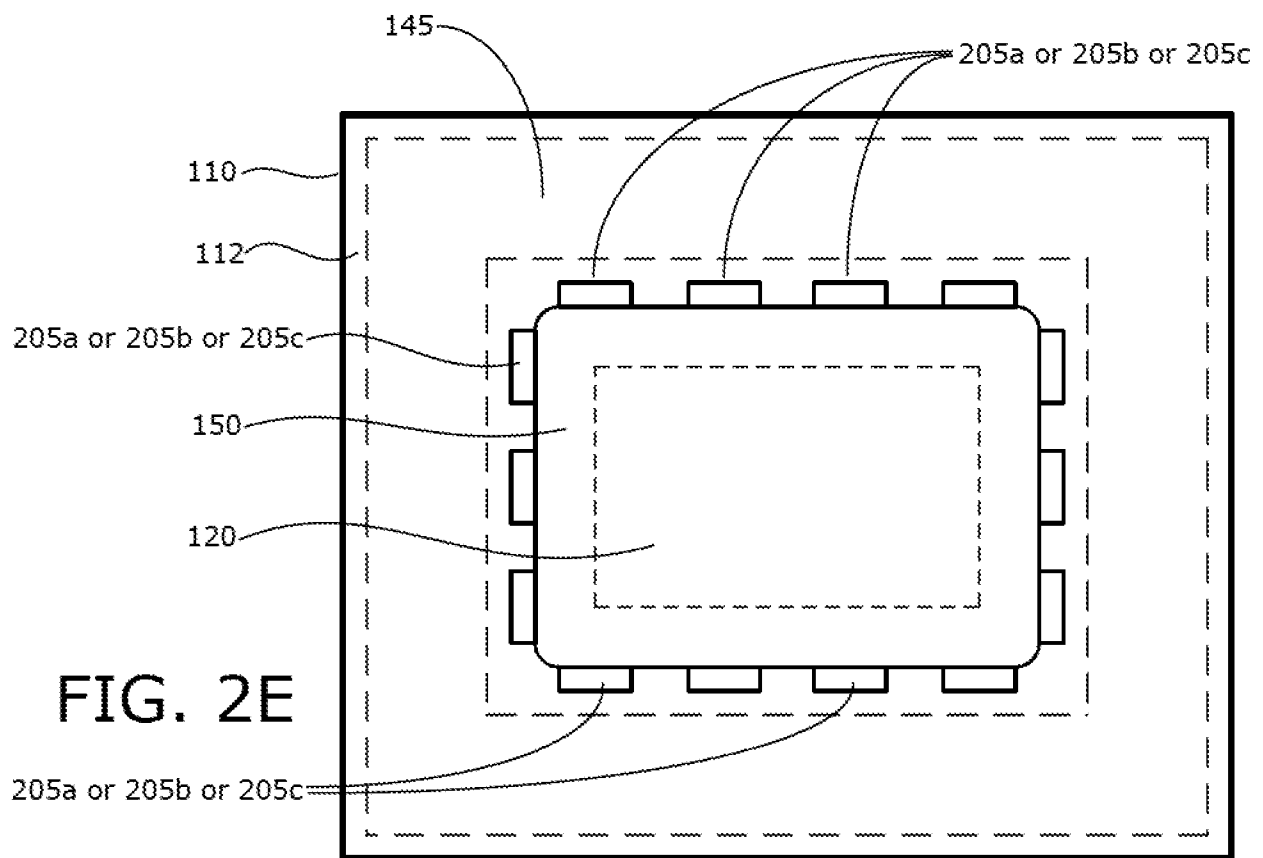
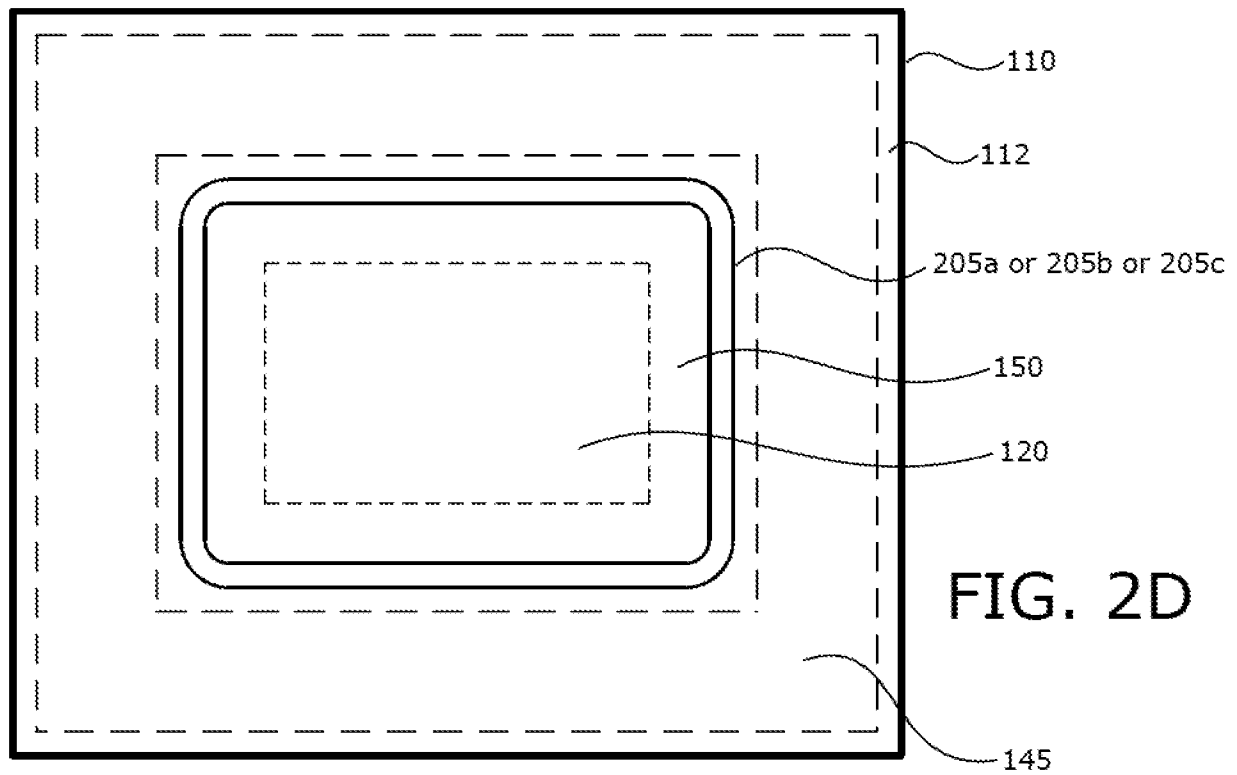


FIG. 1L





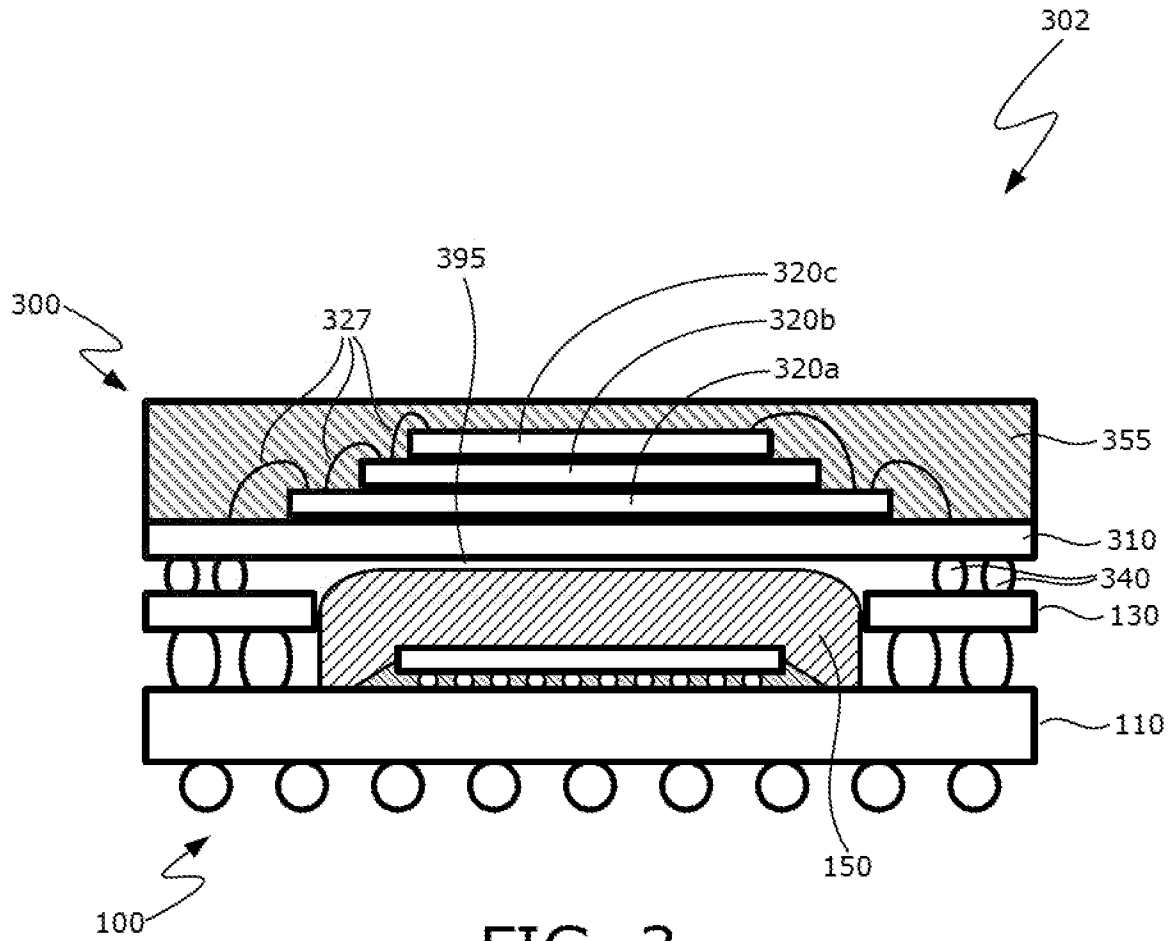


FIG. 3

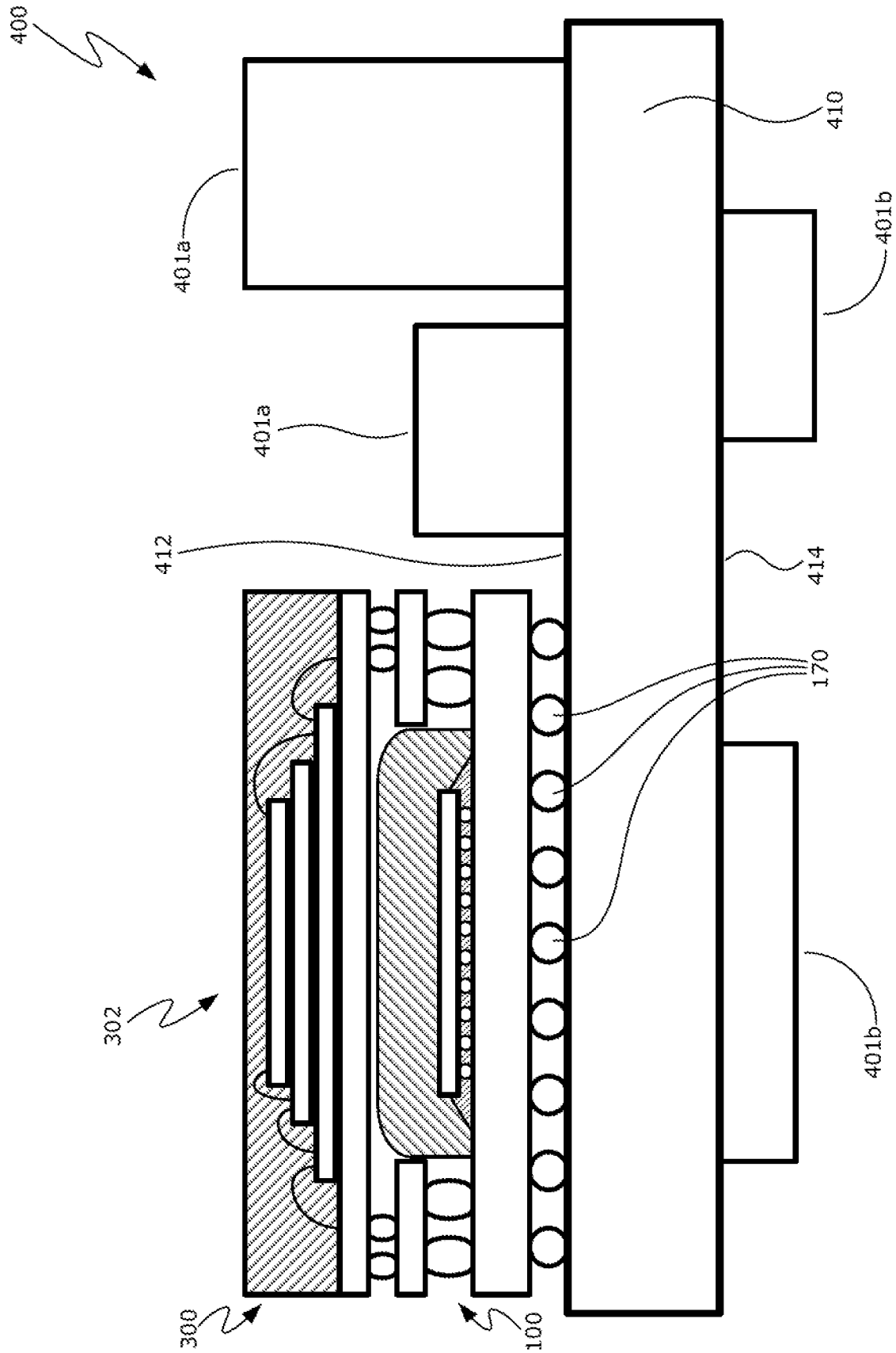


FIG. 4

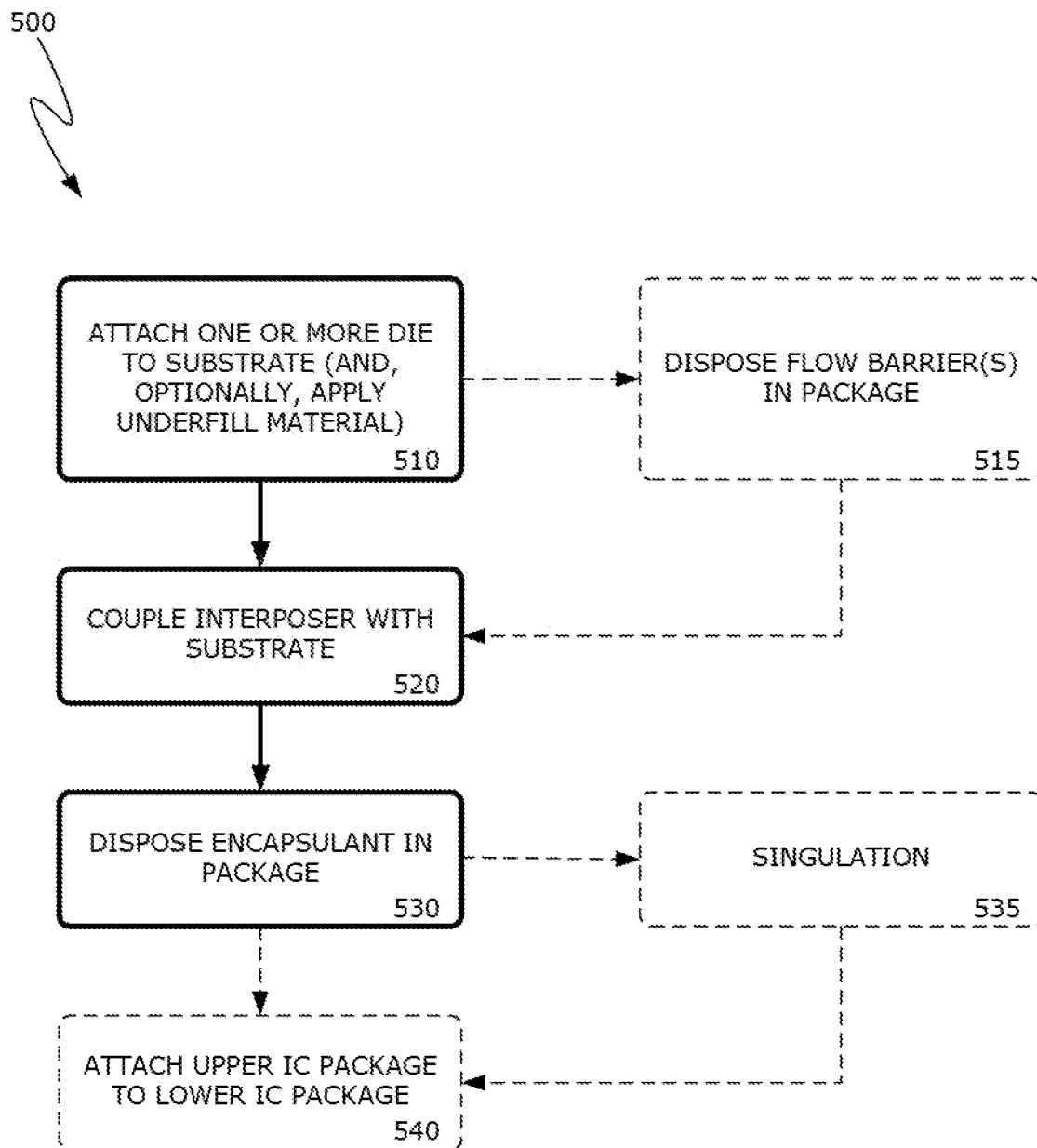


FIG. 5

A. CLASSIFICATION OF SUBJECT MATTER***H01L 23/28(2006.01)i, H01L 23/02(2006.01)i, H01L 23/48(2006.01)i***

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/28; H01L 23/52; H01L 21/56; H01L 23/538; H01L 23/053; H01L 21/98

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: IC package, upper, lower, interposer, encapsulant, PoP

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010-0148344 A1 (HARRY CHANDRA et al.) 17 June 2010	1,5-15,17-20
Y	See abstract; paragraphs [0027]-[0079]; claims 1-20; and figures 1-13.	2-4,16
Y	US 2004-0212082 A1 (JICHENG YANG) 28 October 2004 See abstract; paragraphs [0041]-[0042]; and figure 3.	2-4,16
X	US 2009-0166834 A1 (IN SANG YOON et al.) 02 July 2009 See abstract; paragraphs [0019]-[0048]; and figures 1-6.	1,7-9,11,13-15,18
X	US 2010-0237482 A1 (JOUNGIN YANG et al.) 23 September 2010 See abstract; paragraphs [0040]-[0110]; and figures 1-9.	1,9,12



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

30 MAY 2012 (30.05.2012)

Date of mailing of the international search report

31 MAY 2012 (31.05.2012)

Name and mailing address of the ISA/KR

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Authorized officer

CHOI, SANGWON

Telephone No. 82-42-481-5695



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2011/062550

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