Oct. 13, 1970 B. D. EPLER 3,534,222

ELECTRONIC TIMER CIRCUIT FOR DELAYED APPLICATION OF DISCHARGE POTENTIAL

Filed Nov. 4, 1968 2 Sheets-Sheet 1

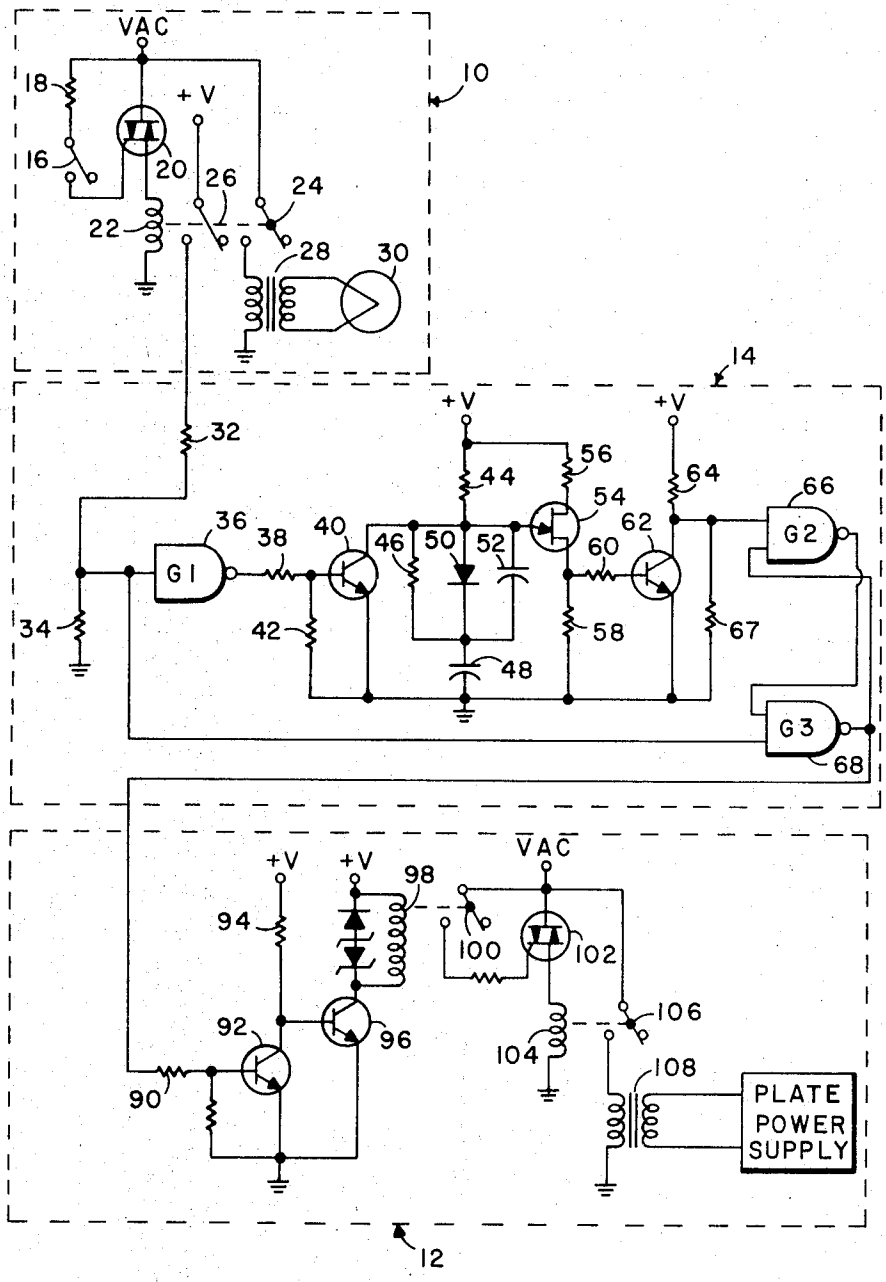


FIG. 1

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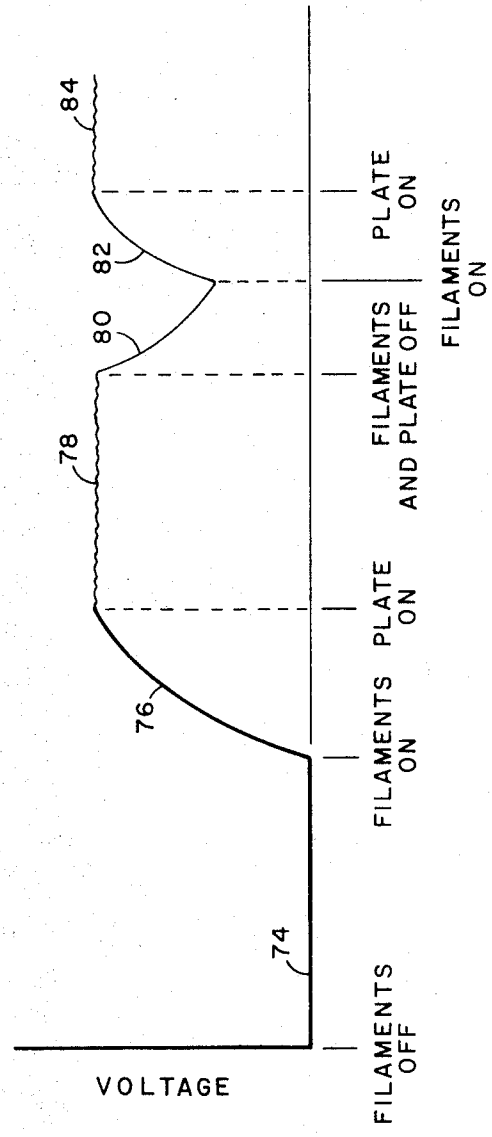


FIG. 2

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ELECTRONIC TIMER CIRCUIT FOR DELAYED APPLICATION OF DISCHARGE POTENTIAL

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U.S. Cl. 315—102 4 Claims

ABSTRACT OF THE DISCLOSURE

A timer especially suited for use in the power control for an electronic power tube including first and second switch means which are interconnected by gating and voltage charging means whereby the closing of the first switch means causes the second switch means to close after a predetermined period of time. Deactuation of the first switch means causes the immediate deactuation of the second switch means.

This invention relates to timers, and in particular to fast acting, solid state circuit timers.

Most presently available timers are rather large mechanical devices which are relatively slow acting and which require considerable power. In many applications such timers are at best merely tolerable and often inadequate. One such application is in the electrical power control for power tubes in radio transmitters. The power tubes must have filament voltage applied for a given length of time before plate voltage is applied to prevent tube damage. Further, should the filament voltage be turned off, the plate voltage must be immediately turned off and held off until the filament voltage is again applied for a period of time which is functionally related to the period of time the filament voltage was off.

An object of this invention is an improved timer.

Another object of this invention is a solid state timer which is fast acting.

Another object of this invention is a solid state timer which requires little power.

Yet another object of this invention is a solid state timer which is especially suited for use in the power control for a radio transmitter.

These and other objects and features of the invention will be apparent from the following description and appended claims.

Briefly, the timer in accordance with the present invention includes a first switch means and a second switch means which are interconnected by gating and voltage charging means whereby the closing or actuation of the first switch means causes the second switch means to close or actuate after a predetermined period of time. Deactuation of the first switch means causes the immediate deactuation of the second switch means. The gating and voltage charging means includes a first gate means which is actuated by the closing of the first switch means. A first circuit means is provided for charging the voltage charging means in response to the actuation of the first gate means, and second circuit means are provided for discharging said voltage charging means in response to the deactuation of said first gate means. Second gate means is provided which is actuated by the accumulation of a predetermined charge on said voltage charging means, and the second switch means is operatively connected to the second gate means and actuated in response to the actuation of the second gate means. Further, the second gate means is operatively connected to the first gate means

whereby the second gate means is deactuated in response to the deactuation of the first gate means, and the second switch means is deactuated in response to the deactuation of the second gate means.

The invention will be more fully understood from the following detailed description of a preferred embodiment and appended claims when taken with the drawing, in which:

FIG. 1 is a schematic diagram of one embodiment of the invention, and

FIG. 2 is a time sequenced plot of the voltage appearing across the capacitive voltage charging means which is employed in the circuit illustrated in FIG. 1.

Referring now to the drawing, FIG. 1 is a schematic diagram of one embodiment of the timer in accordance with the invention. Since the timer has particular application in the power control for an electronic tube, the circuit is illustrated for such an application. It will be appreciated, of course, that the timer may be utilized in numerous applications. In this application first switch means for controlling the tube filament voltage is shown generally at **10**, switch means for controlling the plate power voltage is shown generally at **12**, and gating means and capacitive voltage charging means are shown generally at **14**.

Looking first at the circuit portion **10** for controlling the tube filament voltage, the filament voltage is applied by closing switch **16**. Switch **16** is serially connected with resistor **18** between an A.C. voltage source and the control electrode of triac **20**. The closing of switch **16** triggers triac **20** and allows current to flow through the triac **20** and relay coil **22** which in turn closes contacts **24** and **26**. The closing of contact **24** applies the A.C. voltage source to the primary coil of transformer **28** which energizes the filaments **30** of the electronic tube.

The closing of contact **26** applies a positive voltage across serially connected resistors **32** and **34** and to the input of inverter gate **36** which is connected to the common terminal of resistors **32** and **34**.

The output of gate **36** is connected through resistor **38** to the base of transistor **40**. Resistor **42** is connected between the base of transistor **40** and circuit ground to limit the bias voltage applied to transistor **40**. The collector of transistor **40** is connected through resistor **44** to a positive D.C. voltage potential and through resistor **46** to one terminal of capacitor **48**. The same terminal of capacitor **48** is connected through rectifier **50** and resistor **44** to the positive D.C. voltage source. The other terminal of capacitor **48** is connected to ground. Capacitor **48** is also connected through capacitor **52** to the control electrode of unijunction transistor **54**. The source electrode of unijunction transistor **54** is connected through resistor **56** to the positive D.C. voltage source, and the drain electrode of unijunction transistor **54** is connected through resistor **58** to circuit ground. The drain electrode is also connected through resistor **60** to the base electrode of transistor **62**. The emitter of transistor **62** is grounded and the collector is connected through resistor **64** to a positive D.C. voltage source. The collector is also connected to one of the two inputs to NAND gate **66**. Resistor **68** is connected between the collector of transistor **62** and circuit ground and limits the voltage excursion at the collector of transistor **62**.

The output of NAND gate **66** is connected to one of the two inputs of NAND gate **68**, with the output of NAND gate **68** providing the second input to gate **66**. The second input to gate **68** is taken at the common terminal of resistors **32** and **34**. The output of gate **68** is also applied as a control voltage to the control circuitry

12 for the power supply to the plate of the electronic tube, as described more fully hereinbelow.

Referring again to the gating and voltage charging circuitry shown at 14, when the filament control switch 16 is open, i.e. no voltage is applied to the tube filaments, no voltage appears at the input to inverter gate 36. Gate 36, in response to the "0" input, produces a positive voltage or a "1" which is applied through resistor 38 to forward bias transistor 40. The forward biased transistor 40 provides a short circuit connecting the positive D.C. voltage through resistor 44 to ground. In this situation, no charging current flows through control rectifier 50 to charge capacitor 48. Accordingly, unijunction transistor 54 is nonconducting and the base of transistor 62 is reverse biased. The resulting positive voltage at the collector of transistor 62 is applied as a "1" input to gate 66. The output of NAND gate 66 is a "0" since the other input to gate 66, received from the output of gate 68, is also a "1."

Consider now the closing of switch 16 which applies a voltage to the tube filaments. Contact 26 is closed and applies a positive voltage to the input of gate 36, and gate 36 in turn produces a "0" which is applied to the base of transistor 40. This reverse biases transistor 40 and allows a charging voltage to pass through resistor 44 and control rectifier 50 to capacitor 48. The charging rate for capacitor 48 is determined by the time constant of the charging circuit comprising resistor 44, control rectifier 50 and capacitor 48. As soon as capacitor 44 is charged to a predetermined voltage level, a trigger voltage is applied through capacitor 52 to the control electrode of unijunction transistor 54 which allows current to flow through the unijunction transistor 54. The resulting positive voltage generated across resistor 58 forward biases transistor 62 and drives the voltage on the collector of transistor 62 to ground or "0" level. The removal of this input to gate 66 causes a "1" to appear at the output of gate 66 which is applied to one input of gate 68. The other input to gate 68, derived at the common terminal of resistors 32 and 34, is also a "1," thus the output of gate 68 is a "0." As hereinbelow explained, the "0" appearing at the output of gate 68 effects the closing of switch means in the power supply control circuitry 12 and applies power to the plate of the electronic tube.

Should the filament control switch 16 be opened, removing filament voltage, the output of NAND gate 68 immediately goes to a "1" due to the reception of a "0" from the common terminal of resistors 32 and 34. The "1" at the output of gate 68 causes the plate power supply control circuitry 12 to remove plate voltage, as hereinbelow described. Concurrently therewith, the output of gate 36 becomes a "1" which forward biases transistor 40 and provides a discharge circuit path for capacitor 48 through resistor 46 and transistor 40 to ground. The discharge rate of capacitor 48 is determined by the time constant of the discharge circuitry comprising transistor 40, resistor 46 and capacitor 48. Preferably, the time constant for the discharge circuit path is smaller than the time constant for the charging circuit path, thereby allowing capacitor 48 to discharge appreciably in response to even a momentary removal of filament voltage.

Once the filament control switch 16 is again closed, capacitor 48 again charges through the charging circuitry including resistor 44 and control rectifier 50. After the predetermined voltage level is again reached a "0" again appears at the output of NAND gate 68, as described hereinabove.

The time sequence of the charging and discharging of capacitor 48 is illustrated in FIG. 2. Initially, the filament control switch 16 is open and no voltage appears across capacitor 38, as illustrated by curve 74. As soon as switch 16 is closed and filament voltage is applied to the electronic tube, capacitor 48 begins charging as shown by curve 76. Once the predetermined voltage

level is reached across capacitor 48, a voltage level is maintained by the voltage leakage through capacitor 52 and unijunction transistor 54 as illustrated by the curve 78. When the filament control switch 16 is opened and filament voltage removed, capacitor 48 begins discharging as illustrated by curve 80. The capacitor 48 continues to discharge until the switch 16 is again closed, whereupon capacitor 48 again commences charging as illustrated by curve 82. Again, as soon as the predetermined voltage level is developed across capacitor 48 a more or less constant voltage is maintained as illustrated by curve 84.

Referring now to the plate power supply control circuitry 12, the output of NAND gate 68 is connected through resistor 90 to the base of transistor 92. The collector of transistor 92 is connected through resistor 94 to a positive D.C. voltage source and also to the base of transistor 96. When a "1" is received at the base of transistor 92 from the output of gate 68 (i.e. when the filament control switch 16 is open), transistor 92 is forward biased which drives the voltage on the base of transistor 96 to ground level and renders transistor 96 non-conducting. Relay coil 98 which is connected between the collector of transistor 96 and a positive D.C. voltage potential is de-energized and contact 100 is open. With contact 100 open no voltage is applied to the control electrode of triac 102, and relay coil 104, which is serially connected with triac 102 between ground and an A.C. voltage source, is de-energized. Consequently, contact 106 is open and no voltage is applied to the primary of power transformer 108 and no power is supplied to the plate of the electronic tube.

Upon the receipt of a "0" from the output of gate 68 (i.e. after filament control switch 16 is closed and filament voltage is applied) transistor 92 is reverse biased, transistor 96 is forward biased, and relay coil 98 is energized, closing contact 100. The closing of contact 100 applies a trigger voltage to triac 102, and relay coil 104 is energized, closing contact 106. The closing of contact 106 energizes transformer 108 and power is supplied to the plate of the electronic tube. As above described, as soon as the filament control switch 16 is open, the output of gate 68 becomes a "1" and the plate power supply circuitry 12 is immediately deactuated.

Thus, in this illustrative embodiment, the closing of the first switch means or filament control switch 16, causes the subsequent closing of the second switch means or plate supply circuitry 12 following a predetermined period of time. Thereafter, should the first switch means 16 again be deactuated, the second switch means 12 is immediately deactuated.

While the invention has been described with reference to a specific embodiment, the description is illustrative and is not to be construed as limiting the scope of the invention. Various modifications and changes may occur to those skilled in the art without departing from the spirit and scope of the invention.

What is claimed is:

1. A timer circuit comprising a first switch means, a second switch means, first gate means actuated by the closing of said first switch means, capacitive voltage charging means, first circuit means for charging said capacitive voltage charging means in response to actuation of said first gate means, second circuit means for discharging said capacitive voltage charging means in response to the deactuation of said first gate means, second gate means actuated by the accumulation of a predetermined charge on said capacitive voltage charging means, a second switch means, said second switch means being operatively connected to said second gate means and actuated in response to the actuation of said second gate means, said second gate means being operatively connected to said first gate means whereby said second gate means is deactuated in response to the deactuation of said first gate means, and said second switch means

being deactuated in response to the deactuation of said second gate means.

2. A timer circuit as defined by claim 1 wherein said first circuit means has a longer time constant than said second circuit means.

3. A timer circuit as defined by claim 1 wherein said first gate means is an inverter and said second gate means comprises first and second NAND gates interconnected as a direct coupled fiip-fiop.

4. A timer circuit as defined by claim 1 wherein said timer circuit is operatively connected in the power control for an electronic tube and said first switch means controls the filament voltage for said electronic tube and said second switch means controls the plate voltage for said electronic tube.

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