A ceramic package and a method of manufacturing the same are provided. By using a conductive ceramic substrate as a substrate on which a light emitting diode chip or a semiconductor chip is mounted, a heat-radiating area is increased and heat generated from the light emitting diode chip or the semiconductor chip can be easily radiated. Further, an insulating layer is formed between the conductive ceramic substrate and a surface-mounting external electrode, and thereby a short circuit between the conductive ceramic substrate and the semiconductor chip can be prevented.
Description

CERAMIC PACKAGE AND METHOD OF MANUFACTURING
THE SAME

Technical Field

[1] The present invention relates to a ceramic package and a method of manufacturing the same, and more particularly, to a ceramic package of which heat-radiation characteristic is improved using a conductive ceramic substrate, and a method of manufacturing the same.

Background Art

[2] In general, packages include signal output terminals that are formed of lead frames and connected to a main board, and are molded using a molding material etc. to protect a semiconductor chip or a light emitting chip from environmental factors, such as dust, moisture, and electrical or mechanical load, and to optimize and maximize performance of the semiconductor chip or light emitting chip. The semiconductor includes a single element and integrated circuit and so forth in which various electronic circuits and lines are formed.

[3] A plastic is used for a body in a package in the related art, and the package using the plastic body may be deformed due to heat radiated from a semiconductor chip, for example, a light emitting chip. Therefore, a method to reduce heat stress is required. A method of improving heat-radiation characteristics using a heat sink has been studied to reduce the heat stress. In a package using the heat sink, the plastic body is electrically and thermally isolated from the heat sink. Accordingly, the deformation of the plastic body due to the heat radiated from the semiconductor chip can be prevented. However, when the plastic body is used in the package, it is difficult to manufacture a compact package and a process for manufacturing the package is complicated.

[4] Alternately, a semiconductor chip may be packaged using a ceramic. In this case, an insulating ceramic substrate is used, a predetermined hole is formed in a mounting region for the semiconductor chip on the ceramic substrate, and the semiconductor chip is mounted on the upper surface of the ceramic substrate including the hole. As such, the hole formed in the ceramic substrate enables heat radiation. Further, another insulating ceramic substrate may be formed over the hole, and a semiconductor chip may be mounted on the insulating ceramic substrate.

[5] However, in the package using a ceramic substrate, heat is radiated only through the hole formed in the insulating ceramic substrate, so that heat-radiating area is small and thus the amount of radiated heat is limited. Therefore, there is a demand for a package capable of radiating all of the heat generated from a semiconductor chip by increasing...
the heat-radiating area. The package having the heat-radiating structure is more seriously required for a semiconductor chip such as a semiconductor light emitting chip generating large amount of heat.

Disclosure of Invention

Technical Problem

[6] The present invention provides a ceramic package and a method of manufacturing the same capable of improving heat-radiation ability by using a conductive ceramic substrate to mount a light emitting chip or a semiconductor chip onto without forming a heat sink or a hole.

[7] Further, the present invention provides a ceramic package and a method of manufacturing the same which use a conductive ceramic substrate and are capable of preventing a short circuit between an electrode terminal of a light emitting chip or a semiconductor chip and a conductive ceramic substrate.

Technical Solution

[8] According to an aspect of the invention, a ceramic package includes a conductive ceramic substrate; a semiconductor chip mounted on one surface of the conductive ceramic substrate; and a surface-mounting external electrode formed on the conductive ceramic substrate and connected to the semiconductor chip.

[9] The ceramic package may further include an insulating layer formed between the conductive ceramic substrate and the surface-mounting external electrode.

[10] According to another aspect of the invention, a ceramic package includes a conductive ceramic substrate; a first surface-mounting external electrode formed by laminating an insulating layer and a first metal layer at predetermined regions of an upper surface, a lower surface and one side surface of the conductive ceramic substrate; a second surface-mounting external electrode that is formed of a second metal layer at predetermined regions of an upper surface, a lower surface and another side surface of the conductive ceramic substrate; and a semiconductor chip mounted at a predetermined region on the upper surface of the conductive ceramic substrate.

[11] The one side surface and the another side surface of the conductive ceramic substrate may include an edge connecting both side surfaces of the conductive ceramic substrate.

[12] The one side surface and the another side surface of the ceramic package may face each other.

[13] The semiconductor chip may include a light emitting diode chip.

[14] The ceramic package may further include an insulating ceramic substrate including a predetermined opening through which the light emitting diode chip is exposed to the outside. The insulating ceramic substrate may be formed on the upper surface of the
conductive ceramic substrate on which the light emitting diode chip is mounted.

[15] The ceramic package may further include a conductive ceramic substrate including a predetermined opening through which the light emitting diode chip is exposed to the outside. The conductive ceramic substrate may include an insulating layer formed on the lower surface thereof and may be formed on the upper surface of the conductive ceramic substrate on which the light emitting diode chip is mounted.

[16] According to another aspect of the invention, a method of manufacturing a ceramic package includes forming a plurality of first holes at predetermined regions in a conductive ceramic sheet and forming a first insulating layer at predetermined regions on an upper surface of the conductive ceramic sheet so that the first holes are filled with the first insulating layer, forming a second insulating layer at predetermined regions on a lower surface of the conductive ceramic sheet, removing portions of the first insulating layer filled in the first holes to form second holes and then forming a first metal layer at predetermined regions on the upper surface of the conductive ceramic sheet so that the second holes are filled with the first metal layer, forming a second metal layer at predetermined regions on the lower surface of the conductive ceramic sheet, mounting semiconductor chips at predetermined regions on the upper surface of the conductive ceramic sheet, and cutting the conductive ceramic sheet so that the centers of the second holes are cut.

[17] The conductive ceramic sheet may be formed by laminating a plurality of conductive ceramic sheets.

[18] The first metal layer may be formed on the first insulating layer and on regions except for the regions where the semiconductor chips are mounted.

[19] The second metal layer may be formed on the second insulating layer and regions that are spaced by a predetermined distance from the second insulating layer.

[20] The semiconductor chip may include a light emitting diode chip.

[21] The method may further include forming an insulating ceramic substrate that includes predetermined openings through which the light emitting diode chips are exposed to the outside. The insulating ceramic substrate may be formed on the upper surface of the conductive ceramic substrate on which the light emitting diode chips are mounted.

[22] The method may further include sintering the conductive ceramic substrate and the insulating ceramic substrate after forming the insulating ceramic substrate.

[23] The method may further include forming a conductive ceramic substrate including predetermined openings through which the light emitting diode chips are exposed to the outside. The conductive ceramic substrate may include an insulating layer formed on the lower surface thereof and may be formed on the upper surface of the conductive ceramic substrate on which the light emitting diode chips are mounted.
Advantageous Effects

As described above, according to an aspect of the invention, a conductive ceramic substrate is used as a substrate on which a light emitting diode chip or semiconductor chip is mounted, so that the heat-radiating area is increased as compared to a conventional configuration in which heat is radiated through a hole formed in an insulating ceramic substrate. Therefore, heat generated from the light emitting diode chip or semiconductor chip can be easily radiated.

Further, a short circuit between the conductive ceramic substrate and the semiconductor chip can be prevented by forming an insulating layer between the conductive ceramic substrate and the surface-mounting external electrode.

Brief Description of the Drawings

The above and other features and advantages of the present invention will become more apparent by describing in detail preferred embodiments thereof with reference to the attached drawings in which:

FIG. 1 is a perspective view of a ceramic package on which a light emitting chip is mounted according to an exemplary embodiment of the present invention;

FIG. 2 is a cross-sectional view of the ceramic package on which the light emitting chip is mounted according to the exemplary embodiment of the present invention;

FIGS. 3 to 8 are perspective views sequentially illustrating process of a method of manufacturing the ceramic package on which a light emitting chip is mounted according to the exemplary embodiment of the present invention;

FIG. 9 is a cross-sectional view of a ceramic package on which a light emitting chip is mounted according to another exemplary embodiment of the present invention; and

FIG. 10 is a cross-sectional view of a ceramic package on which a semiconductor chip is mounted according to still another exemplary embodiment of the present invention.

Best Mode for Carrying Out the Invention

Preferred embodiments of the invention will be described in detail hereinafter with reference to accompanying drawings.

FIG. 1 is a perspective view of a ceramic package on which a semiconductor chip is mounted according to an exemplary embodiment of the present invention. FIG. 2 is a cross-sectional view of the ceramic package shown in FIG. 1, taken along a diagonal line.

Referring to FIGS. 1 and 2, an insulating layer 13a and a metal layer 14a are laminated at predetermined regions on side surfaces of a conductive ceramic substrate 11, for example, at four edge surfaces (regions 12) of the hexahedral conductive ceramic substrate 11, the conductive ceramic substrate having excellent thermal con-
ductivity as well as electrical conductivity. The regions of the conductive ceramic substrate 11 on which the insulating layer 13a and metal layer 14a are laminated are not limited to the four edge surfaces. That is, the insulating layer and metal layer may be formed on two side surfaces facing each other, and one or more layers may be formed on each side surface. Further, an insulating layer 13b and a metal layer 14b are formed to have a predetermined thickness at one side with respect to a predetermined region of the central portion on an upper surface of the conductive ceramic substrate 11, that is, a region on which a semiconductor chip 15 is to be mounted later. A metal layer 14c having a predetermined thickness is formed on the other side with respect to the region on which the semiconductor chip 15 is mounted on the upper surface of the conductive ceramic substrate 11. The insulating layers 13a and 13b may be simultaneously formed, and the metal layers 14a, 14b, and 14c may also be formed at the same time. An insulating layer 13c and a metal layer 14d are laminated in regions of a lower surface of the conductive ceramic substrate 11 that is opposite to the regions of the upper surface where the insulating layer 13b and the metal layer 14b are laminated. Further, a metal layer 14e is formed in a region of the lower surface of the conductive ceramic substrate 11 that is opposite to the region on the upper surface where the metal layer 14c is formed. The metal layer 14b formed on the insulating layer 13b which is formed on the upper surface of the conductive ceramic substrate 11, and the metal layer 14d formed on the insulating layer 13c which is formed on the lower surface of the conductive ceramic substrate are connected to each other through the metal layer 14a formed on the side surface of the conductive ceramic substrate, and operate as a first surface-mounting external electrode. Further, the metal layer 14c formed on the upper surface of the conductive ceramic substrate 11 and the metal layer 14e formed on the lower surface thereof are connected to each other through the metal layer 14a formed on the side surface of the conductive ceramic substrate 11, and operate as a second surface-mounting external electrode. An insulating ceramic substrate 16 including an opening formed at a predetermined region thereof is formed on the conductive ceramic substrate 11 on which the first and second surface-mounting external electrodes are formed. The opening of the insulating ceramic substrate 16 is formed so that the region on which the semiconductor chip 15 is mounted is exposed. The semiconductor chip 15 is mounted on the region of the upper surface of the conductive ceramic substrate 11 which is not occupied by the metal layers 14b and 14c and is exposed to the outside through the opening of the insulating ceramic substrate 16, i.e., on the central portion of the conductive ceramic substrate by an adhesive. The semiconductor chip 15 is connected to the first and second surface-mounting external electrodes by wires 17. A molding (not shown) may be provided to protect the semiconductor chip 15 and the surface-mounting external electrodes. The semiconductor
chip 15 may be various elements, such as a semiconductor memory element and a semiconductor light emitting element including a light emitting diode. In a case where the semiconductor chip 15 is a semiconductor light emitting element, a reflective film or a reflective plate may be formed over the opening of the insulating ceramic substrate 16 to improve light emitting efficiency of the semiconductor light emitting element.

Since the conductive ceramic substrate 11 is used in this embodiment of the invention, the insulating layers 13a and 13b should be formed under the first surface-mounting external electrode as described above in order to prevent a short circuit between the conductive ceramic substrate 11 and the first surface-mounting external electrode. That is, when all of the conductive ceramic substrate 11, the first and second surface-mounting external electrodes short-circuited, the semiconductor chip 15 connected to the electrodes by the wires 17 is also short-circuited, so that the semiconductor chip 15 does not operate normally. For this reason, at least one of the first and second surface-mounting external electrodes should be insulated from the conductive ceramic substrate 11. It may be effective that both of the first and second surface-mounting external electrodes are insulated from the conductive ceramic substrate. In such a case, however, an insulating layer deposition process and a patterning process are additionally required, and the number of processes increases.

FIGS. 3 to 8 are views sequentially illustrating process of a method of manufacturing a ceramic package on which a light emitting diode chip is mounted according to the exemplary embodiment of the present invention.

Referring to FIG. 3, a conductive ceramic sheet 110 is provided, and a plurality of first holes 120 is formed at predetermined regions of the conductive ceramic sheet 110 by a first punching process. The conductive ceramic sheet 110 is manufactured by mixing ceramic power with conductive material powder, for example, metal powder. The conductive ceramic sheet obtains conductive property by adjusting the content of the conductive material. Therefore, the conductive ceramic sheet 110 has excellent thermal conductivity in addition to electrical conductivity. Further, the first holes 120 are repeatedly formed at predetermined intervals. For example, the first holes 120 may be formed to have identical intervals in upward, downward, left, and right directions. The first holes 120 may be formed, for example, at regions corresponding to four corners of the rectangular ceramic substrate 111 on which one light emitting diode is mounted. Alternatively, one or two first holes may be formed on one side of the rectangular ceramic substrate 111, and another one or two holes may be formed on the other side thereof facing the one side. In this exemplary embodiment, four first holes 120 formed at four corners of the rectangular ceramic substrate 111 on which one light emitting diode is mounted will be described. The light emitting diode chip is mounted at a central portion of a rectangular region which is surrounded by four adjacent first
holes 120.

Referring to FIG. 4, a first insulating layer 130 is formed in predetermined regions on the conductive ceramic sheet 110. The first insulating layer 130 is formed only one side of each region of the conductive ceramic sheet 110, which is formed between the first holes 120 arranged in one direction of the conductive ceramic sheet 110. In other words, the first insulating layer 130 is formed on the left side of each region, which is formed between the first holes arranged in one direction, of the conductive ceramic sheet 110 so as to be bordered by the first holes 120. As a result, all of the first holes 120 are filled with the first insulating layer 130. Then, a second insulating layer 140 is formed in portions of regions on the lower surface of the conductive ceramic sheet 110 which is opposite to the regions where the first insulating layers 130 are formed on the upper surface. Accordingly, the first and second insulating layers 130 and 140 are formed in predetermined regions of the upper and lower surfaces of the conductive ceramic sheet 110, and the plurality of holes 120 are filled with the first insulating layer 130.

Referring to FIG. 5, a second hole 150 which is smaller than the first hole 120 is formed in each of the plurality of the first holes 120 filled with the first insulating layer by a second punching process. In detail, the second hole 150 is formed by removing a portion of the first insulating layer 130 filled in each of the first holes 120 using the punching process. Therefore, as the second hole 150 is formed, the first insulating layer 130 filled inside the first hole 120 is exposed to the outside.

Referring to FIG. 6, a first metal layer 160 is formed in predetermined regions on the upper surface of the conductive ceramic sheet 110. In detail, the first metal layer 160 is formed at both sides of each region on which light emitting diode is mounted on the conductive ceramic sheet 110. That is, the first metal layer 160 is formed on the first insulating layer 130 and in regions where the first insulating layer 130 is not formed on the upper surface of the conductive ceramic sheet 110. The first metal layer 160 is not formed in the region on which the light emitting diode chips is mounted. Therefore, the plurality of second holes 150 are filled with the first metal layer 160. Further, a second metal layer 170 is formed on the lower surface of the conductive ceramic sheet 110, except for predetermined regions at the central portion. In particular, the second metal layer 170 on the second insulating layer 140 is formed to expose the second insulating layer or to have the same pattern as the second insulating layer 140 to prevent short-circuiting between the second metal layer 170 and the conductive ceramic sheet 110. The first and second metal layers 160 and 170 are formed by a screen printing method or a sputtering method using, for example, Ag, Pd, Pt, or the like. Further, the first and second metal layers 160 and 170 may be formed on the upper and lower surfaces of the conductive ceramic sheet 110 after the second
holes 150 are formed with a metal layer. Therefore, the first and second metal layers 160 and 170 are connected to each other through the second holes 150, and operate as the first and second surface-mounting external electrodes, respectively.

Referring to FIG. 7, an insulating ceramic sheet 180 is provided and then a plurality of openings are formed in the insulating ceramic sheet 180 by a third punching process to expose at least the regions on which semiconductor chips are mounted on the conductive ceramic sheet 110. And the insulating ceramic sheet 180 having the plurality of openings is laminated on the conductive ceramic sheet 110. Then, the ceramic sheets 110 and 180 are simultaneously sintered. The sintering temperature may be in a range of about 700 to 1050°C.

Referring to FIG. 8, a semiconductor chip 190 is mounted on the conductive ceramic sheet 110 which is exposed by the opening 185 of the insulating ceramic sheet 180, and then, the semiconductor chip is connected to the first and second surface-mounting external electrodes using wires 200. Molding (not shown) may be formed to protect the semiconductor chip 190 and the wire. The molding can work as protectors for protecting the semiconductor chip 190. In addition, the molding (not shown) may be formed in a lens shape and control a path of light emitted from the light emitting chip when the semiconductor chip is a light emitting element. The molding (not shown) may be formed of a transparent silicon resin or an epoxy resin. Alternatively, the molding may be formed of an opaque resin through which light can transmit according to a requirement of the light emitting diode. Further, the molding (not shown) may be formed to have a dome shape or a shape with a flat top using a transparent silicon resin, and a predetermined amount of diffusing agent may be added to the silicon resin.

Subsequently, cutting is performed along a line connecting the centers of the second holes 150 formed in the first holes 120. As a result, a separate ceramic package shown in FIG. 1 is completed.

Although the conductive ceramic sheet 110 is a single sheet in the above, but may have a multilayer structure where a plurality of ceramic sheets is laminated. Further, the first holes 120 and the second holes 150 formed in the first holes 120 are formed at four corners of the hexahedral unit chip package. But the present invention is not limited thereto. That is, the first and second holes may be formed on two side surfaces of the hexahedral unit chip package facing each other. Further, one or more holes may be formed on each side surface.

Further, in the above exemplary embodiment, the light emitting diode chip 15 mounted on the upper surface of the conductive ceramic substrate 11 is connected to the first and second surface-mounting external electrodes by the two wires 17, and the insulating ceramic substrate 16 having a vertical opening is provided. However, the
present invention is not limited thereto. That is, as shown in FIG. 9, the light emitting diode chip 15 may be mounted on the second surface-mounting external electrode, and may be connected to the first surface-mounting external electrode using one wire 17. Then, a conductive ceramic substrate 19 insulated by an insulating ceramic sheet 18 may be provided. Further, the diameter of the opening of the conductive ceramic substrate 19 may increase upward. This is achieved by forming the conductive ceramic sheet 19 by laminating a plurality of conductive ceramic sheets. That is, the upper conductive ceramic sheets are formed to have larger openings than the lower conductive ceramic sheets, and the upper and lower conductive ceramic sheets are pressed. According to the configuration, heat is also radiated through the upper conductive ceramic sheet 19 and therefore thermal conductivity can be further improved.

Further, the insulating ceramic sheets and the conductive ceramic sheets may be alternately laminated, in which the upper conductive ceramic sheets are still formed to have larger openings than the lower conductive ceramic sheets, and then the upper and lower conductive ceramic sheets are pressed. An insulating ceramic sheet may be formed at the lowest layer which is in contact with the first and second surface-mounting external electrodes.

FIG. 10 is a cross-sectional view of a ceramic package according to another exemplary embodiment of the present invention.

Referring to FIG. 10, a plurality of holes (not shown) is formed to have a predetermined size at predetermined region of a conductive ceramic substrate 210, and the holes (not shown) are filled with an insulating layer and a metal layer. The insulating layer and the metal layer are formed at predetermined regions on the upper surface of the conductive ceramic substrate 210, i.e., at regions other than a region on which a semiconductor chip is mounted. Another insulating layer and metal layer are formed at regions on the lower surface of the conductive ceramic substrate 210 that are opposite to the regions of the upper surface having the insulating layer and the metal layer formed thereon. Accordingly, the insulating layers and the metal layers formed on the upper and lower surfaces of the conductive ceramic substrate 210 are connected to each other by the insulating layer and metal layer filled in the holes. Subsequently, a plurality of lead frames 230 is formed on the insulating layer 220. A semiconductor chip 240, where desired circuit elements are formed by a processor, is bonded to a region where the lead frames 230 are not formed on the upper surface of the conductive ceramic substrate 210 by an adhesive (not shown). The adhesive (not shown) may be a paste. Further, the semiconductor chip 240 includes an ASIC product or a microprocessor having high frequency characteristics, a chip provided with a high-speed memory, such as DRAM, SRAM, a non-volatile memory element, a sensor
device, or a light emitting device. A plurality of bump electrodes 250 is formed at predetermined regions on the upper surface of the semiconductor chip 240 to be spaced apart by a predetermined distance. The pluralities of metal patterns 230 and the bump electrodes 250 are connected to each other by bonding wires 260. An encapsulation resin 270, such as epoxy molding compound (EMC), is coated to protect the semiconductor chip 240 and the bonding wires 260 from the external environment. Further, a plurality of solder balls 280 may be provided on the lower surface of the conductive ceramic substrate 210.

[49] Since the conductive ceramic substrate is used in the above exemplary embodiment of the present invention as described above, the insulating layers 220 need to be formed under the first and second lead frames to prevent a short circuit between the first and second metal patterns, and the conductive ceramic substrate 210. That is, when the first and second frames are all short-circuited with the conductive ceramic substrate 210, the semiconductor chip 240 connected by the wires is also short-circuited. For this reason, the first and second lead frames should be insulated from the conductive ceramic substrate 210.
Claims

[1] A ceramic package comprising:
   a conductive ceramic substrate;
   a semiconductor chip mounted on one surface of the conductive ceramic substrate; and
   a surface-mounting external electrode formed on the conductive ceramic substrate and connected to the semiconductor chip.

[2] The ceramic package of claim 1, further comprising:
   an insulating layer formed between the conductive ceramic substrate and the surface-mounting external electrode.

[3] A ceramic package comprising:
   a conductive ceramic substrate;
   a first surface-mounting external electrode formed by laminating an insulating layer and a first metal layer at predetermined regions of an upper surface, a lower surface and one side surface of the conductive ceramic substrate;
   a second surface-mounting external electrode that is formed of a second metal layer at predetermined regions of an upper surface, a lower surface and another side surface of the conductive ceramic substrate; and
   a semiconductor chip mounted at a predetermined region on the upper surface of the conductive ceramic substrate.

[4] The ceramic package of claim 3, wherein the one side surface and the another side surface of the conductive ceramic substrate include an edge connecting both side surfaces of the conductive ceramic substrate.

[5] The ceramic package of claim 3, wherein the one side surface and the another side surface of the ceramic package face each other.

[6] The ceramic package of claim 1 or 3, wherein the semiconductor chip includes a light emitting diode chip.

[7] The ceramic package of claim 6, further comprising:
   an insulating ceramic substrate including a predetermined opening through which the light emitting diode chip is exposed to the outside, the insulating ceramic substrate being formed on the upper surface of the conductive ceramic substrate on which the light emitting diode chip is mounted.

[8] The ceramic package of claim 6, further comprising:
   a conductive ceramic substrate including a predetermined opening through which the light emitting diode chip is exposed to the outside and an insulating layer formed on the lower surface thereof, the conductive ceramic substrate being formed on the upper surface of the conductive ceramic substrate on which the
light emitting diode chip is mounted.

[9] A method of manufacturing a ceramic package, the method comprising:
forming a plurality of first holes at predetermined regions in a conductive ceramic sheet, and forming a first insulating layer at predetermined regions on an upper surface of the conductive ceramic sheet so that the first holes are filled with the first insulating layer;
forming a second insulating layer at predetermined regions on a lower surface of the conductive ceramic sheet;
removing portions of the first insulating layer filled in the first holes to form second holes, and then forming a first metal layer at predetermined regions on the upper surface of the conductive ceramic sheet so that the second holes are filled with the first metal layer;
forming a second metal layer at predetermined regions on the lower surface of the conductive ceramic sheet;
mounting semiconductor chips at predetermined regions on the upper surface of the conductive ceramic sheet; and
cutting the conductive ceramic sheet so that the centers of the second holes are cut.

[10] The method of claim 9, wherein the conductive ceramic sheet is formed by laminating a plurality of conductive ceramic sheets.

[11] The method of claim 9, wherein the first metal layer is formed on the first insulating layer and regions except for the regions where the semiconductor chips are mounted.

[12] The method of claim 9, wherein the second metal layer is formed on the second insulating layer and regions that are spaced by a predetermined distance from the second insulating layer.

[13] The method of claim 9, wherein the semiconductor chip includes a light emitting diode chip.

[14] The method of claim 9 or 13, further comprising:
forming an insulating ceramic substrate including predetermined openings through which the light emitting diode chips are exposed to the outside, the insulating ceramic substrate being formed on the upper surface of the conductive ceramic substrate on which the light emitting diode chips are mounted.

[15] The method of claim 14, further comprising:
sintering the conductive ceramic substrate and the insulating ceramic substrate after forming the insulating ceramic substrate.

[16] The method of claim 9 or 13, further comprising:
forming a conductive ceramic substrate including predetermined openings
through which the light emitting diode chips are exposed to the outside and an insulating layer formed on the lower surface thereof, the conductive ceramic substrate being formed on the upper surface of the conductive ceramic substrate on which the light emitting diode chips are mounted.
A. CLASSIFICATION OF SUBJECT MATTER

HOIL 23/15(2006.01)1

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 8 HOIL 23/15

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utility models and applications for Utility models since 1975

Japanese Utility models and applications for Utility models since 1975

Electronic database consulted during the international search (name of database and, where practicable, search terms used)

e-KIPASS (KIPO internal), package, ceramic, substrate, LED

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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<td>KR 10-0592508 B1 (Korea Photonics Tech Ins.) 26 Jun 2006</td>
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Further documents are listed in the continuation of Box C

See patent family annex

Date of the actual completion of the international search

15 JANUARY 2008 (15 01 2008)

Date of mailing of the international search report

15 JANUARY 2008 (15.01.2008)

Name and mailing address of the ISA/KR

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Fax number 82-42-472-7140

Authorized officer

BAK, Jun yung

Telephone No 82-42-481-5729
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Form PCT/ISA/210 (patent family annex) (April 2007)