



(51) International Patent Classification:
H01L 31/115 (2006.01) *H01L 31/117* (2006.01)

(21) International Application Number:
PCT/US2010/021142

(22) International Filing Date:
15 January 2010 (15.01.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/364,042 2 February 2009 (02.02.2009) US

(71) Applicant (for all designated States except US):
REDLEN TECHNOLOGIES INC. [CA/CA]; 1763
Sean Heights, #123, Saanichton, British Columbia V8M
0A5 (CA).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **CHEN, Henry** [US/
CA]; C/o Redlen Technologies, 9865 West Saanich Road,
Suite #107, Sidney, BC V8L 5Y8 (CA). **AWADALLA,
Salah** [US/CA]; C/o Redlen Technologies, 9865 West
Saanich Road, Suite #107, Sidney, BC V8L 5Y8 (CA).
LU, Pinghe [CA/CA]; C/o Redlen Technologies, 9865
West Saanich Road, Suite #107, Sidney, BC V8L 5Y8
(CA). **MARTHANDAM, Pramodha** [IN/CA]; C/o
Redlen Technologies, 9865 West Saanich Road, Suite
#107, Sidney, BC V8LV5Y8 (CA).

(74) Agents: **RADOMSKY, Leon** et al.; The Marbury Law
Group, PLLC, 11800 Sunrise Valley Drive, Suite 1000,
Reston, VA 20191 (US).

(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO,
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP,
KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD,
ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI,
NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD,
SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR,
TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM,
ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ,
TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE,
ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,
MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
ML, MR, NE, SN, TD, TG).

Published:

— without international search report and to be republished
upon receipt of that report (Rule 48.2(g))

(54) Title: SOLID-STATE RADIATION DETECTOR WITH IMPROVED SENSITIVITY

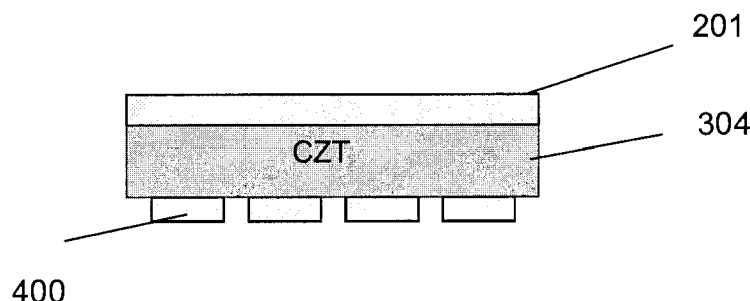


Fig. 2A

(57) Abstract: A radiation detector includes a semiconductor substrate having opposing front and rear surfaces, a cathode electrode located on the front surface of the semiconductor substrate configured so as to receive radiation, and a plurality of anode electrodes formed on the rear surface of said semiconductor substrate. A work function of the cathode electrode material contacting the front surface of the semiconductor substrate is lower than a work function of the anode electrode material contacting the rear surface of the semiconductor substrate.



SOLID-STATE RADIATION DETECTOR WITH IMPROVED SENSITIVITY

CROSS REFERENCE TO RELATED PATENT APPLICATIONS

[0001] The present application claims benefit of United States patent application 12/364,042, filed February 2, 2009, which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

[0002] The present invention generally relates to detectors for gamma-ray and X-ray detection devices.

SUMMARY OF THE INVENTION

[0003] One embodiment of the invention relates to a radiation detector comprising a semiconductor substrate having opposing front and rear surfaces, a cathode electrode located on the front surface of said semiconductor substrate configured so as to receive radiation, and a plurality of anode electrodes formed on the rear surface of said semiconductor substrate. The work function of the cathode electrode material contacting the front surface of the semiconductor substrate is lower than the work function of the anode electrode material contacting the rear surface of the semiconductor substrate.

[0004] Another embodiment of the present invention is a radiation detector system comprising a semiconductor substrate having opposing front and rear surfaces, a cathode electrode located on the front surface of said semiconductor substrate configured so as to receive radiation, a plurality of anode electrodes formed on the rear surface of said semiconductor substrate, and a means for applying a forward bias to the detector during operation such that the anode electrodes is maintained at a higher potential than the cathode electrode and such that the signal is collected from the anode electrodes. The work function of the cathode electrode material contacting the front surface of the semiconductor substrate is lower than the work function of the anode electrode material contacting the rear surface of the semiconductor substrate.

[0005] Finally, another embodiment relates to a method of operating a radiation detector comprising the steps of: a) providing a radiation detector comprising a semiconductor substrate having opposing front and rear surfaces, a cathode electrode located on the front

surface of said semiconductor substrate configured so as to receive radiation, and a plurality of anode electrodes formed on the rear surface of said semiconductor substrate; b) receiving radiation at the cathode electrode; c) applying a forward bias to detector to maintain the anode electrodes at a higher potential than the cathode electrode; and, d) collecting a signal from the anode electrodes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Fig. 1 is a perspective view of a CZT substrate with anode electrode pixels.

[0007] Figs. 2A-D are schematic cross-sectional views of a method of making a detector with a housing.

[0008] Figs. 3A-I are schematic cross-sectional views of a method of making a detector at various stages in the formation of contacts thereon.

[0009] Fig. 4 is a graph showing I-V characteristics of a comparative device having a cathode comprising gold, and not exposed to radiation.

[0010] Fig. 5 is a graph showing I-V characteristics of a comparative device having a cathode comprising gold, and exposed to radiation.

[0011] Fig. 6 is a graph showing I-V characteristics of an embodiment of the present invention having a cathode comprising indium, and not exposed to radiation.

[0012] Fig. 7 is a is a graph showing I-V characteristics of an embodiment of the present invention having a cathode comprising indium, and exposed to radiation

[0013] Fig. 8 is a graph showing the interpixel resistance of edge pixels at of an example embodiment of the present invention having differing interpixel gap widths.

[0014] Fig. 9 is a graph showing the interpixel resistance of center pixels at of an example embodiment of the present invention having differing interpixel gap widths.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0015] The following definitions are used herein:

[0016] Cathode electrode: the electrode on one major surface of the detector substrate where incident gamma rays or x-rays enter the detector, i.e. positioned towards the radiation source.

[0017] Anode electrodes: segmented electrode contacts located on the rear surface of the substrate, i.e. positioned away from the radiation source.

[0018] Forward-bias: The application of an electric potential between the anode and cathode electrical contacts with the anode exposed to a higher potential and cathode experiencing a lower potential. A forward-bias, as used herein, means that the anode is the electrode from which electric signals, such as voltage or current generated by incident gamma rays or x-rays entering the detector, are collected.

[0019] Interpixel or inter pixel: the region or gap separating pixel electrodes. For electrode configurations with non-pixelated discrete contact segments the term is equivalently applied to the gap between contact segments.

[0020] Solder mask: a coating on the semiconductor detector or on the printed circuit board ("PCB"), which is designed to insulate and protect either the segmented anode (pixels) on the semiconductor detector or the mating metal pads on the PCB, keeping them from shorting during PCB-attachment process. The solder mask may have any suitable color, such as a dark green/blue color and occasionally a yellowish color.

[0021] Embodiments of the present invention describe radiation detectors, such as metal-semiconductor-metal (MSM) or heterojunction metal/semiconductor type detector with improved sensitivity. In other words, the detector preferably does not contain a p-i-n or p-n diode (i.e., no semiconductor p-n junction) formed in a semiconductor substrate or tile. In fact, radiation detectors of the embodiments of the present invention provide the additional benefit of room temperature operation without the need of cooling as usually required for p-i-n heterojunction devices. The embodiments of the invention provide the benefit of increased detector sensitivity while also maintaining other beneficial properties such as lower leakage current and high detector energy resolution. Additionally, the embodiments of the invention may offer the further benefit of being reliable and suitable for mass production. In one embodiment, a radiation detector comprises a semiconductor substrate having opposing front and rear surfaces, a cathode electrode located on the front surface of said semiconductor substrate configured so as to receive radiation, and a plurality of anode electrodes formed on

the rear surface of said semiconductor substrate. Preferably, the work function of the cathode electrode material contacting the front surface of the semiconductor substrate is lower than the work function of the anode electrode material contacting the rear surface of the semiconductor substrate. It is important to note herein that prior-art radiation detector devices, such as that disclosed in for example T. Takahashi et al., "High-resolution Schottky CdTe diode for hard X-ray and gamma-ray astronomy", Nuclear Instruments & Methods in Physics Research A 436 (1999) 111-119, have instead utilized indium as the anode electrode material rather than as the cathode electrode material, and apply forward and reverse bias so that the induced signal is collected from the anode and cathode, respectively. For example, a positive bias is placed on the In anode in the device disclosed in the work of T. Takahashi et al. However, signal collection at the anode with indium as the anode electrode material does not present the increased photo-peak count sensitivity benefits of the configuration of the embodiments of the present invention.

[0022] Radiation detectors can be configured in a variety of ways. A common configuration comprises a cathode electrode and a plurality of anode electrodes located on opposite sides of a semiconductor plate or substrate. Typically these radiation detectors have pixilated anode electrode arrays fabricated by various deposition and lithography processes resulting in a gap between pixels, termed the interpixel gap or interpixel region. In an exemplary embodiment of the present invention, the interpixel gap has a width of between 100 and 500 μm . More preferably, the interpixel gap width is between 200 and 400 μm .

[0023] In the preferred embodiments, the radiation detectors comprise a semiconductor material, such as a semiconductor material preferably comprising CdZnTe (CZT) or CdTe, having opposing front and rear surfaces and lacking a p-n or p-i-n junction. Although other types of semiconductor materials exemplified by lead iodide, thallium bromide, gallium arsenide or silicon may be used.

[0024] More preferred is $\text{Cd}_{(1-x)}\text{Zn}_x\text{Te}$ (where x is less than or equal to 0.5), a wide band gap ternary II-VI compound semiconductor with unique electronic properties. This type of semiconductor is useful in gamma-ray and X-ray detectors which are used as spectrometers that operate at room temperature for nuclear radiation detection, spectroscopy and medical imaging applications.

[0025] Additionally, in the preferred embodiments, the radiation detectors comprise a cathode electrode located on the front surface of said semiconductor substrate configured so as to receive radiation, and a plurality of anode electrodes formed on the rear surface of said semiconductor substrate. The work function of the cathode electrode material is preferably less than about 4.5 eV while the work function of the anode electrode material is preferably more than or equal to about 4.8 eV. A cathode electrode material having a work function of less than about 4.5 eV may, for example, be selected from the group comprising one of In, Al, and Ti and alloys thereof. An anode electrode material having a work function of more than or equal to about 4.8 eV may, for example, be selected from the group comprising one of Au, Pt and other noble metals and their alloys. In the embodiments of the present invention, by utilizing a cathode electrode material with a low work-function, such as a work function less than about 4.5 eV, for example, a cathode electrode material comprising indium, a higher density of charge injection, namely electron injection, occurs at the metal/semiconductor interface from the cathode.

[0026] In operation, the anode and cathode of the preferred embodiments is electrically connected to a voltage source. The anode is exposed to a higher potential than the cathode, for example, by applying a positive voltage to the anode while the cathode is grounded or by applying a negative voltage to the cathode and virtually grounding the anode.

[0027] Illustrated in Fig. 1, is an example of pixellated anode electrodes 302 formed on a semiconductor substrate 304, such as a CZT substrate (also referred to as a “tile”). The cathode electrode is formed on the bottom side of the substrate 304.

[0028] Fig. 2A shows the radiation detector device of an embodiment of the present invention containing anode electrode pixels 400 on a rear side of a CZT substrate 304, and containing cathode electrode 201 on a front side of the CZT substrate. Optionally, a protective coating 420 is applied to polished side edges of the CZT tile as shown in Fig. 2B. For example, the CZT tile may be dipped in a protective coating (such as solder mask) to cover the exposed sides and dried for at least 5 hours.

[0029] An optional housing is preferably formed separately and prior to attaching it to a radiation detector. The housing described in US Patent 7,462,833, which is hereby incorporated by reference, may be used as the optional housing. Accordingly, the method of making the detector of one embodiment comprises (a) providing a radiation detector

comprising a semiconductor substrate having opposing front and rear surfaces, a cathode electrode located on the front surface of said semiconductor substrate and a plurality of anode electrodes on the rear surface of said semiconductor substrate, and wherein the work function of the cathode electrode material is lower than the work function of the anode electrode material, (b) providing a separately formed electrically conductive housing, and (c) attaching the housing to the cathode electrode such that the housing and the cathode electrode are in electrical contact. Alternatively, the optional housing may be omitted entirely or substituted with an optional printed circuit board type of cathode plate, such as a gridded PCB type of cathode plate.

[0030] A non-limiting example of a method of particular embodiment is depicted in Figs. 2A – 2D showing side cross-sectional views of the detector at various stages of attaching a housing thereto. Starting with Fig. 2A, a radiation detector and its basic elements, cathode electrode 201, semiconductor substrate 304 and anode electrodes 400 are shown. The anode and cathode electrodes may be formed in either order on substrate 304 as will be described in more detail in Fig. 3. The detector may or may not comprise at least one of a guard ring or screening electrode. Next, an optional protective coating (or solder mask) 420 is applied to edges of the substrate 304, as shown in Fig. 2B. Alternatively, this coating may be removed once a housing is formed thereon, resulting in an air gap between said housing and a side of the detector. Alternatively, this coating 420 is made of other electrically insulating materials, such as Humiseal.

[0031] As shown in Fig. 2C, the electrically conductive housing is attached to the cathode and optionally the sides of the detector. In this illustration, the housing 425 comprises a top portion 440 and an optional side portion 430. The sides of the detector may or may not be glued to the protective coating (or solder mask) 420 covering sides of the detector depending on various reasons such as for example, if one wishes to later remove the protective coating. In this example, the housing is attached to the cathode via an epoxy, although one skilled in the art may chose from other adhesives.

[0032] The electrically conductive housing 425 shields the detector from background electromagnetic fields (or magnetic fields). Additionally, device electric fields are focused using this housing. The housing is also preferably transparent to X-ray or gamma-ray radiation. Further, the housing preferably exhibits little or no oxidation in ambient air, such as under normal operating conditions of the detector. As such, the housing is most preferably

a thin structure and comprises a material transparent to radiation, substantially impervious to background electromagnetic fields and exhibits little or no oxidation at ambient conditions.

[0033] For example the housing may be between about 50 microns and 100 microns thick. In some cases a metal foil is sufficient as a housing.

[0034] Based on the parameters set forth above, one skilled in the art may chose from a host of materials for constructing the housing. In general, metals and metallic alloys are preferred. Any suitable metal which does not substantially oxidize in air may be used. A non-limiting example of suitable metallic alloys includes stainless steel, brass (such Ni/Ti coated brass), NiCo alloys, NiFe alloys, NiFeCo alloys, NiFeMo alloys or NiFeCuMo alloys. A class of metal alloys termed “Mu-metals” is most preferred. Mu-metals are a type of NiFe alloy, particularly effective at screening static or low frequency magnetic fields. In some cases, the aforementioned alloys may be doped with other alloying elements, mechanically pre-treated (e.g. cold worked, hot worked etc.), chemically surface-treated (e.g. surface coating for corrosion resistance) or any combination thereof.

[0035] In a particular embodiment, the housing for a radiation detector comprises a first means for electrically contacting a cathode electrode of a semiconductor radiation detector and a second means for shielding at least one side of a detector. For example, the first means may comprise the top portion 440 while the second means may comprise the side portion 430 of a housing 425. In some cases the side portion 430 extends over a fraction of the thickness of the semiconductor substrate, on at least one side. However, the side portion 430 may be omitted entirely. The top portion 440 is preferably shaped to make optimal electrical contact with a high voltage supply which is in electrical contact with the anodes and cathodes of the radiation detector, and preferably maintains the anode at a higher electrical potential relative to the cathode.

[0036] In some cases a flat top portion 440 is preferred. In another particular embodiment, the housing 425 is hemispherical or dome-shaped and partially or completely covers at least one side of the semiconductor substrate.

[0037] In some embodiments, the housing 425 is shaped to conform to geometry of the detector, more specifically, to geometry of the cathode, to which it is secured. Therefore, one skilled in the art may contemplate various curved or angular housing shapes given the

shape of the detector. In a non-limiting example, the housing is a rectangular or circular-cross-sectioned (e.g. cylinder) shape.

[0038] When the housing is constructed to extend over (partially or completely) at least one side of the substrate, said at least one side is spaced from said housing. This gap is either empty or filled with an insulating material.

[0039] The housing 425 is attached to the cathode electrode 201 such that an electrical conduction path exists between the two. In a preferred case, the housing and the cathode are attached via an electrically conductive material. Most preferably, an electrically conductive polymeric material, such as a conductive epoxy applied to the inner face or surface of the housing is used.

[0040] Fig. 2D illustrates an optional step where a solder mask 450 is disposed over the pixilated anode electrodes 400 providing mechanical protection while allowing external access to the electrodes. Further electrical isolation of the anode electrodes may be achieved with the solder mask 450 when the mask is formed between the pixilated anode electrodes 400 at the interpixel region.

[0041] Accordingly, a particular optional embodiment is directed to a radiation detector comprising a solder mask disposed above the anode electrodes in addition to the housing 425 contacting the cathode electrode 201. Solder masks suitable for embodiments of the present application are described in U.S. Application serial number 11/642,819, filed on December 21, 2006 which is hereby incorporated by reference in its entirety.

[0042] Preferably, the solder mask is photoimageable such that the portions of the solder mask 450 material over the anodes 400 are directly exposed to radiation, such as UV radiation, through a mask. The radiation either cross links or uncross links the exposed portions of the solder mask, depending on the type of epoxy used (i.e., analogous to a positive or negative photoresist). The uncross linked portions are then selectively etched away to form the openings 460 exposing a portion of the anode 400 surfaces. Alternatively, for a non-photoimageable solder mask material, a conventional photoresist mask formed over the solder mask may be used in the patterning step. The entire radiation detector device is covered with the solder mask except for the cathode and the anode regions exposed through the opening. Preferably, only a portion of each anode 400 is exposed in each opening 460 and no portion of the tile 304 is exposed. Thus, the solder mask is used as a protective

coating (i.e., passivation/encapsulation agent) for protecting the entire radiation detector device.

[0043] As described in U.S. Application serial number 11/642,819, the radiation detector device comprising a solder mask may be connected to a readout printed circuit board (PCB), at the underfill filling locations located on the mating pad. The solder balls are placed in the openings 460 formed in the solder mask which serve as electrical interconnects between anodes 400 of the detector device and the conductor pads of the printed circuit board.

[0044] Figs. 3A-I illustrate, without any intent to limit the present embodiments, an example of steps in a method of forming tri-layer metal anode contacts on a semiconductor substrate at positions (pixels) for defining radiation detector cells with an interpixel gap with high resistivity between the detector cells. While tri-layer contacts are illustrated, it should be understood that single layer or bi-layer anode electrodes may also be used. In this example, it is assumed that the semiconductor substrate is made of cadmium zinc telluride (CdZnTe) or cadmium telluride (CdTe), although it will be appreciated that other semiconductor materials, for example lead iodide, thallium bromide, gallium arsenide or silicon, can be used. Also, it will be assumed that the metal used for the metallization layer and the contacts is gold, although it will be appreciated that other metal anode, alloys or other conductive materials, for example platinum, could be used instead.

[0045] Thus, Figs. 3A-3I are a schematic cross-sectional views from the side of a detector substrate at various stages in the formation of gold anode contacts on a CdZnTe substrate. The detailed features and structure at each step of the process are shown, resulting in an array of anode contact pixels on the rear surface of the CZT (drawn as facing up in this illustration), and a single cathode electrode on the front surface of the CZT tile (drawn as facing down in this illustration). In this example, two additional contact layers are added on to the pixilated primary contact layer on the rear side, for improved device assembly. The process can be applied to any array size and pixel configuration for CZT devices. A typical device size is a 20x20x5 mm detector, having 8x8 pixels or 11x11 pixels depending on the application. As a precursor to contact fabrication, the CZT wafer is polished and etched such that high quality clean crystal surfaces are prepared for the deposition process.

[0046] A direct lithography fabrication process is described with reference to Figs. 3A-I, and for the case of the primary anode contact being gold, with two additional contact layers,

and for separately forming of the cathode contact on the opposing side of the CZT tile or substrate 304 shown in Fig. 3A. It is noted, however, that direct lithography process for formation of the anode electrode is only one of many processes that may be used to form the electrodes. Other methods, including but not limited to a lift-off method, may be used to form the electrodes instead. For example, a lift-off method for forming the anode electrodes of the embodiments of the present invention comprises the steps of a) providing the substrate, b) forming a mask (such as a photoresist mask) over the substrate surface, where the pattern comprises portions of mask material and spaces without mask material, c) depositing an anode electrode material over the mask where first portions of the anode electrode material are formed on the substrate in the spaces of the mask pattern while second portions of the anode electrode material are formed on the mask material, and d) removing or lifting-off the mask such that second portions of the anode electrode material formed over the mask material are also removed with the mask, and first portions of the anode electrode material contacting the substrate remain on the substrate.

[0047] In step 1 of the direct lithography process, shown in Fig. 3B a primary layer of gold 200 is deposited onto a rear side of the CZT tile 304 (the rear side is shown facing up in Fig. 3B). The gold layer 200 may be deposited by electroless deposition. Alternatively the gold layer 200 may be deposited by other known techniques, such as sputtering or evaporation. Additionally, a cathode electrode layer 201 comprising indium is deposited by sputtering, electroless plating or other suitable method onto an opposing front side of the CZT tile. The CZT tiles are first cleaned in acetone, as is well known. The clean CZT tiles 304 are appropriately masked and placed in a chamber for sputtering or plating of gold onto a first side and indium onto a second side. Typical thickness of the deposited cathode layer may be between 10-100nm. The deposited gold may be annealed at 90 deg C for 15 minutes to increase adhesion to the substrate. An adhesion test can be done after a few hours using Scotch tape to confirm quality of the adhesion.

[0048] In an optional step 2 shown in Fig. 3C, two additional contact layers are deposited onto the rear side (anode side to be pixilated) of the tile, over the primary contact layer 200. In this example, a Ni layer 312 is deposited using sputtering or a thermal evaporation process to a thickness < 100nm and nominally 50nm. Then another gold layer 310 is deposited using sputtering, thermal evaporation and/or an electroless process to a thickness < 50 nm and

nominally 20nm. Alternative conductive contact material can be substituted for either or both of the additional contact layers.

[0049] In step 3, as shown in Fig. 3D, a photoresist 202 is applied over the contact layer(s). Tiles 304 are dipped in resist, for example Shipley 1805 resist. Excessive resist is removed if necessary from the edge using a Q-tip, making sure the resist does not form any edge bead (especially on the pixilated face) as this would be detrimental for the pixel quality. Generally, the least possible amount of resist should remain on the pixilated face. The resist should be dried out for 10 minutes with the pixilated face kept up and horizontal.

[0050] The resist coating is hardened in step 4 by baking for 10 minutes at 90°C. This step is done to drive excess solvent out of the resist. The tile is now prepared for lithography exposure.

[0051] In step 5, as shown in Fig. 3E a pixel pattern is formed on the rear side of the tile 304 by photolithography. A UV mask 204 is aligned over the CZT tile surface, and the positive resist is exposed to UV. The direct lithography mask shades regions of the resist in a selected pixel pattern and exposes interpixel gaps to UV radiation. A contact mask is shown but other methods will work as well, such as proximity and projection masks. A glass plate is placed on top making sure that the glass plate is horizontal. This ensures uniform contact between the tile and the mask. For the exemplary resist, exposure by a UV lamp (365 nm wavelength) for several minutes is suitable. If desired, a negative resist may be used instead of the positive resist (in which case, the exposure mask's transparent and opaque regions are reversed).

[0052] In step 6 shown in Fig. 3F, the exposed photoresist is developed. The resist developer (for example Microposit developer, MF-319) should cover the tile(s). The tiles are placed into the developer with the pixilated side facing up, developed for 2 minutes and the tile(s) are removed from the developer and rinsed in de-ionized water. The UV exposed resist is removed, in preparation for creating the interpixel gap.

[0053] In step 7 the remaining resist pixel pattern 314 is baked for 20 minutes at 90°C. This step is done to harden the resist further.

[0054] In step 8, shown in Fig. 3G, the exposed contact regions 316 (not covered by the pixel resist pattern 314) are etched. For the example contact materials, the following etching

solution is suitable for etching through either just the primary contact layer or the optional three-layer contact. A 2% Br- Ethanol Glycol (BrEG) solution is prepared by pouring a 25ml of Ethylene Glycol into a plastic beaker, then 0.5ml of Bromine is added using a disposable pipette. Using the same pipette, the solution is mixed thoroughly until it becomes uniform. However, a different pipette or mixing device may also be used. Etching is conducted for approximately 3 minutes. This etching is done to remove unmasked interpixel contact material. To open the interpixel gap to achieve clean interpixel gaps, active spray agitation is performed. Disposable pipettes can be used to create Br-EG constant flow to agitate for better etching. However, a different pipette or agitation or mixing device may also be used. The spray etching technique should rapidly remove contact material flakes from the interpixel gaps, resulting in high interpixel resistance. The tiles are removed from the etchant and rinsed in deionized water.

[0055] In step 9 shown in Fig. 3H, the remaining resist is stripped using an acetone bath, resulting in tile 320 with a pixel array of contacts. No photoresist therefore remains on the CdTe or CdZnTe detector since it is usually a hygroscopic material that in time would absorb humidity and deteriorate the detector performance.

[0056] The overall combination of depositing a metal layer having a work function greater than or equal to about 4.8 eV, such as gold, over the rear substrate surface, depositing a metal layer having a work function less than about 4.5 eV, such as indium, over the front surface, direct photolithography and the etching process results in the improved device performance with minimal leakage current.

[0057] In optional step 10 shown in Fig. 3I, the primary contact material (in this example gold) on the side of the tile 305 of the fabricated CZT device 322 is removed by side polishing. For example, the side of the tile(s) are first polished with 1200 grit then with 0.3 micron as fine polish. An alternate embodiment could, in step 1, mask the sides of the CZT tile instead of depositing gold on the sides. For this reason, the side contact removal step 10 may be optional. The resulting fabricated CZT device has a cathode electrode 201 remaining on a front side, a pixilated anode electrode array formed of a primary contact layer 200 and secondary contact layers 312 and 310, separated by interpixel gaps 316 on a rear side. Fig 3I illustrates the multi-layer pixels as being identical width in cross-section for illustrative purpose.

Examples

[0058] Ohmicity is typically exhibited by a linear current-voltage (I-V) relationship. Indium as the cathode electrode material exhibits greater ohmicity as compared to gold. As shown in Figs. 4-7, current was measured at the cathode between 0-5 V for comparative devices and exemplary embodiments of the present invention with and without being irradiation by a Co-57 source. A linear regression analysis was performed with R^2 which is used to determine the linearity of the curve. It is noted that a maximum of $R^2=1$ represents a perfectly linear curve and therefore, perfect ohmic character.

[0059] As shown in Fig. 4, a regression analysis indicates that a comparative device comprising gold as the cathode electrode material and not exposed to radiation from a Co-57 source results in an R^2 value equal to 0.8532. As shown in Fig. 5, when the device of Fig. 4 is irradiated, a regression analysis of the I-V relationship shows a resulting R^2 value equal to 0.7861 which indicates that ohmicity of the gold cathode has decreased.

[0060] As shown in Fig. 6, a regression analysis shows that an exemplary device comprising indium as the cathode electrode material and not irradiated by a Co-57 source results in an R^2 value equal to 0.9996 indicative of a high degree of linearity for the I-V relationship. As shown in Fig. 7, when the device of Fig. 6 is exposed to radiation, a regression analysis indicates that ohmicity of the indium cathode decreases only very slightly resulting R^2 value equal to 0.9991, still indicative of a high degree of linearity and therefore, Ohmic character.

[0061] It is clear from Figs. 4-7 that by replacing gold as the cathode electrode material with indium, the embodiments of the present invention offer the benefits of enhanced charge collection when operated as a radiation detector for example.

[0062] In order to improve the photo-peak counts, the inventors have discovered various configurations to achieve improved sensitivity of the detectors. For example by changing the material of one of the electrodes, namely by changing the cathode electrode material from gold to indium, the result is increased electrode ohmicity. Also, by changing the active volume of the detector, for example by decreasing the interpixel gap width, an improved device performance results.

[0063] To achieve these results, radiation detectors comprising a semiconductor substrate having opposing front and rear surfaces, a cathode electrode located on the front surface of said semiconductor substrate configured so as to receive radiation, and a plurality of anode electrodes formed on the rear surface of said semiconductor substrate were manufactured. Various elements of the device were changed for a particular experimental run. For example, the interpixel gap was changed from between 600 μm to 460 μm , maintaining the pitch at 2.46 mm, on a detector with gold cathode and anode electrodes. Subsequently, keeping the pixelation on the anode untouched, the cathode was polished off, and metalized with indium. As the last step, the cathode was protected, and the anode was re-fabricated with 300 μm interpixel gap.

[0064] The following are non-limiting examples detailing particular device configurations of the present radiation detector devices of the embodiments of the invention:

Comparative Example 1: In cathode and Au anode with 460 μm interpixel gap

[0065] As a first comparative example of a radiation detector device, a 20x20x5 mm³ radiation detector device with an 8x8 pixel configuration is listed in Table 1 as CE 1. The device comprises: a semiconductor substrate having opposing front and rear surfaces, a cathode electrode comprising gold located on the front surface of said semiconductor substrate configured so as to receive radiation, and a plurality of anode electrodes comprising gold formed on the rear surface of said semiconductor substrate. The plurality of anode electrodes are formed as pixels having an interpixel gap width between each pixel of about 600 μm . The anode and cathode electrodes are electrically connected to a voltage source which provides a means for applying forward-bias electric potential of about 400 V while a Co-57 source is placed 25 mm from the cathode.

Comparative Example 2: In cathode and Au anode with 300 μm interpixel gap

[0066] As a second comparative example of a radiation detector device, a 20x20x5 mm³ radiation detector device with an 8x8 pixel configuration is listed in Table 1 as CE . The device comprises: a semiconductor substrate having opposing front and rear surfaces, a cathode electrode comprising gold located on the front surface of said semiconductor substrate configured so as to receive radiation, and a plurality of anode electrodes comprising gold formed on the rear surface of said semiconductor substrate. The plurality of anode

electrodes are formed as pixels having an interpixel gap width between each pixel of about 460 μm . The anode and cathode electrodes are electrically connected to a voltage source which provides a means for applying forward-bias electric potential of about 400 V while a Co-57 source is placed 25 mm from the cathode.

Example 1: In cathode and Au anode with 460 μm interpixel gap

[0067] As a first example of a non-limiting embodiment of the present invention, a 20x20x5 mm³ radiation detector device with an 8x8 pixel configuration is listed in Table 1. The device of Ex 1 comprises: a semiconductor substrate having opposing front and rear surfaces, a cathode electrode comprising indium located on the front surface of said semiconductor substrate configured so as to receive radiation, and a plurality of anode electrodes comprising gold formed on the rear surface of said semiconductor substrate. The plurality of anode electrodes are formed as pixels having an interpixel gap width between each pixel of about 460 μm . The anode and cathode electrodes are electrically connected to a voltage source which provides a means for applying forward-bias electric potential of about 400 V while a Co-57 source is placed 25 mm from the cathode.

Example 2: In cathode and Au anode with 300 μm interpixel gap

[0068] As a second example of another non-limiting embodiment of the present invention, a 20x20x5 mm³ radiation detector device with an 8x8 pixel configuration is listed in Table 1. The device of Ex 2 comprises: a semiconductor substrate having opposing front and rear surfaces, a cathode electrode comprising indium located on the front surface of said semiconductor substrate configured so as to receive radiation, and a plurality of anode electrodes comprising gold formed on the rear surface of said semiconductor substrate. The plurality of anode electrodes are formed as pixels having an interpixel gap width between each pixel of about 300 μm . The anode and cathode electrodes are electrically connected to a voltage source which provides a means for applying forward-bias electric potential of about 400 V while a Co-57 source is placed 25 mm from the cathode. It is noted that the same Co-57 source was used for all measurements, the measurements were made within a few weeks of each other, and the measurements were taken based on a source strength of about 17 μCi .

TABLE 1					
Example	Interpixel gap (μm)	Cathode/Anode Electrode Material	Bias (Volts)	Average photo- peak counts of center pixels	% Increase over adjacent configuration
CE 1	600	Au/Au	400	2437	-
CE 2	460	Au/Au	400	2726	12
Ex 1	460	In/Au	400	3023	11
Ex 2	300	In/Au	400	3317	10

[0069] Between the configurations of CE 1 and CE 2 as shown in Table 1, an average increase in photo-peak counts of 12% is observed.

[0070] Between the configurations of CE 2 and Ex 1 as shown in Table 1, an average increase in photo-peak counts of 11% is observed.

[0071] Between the configurations of Ex 1 and Ex 2 as shown in Table 1, an average increase in photo-peak counts of 10% is observed.

[0072] The results shown in Table 1 may be summed up as an effective increase in photo-peak counts of 30-50% in advancing the configuration of CE 1 to that of Ex 2.

[0073] Table 2 shows the change in the photo-peak counts of the center pixels between the configurations of CE 1 and CE 2 for various radiation source strengths. In the experiments yielding the results shown in Table 2, only the center pixels are considered to eliminate the edge effect from the analysis as the edge pixels did not show the expected change when the radiation source strength was doubled. As shown in Table 2, an increase in the photo-peak counts ranging from 2-23% results when the interpixel gap is changed from a width of 600 μm to 460 μm . This indicates that reducing the interpixel gap, while maintaining the other aspects of configuration, such as pitch, is advantageous to enhance the sensitivity of the detector.

TABLE 2			
Example	Configuration	Photo-peak count	% Change
CE 1	Au-Au 600 μm	2650	-
CE 2	Au-Au 460 μm	2690	2
CE 1	Au-Au 600 μm	1658	-
CE 2	Au-Au 460 μm	2000	21
CE 1	Au-Au 600 μm	2913	-
CE 2	Au-Au 460 μm	3113	7
CE 1	Au-Au 600 μm	2529	-
CE 2	Au-Au 460 μm	3102	23

[0074] In the next stage, the cathode electrode of the four 460 μm interpixel gap width detectors was changed to In. This was done by maintaining the fabrication by protecting the anode, and suspending the cathode in an electroless In solution. Table 3 shows the results of this change in the configuration.

TABLE 3			
Example	Configuration	Photo-peak count	% Change
CE 2	Au-Au 460 μm	2690	-
Ex 1	In-Au 460 μm	3230	20
CE 1	Au-Au 460 μm	2000	-
Ex 1	In-Au 460 μm	2827	41
CE 1	Au-Au 460 μm	3113	-
Ex 1	In-Au 460 μm	3392	9
CE 1	Au-Au 460 μm	3102	-
Ex 1	In-Au 460 μm	2644	-14

[0075] In the final stage, the anode electrode of the four detectors was re-fabricated with a smaller interpixel gap of 300 μm . Table 4 shows the results of this step. An increase in photo-peak counts of 7-17% is seen with this change. This indicates that the 300 μm interpixel gap is the best for improvement of sensitivity for this particular detector configuration. In

general, the gap width may range from 100 – 500 microns, such as 200-400 microns, depending on other detector materials and dimensions.

TABLE 4			
Example	Configuration	Photo-peak count	% Change
Ex 1	In-Au 460 μ m	3230	-
Ex 2	In-Au 300 μ m	3522	9
Ex 1	In-Au 460 μ m	2827	-
Ex 2	In-Au 300 μ m	3032	7
Ex 1	In-Au 460 μ m	3392	-
Ex 2	In-Au 300 μ m	3622	7
Ex 1	In-Au 460 μ m	2644	-
Ex 2	In-Au 300 μ m	3094	17

[0076] It is noted that for additional examples of the embodiments of the invention disclosed herein, the interpixel gap was reduced further to 100 μ m but the measured interpixel resistance of these detectors, on average, were 2 orders of magnitude smaller than for embodiments of the present invention comprising a 460 μ m interpixel gap width. In addition, the resistance profile showed a sharp decrease at higher biases indicating the possibility of electrical breakdown. For example, Figure 8 shows a comparison of the interpixel resistance of edge pixels of the example embodiments of the present invention comprising 460 μ m, 300 μ m and 100 μ m interpixel gap widths. Figure 9 shows a similar comparison of the center pixels of detectors in these configurations. As noted above, the center pixels typically have the best interpixel resistance in the entire detector. Moreover, while the exemplary embodiment comprising a 300 μ m interpixel gap widths exhibit marginally lower resistance than the exemplary embodiment comprising a 460 μ m interpixel gap width, the resistance profile is still sufficiently flat to ensure electrical stability. Conversely, the exemplary embodiment comprising a 100 μ m interpixel gap width exhibits a resistance two orders of magnitude lower than that of the exemplary embodiment comprising the 460 μ m interpixel gap width, which tends to decrease very sharply towards higher biases. In other words, while the exemplary embodiment comprising a 100 μ m interpixel gap width shows superior sensitivity, it has poor interpixel resistance, and the interpixel resistance is a very important factor in the energy resolution performance of radiation detectors.

[0077] Although the foregoing refers to particular preferred embodiments, it will be understood that the present invention is not so limited. It will occur to those of ordinary skill in the art that various modifications may be made to the disclosed embodiments and that such modifications are intended to be within the scope of the present invention. All of the publications, patent applications and patents cited herein are incorporated herein by reference in their entirety.

WHAT IS CLAIMED IS:

1. A radiation detector, comprising:
a semiconductor substrate having opposing front and rear surfaces;
a cathode electrode located on the front surface of said semiconductor substrate configured so as to receive radiation; and
a plurality of anode electrodes formed on the rear surface of said semiconductor substrate;
wherein a work function of the cathode electrode material contacting the front surface of the semiconductor substrate is lower than a work function of the anode electrode material contacting the rear surface of the semiconductor substrate.
2. The radiation detector of claim 1, wherein the work function of the cathode electrode material is less than about 4.5 eV, and the work function of the anode electrode material is greater than or equal to about 4.8 eV.
3. The radiation detector of claim 1, wherein the cathode electrode material comprises one of In, Al, and Ti.
4. The radiation detector of claim 1, wherein the anode electrode material comprises one of Au and Pt.
5. The radiation detector of claim 1, wherein the semiconductor substrate comprises CdTe or CZT, and the substrate lacks a p-n or p-i-n junction.
6. The radiation detector of claim 1, wherein the plurality of anode electrodes are configured as pixels with an interpixel gap between each two adjacent anode electrode pixels.
7. The radiation detector of claim 6, wherein said interpixel gap width is between 100 and 500 μm .
8. The radiation detector of claim 7, wherein said interpixel gap width is between 200 and 400 μm .
9. The radiation detector of claim 1, further comprising an electrically conductive housing located in electrical contact with the cathode electrode.

10. The radiation detector of claim 1, further comprising a voltage source electrically connected to the anode and the cathode electrodes.
11. A radiation detector system, comprising:
 - a semiconductor substrate having opposing front and rear surfaces;
 - a cathode electrode located on the front surface of said semiconductor substrate configured so as to receive radiation;
 - a plurality of anode electrodes formed on the rear surface of said semiconductor substrate, wherein a work function of the cathode electrode material contacting the front surface of the semiconductor substrate is lower than a work function of the anode electrode material contacting the rear surface of the semiconductor substrate; and
 - a means for applying a forward bias to the detector during operation such that the anode electrodes is maintained at a higher potential than the cathode electrode and such that the signal is collected from the anode electrodes.
12. The radiation detector system of claim 11, wherein the work function of the cathode electrode material is less than about 4.5 eV, and the work function of the anode electrode material is greater than or equal to about 4.8 eV.
13. The radiation detector system of claim 11, wherein the cathode electrode material comprises one of In, Al, and Ti, the anode electrode material comprises one of Au and Pt, and the semiconductor substrate comprises CdTe or CZT.
14. A method of operating a radiation detector, comprising:
 - providing a radiation detector comprising:
 - a semiconductor substrate having opposing front and rear surfaces;
 - a cathode electrode located on the front surface of said semiconductor substrate configured so as to receive radiation; and
 - a plurality of anode electrodes formed on the rear surface of said semiconductor substrate, wherein a work function of the cathode electrode material contacting the front surface of the semiconductor substrate is lower than a work function of the anode electrode material contacting the rear surface of the semiconductor substrate;
 - receiving radiation at the cathode electrode;

applying a forward bias to detector to maintain the anode electrodes at a higher potential than the cathode electrode; and

collecting a signal from the anode electrodes.

15. The method of claim 14, wherein the work function of the cathode electrode material is less than about 4.5 eV, and the work function of the anode electrode material is greater than or equal to about 4.8 eV.
16. The method of claim 14, wherein the cathode electrode material comprises one of In, Al, and Ti, the anode electrode material comprises one of Au and Pt, and the semiconductor substrate comprises CdTe or CZT.
17. The method of claim 14, wherein said forward bias injects electrons from said cathode electrode material into the front surface of the semiconductor substrate.
18. The method of claim 14, wherein the radiation comprises at least one of gamma ray and X-ray radiation.
19. The method of claim 14, wherein the plurality of anode electrodes are configured as pixels with an interpixel gap between each two adjacent anode electrode pixels and the signal comprises a measured current or voltage which corresponds to the radiation received at each pixel.
20. The method of claim 19, wherein said interpixel gap width is between 100 and 500 μm .

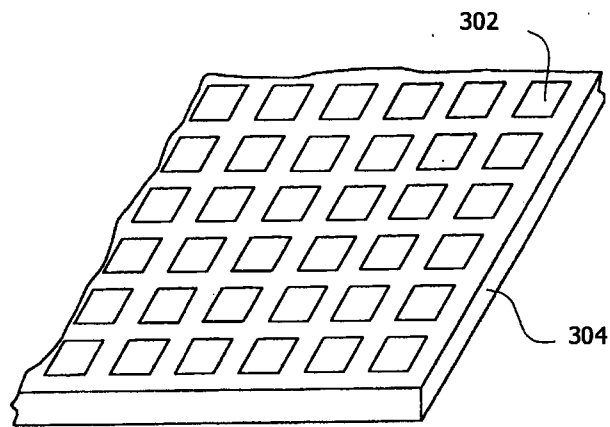


Fig. 1

2/10

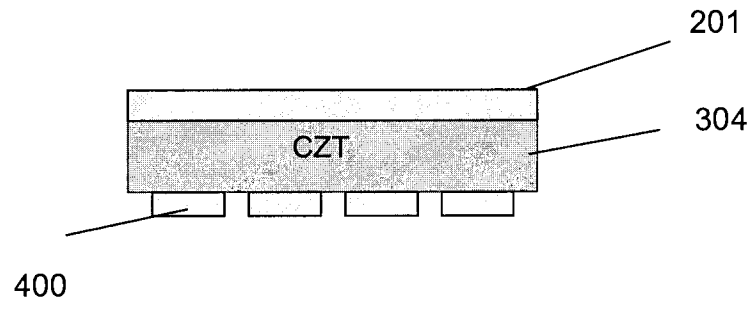


Fig. 2A

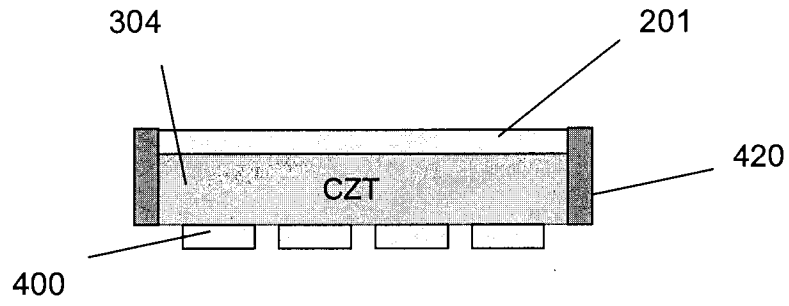


Fig. 2B

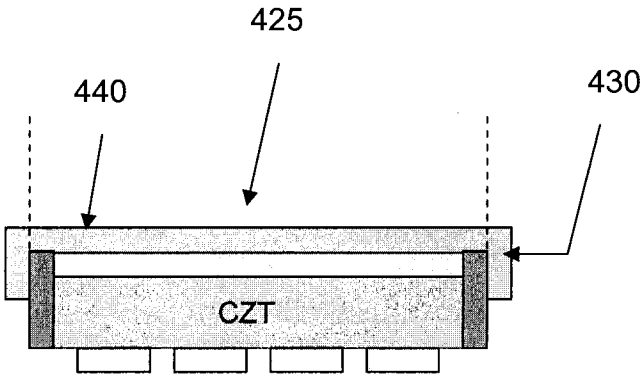


Fig. 2C

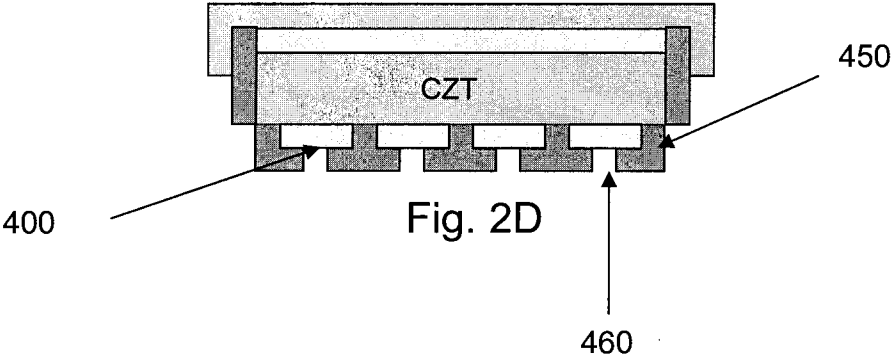


Fig. 2D



Fig. 3A

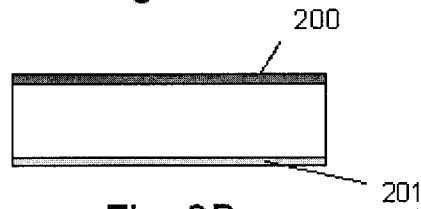


Fig. 3B

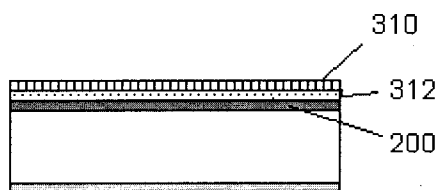


Fig. 3C

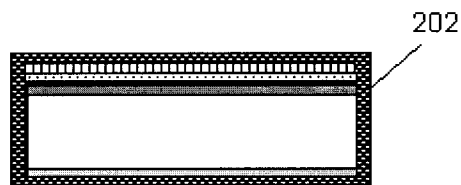


Fig. 3D

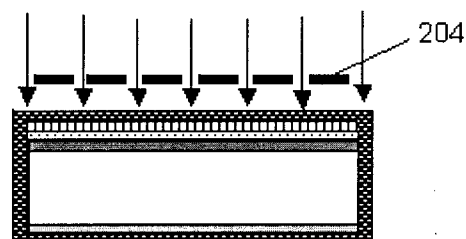


Fig. 3E

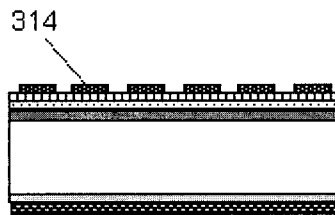


Fig. 3F

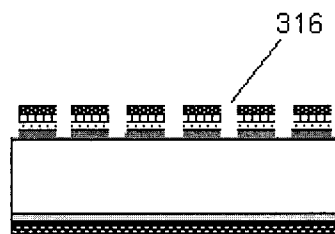


Fig. 3G

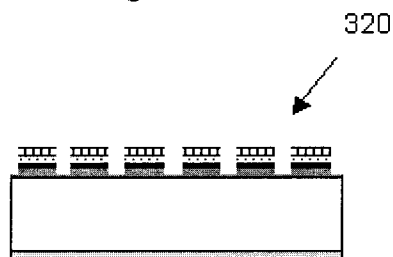


Fig. 3H

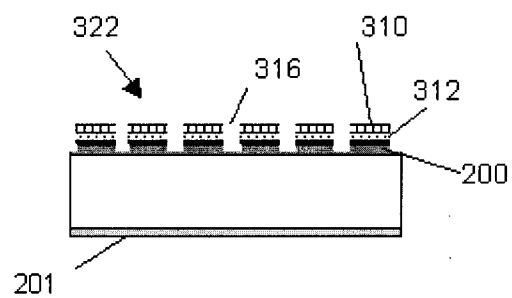


Fig. 3I

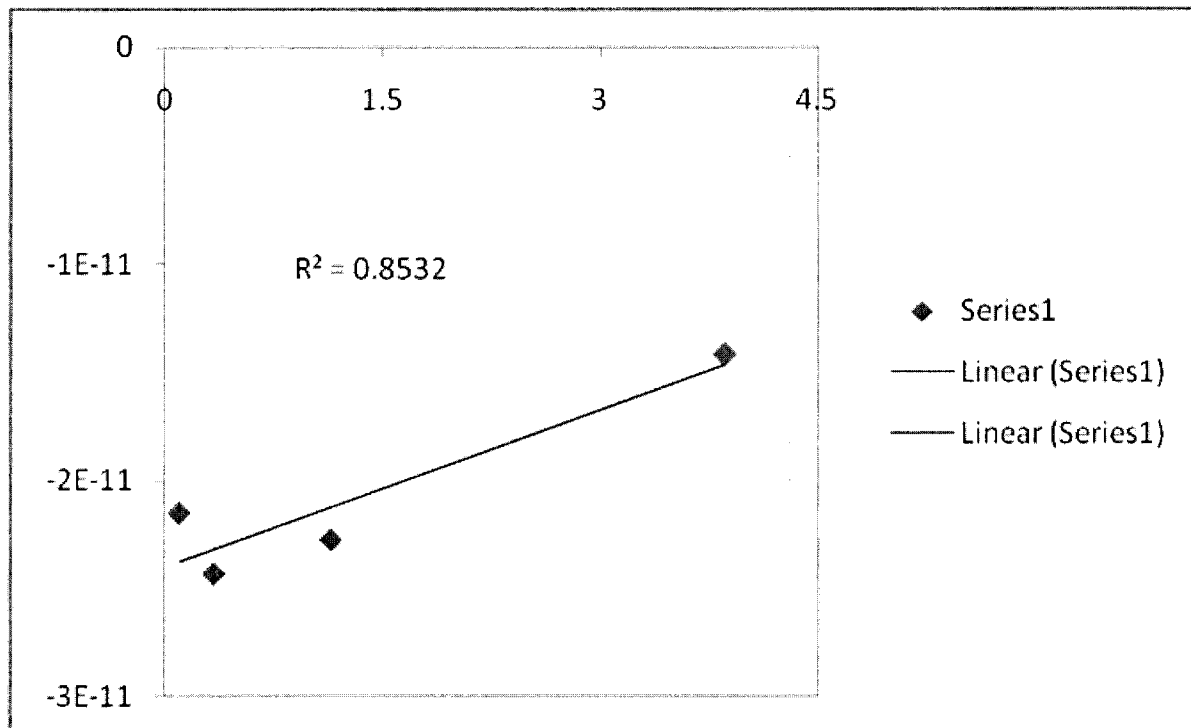


Fig. 4

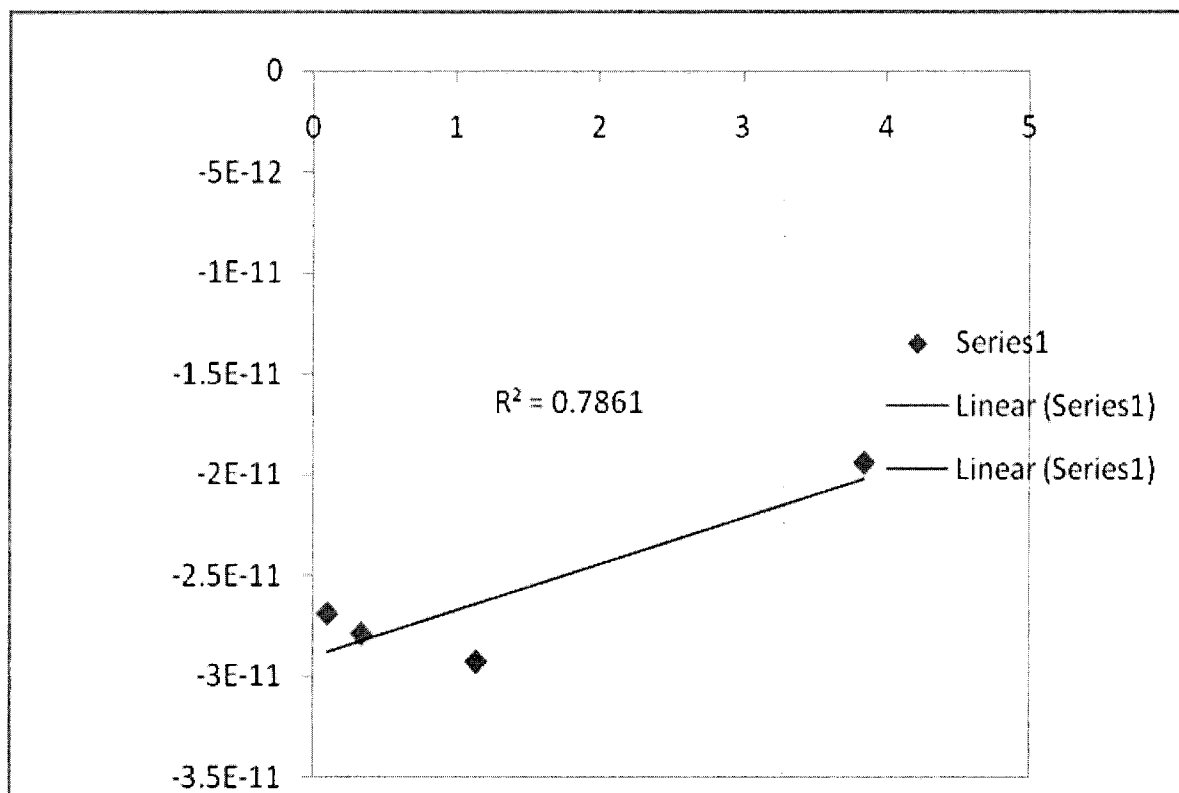


Fig. 5

7/10

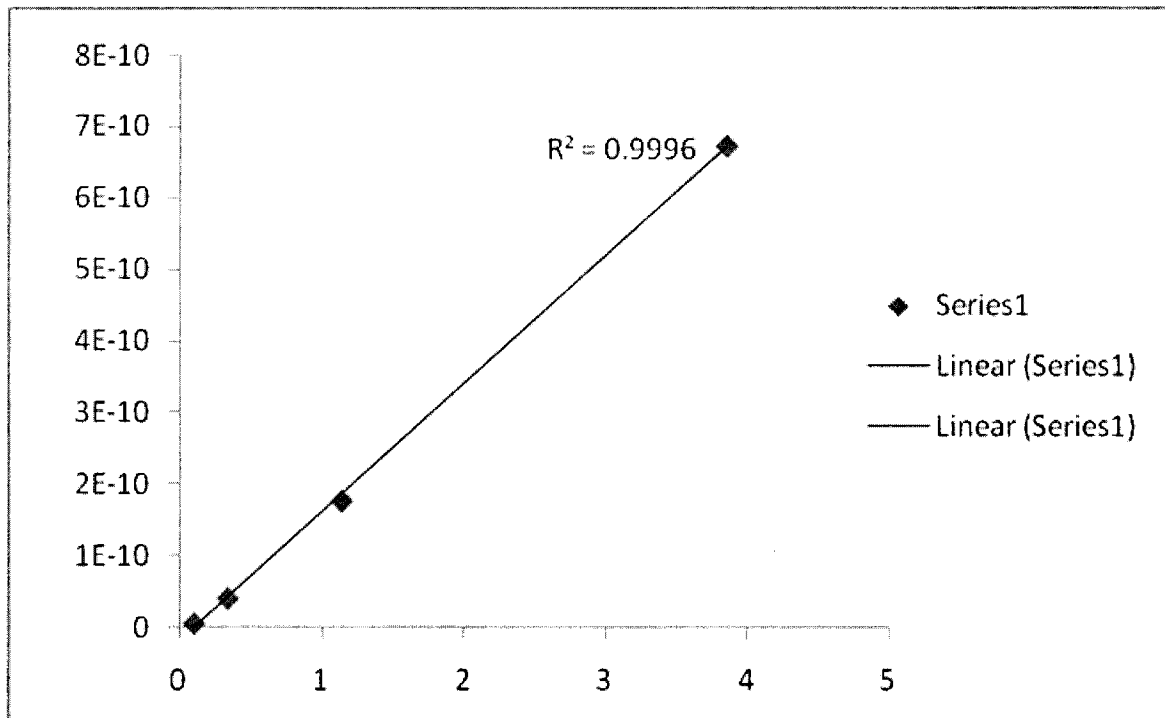


Fig. 6

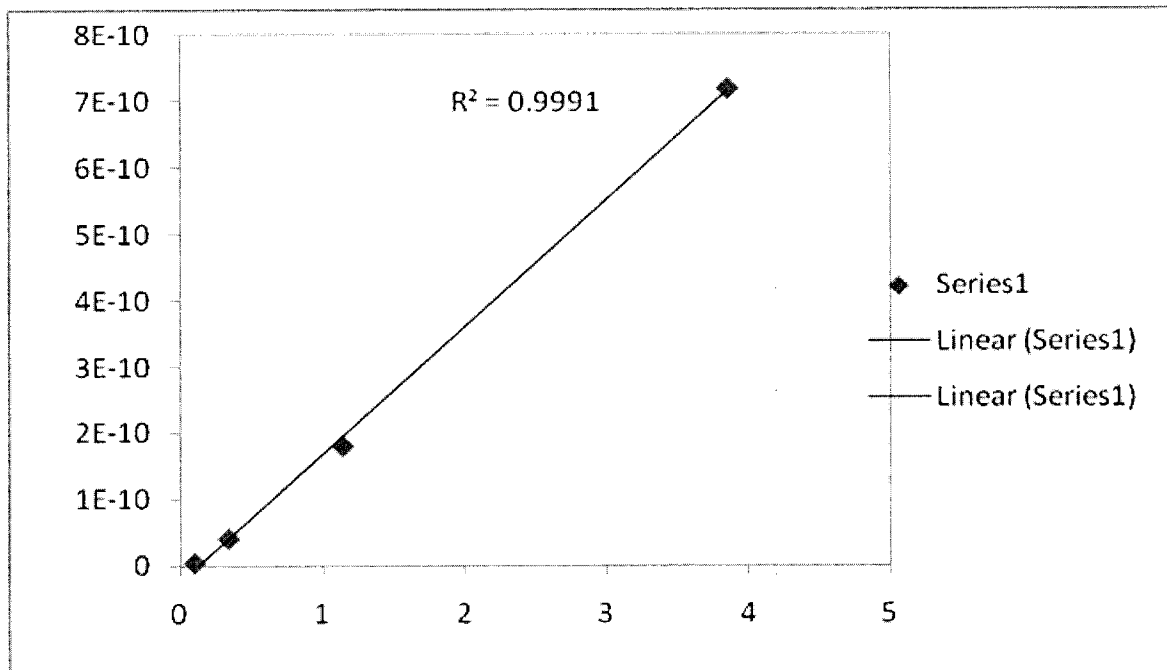


Fig. 7

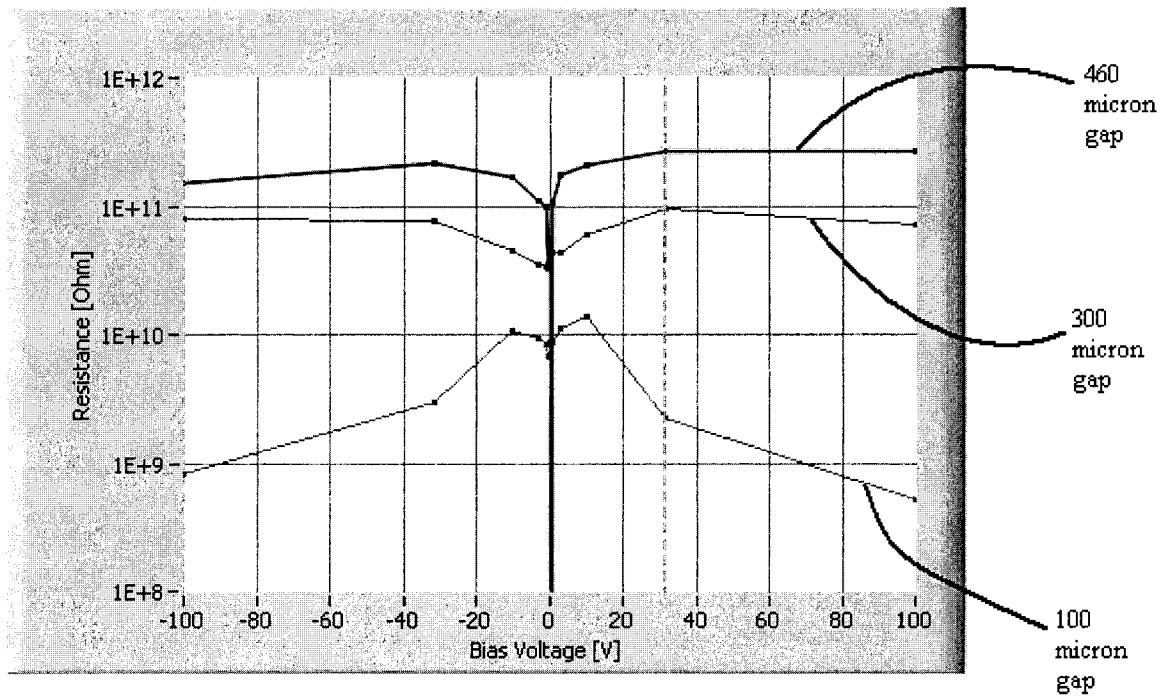


Fig. 8

10/10

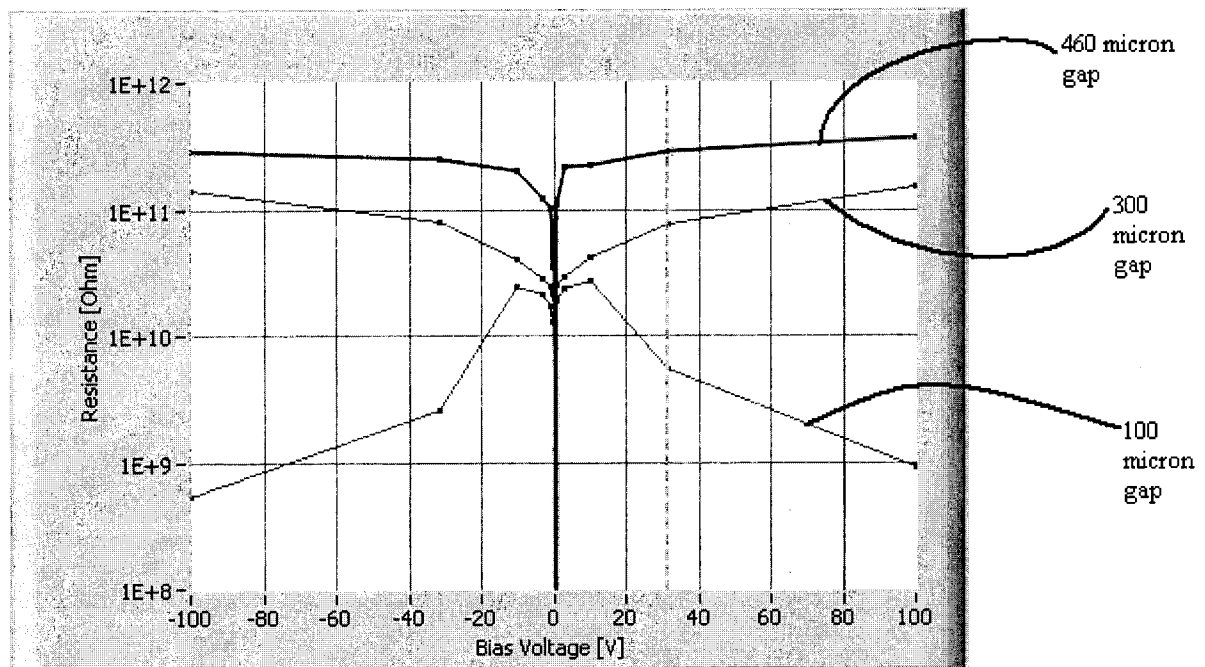


Fig. 9