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- with international search report (Art. 21(3))
- with amended claims and statement (Art. 19(1))

(54) Title: HYDROFLUOROCARBON GAS-ASSISTED PLASMA ETCH FOR INTERCONNECT FABRICATION

(57) Abstract: In one embodiment, a method for hydrofluorocarbon gas-assisted plasma etch for interconnect fabrication includes providing a layer of a dielectric material and etching a trench in the layer of the dielectric material, by applying a mixture of an aggressive dielectric etch gas and a polymerizing etch gas to the layer of the dielectric material. In another embodiment, an integrated circuit includes a plurality of semiconductor devices and a plurality of conductive lines connecting the plurality of semiconductor devices. A pitch of the plurality of conductive lines is approximately twenty-eight nanometers.



HYDROFLUOROCARBON GAS-ASSISTED PLASMA ETCH FOR INTERCONNECT FABRICATION

BACKGROUND OF THE INVENTION

[0001] The present invention relates generally to integrated circuits and relates more specifically to metal patterning processes for use in manufacturing integrated circuits.

[0002] Integrated circuits commonly use metal interconnects (or “lines”) to connect transistors and other semiconductor devices on the ICs. These interconnects are typically fabricated during back end of line (BEOL) processes, after the individual semiconductor devices have been formed on the wafer.

[0003] These interconnects are typically fabricated using an additive damascene process in which an underlying insulating layer (*e.g.*, silicon oxide) is patterned with open trenches. A subsequent deposition of a conductive metal on the insulating layer fills the trenches with metal. The metal is removed to the top of the insulating layer, but remains within the trenches to form a patterned conductor. Successive layers of insulator and metal are formed according to this damascene process, resulting in a multilayer metal interconnect structure.

SUMMARY OF THE INVENTION

[0004] In one embodiment, a method for hydrofluorocarbon gas-assisted plasma etch for interconnect fabrication includes providing a layer of a dielectric material and etching a trench in the layer of the dielectric material, by applying a mixture of an aggressive dielectric etch gas and a polymerizing etch gas to the layer of the dielectric material.

[0005] In another embodiment, a method for hydrofluorocarbon gas-assisted plasma etch for interconnect fabrication includes providing a capping layer, providing a layer of a dielectric material directly over the capping layer, and providing a mask layer directly over the layer of the dielectric material. The mask layer is patterned to expose portions of the layer of the dielectric material, and the portions of the layer of the dielectric material

are then etched to form a plurality of trenches. The etching is performed using a mixture of an aggressive dielectric etch gas and a polymerizing etch gas, and wherein the etching stops at the capping layer. The plurality of trenches is filled with a conductive metal to form a plurality of conductive lines.

[0006] In another embodiment, an integrated circuit includes a plurality of semiconductor devices and a plurality of conductive lines connecting the plurality of semiconductor devices. A pitch of the plurality of conductive lines is approximately twenty-eight nanometers.

[0007]

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] So that the manner in which the above recited features of the present invention can be understood in detail, a more particular description of the invention may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0009] Figures 1A-1E are cross sections illustrating various stages of fabrication of an integrated circuit, according to embodiments of the present disclosure.

DETAILED DESCRIPTION

[0010] In one embodiment, a method and apparatus for hydrofluorocarbon gas-assisted plasma etch for interconnect fabrication is disclosed. Metal interconnects are typically formed during the back end of line (BEOL) stage of integrated circuit fabrication. For instance, a dry etch process using a fluorocarbon gas can be employed to define trenches in a dielectric layer of the integrated circuit. A conductive metal is then deposited in the trenches to form the interconnects. Using a fluorocarbon gas with low polymerization (such as carbon tetrafluoride (CF_4), sulfur hexafluoride (SF_6), or nitrogen trifluoride (NF_3)), one can define trenches that will provide good line-to-via connections; however such gases are not selective to the hard mask layer and tend not to maintain the pattern dimensions of the interconnects. Using a fluorocarbon gas with high polymerization (such as perfluorocyclobutane (C_4F_8), hexafluorobutadiene (C_4F_6), octafluorocyclopentene (C_5F_8), fluoromethane (CH_3F), fluoroform (CHF_3), or heptafluorocyclopentene (C_5HF_7)), one can achieve better selectivity and maintain the

pattern dimensions; however, these gases are prone to aspect ratio-dependent etching and etch stop that result in poor line-to-via connections. Additional gases can be added to promote dissociation, mixing, and improve the resultant line profiles, such as argon (Ar), nitrogen (N₂), carbon monoxide (CO), oxygen (O₂), carbon dioxide (CO₂), or the like.

[0011] Embodiments of the invention etch a pattern of trenches into a dielectric layer of an integrated circuit using a mixture of an aggressive dielectric etch gas and a polymerizing etch gas. Within the context of the disclosure, an aggressive dielectric etch gas is understood to be a fast-acting, non-selective chemical etching agent that leaves minimal deposits. The polymerizing etch gas passivates the vertical sidewalls of the trenches and protects them from damage and lateral etching by the aggressive dielectric etch gas. The resultant trenches maintain target pattern dimensions and sidewall profiles, allowing small, dense patterns to be formed. Moreover, the etch can be performed quickly and with minimal to no reactive ion etch lag.

[0012] Figures 1A-1E are cross sections illustrating various stages of fabrication of an integrated circuit 100, according to embodiments of the present disclosure. As such, Figures 1A-1E also collectively serve as a flow diagram illustrating portions of one embodiment of a method for fabricating the integrated circuit 100, according to the present invention.

[0013] In particular, Figure 1A illustrates the integrated circuit 100 at an intermediate stage in the processing, i.e., after front end of line processing is complete, but prior to the completion of back end of line processing. In other words, the integrated circuit 100 does not start out in the form illustrated in Figure 1A, but may develop into the illustrated structure over several processing steps which are not illustrated but are well-known to those of skill in the art.

[0014] The integrated circuit 100 generally comprises a front end 102, which may include a semiconductor wafer 104 (formed, for example, from crystalline silicon (Si), germanium (Ge), silicon germanium (SiGe), gallium arsenide (GaAs), or other semiconductor materials) and a pattern of individual, unconnected structures formed on the semiconductor wafer 104, such as a pattern of gates 106₁-106_n (hereinafter collectively referred to as “gates 106”). The gates 106 may comprise a number of transistors and/or other semiconductor devices. For the purposes of clarity, the front end 102 of the integrated circuit 100 is illustrated in a simplified form.

[0015] One embodiment of the present disclosure deposits a capping layer 108 on the front end 102. In one embodiment, the capping layer 108 may be formed, for example, from silicon nitride (SiN), silicon carbonitride (SiCN), or silicon oxycarbonitride (SiC_xN_yO_z). The capping layer 108 may be deposited, for example, via plasma-enhanced chemical vapor deposition (PECVD). A dielectric layer 110 is deposited directly on the capping layer 108 and may be formed from a porous dielectric material such as a low-k dielectric, an ultra-low-k dielectric (ULK), silicon dioxide (SiO₂), or other dielectric materials. The dielectric layer 110 may also be deposited via PECVD. A mask layer 112 is then deposited directly on the dielectric layer 110. The mask layer 112 may be formed from a metal, from silicon nitride (SiN), from photoresist, or from other materials. In one example, the mask layer 112 comprises a multilayer mask, such as a trilayer resist (which may comprise, for example, layers of resist, silicon-containing anti-reflective coating (SiARC), and carbon hard mask). The mask layer 112, if composed of photoresist, may be deposited via spin coating. Collectively, the capping layer 108, dielectric layer 110, and mask layer 112 form the beginnings of the back end 114 of the integrated circuit 100.

[0016] As illustrated in Figure 1B, the mask layer 112 is patterned to expose portions of the dielectric layer 110. In one embodiment the mask layer 112 is patterned using a photolithography technique, such as optical lithography or direct write electron beam lithography. In one embodiment, the photolithography technique includes a positive resist that allows removal of the mask layer 112 down to the dielectric layer 110, except for the portions of the mask layer 112 illustrated in Figure 1B.

[0017] As illustrated in Figure 1C, the dielectric layer 110 is next etched, using a mixture of an aggressive dielectric etch gas and a polymerizing etch gas. Thus, the aggressive dielectric etch gas and the polymerizing etch gas are applied simultaneously in the mixture. The aggressive dielectric etch gas may comprise, for example, a fluorocarbon gas such as carbon tetrafluoride (CF₄), sulfur hexafluoride (SF₆), or nitrogen trifluoride (NF₃). The polymerizing etch gas may comprise, for example, a hydrofluorocarbon gas compound such as heptafluorocyclopentene (C₅HF₇). In other examples, the polymerizing etch gas may comprise perfluorocyclobutane (C₄F₈), hexafluorobutadiene (C₄F₆), octafluorocyclopentene (C₅F₈), or fluormethane (CH₃F), fluoroform (CHF₃). In one embodiment, the mixture of gases comprises approximately twenty to forty parts aggressive dielectric etch gas to one part polymerizing etch gas. The ratio can be adjusted as needed based on design requirements. For example, a greater

concentration of aggressive dielectric etch gas may be useful when wider interconnects are desired. Most ratios will produce desirable results within a range of -10° Celsius to 60° Celsius.

[0018] The aggressive etch gas removes the portions of the dielectric layer 110 that do not reside directly beneath the remaining portion of the mask layer 112, down to the capping layer 108, which functions as a selective etch stop. The etch results in the formation of one or more trenches 116₁-116_m (hereinafter collectively referred to as “trenches 116”) in the dielectric layer 110. As the aggressive etch gas is removing the dielectric material, the polymerizing etch gas deposits a carbon-rich layer on the exposed vertical sidewalls of the trenches 116 (as illustrated by passivation layers 118). Thus, the passivation layers 118 protect portions of the porous dielectric layer 110 from damage due to prolonged exposure to the aggressive etch gas.

[0019] As illustrated in Figure 1D, the mask layer 112 is next stripped (e.g., via a plasma etch) and wet cleaned. This also results in the passivation layers 118 being removed. A conductive metal layer 120 is then deposited directly on the dielectric layer 110. The conductive metal layer 120 fills the trenches 116 in the dielectric layer 110, thereby forming a pattern of fine lines or interconnects in the back end 114 of the integrated circuit 100. The conductive metal layer 120 may comprise, for example, copper (Cu), a copper alloy, gold (Au), nickel (Ni), cobalt (Co), silver (Ag), ruthenium (Ru), or any other material that does not readily form a volatile species. Deposition of the conductive metal layer 120 may be performed via electroplating and/or other deposition techniques, and may or may not be preceded by deposition of a barrier layer over the dielectric layer 110.

[0020] As illustrated in Figure 1E, the conductive metal layer 120 is next planarized (e.g., via chemical mechanical planarization or other techniques) down to the dielectric layer 110. The remaining portions of the conductive metal layer (e.g., the portions filling the trenches) form a pattern of thin conductive lines or interconnects 122₁-122_m (hereinafter collectively referred to as “interconnects 122”).

[0021] Additional fabrication steps may follow to form additional layers of the integrated circuit 100. For instance, additional layers of interconnects may be formed using the techniques described above and/or other techniques. Additionally, the process described above to fabricate the interconnects could be used to fabricate other components

of the integrated circuit 100, including vias and contacts. Thus, application of the disclosed techniques is not limited to the fabrication of interconnects.

[0022] Thanks to the passivation of the vertical trench sidewalls by the polymerizing etch gas, the interconnects that are formed as a result of the illustrated process have even, uniform profiles with precise dimensions (e.g., trench and via width). This allows small, dense patterns of high-yielding interconnects to be fabricated. For instance, pattern densities with pitches as small as approximately twenty-eight nanometers may be obtained. Moreover, the mixture of the polymerizing etch gas and aggressive dielectric etch gas reduces the occurrence of pattern-dependent etch rates. The vertical etch rate of the trenches is actually quite fast since the aggressive dielectric etch gas forms the majority of the etch gas mixture; however, the hydrogen in the polymerizing etch gas removes some of the fluorine in the aggressive dielectric etch gas and allows a more carbon-rich layer to deposit on the trench sidewalls.

[0023] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised (such as embodiments pertaining to contact and via-level etching) without departing from the basic scope thereof. Various embodiments presented herein, or portions thereof, may be combined to create further embodiments. Furthermore, terms such as top, side, bottom, front, back, and the like are relative or positional terms and are used with respect to the exemplary embodiments illustrated in the figures, and as such these terms may be interchangeable.

What is claimed is:

1. A method, the method comprising:
providing a layer of a dielectric material; and
etching a trench in the layer of the dielectric material, by applying a mixture of an aggressive dielectric etch gas and a polymerizing etch gas to the layer of the dielectric material.
2. The method of claim 1, wherein the aggressive dielectric etch gas comprises a fluorocarbon gas, and the polymerizing etch gas comprises a hydrofluorocarbon gas compound.
3. The method of claim 2, wherein the mixture comprises approximately twenty to forty parts aggressive dielectric etch gas to one part polymerizing etch gas.
4. The method of claim 2, wherein the aggressive dielectric etch gas comprises carbon tetrafluoride.
5. The method of claim 2, wherein the aggressive dielectric etch gas comprises sulfur hexafluoride.
6. The method of claim 2, wherein the aggressive dielectric etch gas comprises nitrogen trifluoride.
7. The method of claim 2, wherein the polymerizing etch gas comprises perfluorocyclobutane.
8. The method of claim 2, wherein the polymerizing etch gas comprises heptafluorocyclopentene.
9. The method of claim 1, further comprising:
depositing a conductive metal in the trench to form a conductive line.

10. The method of claim 1, further comprising:
providing a capping layer beneath the layer of the dielectric material, wherein the etching stops at the capping layer.
11. A method, comprising:
providing a capping layer;
providing a layer of a dielectric material directly over the capping layer;
providing a mask layer directly over the layer of the dielectric material;
patterning the mask layer to expose portions of the layer of the dielectric material;
etching the portions of the layer of the dielectric material to form a plurality of trenches, wherein the etching is performed using a mixture of an aggressive dielectric etch gas and a polymerizing etch gas, and wherein the etching stops at the capping layer;
and
filling the plurality of trenches with a conductive metal to form a plurality of conductive lines.
12. The method of claim 11, wherein the aggressive dielectric etch gas comprises a fluorocarbon gas, and the polymerizing etch gas comprises a hydrofluorocarbon gas compound.
13. The method of claim 12, wherein the mixture comprises approximately twenty to forty parts aggressive dielectric etch gas to one part polymerizing etch gas.
14. The method of claim 12, wherein the aggressive dielectric etch gas comprises carbon tetrafluoride.
15. The method of claim 12, wherein the aggressive dielectric etch gas comprises nitrogen trifluoride.
16. The method of claim 12, wherein the aggressive dielectric etch gas comprises sulfur hexafluoride (SF₆).

17. The method of claim 12, wherein the polymerizing etch gas comprises heptafluorocyclopentene.

18. The method of claim 12, wherein the polymerizing etch gas comprises perfluorocyclobutane.

19. An integrated circuit, comprising:
a plurality of semiconductor devices; and
a plurality of conductive lines connecting the plurality of semiconductor devices,
wherein a pitch of the plurality of conductive lines is approximately twenty-eight nanometers.

20. The integrated circuit of claim 19, wherein each of the plurality of conductive lines comprises:
a line of a conductive metal; and
a carbon-containing layer positioned directly between the conductive metal and a dielectric material.

AMENDED CLAIMS

received by the International Bureau on 06 January 2017 (06.01.2017)

What is claimed is:

1. A method, the method comprising:
providing a layer of a dielectric material; and
etching a trench in the layer of the dielectric material, by applying a mixture of an aggressive dielectric etch gas and a polymerizing etch gas to the layer of the dielectric material, wherein a ratio of the aggressive dielectric etch gas to the polymerizing etch gas in the mixture is sufficient to line sidewalls of the trench with a passivation layer as the trench is being etched.
2. The method of claim 1, wherein the aggressive dielectric etch gas comprises a fluorocarbon gas, and the polymerizing etch gas comprises a hydrofluorocarbon gas compound.
3. The method of claim 2, wherein the mixture comprises approximately twenty to forty parts aggressive dielectric etch gas to one part polymerizing etch gas.
4. The method of claim 2, wherein the aggressive dielectric etch gas comprises carbon tetrafluoride.
5. The method of claim 2, wherein the aggressive dielectric etch gas comprises sulfur hexafluoride.
6. The method of claim 2, wherein the aggressive dielectric etch gas comprises nitrogen trifluoride.
7. The method of claim 2, wherein the polymerizing etch gas comprises perfluorocyclobutane.
8. The method of claim 2, wherein the polymerizing etch gas comprises heptafluorocyclopentene.
9. The method of claim 1, further comprising:

depositing a conductive metal in the trench to form a conductive line.

10. The method of claim 1, further comprising:
 - providing a capping layer beneath the layer of the dielectric material, wherein the etching stops at the capping layer.
11. A method, comprising:
 - providing a capping layer;
 - providing a layer of a dielectric material directly over the capping layer;
 - providing a mask layer directly over the layer of the dielectric material;
 - patterning the mask layer to expose portions of the layer of the dielectric material;
 - etching the portions of the layer of the dielectric material to form a plurality of trenches, wherein the etching is performed using a mixture of an aggressive dielectric etch gas and a polymerizing etch gas, wherein the etching stops at the capping layer, and wherein a ratio of the aggressive dielectric etch gas to the polymerizing etch gas in the mixture is sufficient to line sidewalls of the trench with a passivation layer as the trench is being etched; and
 - filling the plurality of trenches with a conductive metal to form a plurality of conductive lines.
12. The method of claim 11, wherein the aggressive dielectric etch gas comprises a fluorocarbon gas, and the polymerizing etch gas comprises a hydrofluorocarbon gas compound.
13. The method of claim 12, wherein the mixture comprises approximately twenty to forty parts aggressive dielectric etch gas to one part polymerizing etch gas.
14. The method of claim 12, wherein the aggressive dielectric etch gas comprises carbon tetrafluoride.
15. The method of claim 12, wherein the aggressive dielectric etch gas comprises nitrogen trifluoride.

16. The method of claim 12, wherein the aggressive dielectric etch gas comprises sulfur hexafluoride (SF_6).
17. The method of claim 12, wherein the polymerizing etch gas comprises heptafluorocyclopentene.
18. The method of claim 12, wherein the polymerizing etch gas comprises perfluorocyclobutane.

STATEMENT UNDER ARTICLE 19

As noted in the International Search Report and Written Opinion dated 12 August 2016, claims 1-20 are pending in the present application. Independent claims 1 and 11 have been amended to facilitate expeditious prosecution, with support found at least in paragraphs 0011 and 0017-0018 of the Applicant's disclosure. Claims 19-20 are cancelled without prejudice by the Applicant. Applicant has identified the amendments in the markup above. Applicant has also provided replacement claims sheets at the end of this response.

100



FIG. 1A

100

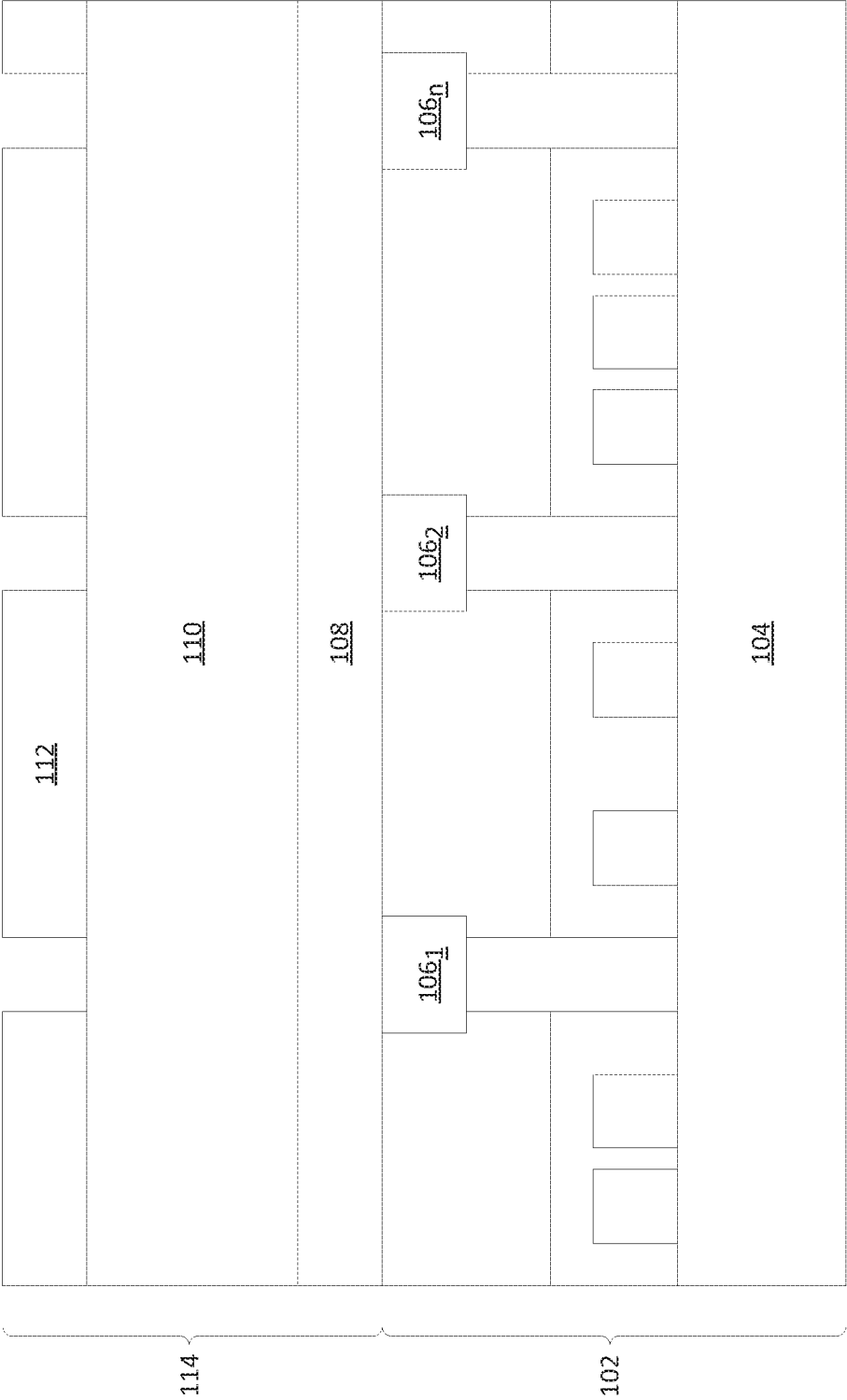


FIG. 1B

100

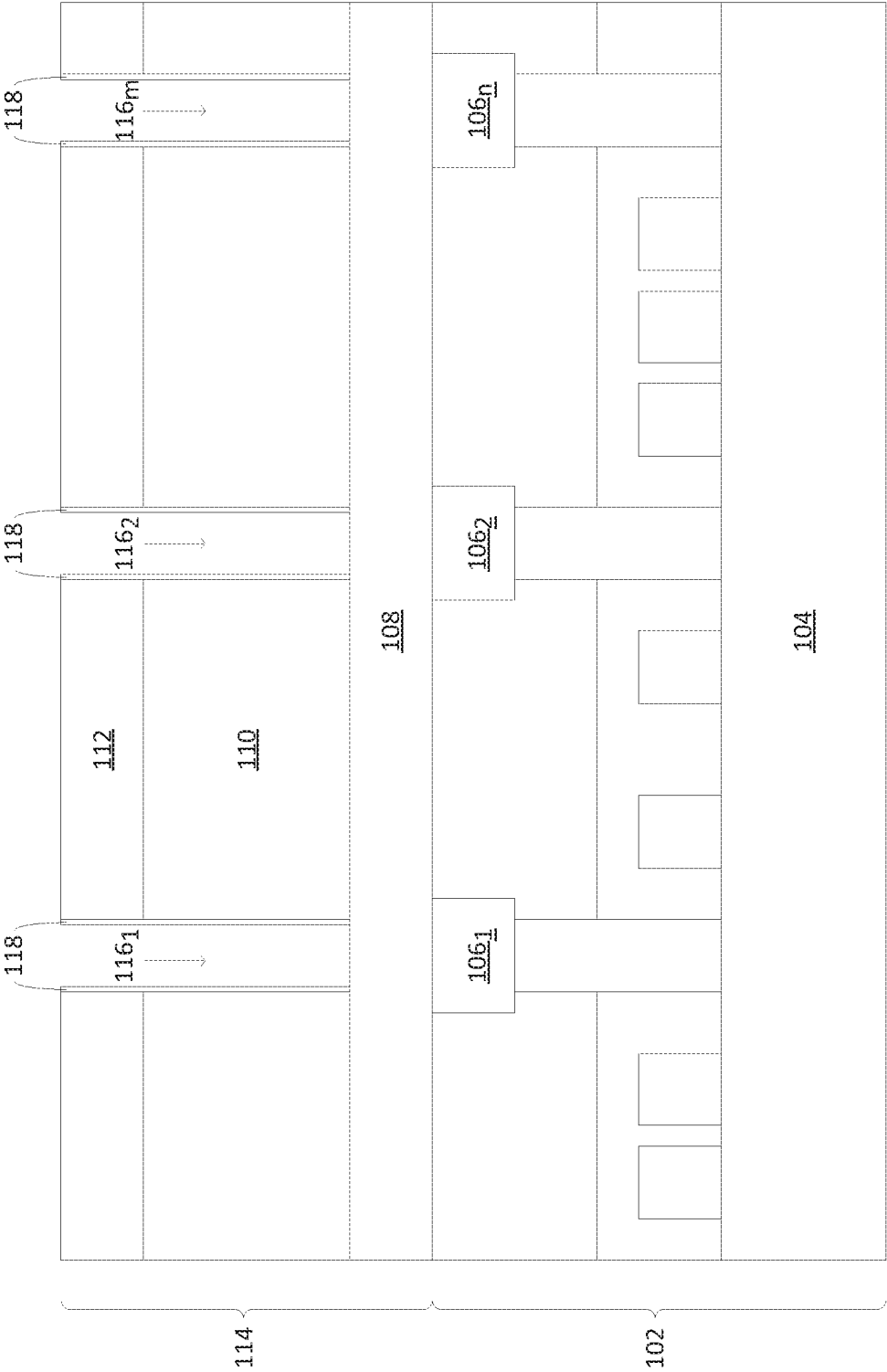


FIG. 1C

100

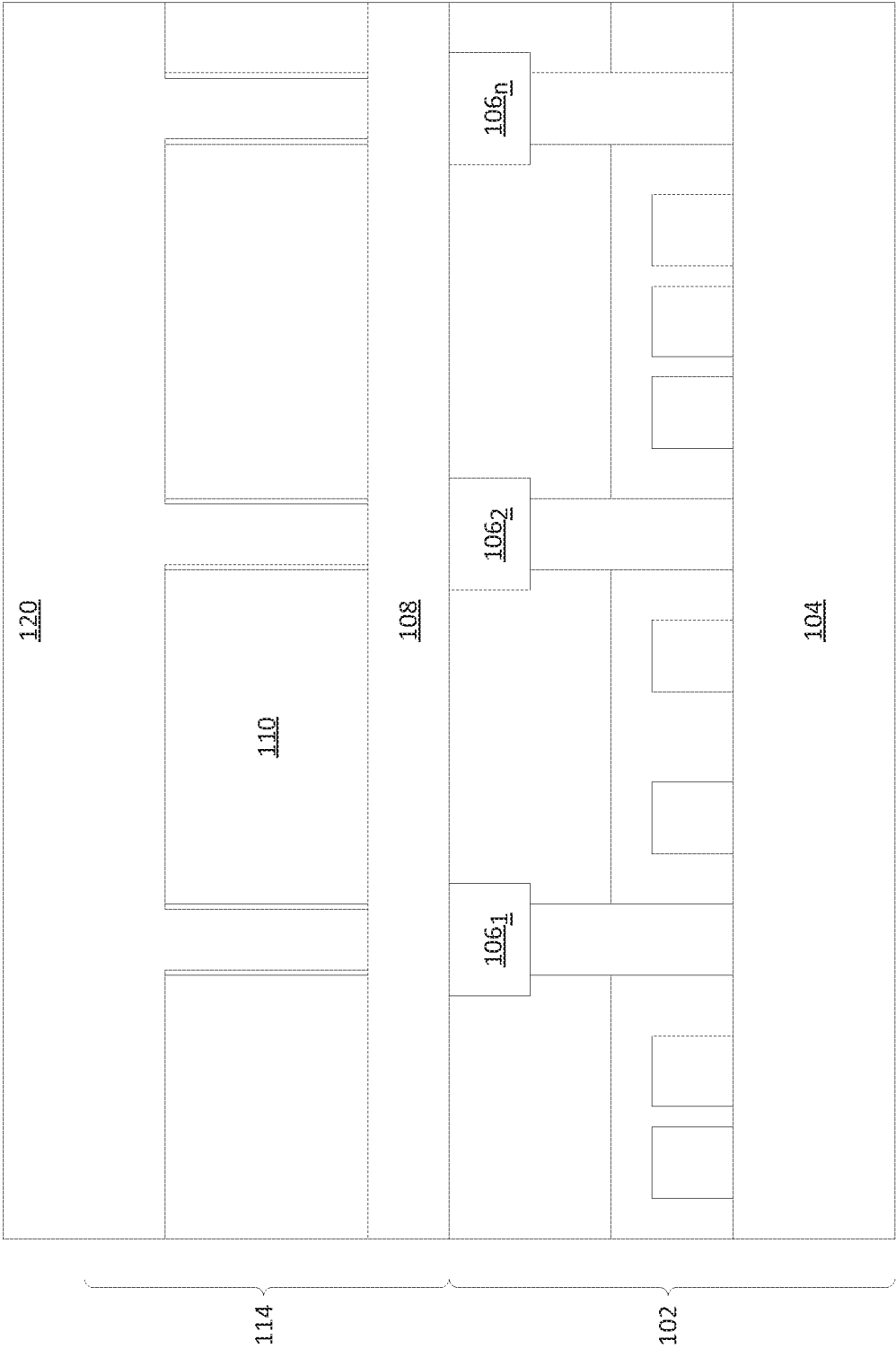


FIG. 1D

100

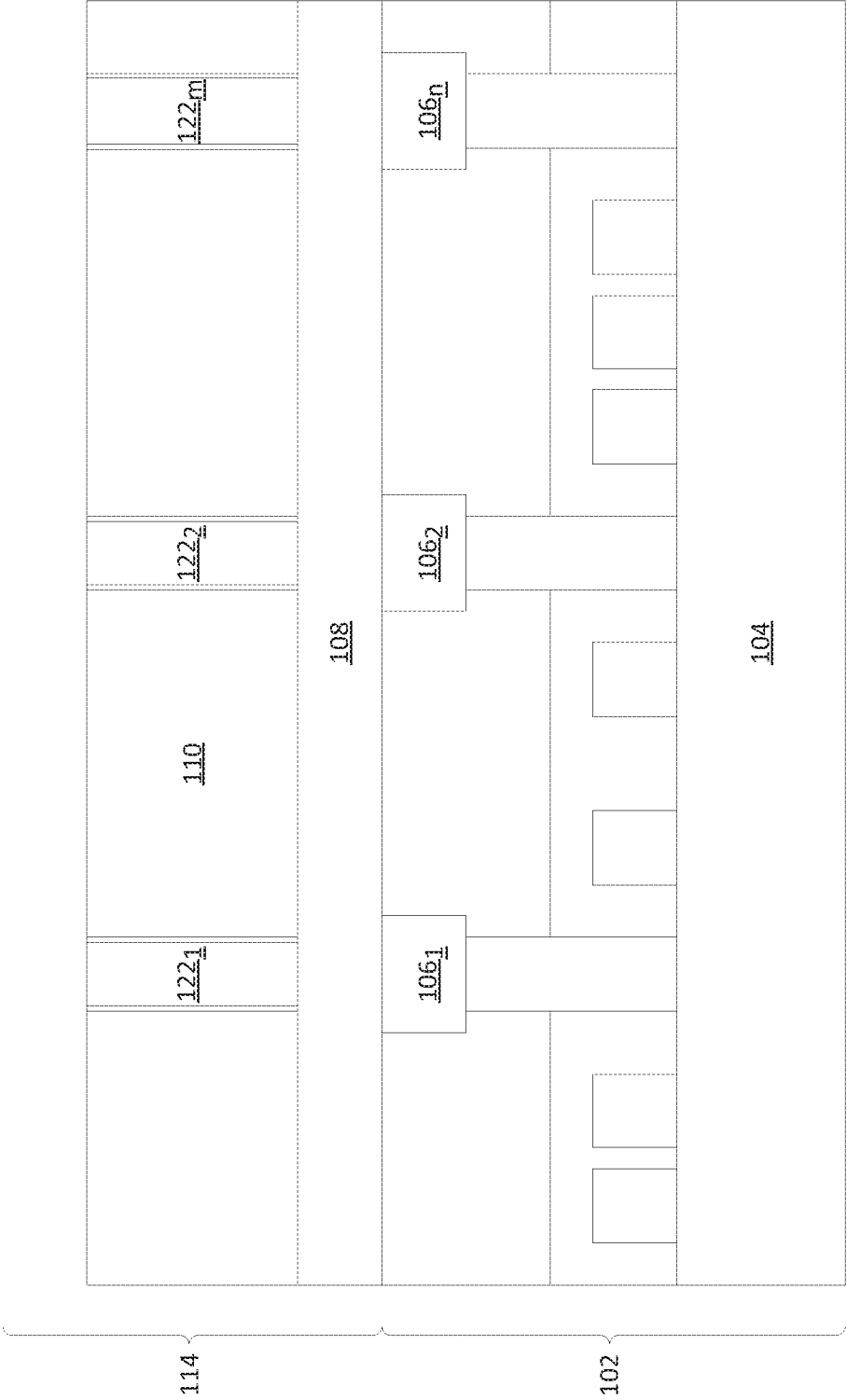


FIG. 1E

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 16/23935

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Group 1: Claims 1-18, drawn to a method comprising providing a capping layer, providing a layer of dielectric material directly over the capping layer, etching portions of the layer of dielectric material to form trenches by applying a mixture of an aggressive dielectric etch gas and a polymerizing etch gas, and wherein the etching stops at the capping layer.

Group 2: Claims 19-20, drawn to an integrated circuit comprising a plurality of semiconductor devices; and a plurality of conductive lines connecting the plurality of semiconductor devices, wherein a pitch of the plurality of conductive lines is approximately 28 nanometers.

The inventions listed as Groups I-II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

- Please see extra sheet for continuation -

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-18

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 16/23935

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01L 21/302; H01L 21/768; H01L 21/027; H01L 21/3065; H01L 21/31; H01L 23/522 (2016.01)

CPC - H01L 21/311; H01L 21/32135; H01L 21/3065; H01L 21/76802; H01L 21/76807; H01L 23/522

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8) - H01L 21/302; H01L 21/768; H01L 21/027; H01L 21/3065; H01L 21/31; H01L 23/522 (2016.01)

CPC - H01L 21/311; H01L 21/32135; H01L 21/3065; H01L 21/76802; H01L 21/76807; H01L 23/522

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Patents and non-patent literature (classification, keyword; search terms below)Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatBase, Google Scholar (NPL), Google Patents; search terms: dielectric material, layer, etching, trench, mixture, conductive line, depositing, conductive metal, capping layer, etch stop, mask layer, carbon tetrafluoride, sulfur hexafluoride, nitrogen trifluoride, perfluorocyclobutane, heptafluorocyclopentane

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ----- Y	US 2005/0023694 A1 (BJORKMAN et al.) 03 February 2005 (03.02.2005) para [0003], [0006]-[0007], [0012], [0014], [0029]-[0030], [0034]-[0035], [0038], [0084], [0096]; Fig. 1A-1C	1-4, 7, 9-14, 18 ----- 8, 17
X	US 2014/0120733 A1 (CHEUNG et al.) 01 May 2014 (01.05.2014) para [0002]-[0003], [0008], [0010], [0027]-[0029], [0037]; Fig. 2A-2C, 3A	1-2, 5-6, 11-12, 15-16
Y	US 2005/0247670 A1 (YAMADA et al.) 10 November 2005 (10.11.2005) para [0001]-[0002], [0021], [0023]	8, 17
A	US 2006/0024956 A1 (ZHIJIAN et al.) 02 February 2006 (02.02.2006) entire document	1-18
A	US 2006/0024956 A1 (ZHIJIAN et al.) 02 February 2006 (02.02.2006) entire document	1-18
A	US 6,410,426 B1 (XING et al.) 25 June 2002 (25.06.2002) entire document	1-18

☐ Further documents are listed in the continuation of Box C.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

07 July 2016 (07.07.2016)

Date of mailing of the international search report

12 AUG 2016

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US, Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450

Facsimile No. 571-273-8300

Authorized officer:

Lee W. Young

PCT Helpdesk: 571-272-4300
PCT OSP: 571-272-7774

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 16/23935

Continuation of:

Box NO III. Observations where unity of invention is lacking

Special Technical Features

Group II does not require a method comprising providing a capping layer, providing a layer of dielectric material directly over the capping layer, etching portions of the layer of dielectric material to form trenches by applying a mixture of an aggressive dielectric etch gas and a polymerizing etch gas, and wherein the etching stops at the capping layer, as required by Group I.

Group I does not require an integrated circuit comprising a plurality of semiconductor devices, and a plurality of conductive lines connecting the plurality of semiconductor devices, wherein a pitch of the plurality of conductive lines is approximately 28 nanometers, as required by Group II.

Shared Common Features

Groups I-II share the technical feature of dielectric material and plurality of conductive lines of a conductive metal. However, this shared technical feature does not represent a contribution over prior art, because the shared technical feature is disclosed by US 2005/0023694 A1 to Bjorkman et al. (hereinafter "Bjorkman"). Bjorkman teaches dielectric material and a plurality of conductive lines or trenches of deposited conductive metal (para [0007], [0014]; horizontal interconnects (lines/trenches) from etching dielectric layers and depositing conductive materials, such as copper).

As the common technical features were known in the art at the time of the invention, these cannot be considered a special technical feature that would otherwise unify the groups.

Groups I-II therefore lack unity under PCT Rule 13 because they do not share a same or corresponding special technical feature.